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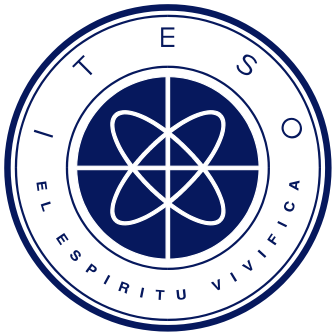
Departamento de Electrónica, Sistemas e Informática

ESPECIALIDAD EN DISEÑO DE SISTEMAS EN CHIP



Design and Physical Implementation of an Analog Receiver for a SerDes System on Chip in 130nm CMOS Technology

Tesina para obtener el grado de

ESPECIALISTA EN DISEÑO DE SISTEMAS EN CHIP

Presenta:

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ABSTRACT

Serial I/O's (inputs/outputs) are the backbone of modern communications; they are present in most if not all computing systems and today's high-bandwidths applications push data rates to the Gigabit per second speed.

SerDes are at the core of these high-bandwidth serial communications, this mixed signal system is in charge of converting data from parallel (at low data rate) to serial (High data rate) and vice versa for off-chip communications.

The major functional blocks of a SerDes are the Analog Receiver, Analog Transmitter, PISO (Parallel Input Serial Output) & SIPO (Serial Input Parallel Output).

In this work the design and physical implementation of an analog receiver module for a SerDes with a data rate of 2.5 Gbps suitable for PCI Express Gen 1, is presented. The proposed analog receiver consists of three major blocks; a High-speed differential amplifier; a CML to CMOS circuit and a Bias circuit, it was designed in CMOS 130nm process technology (GLOBALFOUNDRIES cmrf8sf Process Design Kit) with a supply voltage of 1.2V using Cadence Virtuoso EDA.

This work presents the whole design cycle organized in a step-by-step fashion from circuit design, pre-layout verification, layout design & post-layout verification, so the reader could reproduce it or use it as a guideline to carry out similar designs.

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CHAPTER 1: BACKGROUND, SERDES SYSTEM

1.1. SerDes System Description

A SerDes is a mixed signal system used in most high-speed digital ICs for off-chip communications (chip to chip, board to board), it uses differential signaling to enable high data rates (> 1Gbps) compared to the classical single-ended parallel communication.

Serial I/O's have several advantages over parallel I/O's, it reduces pin count (moves same or even more amount of data and reduces PCB pin count), reduces simultaneous switching (avoids ground bouncing, reduces power integrity issues), reduces EMI due to extreme care on signal integrity and optimizes cost (cheaper packages, connectors, fewer pins).

Some examples of industry standards using SerDes are [1]:

- Fiber Channel (FC)
- PCI Express
- Advanced Switching Interface
- Serial ATA

The SerDes to be designed in this graduate program will comply with the PCI Express Gen one specifications.

1.2. PCI Express Overview

The PCI Express architecture is specified in layers, as shown in Figure 1.1 Compatibility with the PCI addressing model (a load-store architecture with a flat address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms defined in the PCI plug-and-play specification [2].

The software layers generate read and write requests that are transported by the transaction layer to the I/O devices using a packet-based, split-transaction protocol. The link layer adds sequence numbers and CRC (Cyclic redundancy check) to these packets to create a highly reliable data transfer mechanism. The basic physical layer consists of a dual simplex channel implemented as a transmit pair and a receive pair.

The transmitter and receiver pair together are called a lane. The initial speed of 2.5 Gbps provides a nominal bandwidth of about 250 MB/s in each direction per PCI Express lane. Once overhead is taken into account, about 200 MB/s of this is usable by the device for data movement.

This rate represents a twofold to fourfold increase over most classic PCI boards. Unlike PCI, where the bus bandwidth was shared among devices, this bandwidth is provided to each device [2].

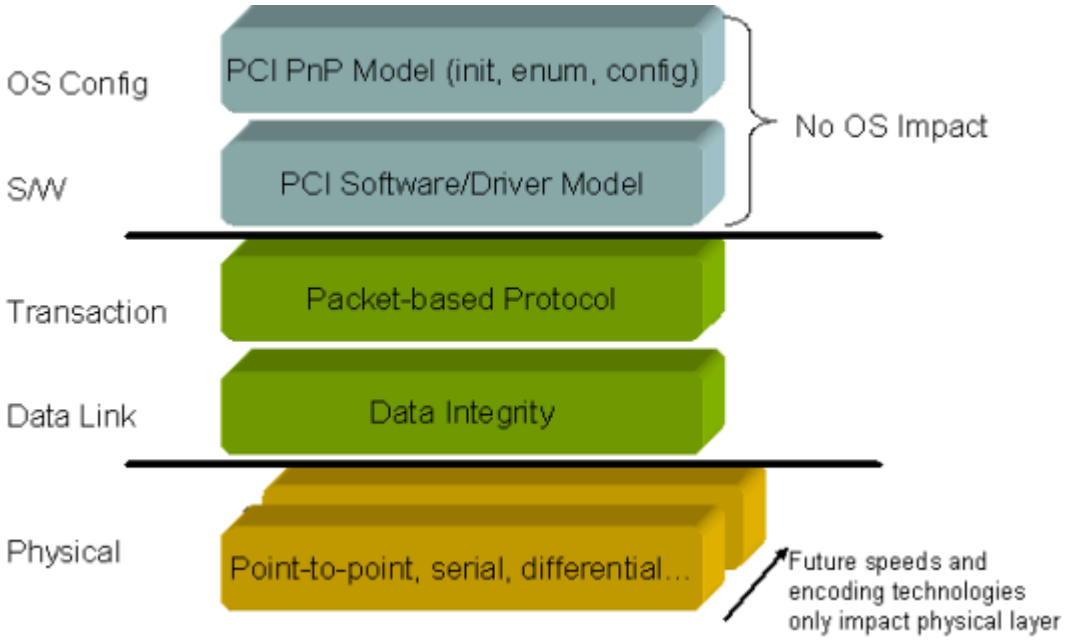

Figure 1-1: PCI Express Layered Architecture *[2]*

In our SerDes project, we are focusing on the physical layer.

1.2.1. PCI Express Physical Layer

PCI Express link consists of two low-voltage AC-coupled differential pairs of signals (a transmit pair and a receive pair) as shown in Figure 2 [2]. The physical link signal uses a de-emphasis scheme to reduce intersymbol interference, thus improving data integrity.

A data clock is embedded using the 8b/10b encoding scheme to achieve very high data rates. The initial signaling frequency is 2.5 Gb/s/direction (Generation 1 signaling), and this is expected to increase in line with advances in silicon technology to 10 Gb/s/direction (the practical maximum for signals in copper).

The physical layer transports packets between the link layers of two PCI Express agents [2] [3].

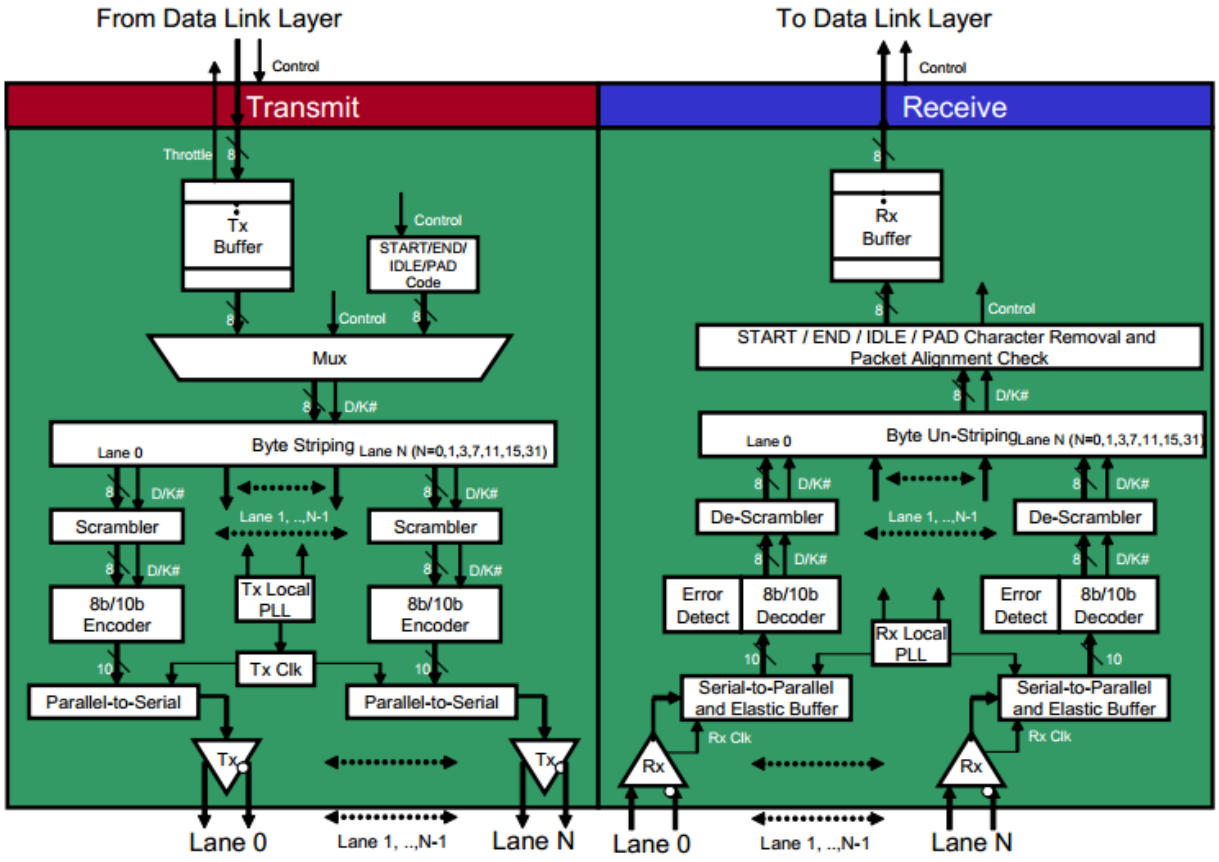

Figure 1-2: PCI Express Physical Link in detail [3]

1.3. SERDES Blocks Description

1.3.1. Analog Receiver

Analog receiver is in charge of amplifying the incoming differential data that's been attenuated due to channel loss effects; it may include an equalization circuitry such as a CTLE (Continuous time linear equalizer) to improve signal quality.

1.3.2. Analog Transmitter

Analog transmitter is in charge of transmitting the serial data out; it may include a driver strength selection and an equalization circuit to implement pre-emphasis, de-emphasis and impedance modulation to account for channel loss.

1.3.3. Digital De-Serializer (SIPO)

Digital Serializer in charge of taking the serial stream from the analog receiver and change it into parallel data. Inside the De-serializer a decoder is needed if the data received is in an 8b/10b or another encoding scheme to recover the real data. A CDR (Clock and data recovery) to synchronize incoming data with system reference clock is also required.

1.3.4. Digital Serializer (PISO)

This block is in charge of taking the parallel stream of data and change it into serial data to be sent by the analog transmitter block. Inside the serializer, an encoder is needed if the data to be transmitted, is required to be encoded in 8/10b or another encoding scheme.

1.3.5. BIST/ DFTs

Logic circuitry that enables the testing of the individual blocks to ensure proper functionality independent of other blocks, this may include loopbacks and monitor pins for internal signals.

1.4. Project Scope

The Objective of this project is to design and verify all the basic blocks that form a high-speed SerDes physical layer using the cmrf8sf 130nm process technology from Global Foundries. The SerDes architecture is depicted in figure 1.3.

This design is targeted to work at 2.5 Gbps using the PCIe Gen1 protocol with the knowledge acquired through all the System on Chip Design specialization courses by July of 2016.

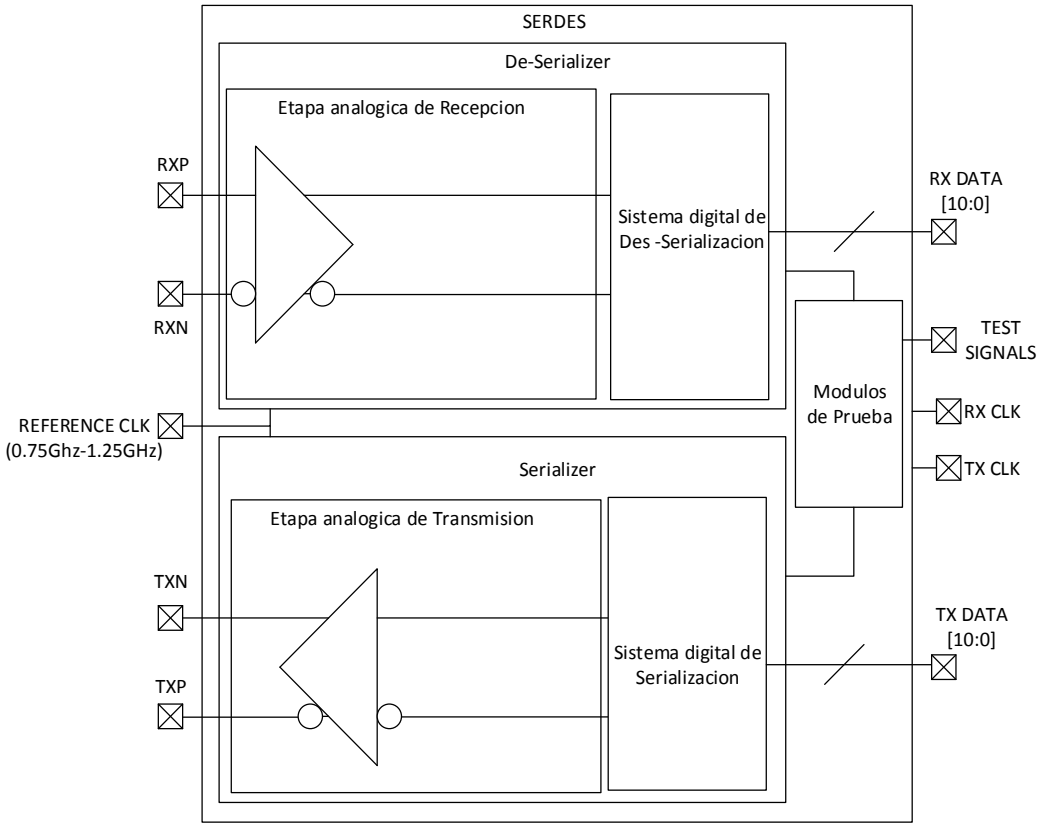

Figure 1-3: SerDes Block diagram *[4]*.

1.4.1. Assumptions

- The required technical knowledge/Skills to fulfill the design of each block will be acquired through all the System on Chip specialization courses provided by ITESO.
- The timeline is sufficient to complete all the necessary design & verification stages of the project.
- The Cadence IC design Suite (Virtuoso) will be available through all the project life cycle.
- The PDK design parameters (cmrf8sf 130 nm process) provided by MOSIS are complete and do not require further verification.
- A reference clock will be given to the SerDes system to synchronize the digital portion of the design.
- There are enough resources (team of 6 classmates plus six project advisers) to design all functional blocks.
- All design dependencies (blocks assigned to each member of the design team) will be finished on time for the integration.
- All necessary software tools will be available.

1.4.2. Constrains

- The Design will be implemented using cmrf8sf process from GLOBALFOURNDRIES 130nm technology.
- The Design tool to be used will be Cadence IC design Suite.
- The Design frequency operation is up to 2.5 Gbps.
- Project completion is set for July 30 2016.
- Design tools are only available on-site (ITESO).
- The Design is intended to work at VDD = 1.2V.
- Area restriction for MOSIS academic projects (2x2 mm maximum for all SerDes system including the PAD frame).
- PKG restriction 40 pins for the fabricated chip.
- Protocol restriction to PCIe Gen1.
- Chip fabrication scheduled to August 15, 2016.
- Package selection provided by MOSIS.

1.4.3. Out of Scope

- PLL design.

CHAPTER 2: DESIGN OF THE ANALOG RECEIVER MODULE

2.1. Architecture Description

The analog receiver module architecture consists of three main blocks: the high-speed differential amplifier that receives a differential signal from the external world and amplifies it so the other stages can process it.

This block needs to have the enough bandwidth in order to process signals at 2.5 Gbps data rate; a bias circuit that ensures that the high-speed amplifier is properly biased despite PVT (Process, Voltage & Temperature) variations; and finally a CML (Current Mode Logic) to CMOS circuitry in charge of transforming the signal from the analog domain to the digital Fdomain.

This block also contains a DCC (duty cycle corrector) circuit that helps the duty cycle to remain as close as possible to 50% across PVT variations. Figure 2.1 shows the block diagram and figure 2.2 the circuit architecture.

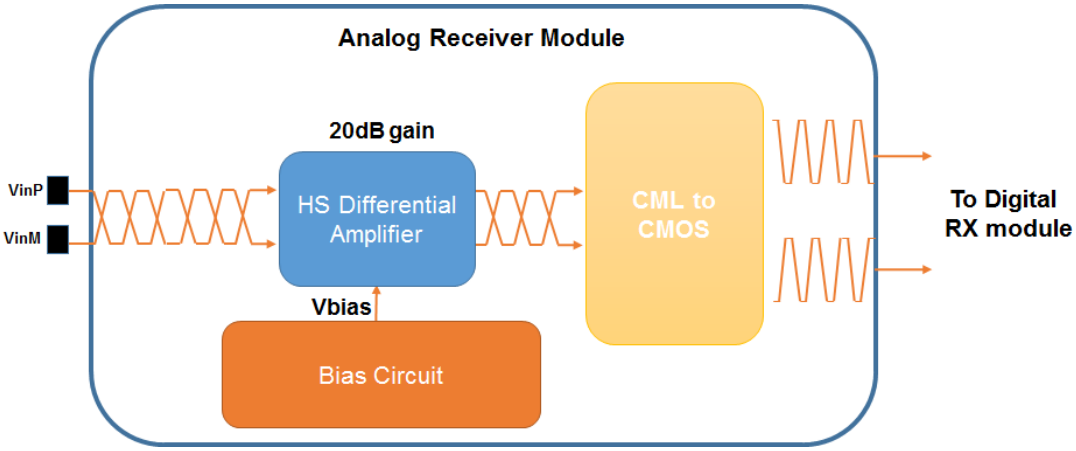

Figure 2-1: Analog Receiver Top Block Diagram.

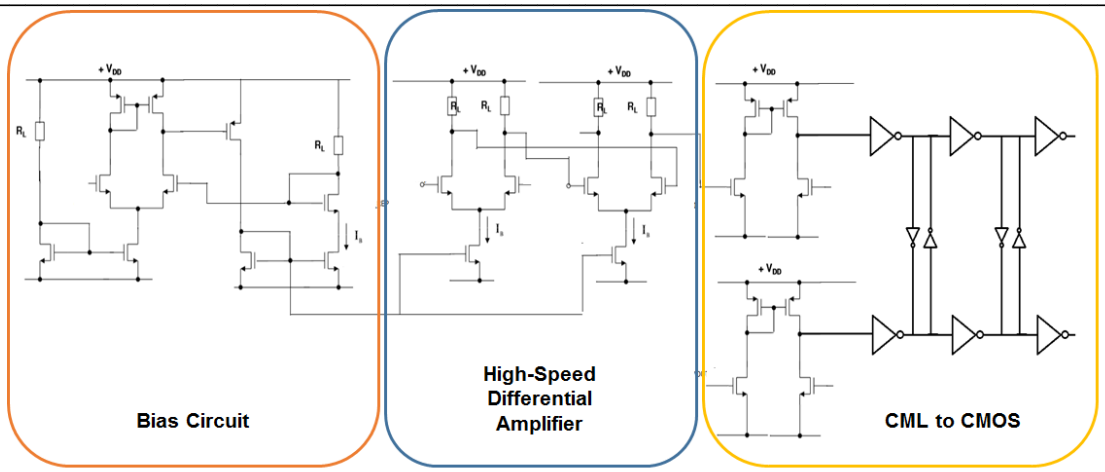

Figure 2-2: Analog Receiver Architecture.

2.2. High-speed differential amplifier (HS-OTA).

The high-speed differential amplifier consists of two OTA's (Operational Transconductance Amplifiers) with resistive loads in cascade. This topology shown in figure 2.3 was chosen because it can handle higher bandwidths compared with OTA's with active loads and it does not require feedback, so it can be cascaded to achieve higher voltage gains without having instability issues.

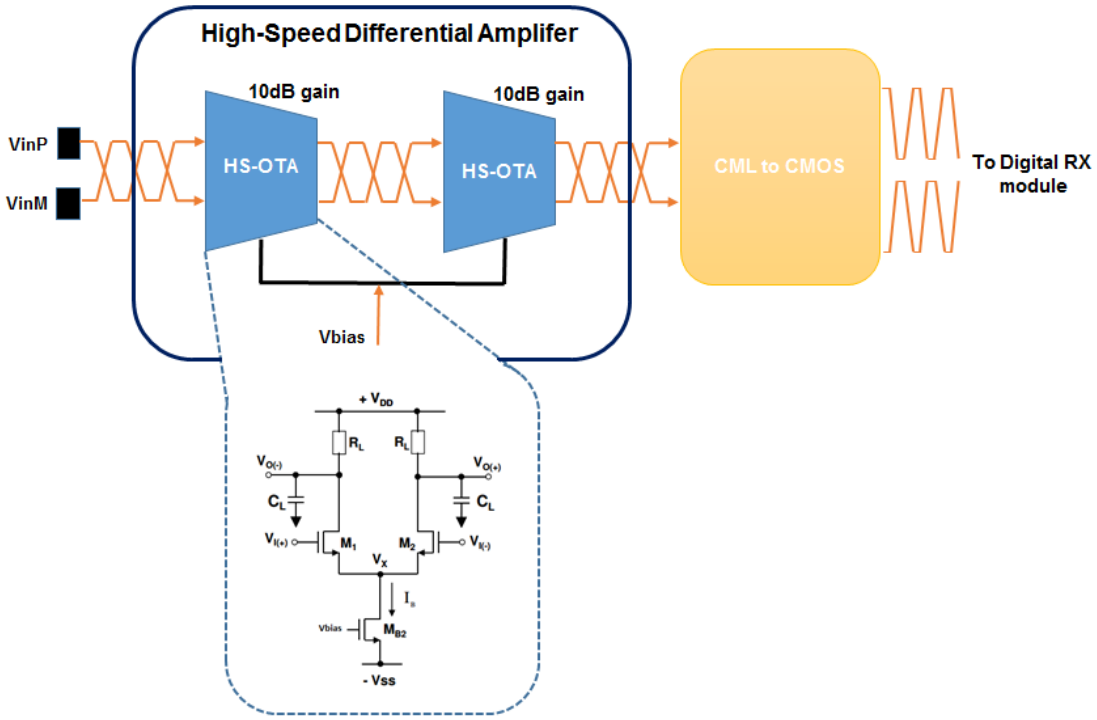

Figure 2-3: High-speed differential amplifier block diagram & OTA Topology.

2.2.1. HS-OTA design requirements

Table 2.1 shows the design needs of the HS-OTA block. A gain of 20 dB (or 10 V/V) was set for this amplifier according to PCIe gen1 specifications. Notice for PCIe gen1 the minimum amplitude at the receiver pins is 40 mV peak to peak [5], so a gain of 10 V/V will ensure a ~400 mV at the output of the HS-OTA in the worst case condition. On the other hand, this signal amplitude is good enough to be handled by the CML to CMOS circuit.

Parameter	Design spec
Gain	20 dB
3 dB BW	2.5 GHz
VDD	1.2 V
VCM IN	840 mV
VCM OUT	840 mV
Load	20 fF

Table 2-1: HS-OTA Design Requirements.

2.2.2. Design procedure of the HS-OTA

As shown in figure 2.3, the HS-OTA consists of two OTA stages connected in cascade targeting 10 dB gain each stage. As first consideration in the design procedure, the load capacitance seen by the first OTA (second OTA input capacitance) is 20 fF, then the sizing of the transistors, bias current and load resistance was obtained by using the first order models of MOSFET.

It should be noted that this approach will give just an estimation of the transistor sizing required, resistor value to set output common mode and bias current. A second consideration in the design was an overdesign in $\boldsymbol{\omega_{3dB}}$ in order to reach 3 GHz to account for this approximation. Components values were obtained as indicated below [6]:

$$R_{out} = \frac{1}{\omega_{3dB} C_L} = \frac{1}{2\pi(3\ x10^{9})(20x10^{-15})} = 2.653\ K\Omega \tag{1}$$

$$gm = \frac{A_v}{R_{out}} = \frac{3.2}{2.653x10^{3}} = 1.192\ mS \tag{2}$$

$$I_B = \frac{2(V_{DD} - V_{OCM})}{R_{out}} = \frac{2\ (1.2 - .840)}{2.653x10^{3}} = 271.434\ uA \tag{3}$$

$$\frac{W}{L} = \frac{gm^2}{I_B\ K_n} = \frac{(1.192\ x\ 10^{-3})^2}{(271.434\ x\ 10^{-6})\ (305.6\ x\ 10^{-6})} = 17.133 \tag{4}$$

$$L = 270\ nm\ \ W = 4.626\ um \tag{5}$$

The width of the differential pair transistors had to be adjusted to achieve the necessary g_m hence the $\boldsymbol{\omega_{3dB}}$ bandwidth (see table 2.2). This is necessary because our hand calculations using basic models leads to approximate values while models used by the Spectre simulator are more complex and, it computes values that are more precise. With these initial results we achieved a single HS-OTA stage.

$$\omega_{3dB} = 3.11\ GHz \tag{6}$$

$$A_v = 10.01\ dB \tag{7}$$

To achieve the necessary 20 dB gain, this HS-OTA was a cascaded. Simulation results of cascaded HS-OTA show that the ω_{3dB} dropped to 1.16 GHz while voltage gain remains in 20 dB. With this information we, proceed to calculate the real load capacitance seen by the first OTA as follows (8).

$$C_{pout1} = \frac{1}{BW*(R_L \,||\, rds)} = \frac{1}{BW*\frac{1}{\left(\frac{1}{R_L}+gds\right)}} \approx 38\ fF \tag{8}$$

Then, we calculated the BW degradation as follows (9):

$$Degradation_{\%} = \frac{BW_{Cascada}}{BW_{simple}} = 37.29\% \tag{9}$$

Now we re-calculate the target BW on the cascade topology as follow (10)

$$NewBW = BW_{original} * (100\% + Degradación_{\%}) \approx 4\ GHz \tag{10}$$

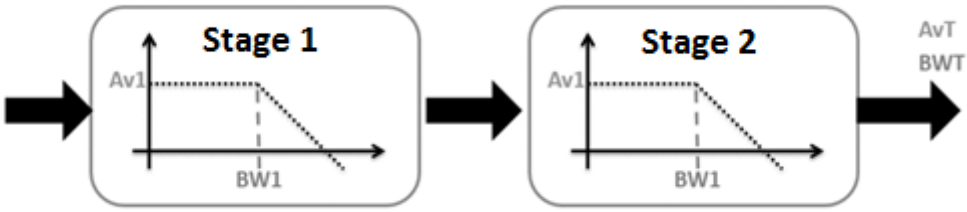

Figure 2-4: HS-OTA Cascade BW and Voltage Gain.

With this new BW, we re-designed the OTA with the following modified design requirements (Table 2.2)

Parameter	Design spec
Gain	10 dB
3 dB BW	5 GHz
Load	40 fF

Table 2-2: 2nd Iteration in HS-OTA Design Requirements.

Notice that we over-design to 5 GHz instead of 4 G Hz to give some margin of GBW result. Following the procedure and design equations described before we arrived at the following results in Table 2.3.

Parameter	Value
W	19 um
L	180 nm
I_B	904.8 µA
R_L	795.8 Ω

Table 2-3: Final Pre-Layout Design Parameters.

2.3. CML to CMOS circuit

The CML to CMOS circuit block function is to take the current mode logic level 840 mV common mode and small differential signals to a single-ended CMOS with a common mode of 600 mV and a swing of 1.2 V so that the digital logic can process it.

The block consists of two differential to single ended converter that take the signal handled by the HS-OTA and change its common mode from 0.7*VDD to 0.5*VDD and also changes it from differential to single ended. The reason for using two converters is to produce a complementary single-ended signal that will be utilized by the DCC circuit to correct duty cycle mismatch. Once the signal is converted to single-ended, it is then fed to three inverters to increase the signal strength and to have rail to rail swing.

The DCC circuit consists of 2 inverters back to back. This array acts like a latch forcing both outputs to be the same. With this circuit the duty cycle will be as close as possible to 50%, figure 2.5 shows the CML to CMOS circuit block.

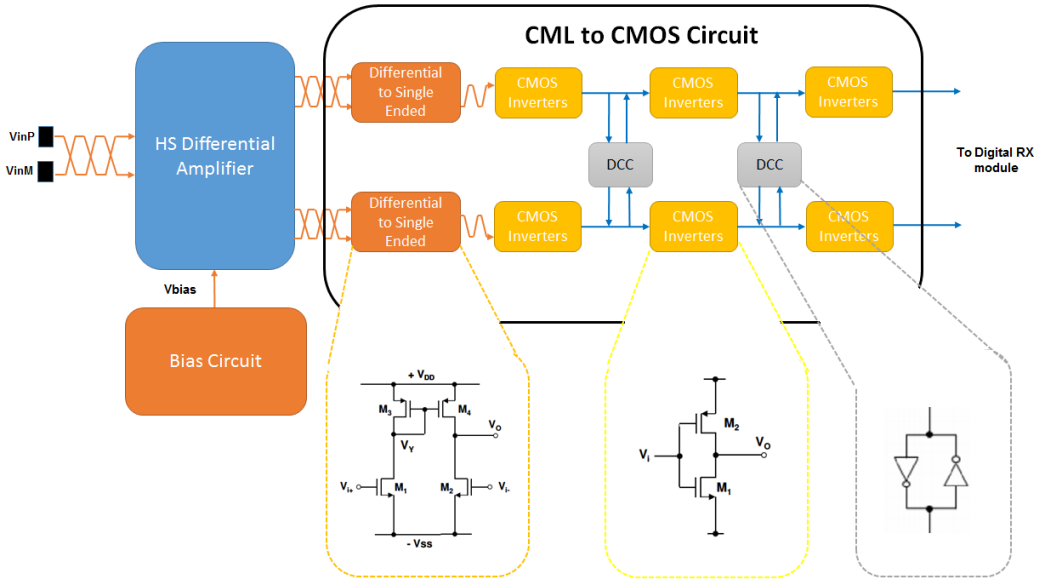

Figure 2-5: CML to CMOS Circuit Blocks.

2.3.1. CML to CMOS design requirements

The requirements for this circuit are summarized in Table 2.4:

Parameter	Design spec
VOCM	600mV
Duty Cycle	~ 50%
Cin max	20 fF

Table 2-4: Design Specifications of CML to CMOS Circuit,

The C_{in} restriction is to maintain our bandwidth $\boldsymbol{\omega_{3dB}}$ = 2.5 GHz obtained from the HS-OTA design.

Notice the load capacitance seen by the HS-OTA will be set this block input capacitance more precisely by the differential to single-ended circuit, then the size of the differential to single-ended NMOS transistors in the differential pair will set this value. On the HS-OTA design, we ensure that the bandwidth required was obtained by setting a max capacitive load of 20 fF.

2.3.2. CML to CMOS design methodology

To design this circuit, it is important to keep in mind that the circuit will work on the transistor's nonlinear region, meaning that we will analyze the output parameters using transient simulations rather than AC analysis.

2.3.3. Inverter design

The first block to be designed is the inverter. The design was done in such way that the rise and fall times measured at 20% and 80% of the signal swing were as equal as possible with enough strength to drive a capacitive load of 20 fF; we started with the minimum W = 160 nm and set L = 180 nm to match our HS-OTA transistor Length.

On the first try we set W_p 2.5 times Wn to take into account the mobility difference of NMOS and PMOS, then the calculation of W_n and W_p was iterated until we reach the final Wn and WP size that meet the rise time requirement (see Table 2.5).

Parameter	Value
W_p	3.4 um
W_n	1.2 um
L_p=L_n	180 nm

Table 2-5: Transistors' Sizes of Inverter Cell.

Once one inverter was designed, we cascade two inverters increasing the W by a factor of 3 every stage following the tapering buffer design methodology to obtain the best power consumption, delay and jitter trade-off [7], giving us the next final values summarized in Table 2.6.

Parameter	1st inverter	2ncd inverter	3rd inverter
W_p	3.4 um	10.2 um	30.6 um
W_n	1.2 um	3.6 um	10.8 um
$L_n = L_p$	180 nm	180 nm	180nm

Table 2-6: Transistors' Size of Tapering Buffers.

2.3.4. Differential to Single-Ended circuit design methodology

Next block to be designed is the converter of the differential to single-ended circuit (Fig. 5). Some requirements to be taken into account in conception this block are: (1) this circuit has to provide as much current as possible to reach the largest swing possible and set the output common mode from 0.7 * VDD to 0.5 * VDD, without sacrificing the 2.5 GHz bandwidth. This circuit has a capacitive load given by the input capacitance of the first inverter of the tapering buffer.

The design of converter differential to single ended circuit started by using the following initial considerations: Lp = Ln = 180nm and Wp = 2.5 * Wn, then the PMOS where sized to set the V_{OCM} following equation (11).

$$V_{OCM} = V_{DD} + |V_{THp}| - \sqrt{\frac{I_B}{K_P\left(\frac{w}{l}\right)}} \tag{11}$$

The design was iterated increasing W_n and fixing the V_{ocm} accordingly until the bandwidth from the previous stage reached min ~ 2.5 GHz, the final transistor sizes that met the requirements are summarized in Table 2.7.

Parameter	value
W_p	3.4 um
W_n	1.2 um
L_p=L_n	180 nm

Table 2-7: Transistors' Size of Differential To Single-ended Circuit.

2.3.5. Design of Duty Cycle Corrector inverter circuit

The design of the DCC inverters was re-sized as follows: W_{DCC} = ½ $W_{Inverter}$ direct path, this consideration was done to avoid the signal on the direct path latches. This consideration will give enough strength to the DCC inverters to force the duty cycle to reach as close as 50%, the transistor sizes end up as follows (Table 2.8)

Parameter	1st DCC inverter	2nd DCC inverter
W_p	1.7 um	5.1 um
W_n	0.6 um	1.8 um
$L_n = L_p$	180 nm	180 nm

Table 2-8: DCC Circuit Transistors' Size

2.4. Bias Circuit

The Bias circuit consists of three blocks shown in figure 2.6; a high-gain OTA, a replica circuit of the HS-OTA and a resistor divider network. The replica circuit as its name implies it is a copy of one of the branches of the HS-OTA, we use this copy to sense the HS-OTA PVT variations, and this signal is fed to one of the inputs of the high-gain OTA. The signal generated by the replica circuit acts as a control voltage that forces the input of the High-Gain OTA (the voltage set by the resistor divider in figure 2.6) to be equal to a reference voltage. This control voltage is in turn fed to a PMOS transistor that converts this voltage to a control current and then reflected to the branch that is intended to control.

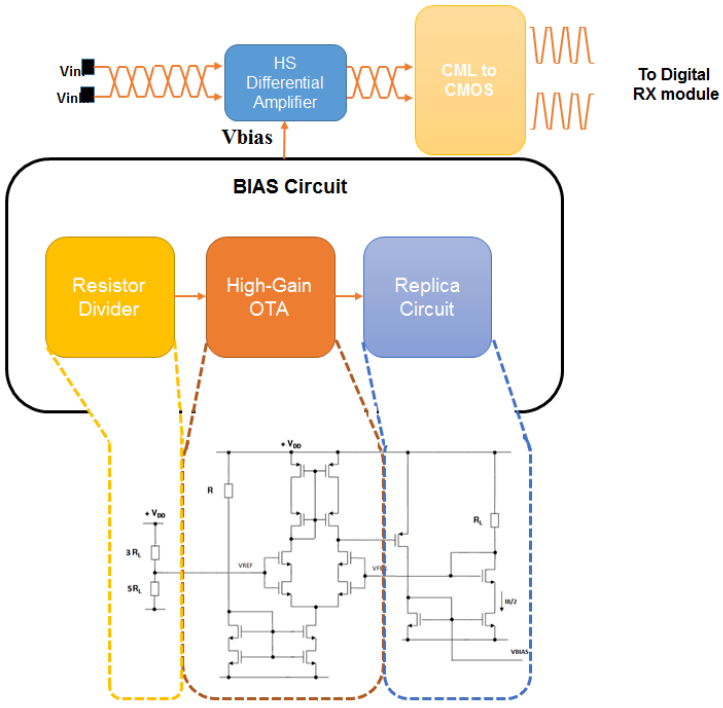

Figure 2-6: Bias Circuit Blocks.

2.4.1. High-Gain OTA Design Requirements

Table 2.9 shows the design needs of the High-Gain OTA design; a 40 dB gain is assumed to be enough to control the replica circuit and the 10 MHz Gain-bandwidth product should be sufficient since the node that will be monitored is not expected to move at higher frequencies.

Parameter	Design spec
Gain	40 dB
GBW	10 MHz
V_{DD}	1.2 V
V_{CM} IN	840 mV
V_{CM} OUT	840 mV
C_{Load}	1 pF

Table 2-9: High-Gain OTA Design Requirements.

2.4.2. High-Gain OTA Design Methodology

The first topology chosen for this block was the one shown in figure 2.7; this is the simplest one and usually, offers good voltage gain ensuring stability due to the second pole always set at twice the frequency of the dominant pole.

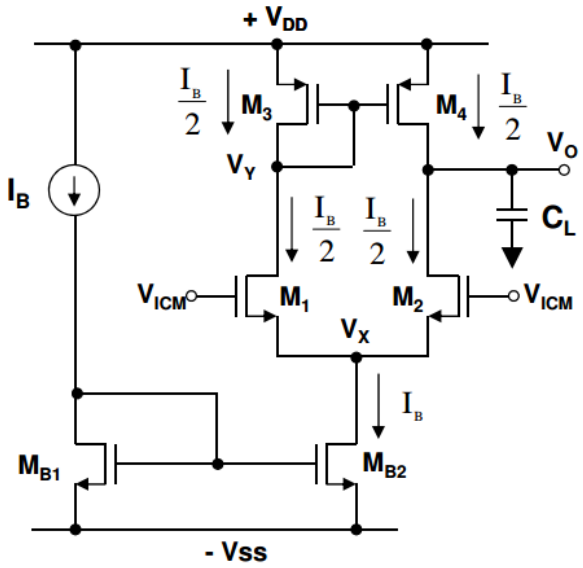

Figure 2-7: Simple OTA Topology

The design equations and procedure to obtain the output resistance, bias current, and first transistor size are describe below [8].

$$GBW = \frac{gm}{C_L} \tag{12}$$

$$gm = 2\,\pi\,C_L\,GBW \tag{13}$$

$$gm = 2\,\pi * (10\,x\,10^{6}) * \ (1\,x\,10^{-12}) = 62.8\,uS \tag{14}$$

$$Av = gm * Rout \tag{15}$$

$$Rout = \frac{Av}{gm} = \frac{100}{62.8\,x\,10^{-6}} = \ 1.592\,K\Omega \tag{16}$$

$$gm\ = \frac{I_B}{V_{Dsat}}\ , assuming\ V_{DSAT} = 200mv \tag{17}$$

$$I_B = \ gm * \ V_{DSAT} = \ (6.28\,x\,10^{-6}) * 0.200\ = \mathbf{12.6\ uA} \tag{18}$$

$$V_{OCM} = \ V_{DD} - |V_{THP}| - \sqrt{\frac{I_B}{K_P\left(\frac{W}{L}\right)_P}} \tag{19}$$

$$\left(\frac{W}{L}\right)_P = \frac{I_B}{K_P(V_{DD} - V_{OCM} - |V_{THP}|)^2} = \frac{12.6\,x\,10^{-6}}{(69\,x\,10^{-6})(1.2 - \ .840 - 251.7\,x10^{-6})} = 15.56 \tag{20}$$

$$\left(\frac{w}{L}\right)_N = \frac{gm^2}{I_B\,K_N} = \frac{(62.6\,x10^{-6})^2}{(12.6\,x\,10^{-6})(305.6\,x\,10^{-6})} = 1.024 \tag{21}$$

The first approach was to set L = 2*Lmin = 240 nm, this gave us a Wp = 11.2 um and Wn = 737 nm, with this W and L values we obtain a voltage gain of only 21 dB gain, which is far from what it was targeted. This is due to the poor output resistance of cmrf8sf process parameters. Through several iterations made to try of obtaining the necessary voltage gain without success, it was decided to change the topology to the one shown in figure 2.8.

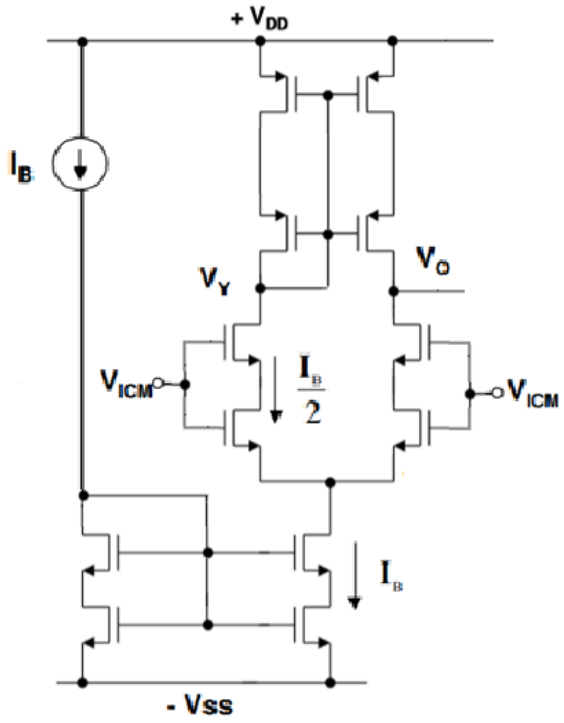

Figure 2-8: Enhanced Rout Simple OTA Topology.

This topology works as a pseudo cascode array; by stacking another pair of transistors on the output node which increases the output resistance. The design of this topology started off with the best result obtained with the simple OTA design, The sizing of the stacked transistor were carefully done to allow the transistors in the bottom to remain in saturation hence giving a better output resistance described in the equation (22) & (23) and hence a better DC voltage gain:

$$R_{out} = (gm_{casn} r_{oncas} r_{on}) | (gm_{casp} r_{ocasp} r_{0p}) \tag{22}$$

$$A_V = gm_{dp} * (gm_{casn} r_{oncas} r_{on}) | (gm_{casp} r_{ocasp} r_{0p}) \tag{23}$$

Regarding the tail transistors, these were sized two times the bottom transistors of the cascode topology and stacked as well to ensure that they could manage the required current. The current mirror also was stacked to allow better output resistance and hence have a less error on copying the bias current, the resistor to set the bias current was designed with the following equation (24).

$$R = \frac{V_{DD} - V_{GS}}{I_B} = \frac{1.2 \; - .359}{12.6 \; x \; 10^{-6}} = 66.74 \; K\Omega \tag{24}$$

These theoretical results were iterated in the simulator and slightly modified to achieve the desired values; the final parameters are shown in the table 2.10.

Parameter	Design spec
IB	12.6 uA
Ln = Lp = Lmirror	2um
Wncas	128 um
Wn	4 um
Wpcas	42.1 um
Wp	25 um
Wnmirror	8 um
Rmirror	67.74 $K\Omega$
Cload	1 pF

Table 2-10: High-Gain OTA Final Parameters.

2.4.3. Replica Circuit Design Methodology

The replica circuit shown in figure 2.9 is a copy of one of the branches of the HS-OTA designed. The main considerations to be taken into account are M1 = M4, RL = $RL_{HS\text{-}OTA,}$ and M5 = M3 * 1/2, the latter is because in the replica circuit, current is only ½ * I_B and we want to mirror I_B so the size has to be 1:2.

Another important design consideration that is worth point out is the M4 diode connection. This is done because on the HS-OTA we have the design constraint of V_{OCM} = V_{ICM}, this set the V_G in M1 is equal to V_D to mimic the same electrical characteristic on the replica circuit we tie the Drain voltage and the Gate voltage on the M4 transistor in the replica circuit.

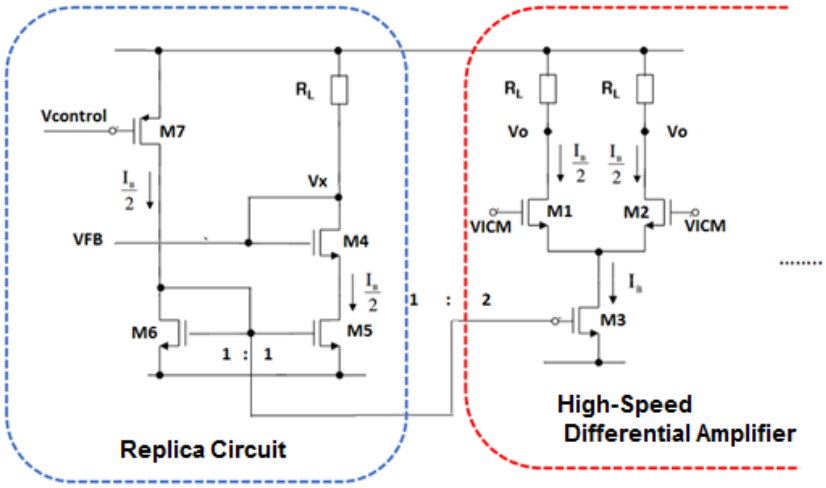

Figure 2-9: Replica Circuit.

The purpose of this replica circuit is to control the voltage on the output nodes V_O of the HS-OTA, so it is always at the same value. To do that, we need to sense the V_X with the High-Gain OTA and with a reference voltage that is what we want to set the V_O to generate a proportional $V_{control}$.

$V_{control}$ is converted to current with the branch that contains the transistor M7 and M6, then the size of transistor M6 has to be equal to M5, so the control current is mirrored 1:1. On the other hand, to size the transistor M7 we first used equations (25) & (26):

$$I_{DS} = \frac{1}{2} K_P \frac{W}{L} (V_{GS} - V_{TH})^2 \tag{25}$$

$$\frac{W}{L} = \sqrt{\frac{I_B K_P}{(V_{GS} - V_{THP})}} \tag{26}$$

This was the first approach but the value obtained created a mismatch at the output of the High-gain OTA, so the W/L was adjusted until the output of the High-gain OTA was set at 0.7 * VDD, the transistor sizes of the replica circuit are shown in the following table 2.11.

Parameter	Design spec
W_{M4}	19.2 um
W_{M5}	19.2 um
W_{M6}	19.2 um
W_{M7}	428 um
$L_{M4,M5,M6}$	180 nm
L_{M7}	720 nm
R_L	795.8 Ω

Table 2-11: Replica Circuit's Transistor Sizing.

2.4.4. Resistor Divider Design Methodology

The resistor divider serves as the reference voltage that we want to set the V_X node of the replicate circuit. It also sets the V_O of the HS-OTA, i.e. the voltage needed on that node is 0.7 *VDD. To obtain the reference voltage, we have used ten resistors with the same value used in the HS-OTA and connect the reference input of the High-gain OTA to the third resistor.

This connection ensures that we will see 0.7 VDD at that node. We choose to use the same resistor on the HS-OTA so any change due to process on the resistors would reflect the same in this reference network. The resistor network is shown in the figure 2.10.

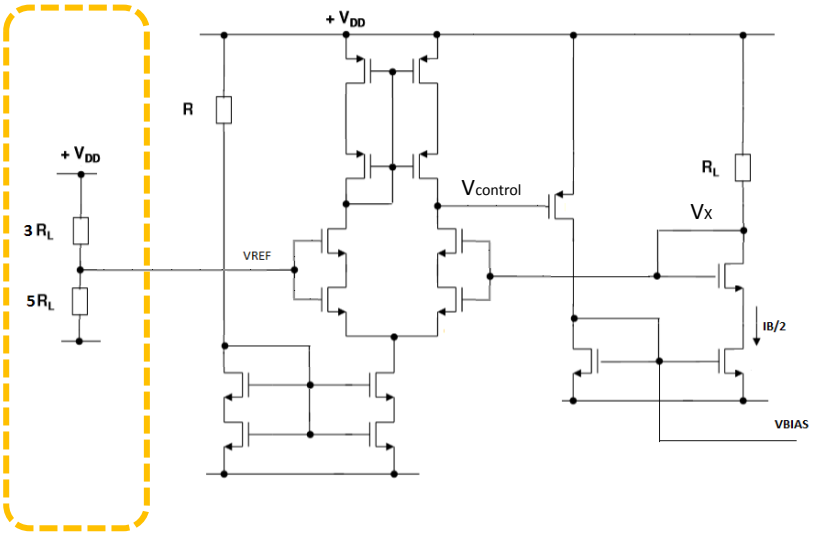

Figure 2-10: Resistor Network on Bias Circuit.

CHAPTER 3: ANALOG RECEIVER PRE-LAYOUT VERIFICATION

3.1. HS-OTA Pre-layout Design Verification

Figure 3.1 and figure 3.2 show the schematic of the HS-OTA and the test bench used for the pre-layout verification respectively. First performance verification was done with typical process parameters, nominal voltage, and nominal temperature.

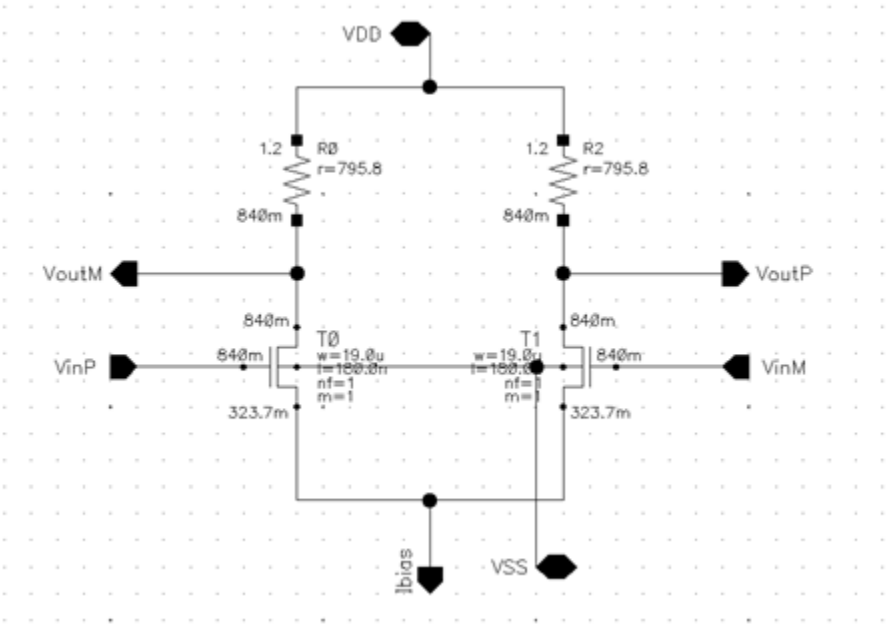

Figure 3-1: HS-OTA Single Stage Schematic.

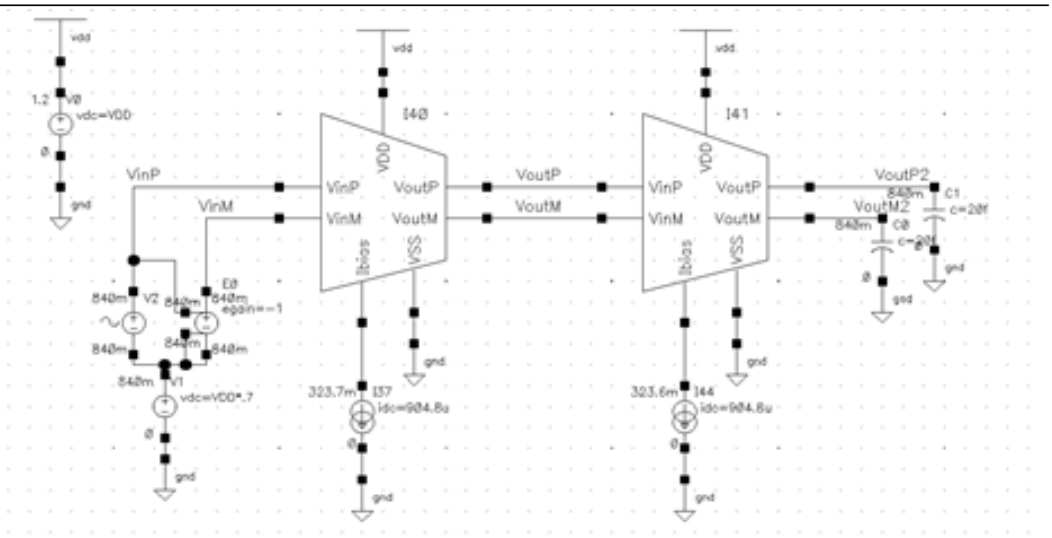

Figure 3-2: HS-OTA Test Bench.

As we can see in the results of AC analysis (figure 3.3) and transient response (figure 3.4), the OTA complies with the design requirements. At this stage we only have tested this portion of the design as stand-alone, we will later verify the results at the top level, i.e. connecting the HS-OTA with the CML to CMOS and Bias Circuits.

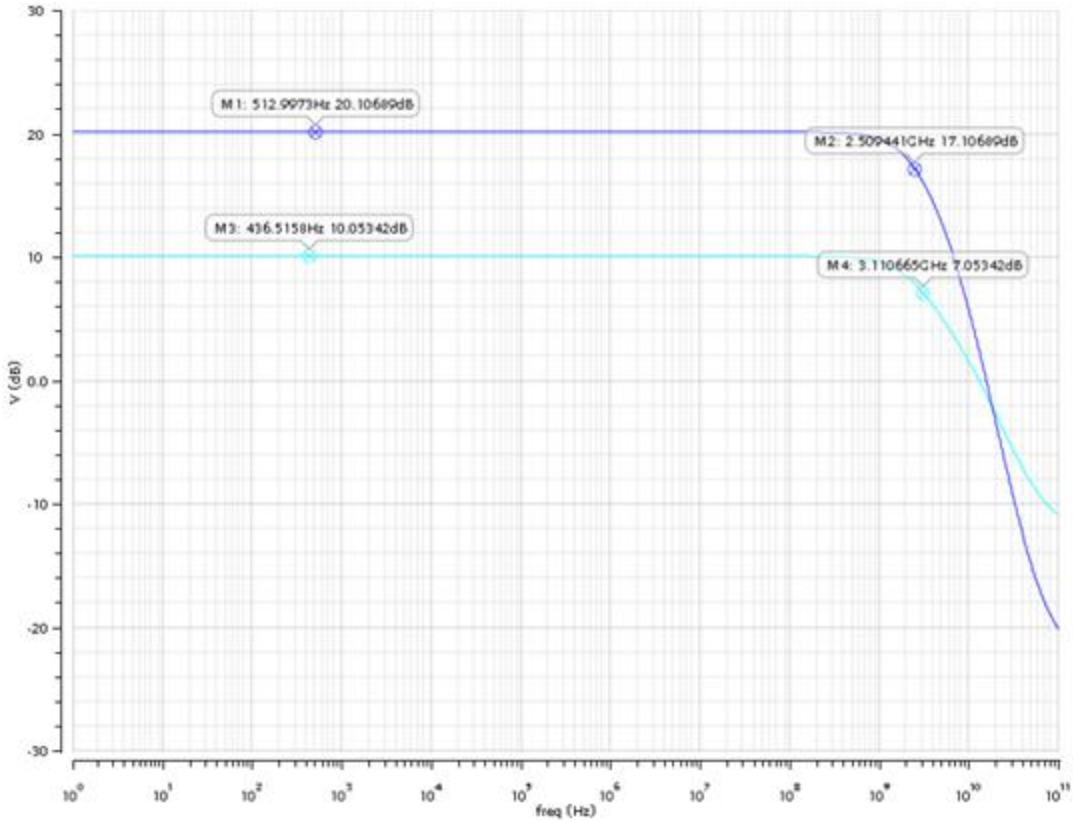

Figure 3-3: HS-OTA AC Response.

Figure 3.4 shows the transient response in single-ended and figure 3.5 the differential response respectively; as we can see in the differential response, the signals swing reach up to 379.54 mV with a differential analog input of 40 mV, the input signal frequency is 1.25 GHz. At this particular frequency, the voltage gain is 19.54 dB.

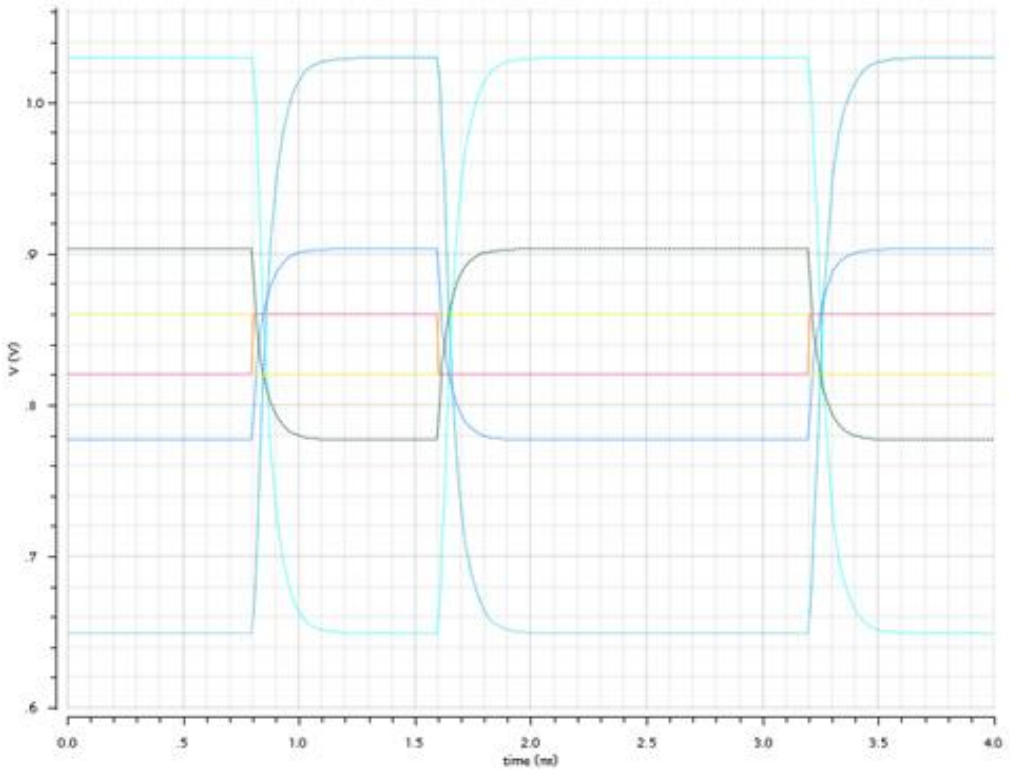

Figure 3-4: HS-OTA Single-Ended Response.

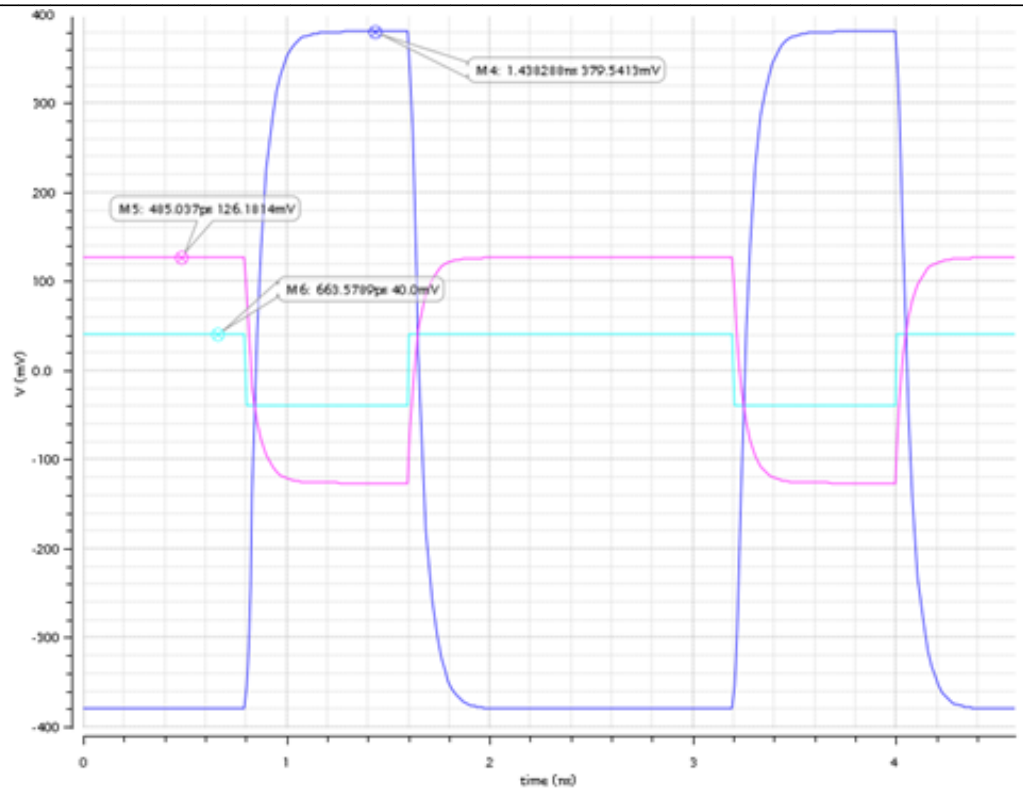

Figure 3-5: HS-OTA Differential Transient Response.

3.2. CML to CMOS Pre-layout design verification

3.2.1. Inverters Pre-layout design verification

The first block designed and verified were the inverters, figure 3.6, 3.7 and 3.8 show the schematics of the 1st, 2nd, and 3rd inverters respectively. As we can see in Figures 3.6 to 3.8, the W were scaled by three times each stage. Figure 17 shows the schematic used for the verification of the design.

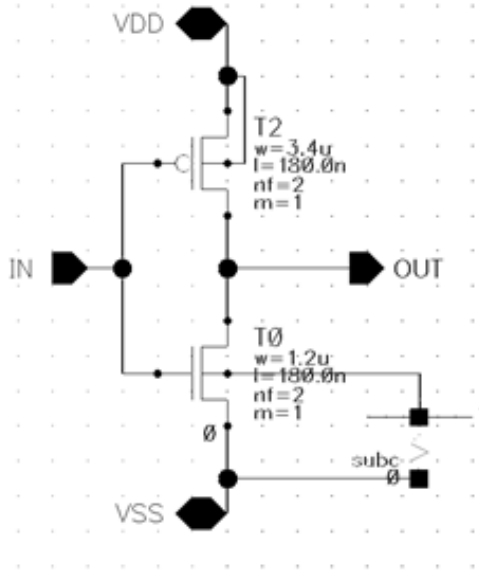

Figure 3-6: First Inverter Schematic.

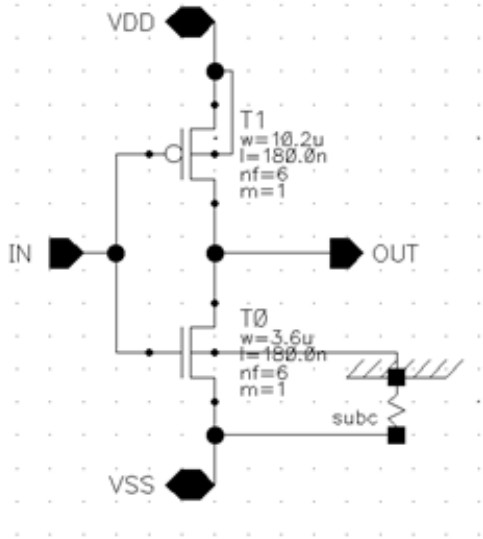

Figure 3-7: Second Inverter Schematic.

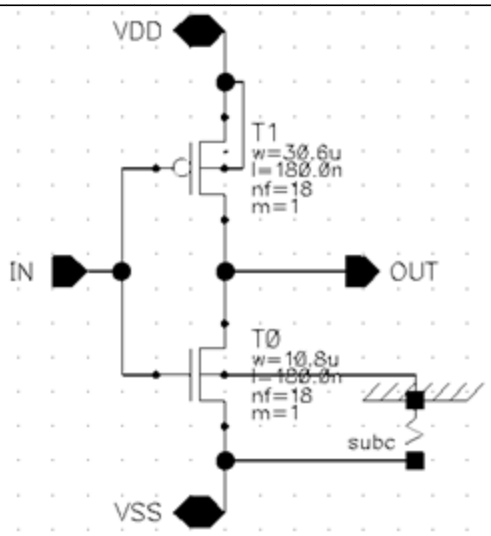

Figure 3-8: Third Inverter Schematic.

Figure 3.9 shows the transient response of the 3rd inverter with 20 fF load, it can be noted that it complies with the design requirement to have the rise and fall times as close as possible, the rise time = 26.46 ps and fall time = 24.67 ps as indicated in Figure 3.9.

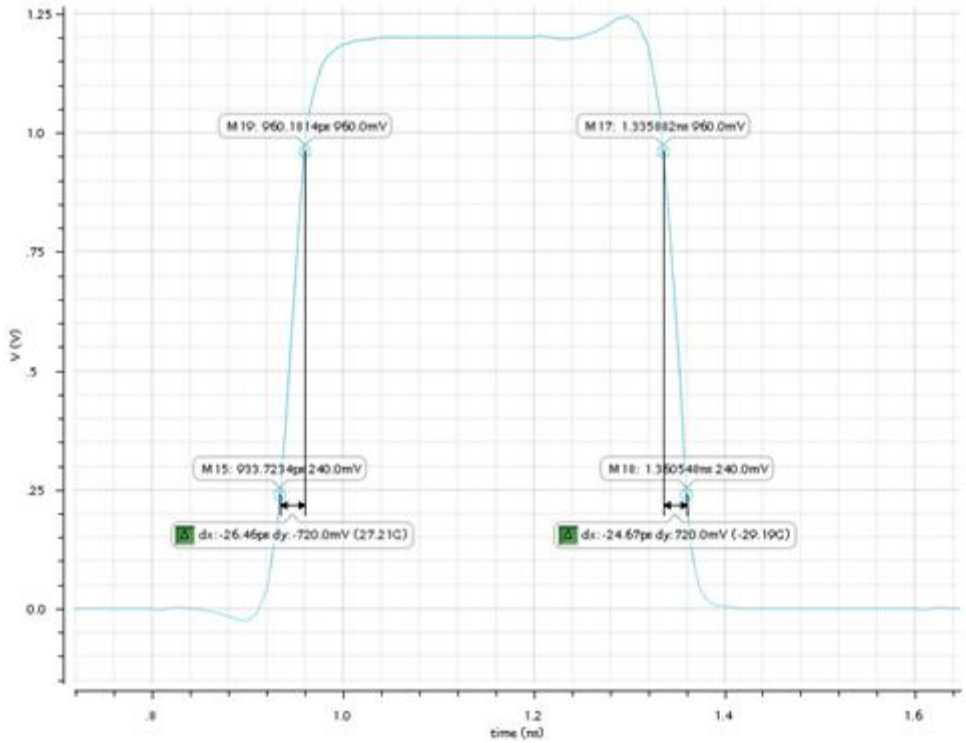

Figure 3-9: Third Inverter Transient Response.

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3.2.2. Differential to single-ended Pre-layout design verification

Figure 3.10 shows the schematic of the differential to single-ended circuit, and figure 3.11 shows the test bench used for verification and tuning the design of this circuit. As discussed in the design methodology section, we used this test bench to verify the change of common mode from 0.7 VDD to 0.5 VDD and the bandwidth of the HS-OTA at 2.5 GHz.

Figure 3.12 shows the transient response of the differential to single-ended circuit with an input stimulus of 40 mV differential and 1.25 GHz frequency with “1011010101” 10-bit pattern. We observe the design complies with the design requirements.

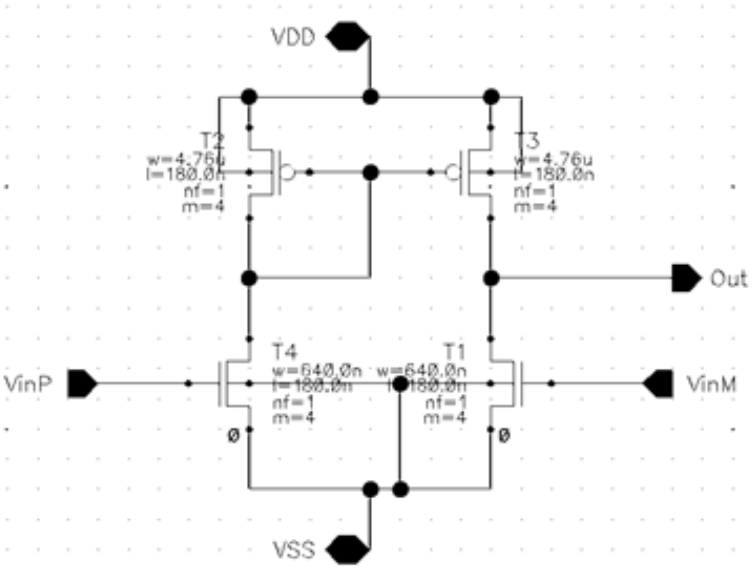

Figure 3-10: Differential to Single-Ended Circuit Schematic.

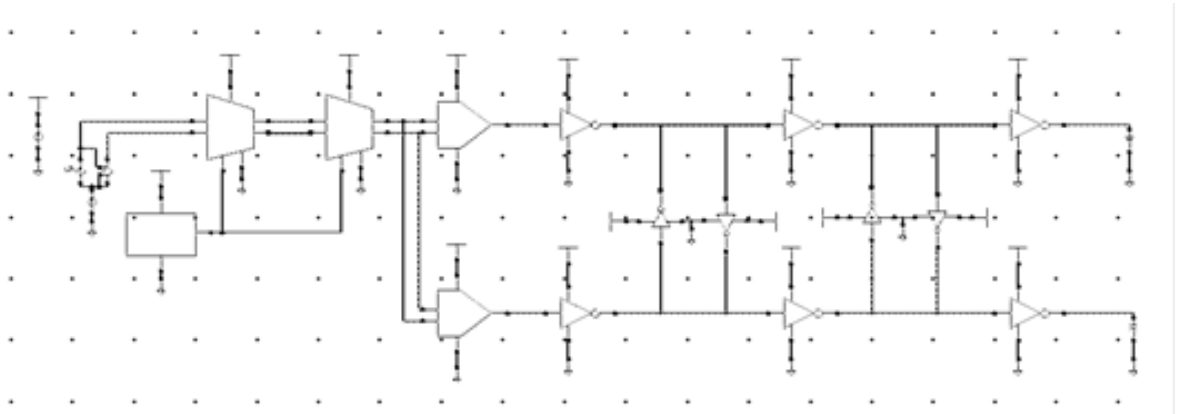

Figure 3-11: Analog Receiver Top-Level Test Bench.

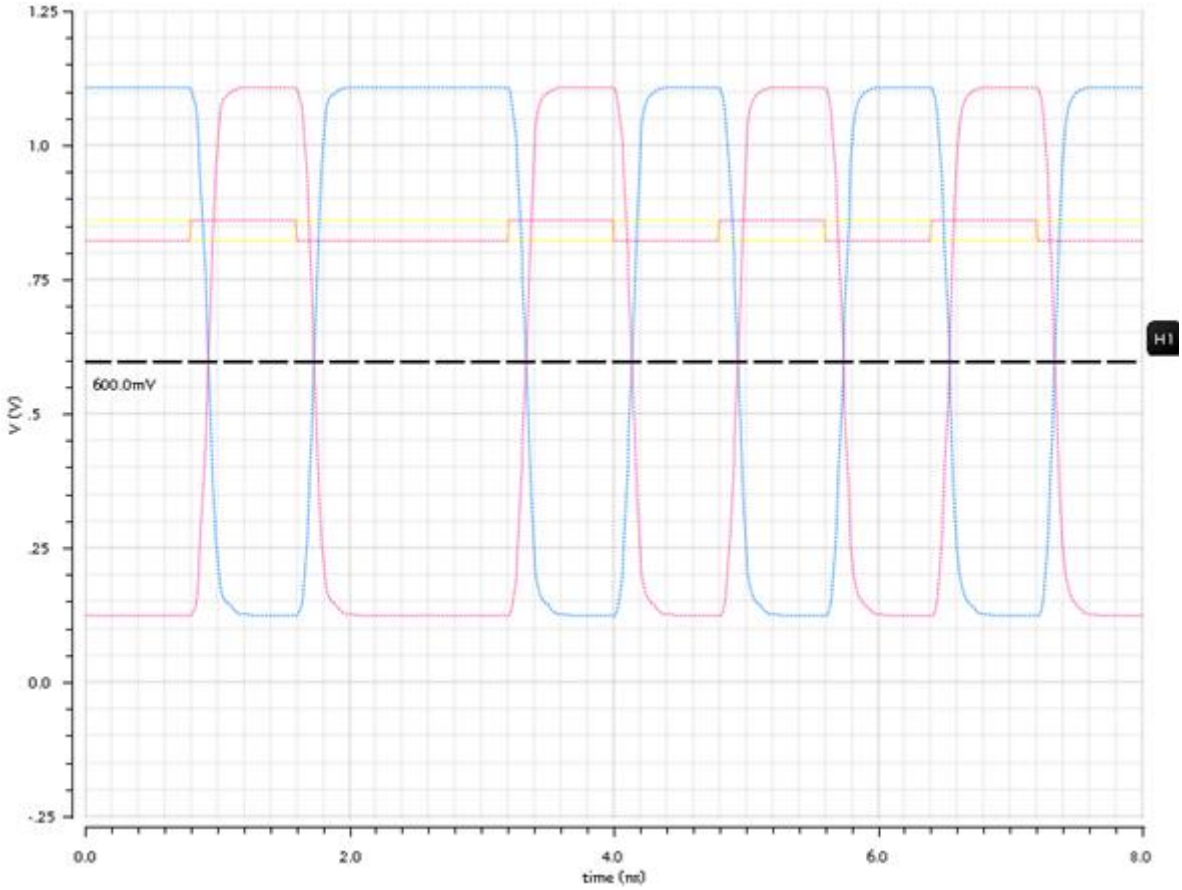

Figure 3-12: Differential To Single-Ended Transient Response.

3.3. Bias Circuit Pre-Layout Design Verification

3.3.1. High-Gain OTA Pre-Layout Design Verification

Figure 3.13 shows the schematic used for the pre-layout verification. Figure 3.14 shows the test bench using a 1 pF load and nominal conditions (Nominal PVT). As we can see in the results in figure 3.15, the obtained voltage gain is close to 40 dB, and the GBW reaches 7.9 MHz; these results are considered well enough for the Bias circuit purpose.

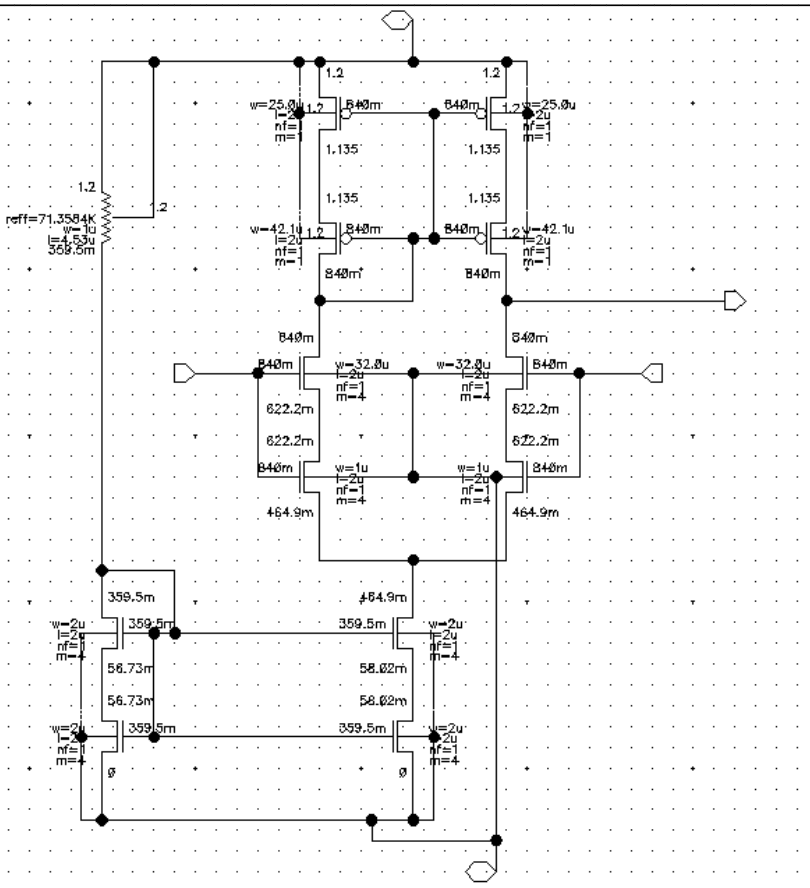

Figure 3-13: High-Gain OTA Schematic.

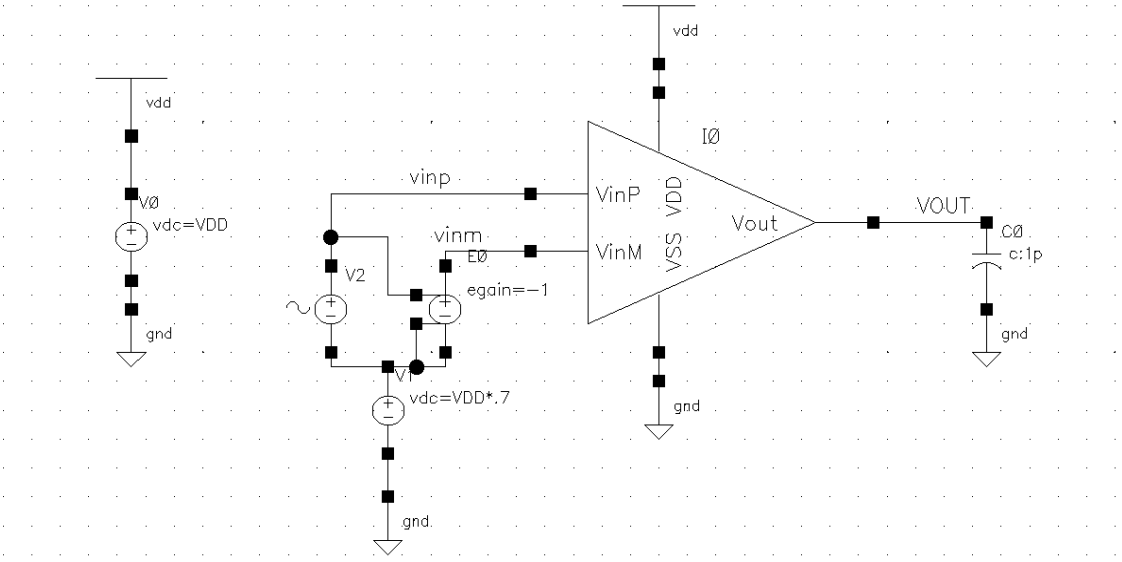

Figure 3-14: High-Gain OTA Test Bench.

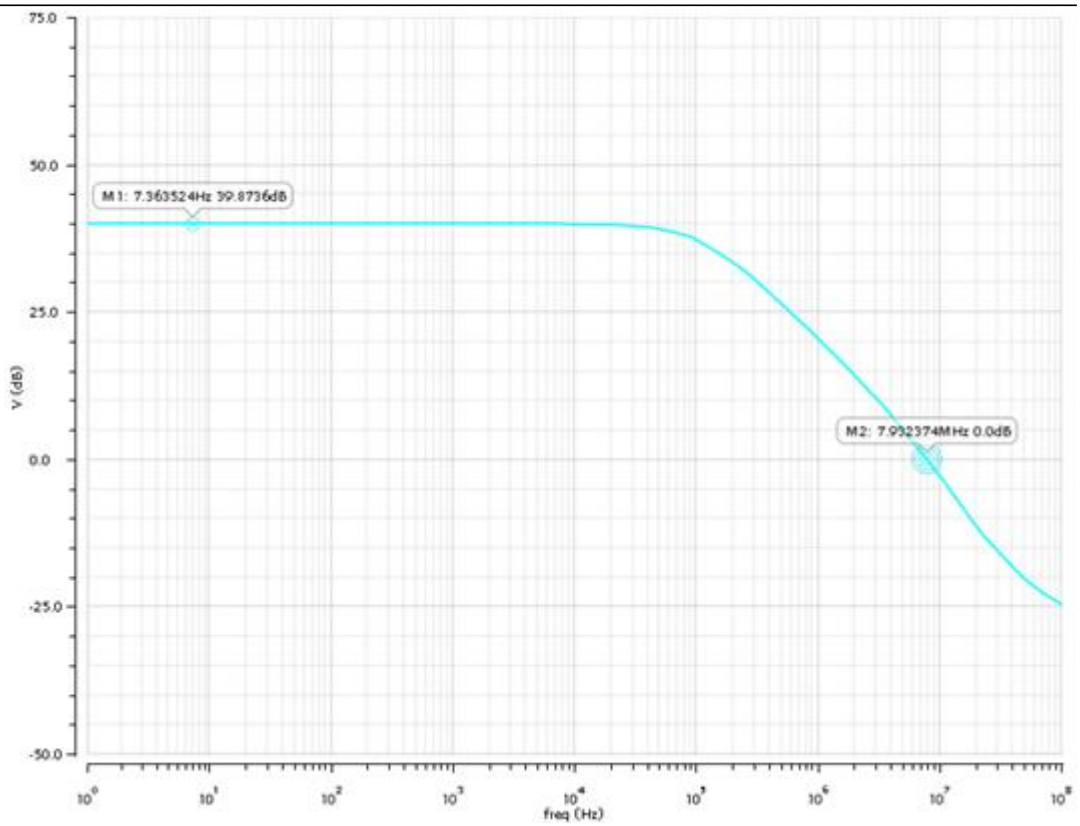

Figure 3-15: High-Gain OTA Voltage Gain Response.

3.3.2. Bias Circuit Top Pre-layout design verification

Once the High-Gain OTA has been verified and it satisfies the requirements, we proceed to validate the Bias circuit at the top level with all three blocks connected (High-Gain OTA + replica circuit + resistor divider). Note this is a close loop system then we must verify the circuit loop gain, its stability across PVT and the effect of mismatch.

To measure the loop gain, we use the Middlebrooks's method [9] that requires opening the loop and measure a shunt current and a series voltage. Figure 3.16 and 3.17 shows the test bench used for this purpose. As we can see on these figures, the loop is opened at the feedback point, a test voltage and current sources are placed without disturbing the circuit's behavior.

Figure 3.18 shows the phase distribution of a mismatch analysis at worst-case corner (Process fast, high voltage, low temperature); we set at minimum phase margin of 50 degrees to be considered safe. As we can see in the plot the circuit's phase margin is always greater than 50 degrees. It is worth point out that a capacitor of 7 pF was put on the output of the amplifier to tie to VDD. This capacitor was used to reduce the Gain-bandwidth product and improve the phase margin of the circuit.

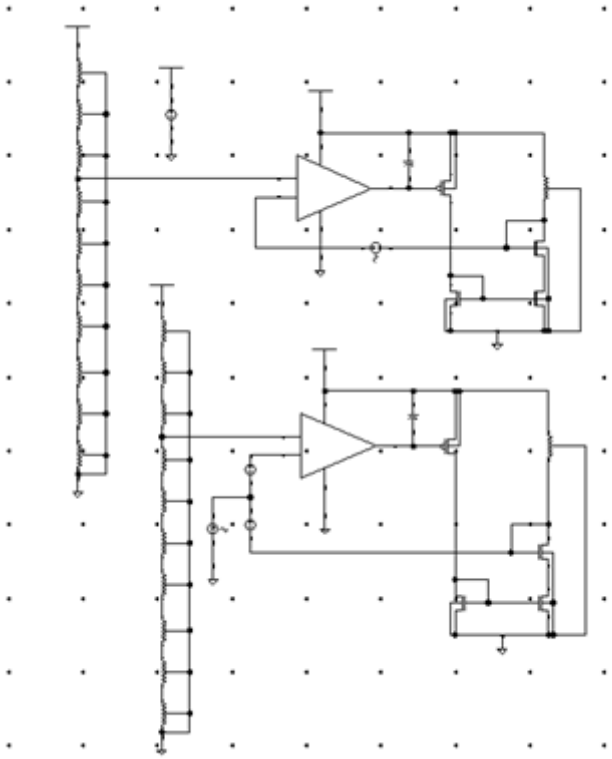

Figure 3-16: Close Loop Verification Test Bench.

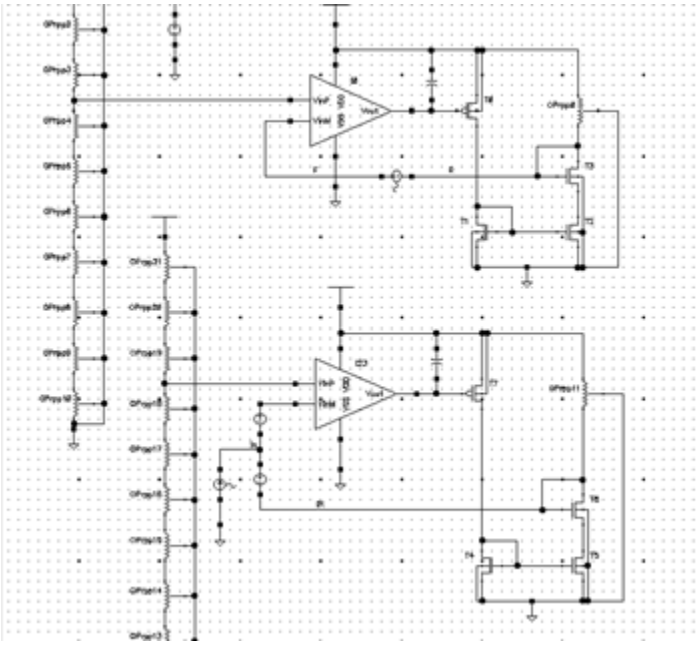

Figure 3-17: Close Loop Verification Test Bench Zoom

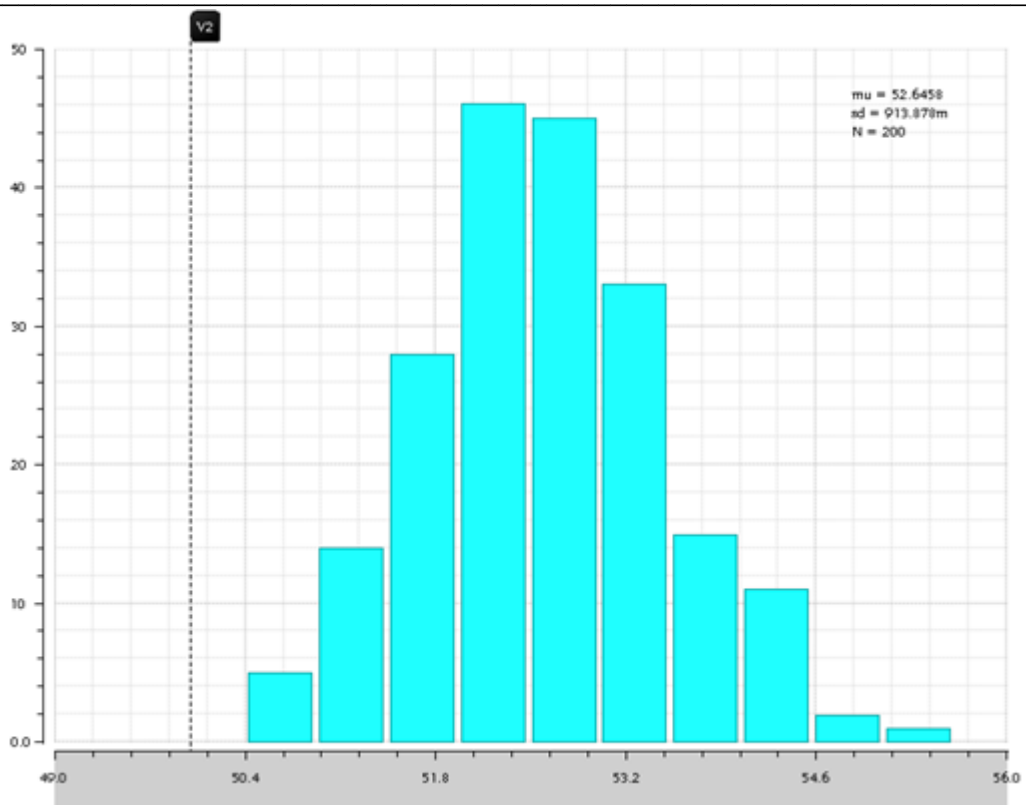

Figure 3-18: Phase Margin Distribution Results.

3.4. Analog Receiver Top Level Pre-layout design verification

With all blocks verified as standalone cells, we now proceed to test the whole analog receiver at the top level. Figure 3.19 shows the top-level testbench used; the load used for the top level is 20 fF. Notice this capacitive load might be adjusted depending on the C_{in} of the digital RX module but 20 fF is a good estimation.

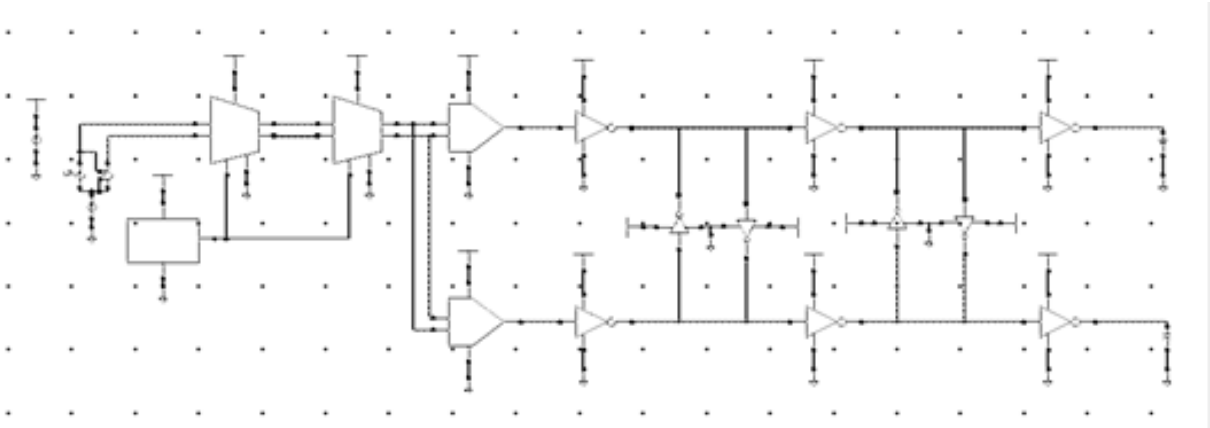

Figure 3-19: Analog Receiver Module Top-Level Test Bench.

The bandwidth of the HS differential amplifier was verified again now at the top level across PVT and mismatch, the PVT corners used for testing of the top level are shown in Table 3.1, and the PVT AC response is provided in figure 3.20 and the mismatch at nominal PVT response is given in figure 3.21.

The results indicate that the worst voltage gain and 3 dB BW are 16.9 dB and 2.47 GHz respectively in the SS process and 125 C temperature (Figure 3.20). These results are good enough for the functionality of the analog receiver, in the appendix are the mismatch results at other PVT corners.

Process	Temperature	Voltage
Typical	65 C	1.2 V
Fast	125 C	1.26 V
Slow	125 C	1.26 V
Fast	- 40 C	1.14 V
Slow	- 40 C	1.14 V

Table 3-1: PVT Corners [10].

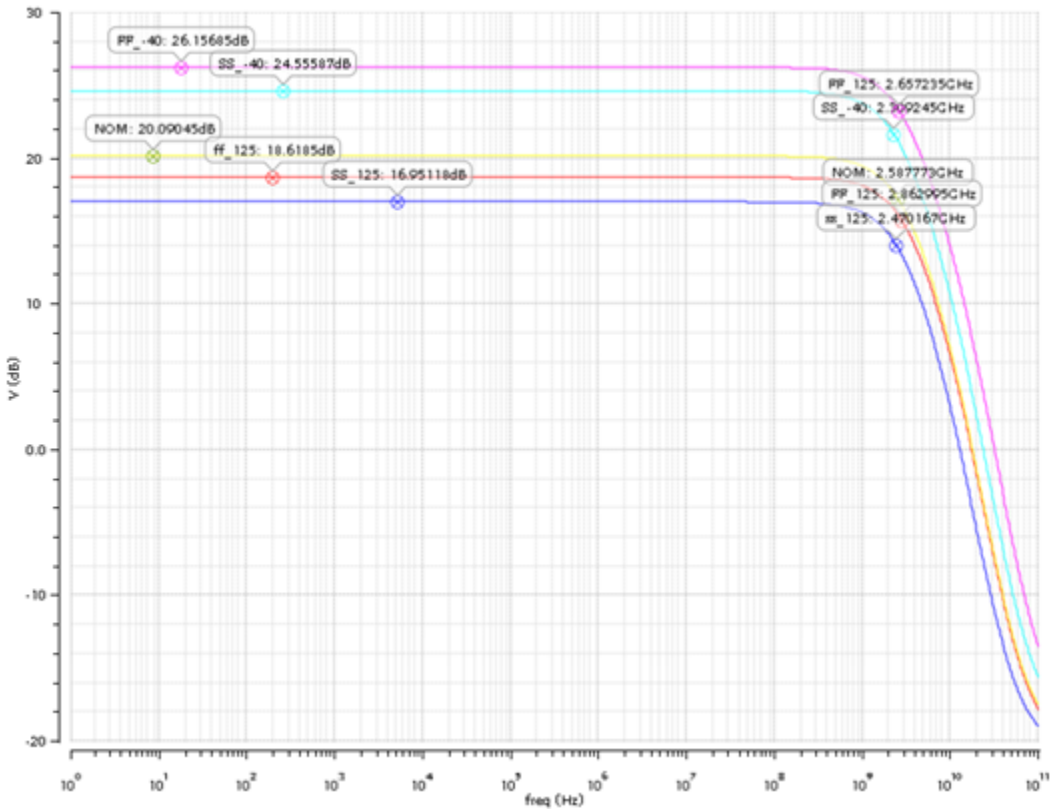

Figure 3-20: HS-OTA PVT AC Response.

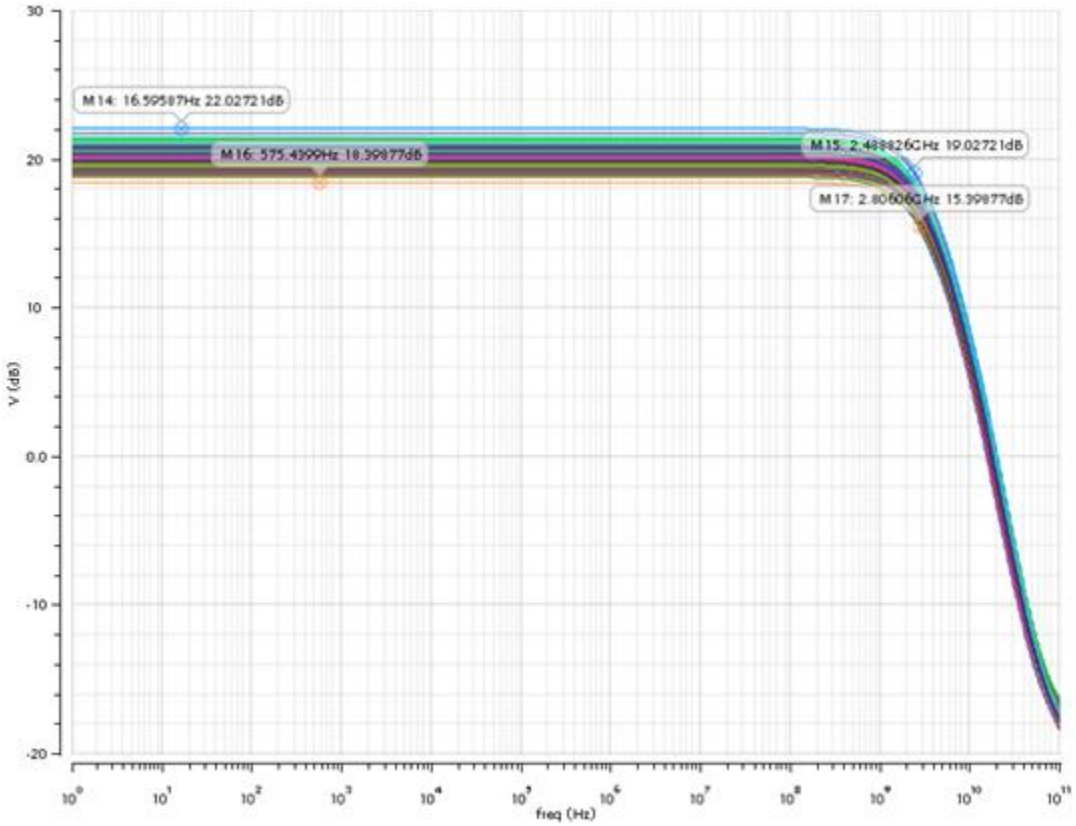

Figure 3-21: HS-OTA AC Response under Mismatch Analysis.

Following the signal path, we also verified the CML to CMOS response; figure 3.22 shows the differential to single ended transient response at nominal conditions. We see that the signal crosses at 600 mV which is the requirement set for the design, the signal does not reach full rail to rail swing, but its amplitude is sufficient to drive the first inverter and then reach the rail to rail swing.

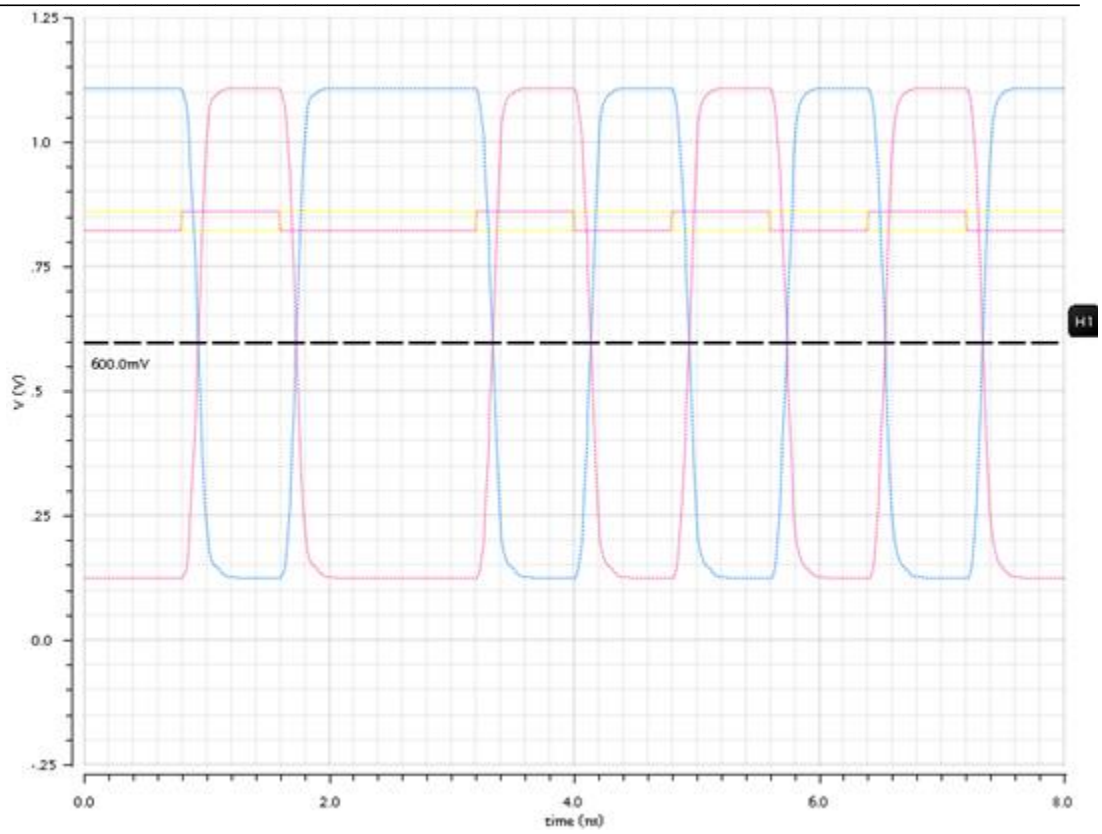

Figure 3-22: Differential To Single-Ended Transient Response at Nominal PVT

Figure 3.23, 3.24 and 3.25 shows the transient response of the first, second and third inverters respectively with the same stimulus. As we can see on each stage the output signal reaches rail to rail swing, and the crossing is at around ~ 600 mV, at each stage, we have a faster slew rate.

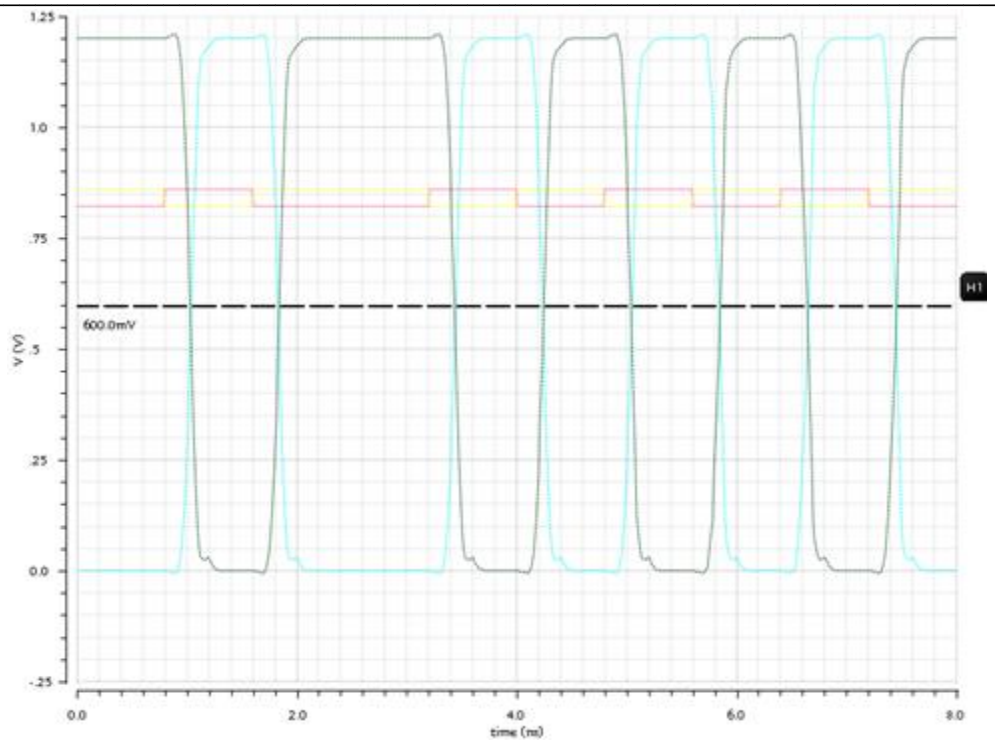

Figure 3-23: First Inverter Transient Response at Nominal PVT

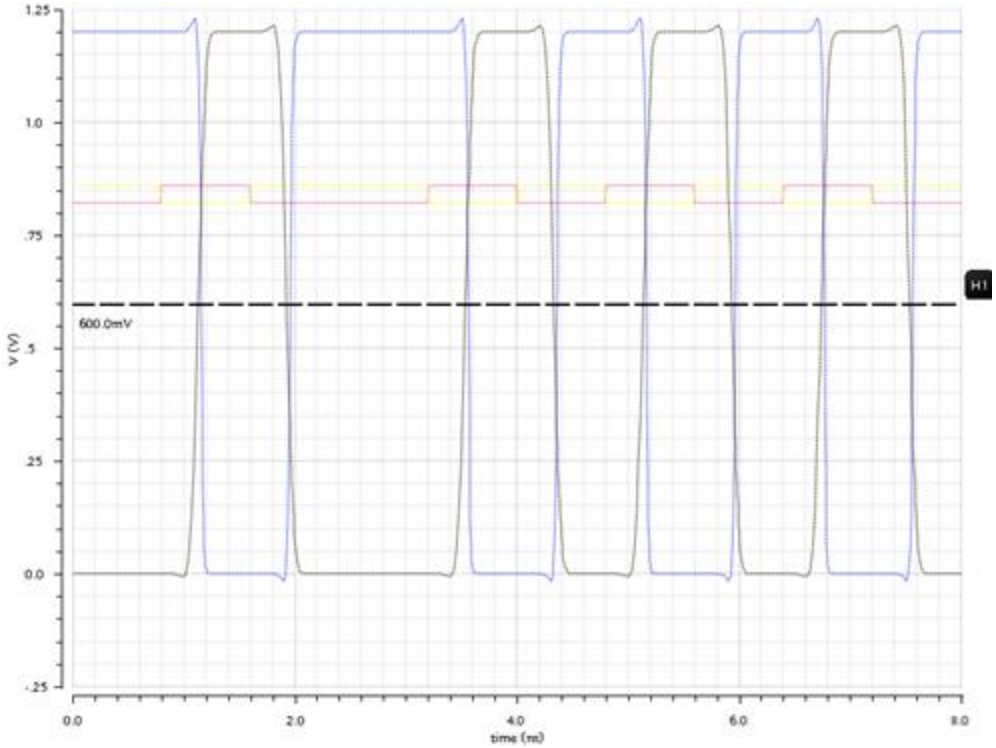

Figure 3-24: Second Inverter Transient Response at Nominal PVT

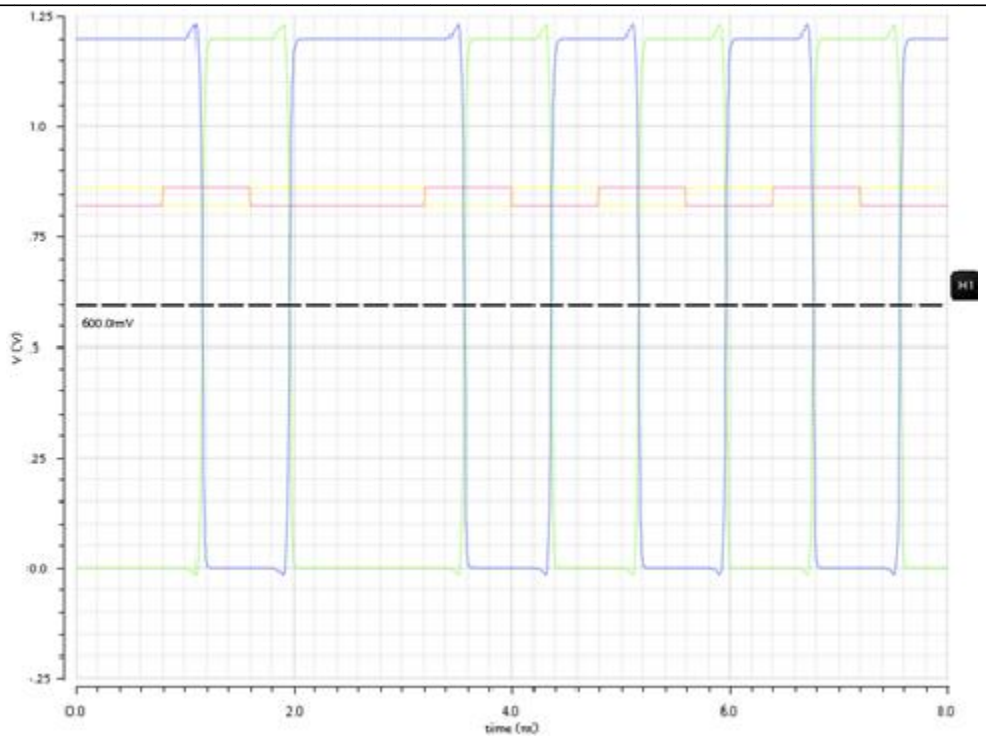

Figure 3-25: Third Inverter Transient Response at Nominal PVT

Finally, we did a mismatch analysis monitoring the output of the last inverter in the analog receiver. We have performed a transient analysis at nominal PVT conditions (see the result in figure 3.26), in which we can observe the output tracks the input stimulus without any issues.

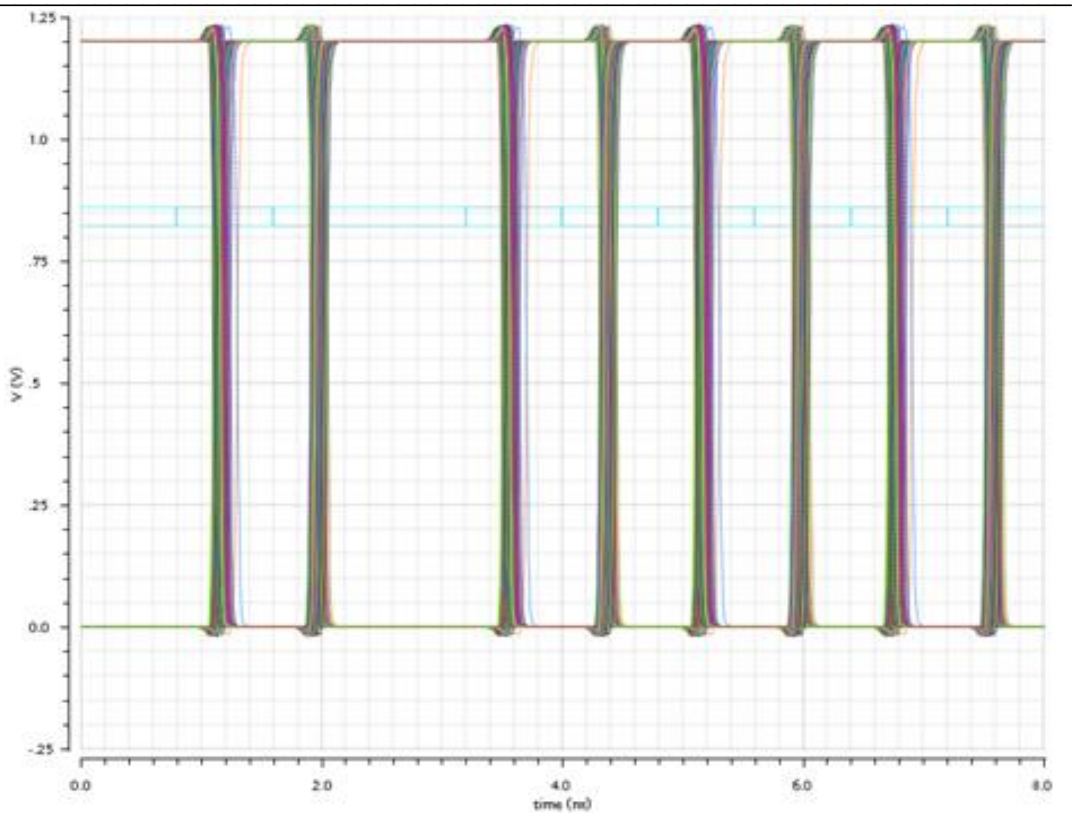

Figure 3-26: Analog Reciever Top Transient Response Under Mismatch Analysis at Nominal PVT

All previous results give us confidence that our design complies with the specifications at the pre-layout phase. Now we can continue with the layout design and finally do post-layout verifications and make all the necessary adjustments if needed.

CHAPTER 4: ANALOG RECEIVER LAYOUT DESIGN

4.1. HS-OTA Circuit Layout

For the layout design of the HS-OTA, the ideal resistors were changed by the resistor pCell of the cmrf8sf process and also a nwell contact was added. It is worth notice that the number of fingers and multiplicity were modified in transistor pCells. This was done to have an easier time doing the layout design, the overall W/L remains the same as in the pre-layout schematic, figure 4.1 shows the final schematic for the layout design.

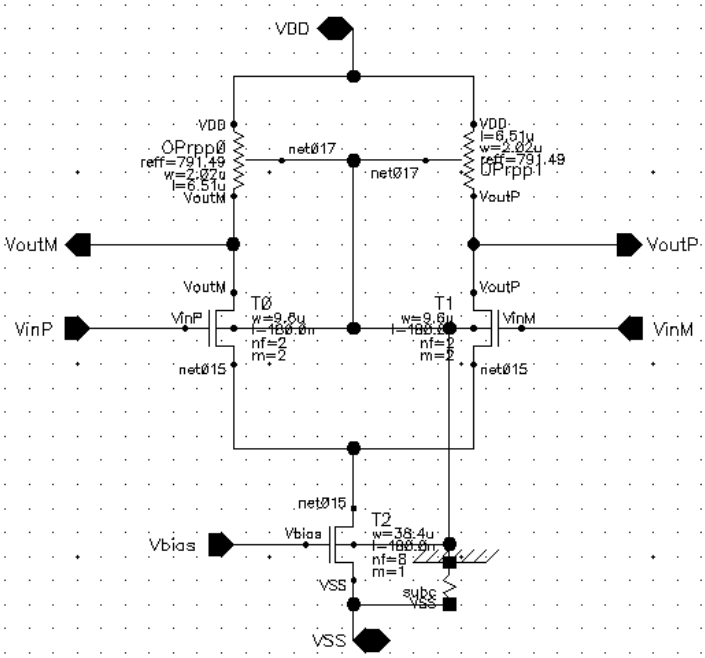

Figure 4-1: HS-OTA Single Stage Schematic For Layout Design.

Because analog circuits are sensitive to process variations as a function of layout position on the wafer, the Common Centroid layout technique was used to reduce this effect. Shown in figure 4.2 are devices A and B that have been split up into two areas as Common Centroid where process gradient effects are minimized [12].

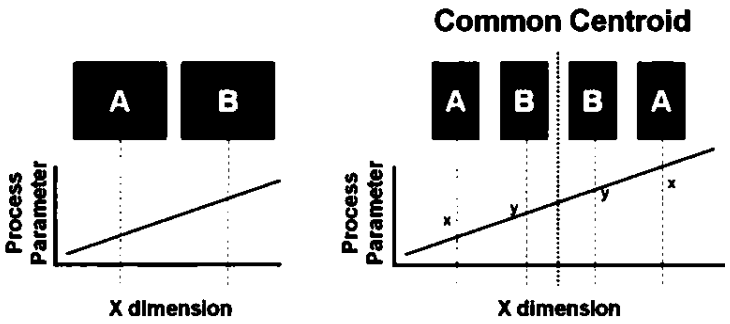

Figure 4-2: Common Centroid Layout Technique.

Figure 4.3 shows the first layout of the HS differential amplifier, the differential pair (in the middle) was done following the common centroid technique, and the tail transistor(bottom) was done interdigitated, at the bottom the nwell contact can be seen.

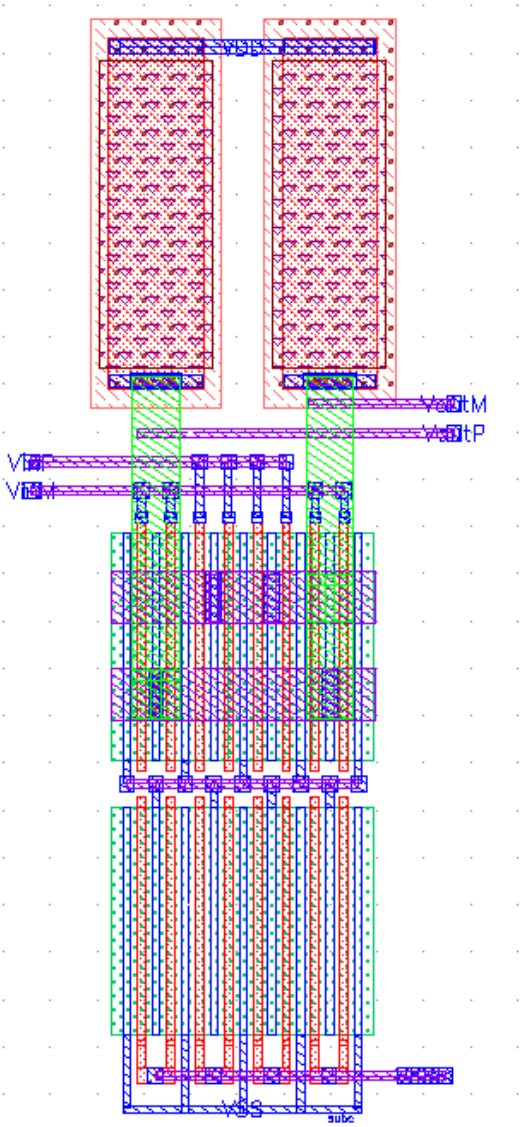

Figure 4-3: HS-OTA Single Stage Layout.

4.2. CML to CMOS Circuit Layout

4.2.1. Inverters Circuit Layout

Figure 4.4, 4.5 and 4.6 show the layout of the first, second and third inverter on the CML to CMOS circuit; all these inverters have the same height to make the integration easier.

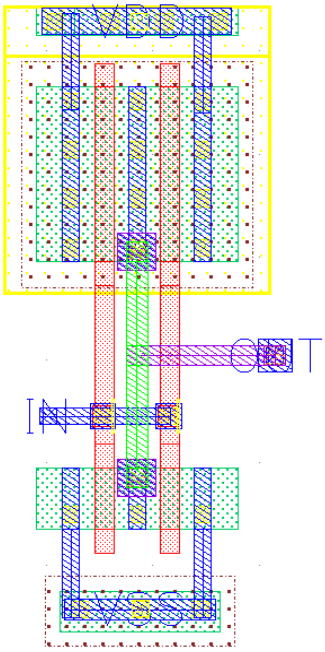

Figure 4-4: First Inverter Layout.

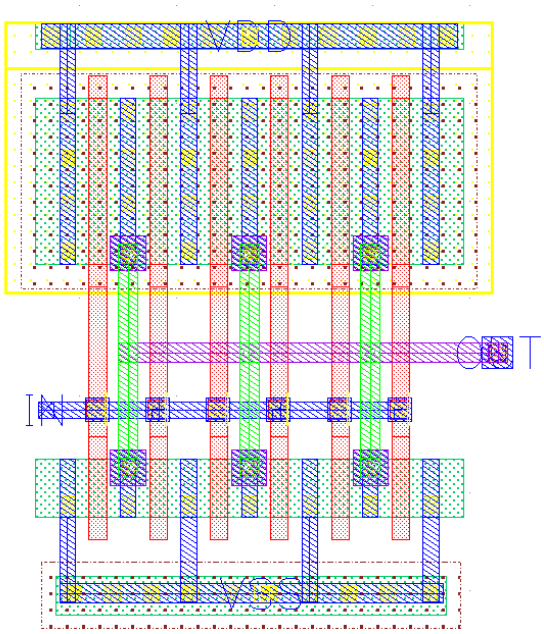

Figure 4-5: Second Inverter Layout.

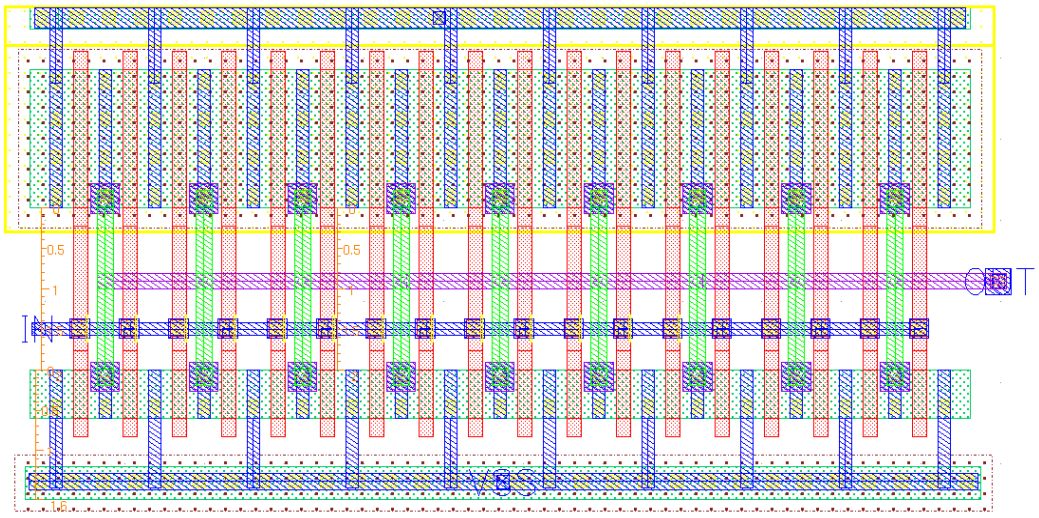

Figure 4-6: Third Inverter Layout.

The inverters used in the DCC layouts are the same as the first and second inverter only the W is half the value.

4.2.2. Differential to single-ended circuit Layout

Figure 4.7 shows the schematic used for the layout of the differential to single-ended circuit; for this layout, the common centroid technique was used as well both in the current mirror load and the differential pair. Figure 4.8 shows the first layout; pCell were utilized for the transistors, and the nwell connector can be seen at the bottom.

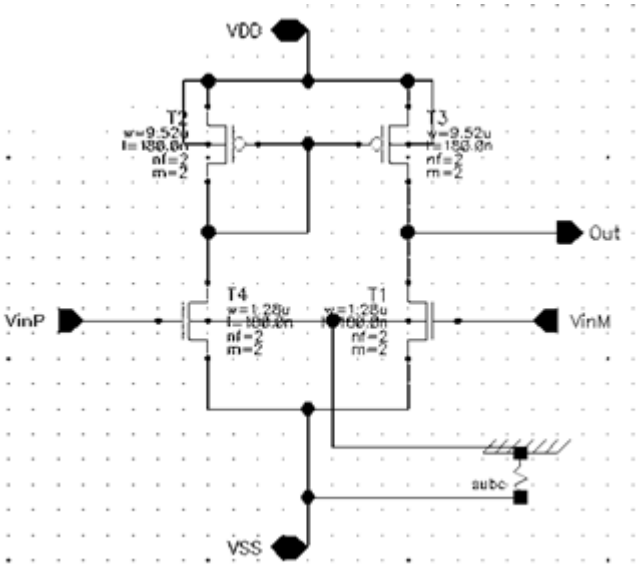

Figure 4-7: Differential To Single-Ended Schematic For Layout.

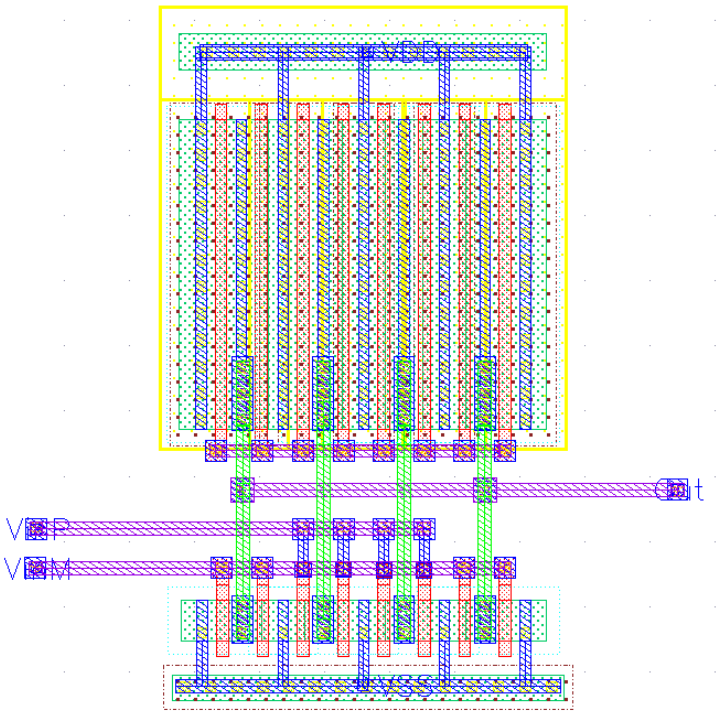

Figure 4-8: Differential To Single-Ended Layout.

4.3. Bias circuit Layout

4.3.1. High-Gain OTA Layout

Figure 4.9 shows the schematic used for the High-Gain OTA layout; it was decided to split the resistor into ten independent resistors so we can place them manually, this circuit also was done using the common centroid technique. Figure 4.10 shows the first layout of the High-Gain OTA.

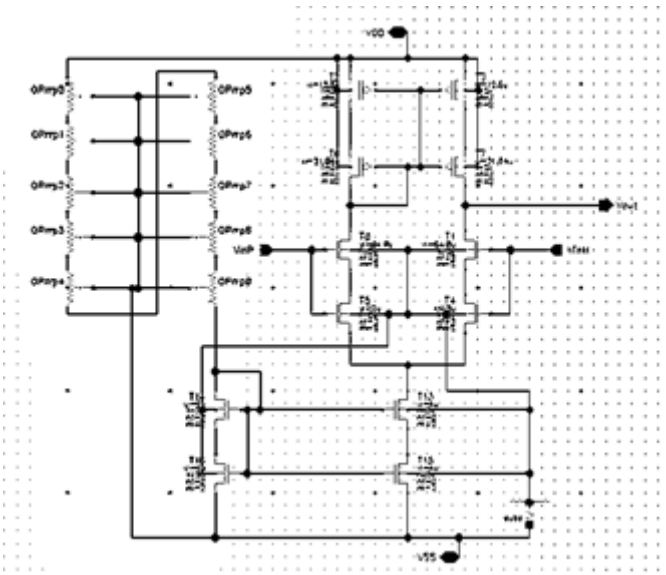

Figure 4-9: High-Gain OTA Schematic For Layout.

The layout in figure 4.10 was carried out using the common centroid technique in all component (current mirror load, differential pair & tails) it is worth nothing that this layout was challenging due to the pseudo cascode topology. The resistor arrangement was made so the total height of the resistors matches almost same the total High-Gain OTA's height.

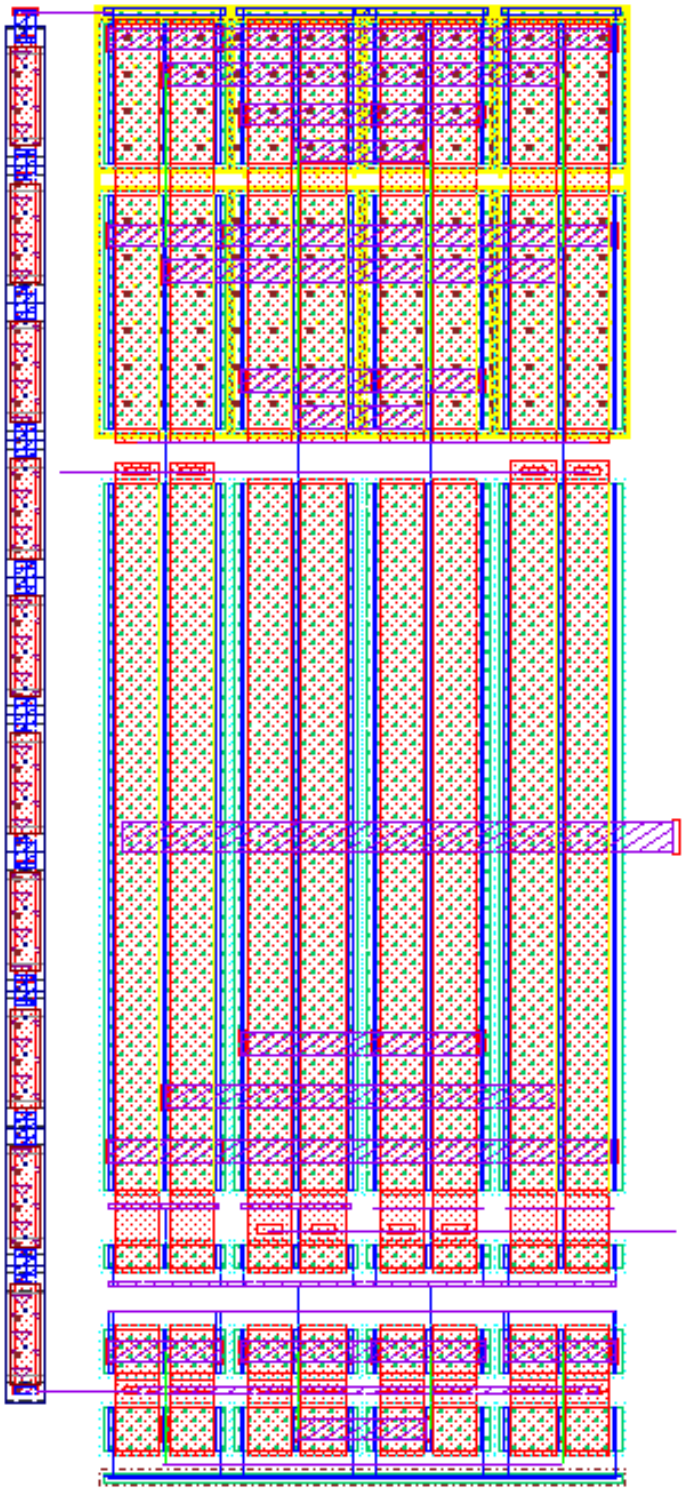

Figure 4-10: High-Gain OTA Layout.

4.3.2. Bias Circuit Top Layout

Figure 4.11 shows the Bias Circuit's layout. At the layout's top-right corner the replica circuit is shown. This portion of the layout was placed here, so it was as close as possible to the HSRX Path layout.

Bias circuit requires large capacitor (at least seven pF) to ensure stability, thus for the capacitors layout; we have used "dual mim" type capacitors from cmrf8sf library. In particular, 7.3 pF was achieved with eight dual mim capacitors of 11 µm x 11 µm each connected in parallel. The placement of capacitors was done in such way that the final layout would give a rectangular shape to help its integration to the HSRX path.

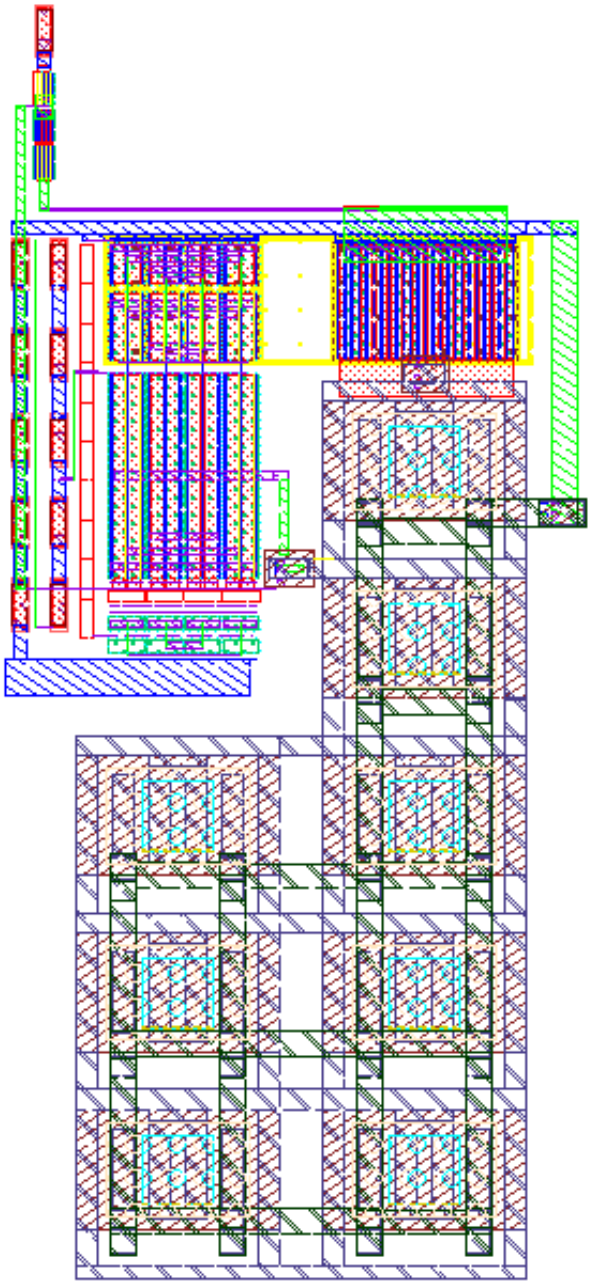

Figure 4-11: Bias Circuit Top Layout.

4.4. Analog Receiver Floor Plan and Layout integration

4.4.1. Analog Receiver Floor Plan

In order to integrate the analog receiver layout and facilitate its LVS and DRC verifications, it was decided to break down the layout design into two main blocks: the HSRX path, which consists of the HS differential Amplifier plus the CML to CMOS circuit, and the Bias Circuit, figure 4.12 shows the floor plan diagram of the analog receiver module.

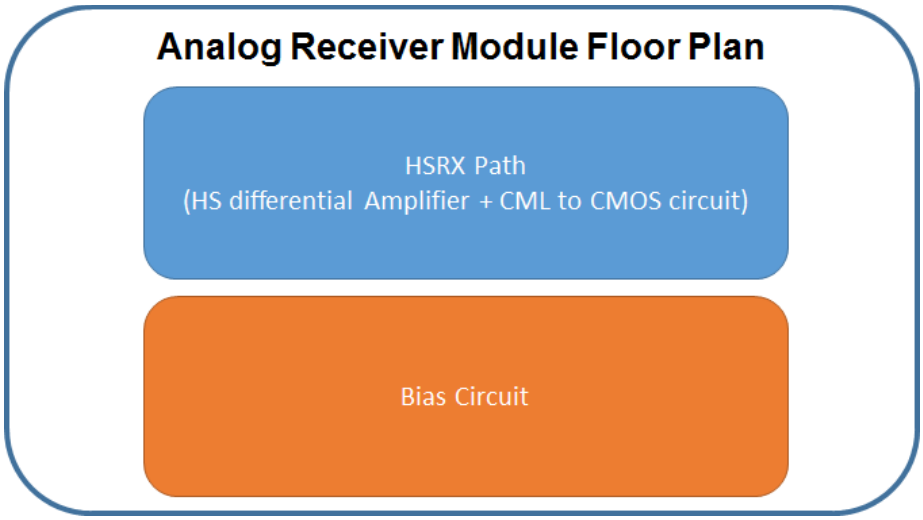

Figure 4-12: Analog Receiver Floor Plan Diagram.

4.4.2. HSRX Path Layout

Figure 4.13 shows the layout of the HSRX Path. At the left side, we see the two cascaded HS-OTAs that conforms the HS differential amplifier and at the right side, the differential to single-ended and inverters that compose the CML to CMOS circuit. The wiring was done as symmetrical as possible to avoid unbalanced charges, especially on the differential pairs.

For the Analog modules (High-Speed differential amplifier & Bias High-Gain OTA) the common centroid layout technique was used, for the digital modules (Inverters), were broken down in fingers.

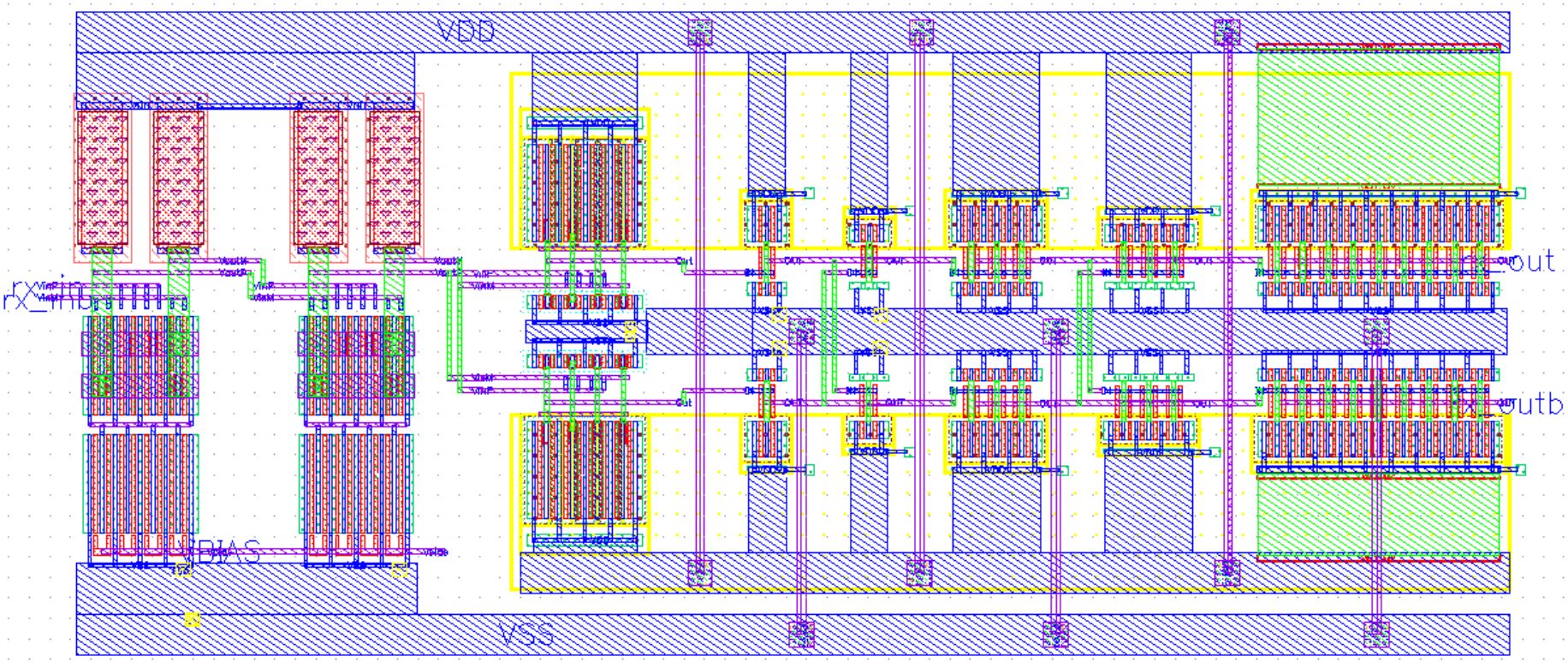

Figure 4-13: HSRX Path Layout.

4.4.3. Analog Receiver Layout Integration

Figure 4.14 shows the layout of whole Analog Receiver module which integrates the HSRX Path (the top) and the Bias Circuit (bottom). This occupy an area of 91.48 µm x 205.74 µm = 18,822 μm^2 = 0.018 mm^2. Notice the SerDes chip area target is four mm^2. Therefore the Analog Receiver module layout should not be an area issue when integrates with others modules of SerDes chip.

Figure 4.15 shows a close-up of the HSRX Path layout, in which we observe the replica circuit is as close as possible to the HS-OTA. In the same sense, Figure 4.16 shows a close-up at the High-Gain OTA showing how it is connected to the Capacitors array and the PMOS used to convert the voltage response to current.

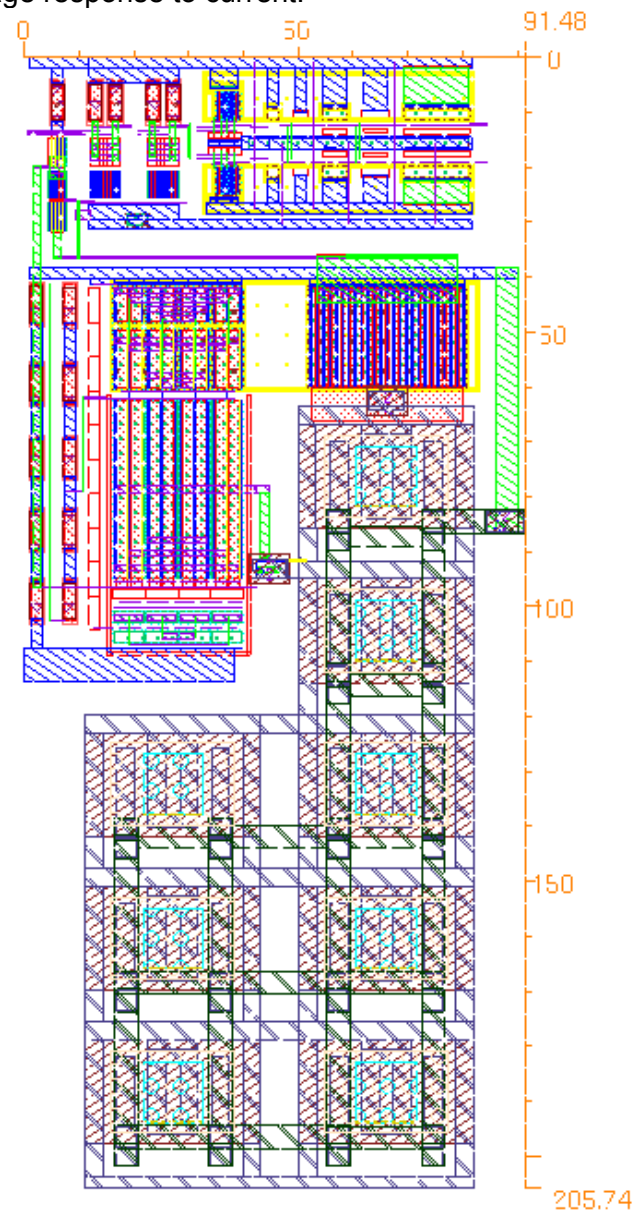

Figure 4-14: Analog Receiver Top Layout

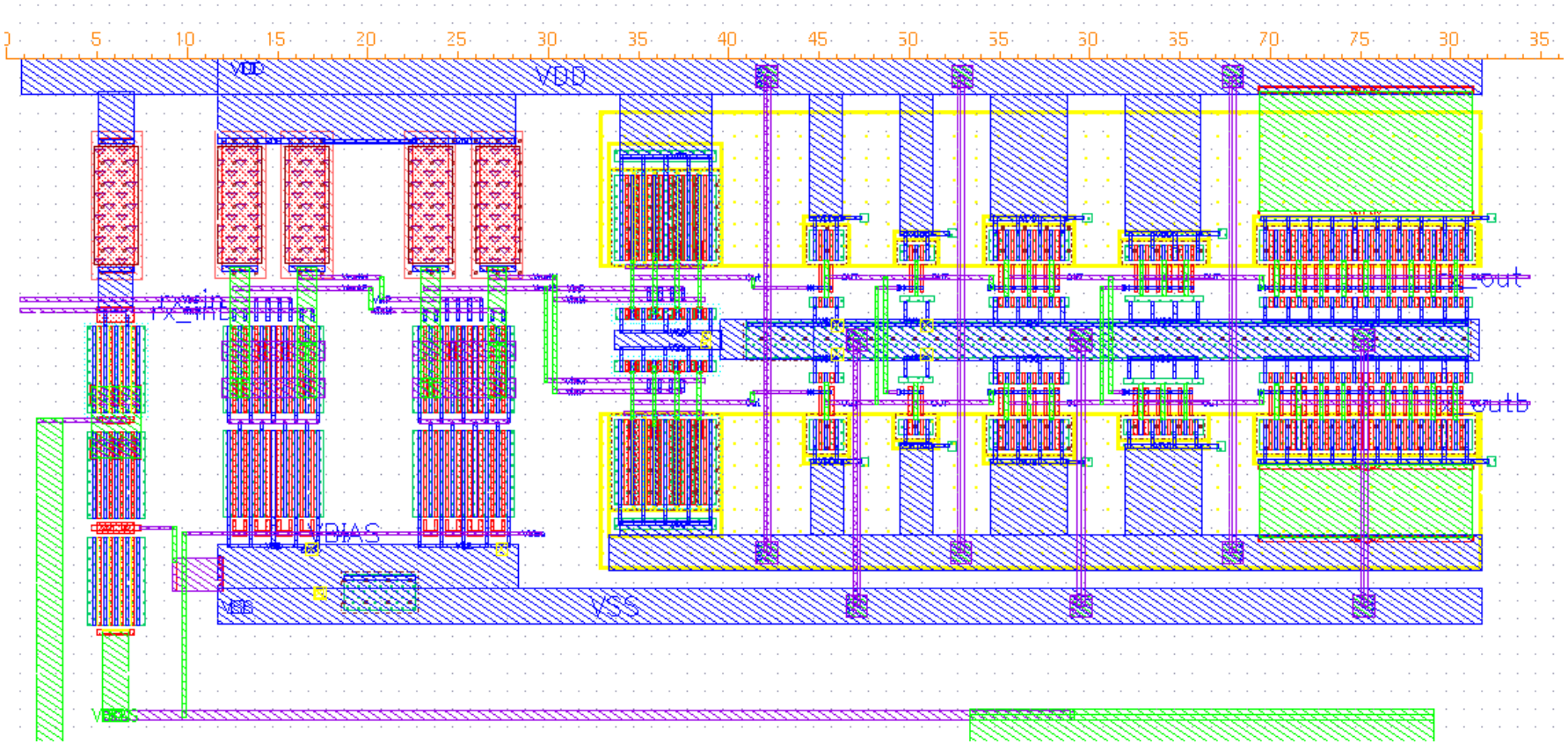

Figure 4-15: Analog Receiver Top Layout Zoom to HSRX Path.

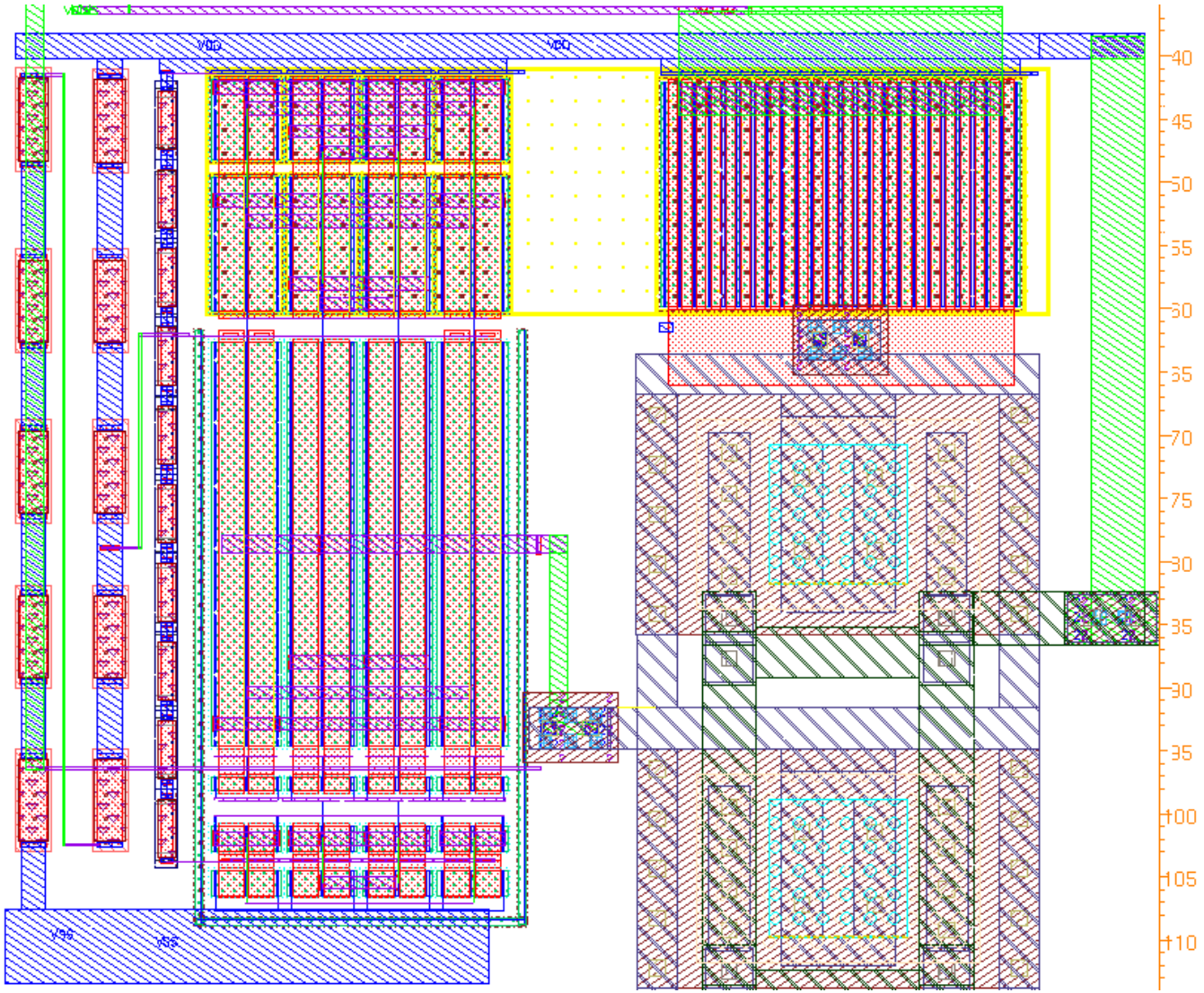

Figure 4-16: Analog Receiver Top Layout Zoom to High-Gain OTA.

CHAPTER 5: ANALOG RECEIVER POST-LAYOUT VERIFICATION

5.1. Analog Receiver Post-layout design verification

Once the Layout design stage was finished, we perform post-layout simulations; we used the test bench shown in figure 5.1. Figure 5.2 shows the specific connection of HSRX Path and Bias circuit.

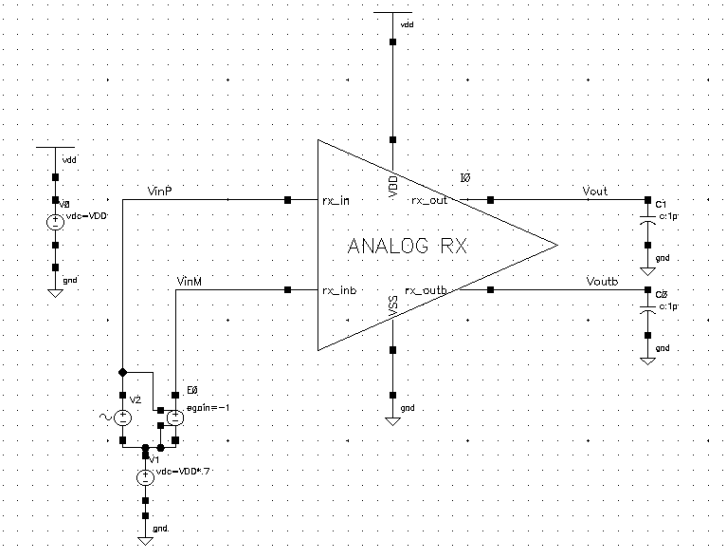

Figure 5-1: Analog Receiver Top-Level Test Bench.

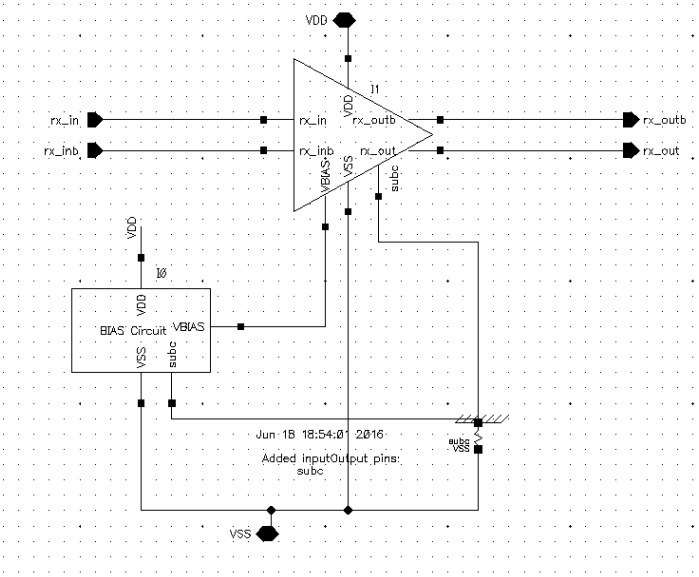

Figure 5-2: Analog Receiver Hierarchy Top-Level Test Bench.

Before post-layout simulations, we have extracted parasitics from the layout using Mentor Graphics' Calibre PEX tool. Table 1 and 2 show a summary of parasitic resistances and capacitances extracted from HSRX Path and Bias circuit respectively. It is important to notice that even though the layout wiring was done as symmetrical as possible, we notice however some unbalance in capacitance. The more sensitive nets to this unbalance are the ones of differential OTAs.

VoutP and VoutN presents a difference of 7.9% as seen in the table 1 rows 3 and 4 and column C + CC total, VoutP2 and VoutM2 in rows 5 and 6 have a 5.8% difference; this could lead to an error on the bandwidth and gain target. Nevertheless, we can tune these wiring to lower these capacitance differences if needed.

Layout Net	Source Net	R_Count	C_Total(F)	CC_Total(F)	C+CC_Total(F)
VDD	VDD	279	46.498E-15	15.509E-15	62.007E-15
VSS	VSS	359	23.791E-15	15.366E-15	39.157E-15
3	VoutP	43	1.412E-15	4.955E-15	6.367E-15
4	VoutM	43	1.300E-15	4.599E-15	5.899E-15
5	VoutP2	51	2.218E-15	6.482E-15	8.700E-15
6	VoutM2	51	2.159E-15	6.063E-15	8.222E-15
7	VoutSingle2	17	1.336E-15	2.814E-15	4.150E-15
8	VoutSingle	17	1.334E-15	2.816E-15	4.151E-15
9	VoutB_1	41	2.444E-15	2.774E-15	5.217E-15
10	VoutB1	41	2.419E-15	2.616E-15	5.035E-15
11	VoutB_2	129	5.217E-15	5.746E-15	10.963E-15
12	VoutB2	129	5.189E-15	5.592E-15	10.781E-15
VBIAS	VBIAS	31	2.692E-15	1.750E-15	4.441E-15
rx_inb	rx_inb	7	584.756E-18	1.095E-15	1.680E-15
rx_in	rx_in	7	641.001E-18	1.069E-15	1.710E-15
rx_outb	rx_outb	53	1.063E-15	4.142E-15	5.206E-15
rx_out	rx_out	53	1.085E-15	4.035E-15	5.120E-15
175	XI88/net14	25	628.653E-18	2.417E-15	3.046E-15
176	XI59/net14	25	628.915E-18	2.420E-15	3.049E-15
X173/18	XI114/net015	150	660.110E-18	5.894E-15	6.554E-15
X174/18	XI115/net015	150	660.110E-18	5.888E-15	6.548E-15

Table 5-1: HSRX Path (HS-OTA + CML to CMOS Circuit) Extraction Results.

Layout Net	Source Net	R_Count	C_Total(F)	CC_Total(F)	C+CC_Total(F)
VDD	VDD	129	4.25E-14	1.30E-13	1.73E-13
2	net032	358	9.44E-14	1.16E-13	2.10E-13
3	net6	70	1.11E-14	1.31E-14	2.42E-14
4	4	1	3.40E-15	2.02E-15	5.41E-15
5	net22	113	8.62E-16	3.34E-15	4.20E-15
VBIAS	VBIAS	138	7.90E-15	2.20E-14	2.99E-14
7	net1	13	8.12E-15	4.79E-15	1.29E-14
VSS	VSS	154	1.56E-14	4.24E-15	1.98E-14
X27/20	XI0/net018	435	4.53E-15	5.93E-15	1.05E-14
X27/21	XI0/net02	39	6.68E-15	3.51E-15	1.02E-14
X27/22	X27/22	1	1.46E-16	2.60E-17	1.72E-16
X27/23	X27/23	1	1.46E-16	0	1.46E-16
X27/24	X27/24	1	1.46E-16	0	1.46E-16
X27/25	X27/25	1	1.45E-16	5.51E-18	1.50E-16
X27/26	X27/26	1	1.35E-16	2.29E-17	1.58E-16
X27/27	X27/27	1	1.35E-16	2.22E-17	1.57E-16
X27/28	X27/28	1	1.46E-16	3.26E-17	1.78E-16
X27/29	X27/29	1	1.46E-16	0	1.46E-16
X27/30	X27/30	1	1.46E-16	0	1.46E-16

Table 5-2: Bias Circuit Extraction Results.

5.2. HS-OTA Post-layout Design Verification

Figure 5.3 shows the AC response comparison of the HS-OTA pre-layout vs. post layout at nominal PVT (Typical process, 1.2 V of supply voltage & 65 °C operating temperature).

The solid line represents the Post-Layout response, and the dotted line represents the Pre-Layout response. It is interesting to notice that post-layout AC response gives more voltage gain ~1% higher, while the 3 dB Bandwidth decreases ~17%. These variations are attributed to layout parasitics.

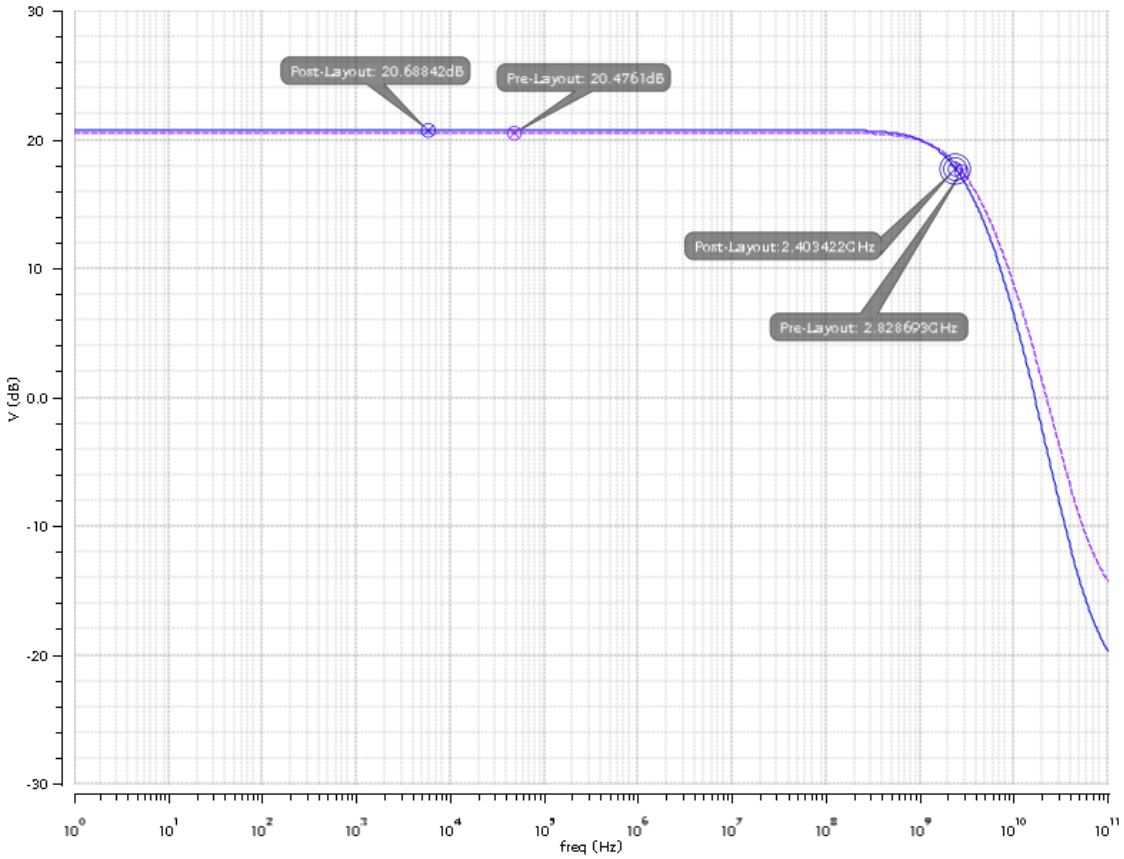

Figure 5-3: HS-OTA Pre-Layout vs. Post-Layout AC Response at Nominal PVT.

Figure 5.4, shows the AC response at different PVT corners shown in Table 5.3, again the solid line represents the Post-layout response and the dotted line the Pre-layout response, Post-layout response has ~1% higher voltage gain in all PVT cases versus Pre-layout.

The maximum value of voltage gain (26.79 dB) is achieved at ff process and -40C temperature and the lowest value of voltage gain (17.51 dB) at ss process and 125C temperature.

Figure 5.5, shows the 3 dB Bandwidth at the different PVT corners, all cases have the difference of ~400MHz, highest bandwidth is achieved at ff process and 125 C temperature, lowest bandwidth is obtained at ss process and -40C temperature.

Process	Temperature	Voltage
Typical	65 C	1.2 V
Fast	125 C	1.26 V
Slow	125 C	1.26 V
Fast	- 40 C	1.14 V
Slow	- 40 C	1.14 V

Table 5-3: PVT Corners.

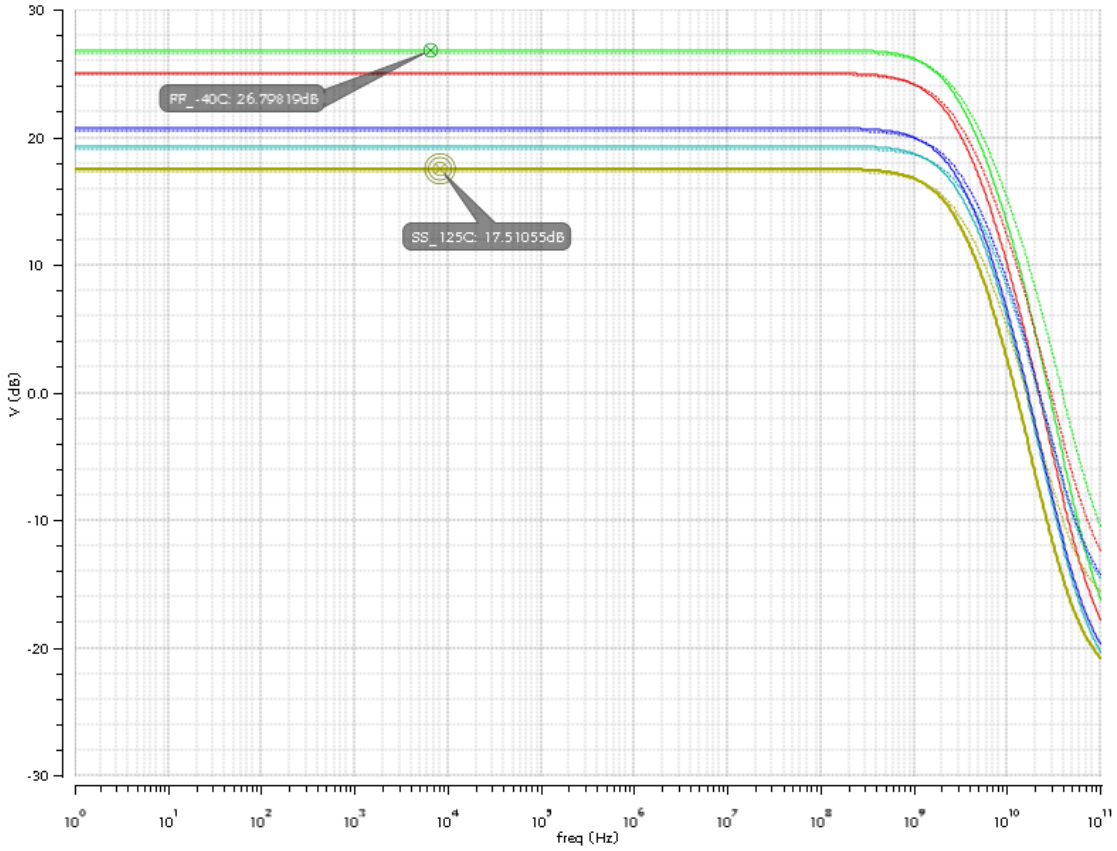

Figure 5-4: HS-OTA Pre-Layout vs. Post-Layout AC Response across PVT Corners.

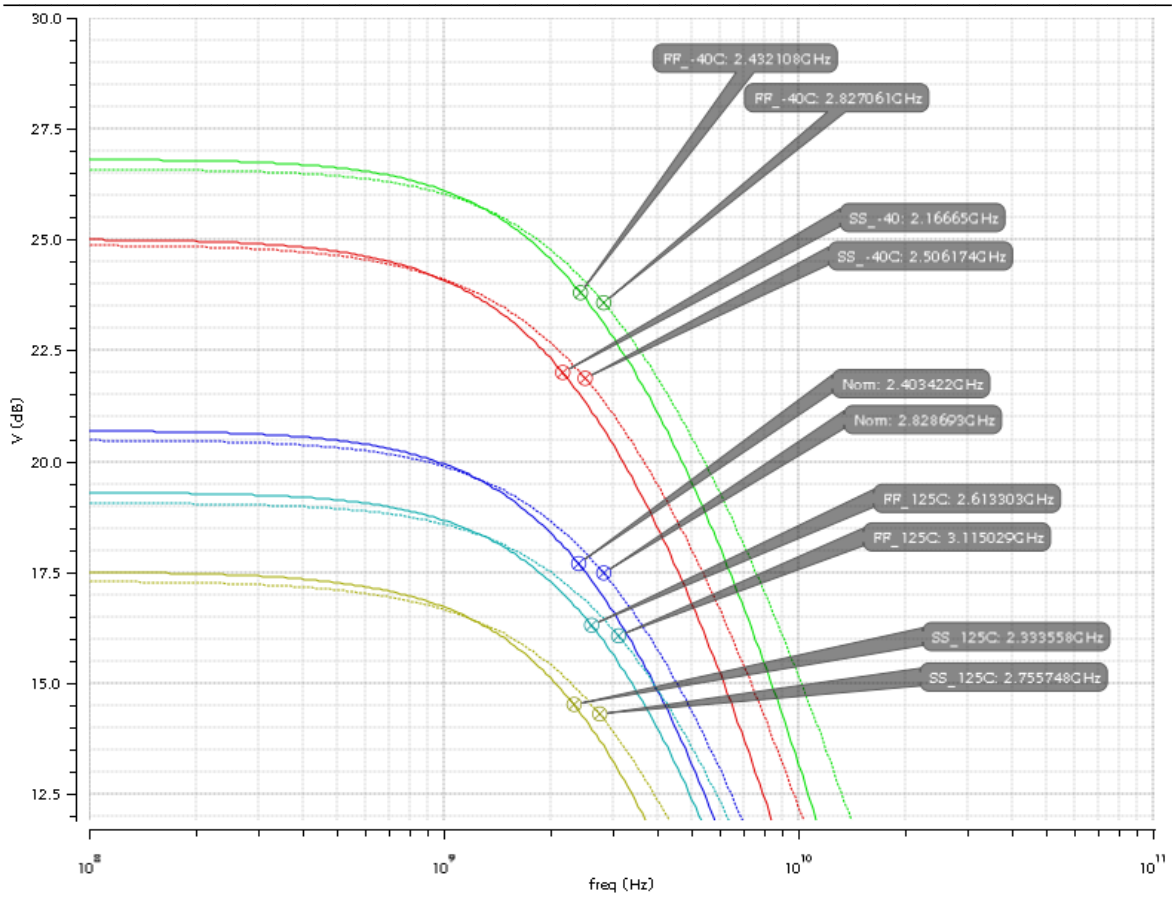

Figure 5-5: HS-OTA Pre-Layout vs. Post-Layout 3 dB BW across PVT Corners.

5.3. CML to CMOS Post-Layout Design Verification

5.3.1. Differential to single-ended circuit Post-layout Design Verification

Figure 5.6 shows the comparison of pre-layout and post-layout of Differential to Single Ended circuit transient response at nominal PVT. The transient response shows a shift in the common mode voltage from 591.90 mV to 605.088 mV, i. e. a difference of 2.2% in common mode voltage.

Notice, however, this shift does not represent an issue it actually helps us to get closer to the 600 mV common mode voltage needed. Another feature to highlight is the delay of the post-layout Response: However, this is not a concern since there are no phase requirements to be meet in embedded clock serial interfaces.

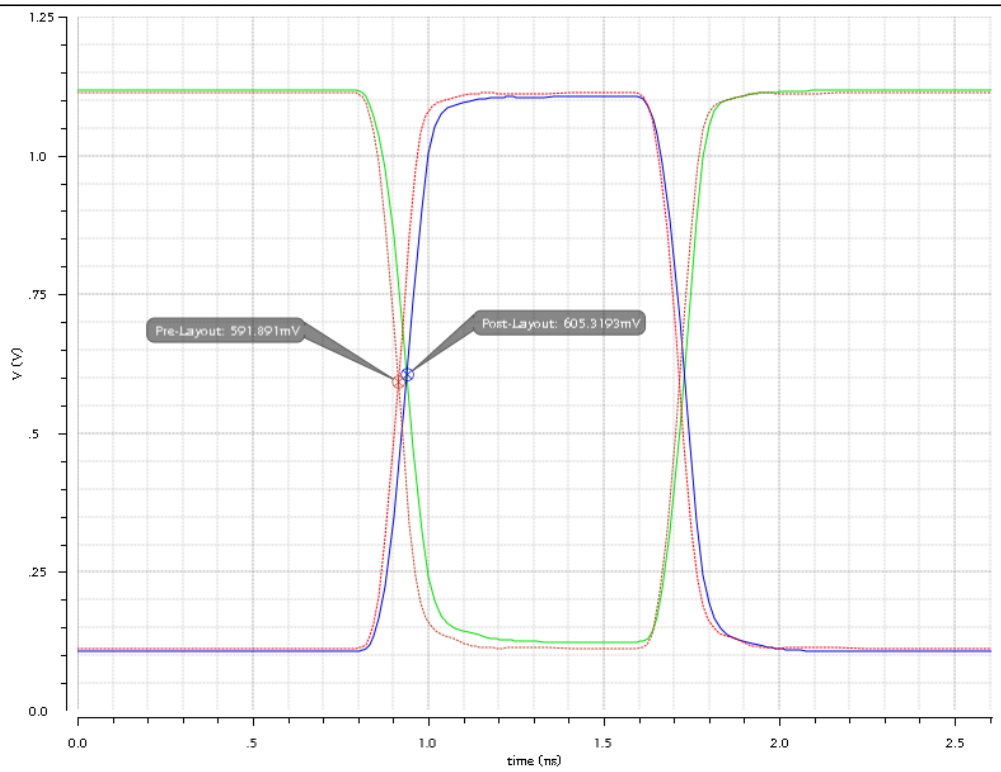

Figure 5-6: Differentia to Single-Ended Pre-Layout vs. Post-Layout Transient Response at Nominal PVT

5.3.2. Inverters Post-layout Design Verification

Figure 5.7 to 5.9 shows the transient response comparison of the inverters that comprise the CML to CMOS circuit. On the transient response of the first inverter to the third inverter, we can see a major shift from 638.1689 mV to 620.2021 mV (i.e. a difference of 2.8%). Fortunately, this change moves the common mode voltage to the required value of 600 mV.

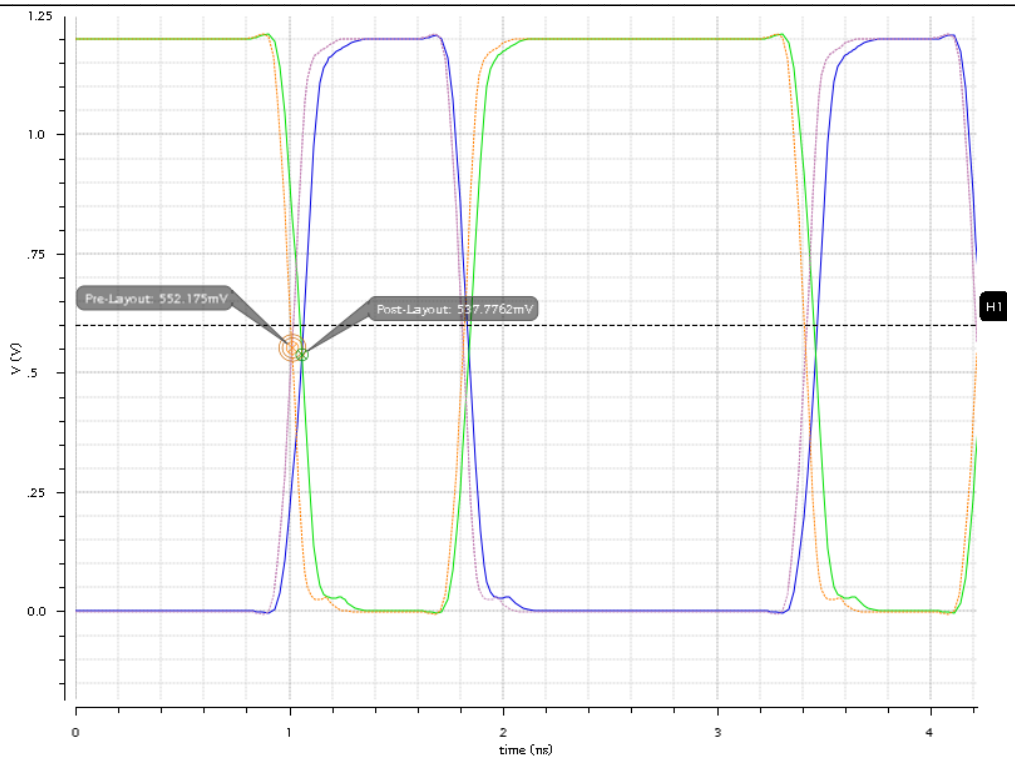

Figure 5-7: First Inverter Pre-Layout vs. Post-Layout Transient Response at Nominal PVT.

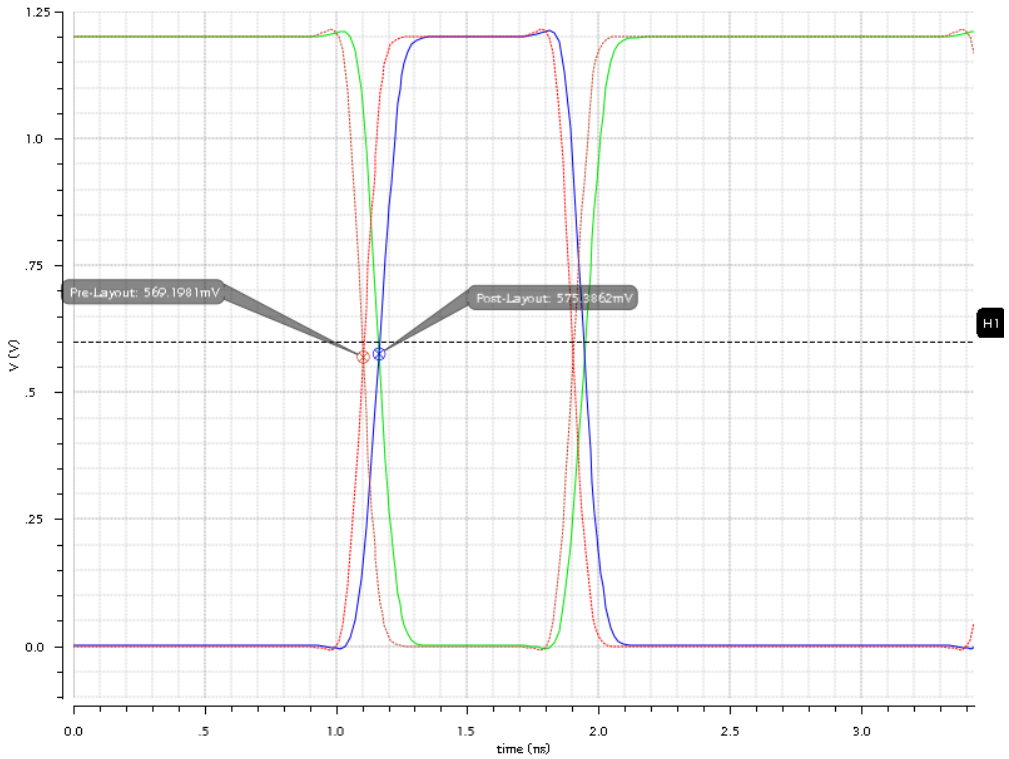

Figure 5-8: Second Inverter Pre-Layout vs. Post-Layout Transient Response at Nominal PVT.

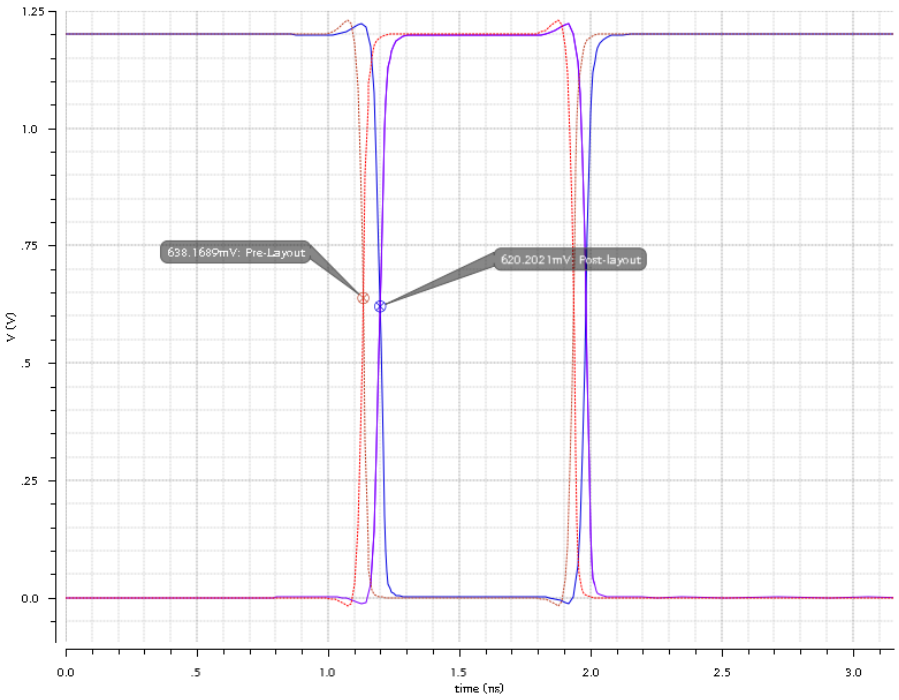

Figure 5-9: Third Inverter Pre-Layout vs Post-Layout Transient Response at Nominal PVT.

5.4. High-Gain OTA Post-Layout Design Verification

Using the same test bench as the pre-layout phase (Figure 3.14), the post-layout of the high-gain OTA was carried out, the results are shown in figure 5.10, the gain and GBW increased due to the differential pair and current mirror load was broken down in fingers given a slightly higher g_m and lower parasitic capacitances, with this growth we meet the 40 dB target.

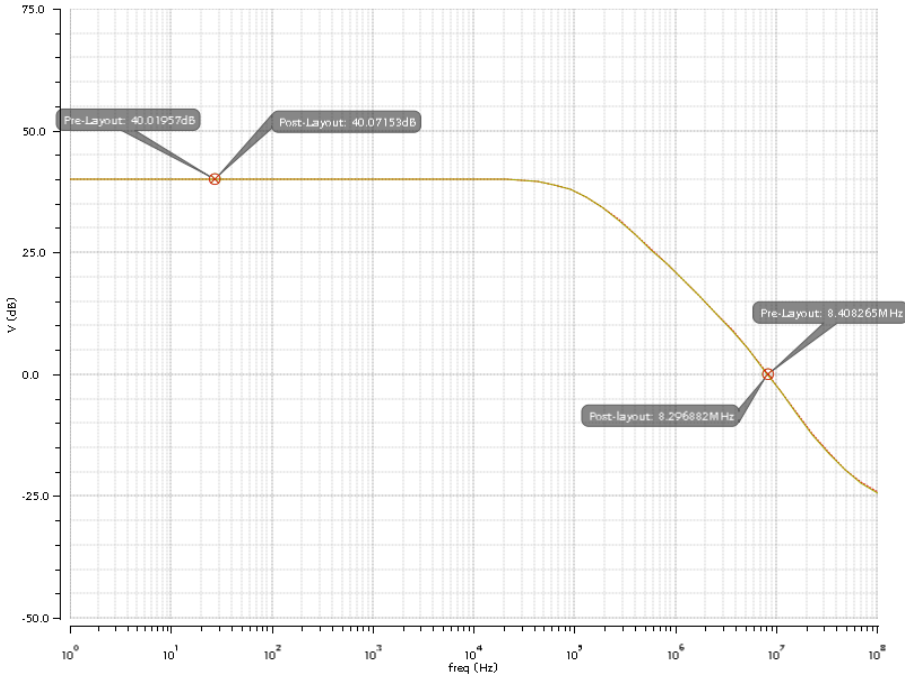

Figure 5-10: High-Gain OTA Pre-Layout vs. Post-Layout AC Response.

5.5. Analog Receiver Top Post-Layout Design Verification

Figure 5.11 shows the transient response of the Analog Reciever module top at nominal PVT conditions. This simulation indicates that the output tracks correctly the input signal at 1.25 GHz (see the red dotted line in 5.10 graph).

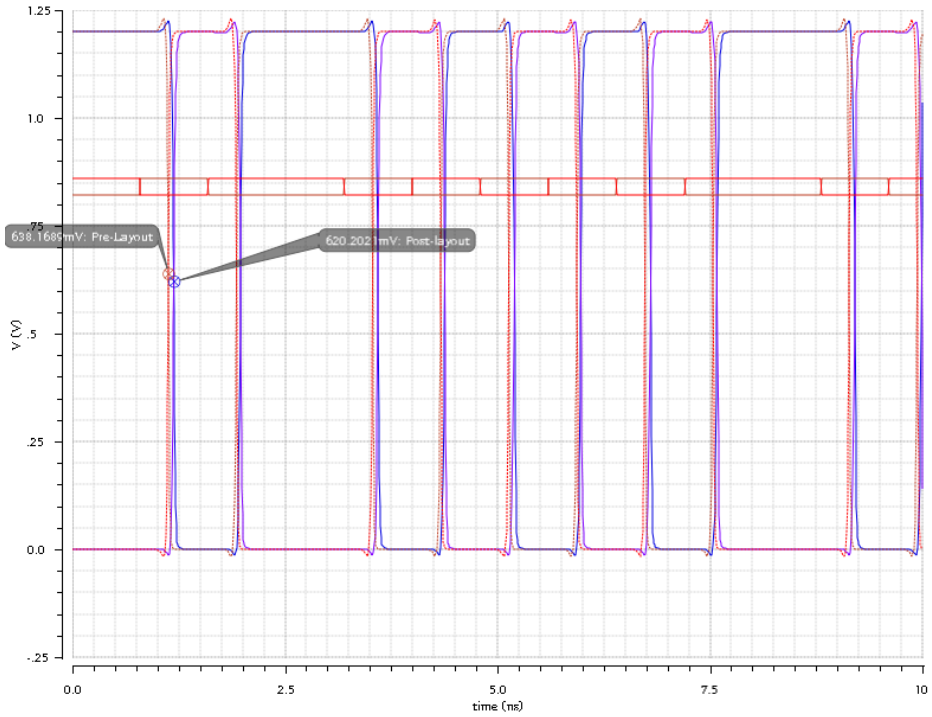

Figure 5-11: Analog Receiver Post-Layout Response at Nominal PVT.

Figure 5.12 shows the transient response of the Analog Reciever module at the same PVT corners used to validate the HS-OTA. This simulation indicates that the output tracks correctly the input signal at 1.25 GHz (see the red dotted line in figure 5.11 graph) in all cases.

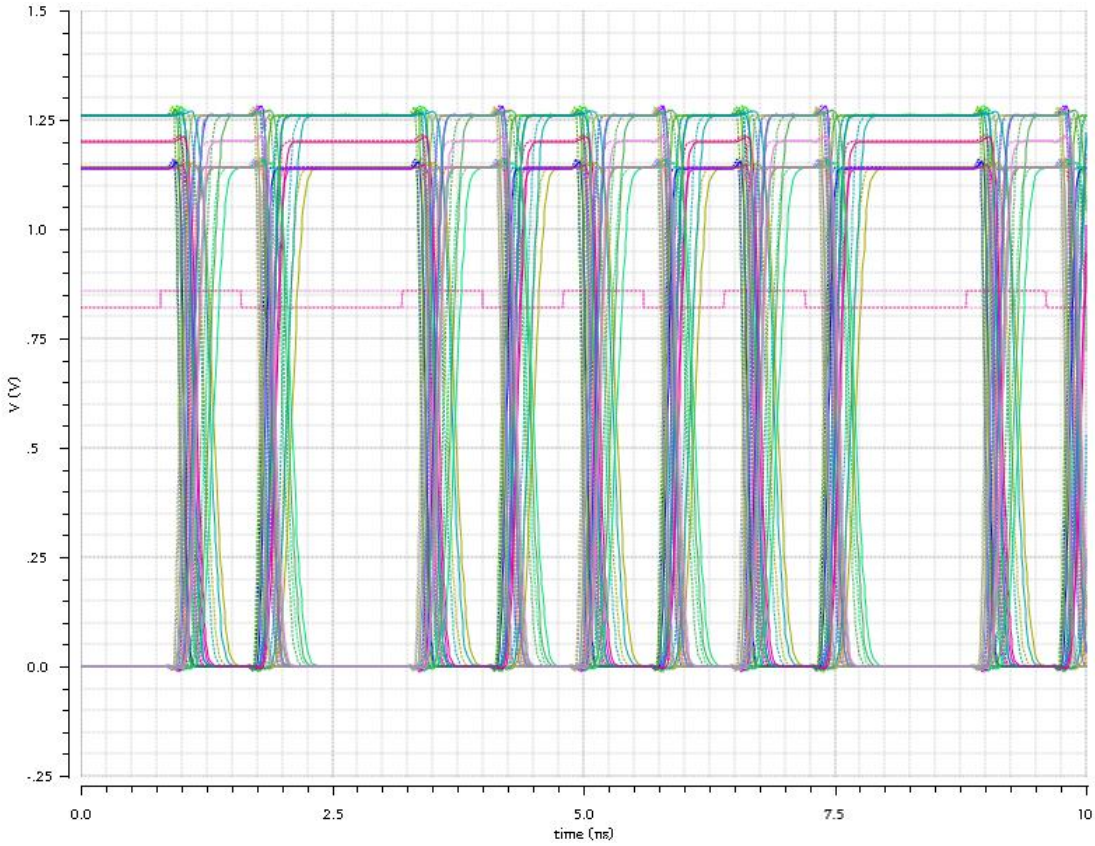

Figure 5-12: Analog Receiver Post-Layout Transient Response across PVT Corners.

Figure 5.13 shows the Post-Layout transient response under a mismatch analysis at nominal PVT conditions; the results indicate no functional issues or any unusual distortion.

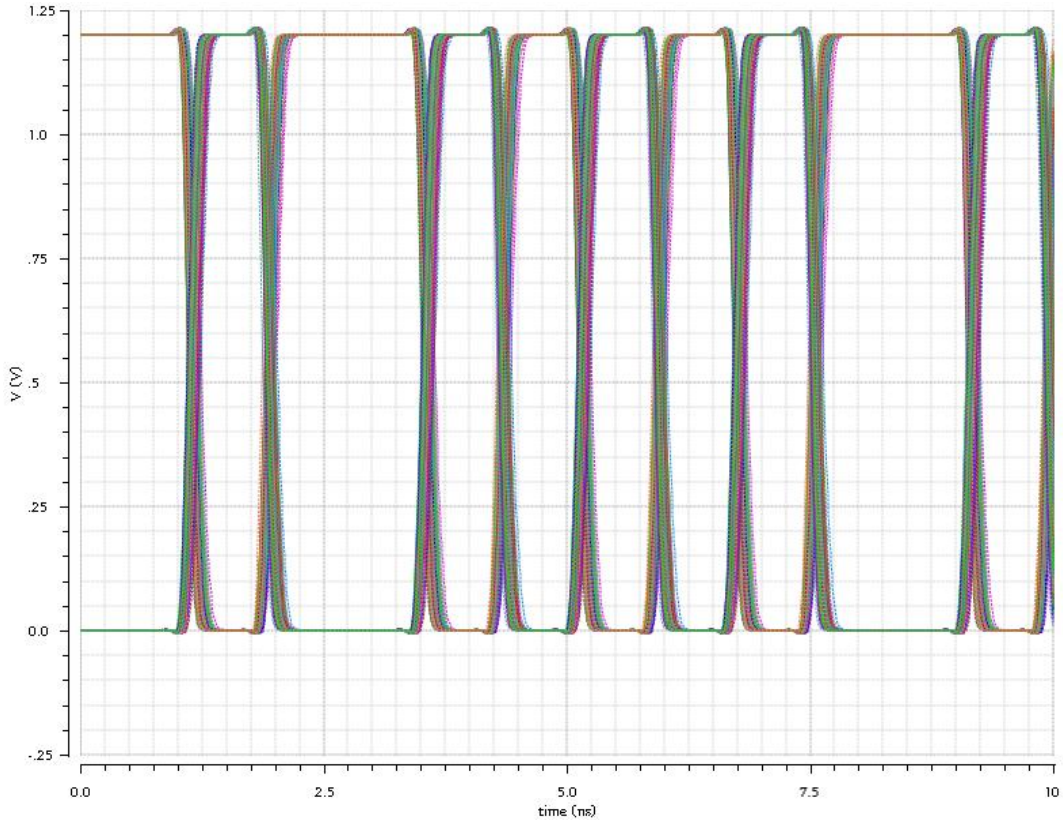

Figure 5-13: Analog Receiver Post-Layout Transient Response Under Mismatch Analysis.

In all simulations, we do not see great picking at transitions on the transient response. All these results allow us to conclude that layout of receiver module complies with design specifications.

CHAPTER 6: ANALOG RECEIVER LAYOUT OPTIMIZATIONS

6.1. Analog Receiver Layout Optimizations

After the first layout was done and verified, the following improvements were added: dummy devices (transistors & resistors) and guard rings to key analog circuits.

Ending devices such as the transistors in the differential pair, tail, and resistors shown in the original layout of the HS-OTA (see figure 4.3) have different boundary conditions than the inner elements, these differences cause that these devices end up with electrical parameters increasing mismatch effects, the V_{th} voltage is a key parameter that is affected by this. The HS-OTA is very sensitive to this issues, matching of the differential pair is essential for its operation. By adding dummy devices, we reduce this boundary conditions.

Guard rings serve various purposes, they prevent minority carriers injected by one device from interfering with the operation of another device (i.e. digital blocks in our chip), prevent latch up, and also block noise coupling that might otherwise interfere with the operation of analog circuitry [12]. All these improvements will give us more confidence that the manufacturing variations will reduce, increasing the circuit's reliability.

6.1.1. HS-OTA Optimized Layout

Figure 6.1 shows the HS-OTA schematic with dummy transistors and resistors; this has to be done to pass the LVS verification. Note that these devices are shorted so they do not affect the original circuit functionality.

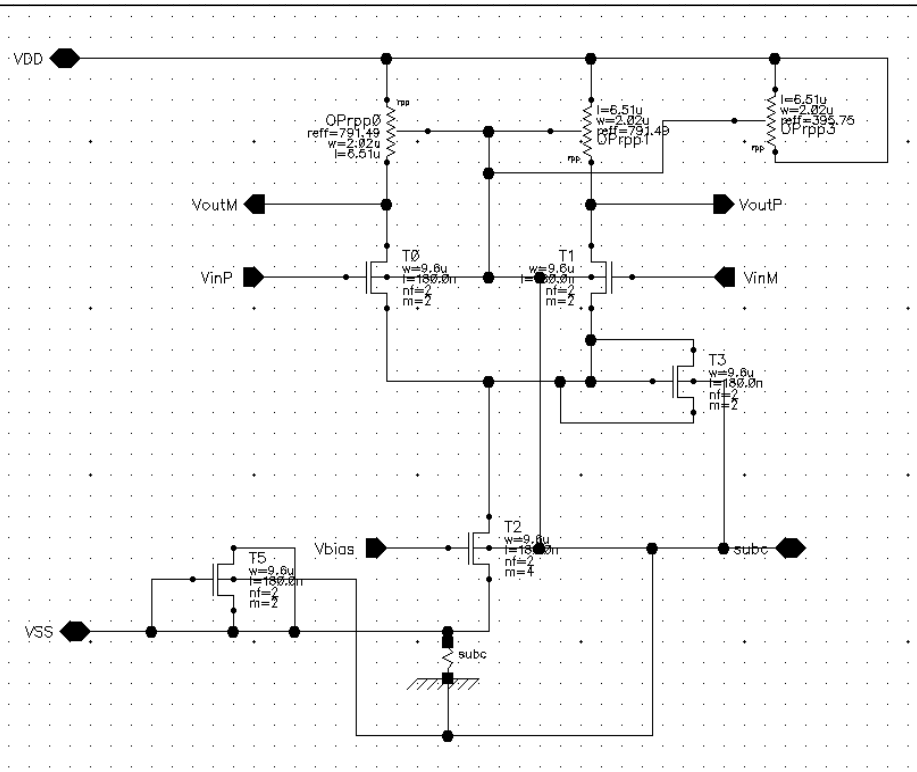

Figure 6-1: HS-OTA Single Stage Schematic with dummy Transistors & Resistors.

Figure 6.2 shows the improved layout of the HS-OTA, at the top we can see the dummy resistors, and the differential pair and tail also have dummy transistors, also notice that unnecessary metal one vias were removed since all the routing was done on metal two at the top level. The guard ring was placed as close as possible to the active devices.

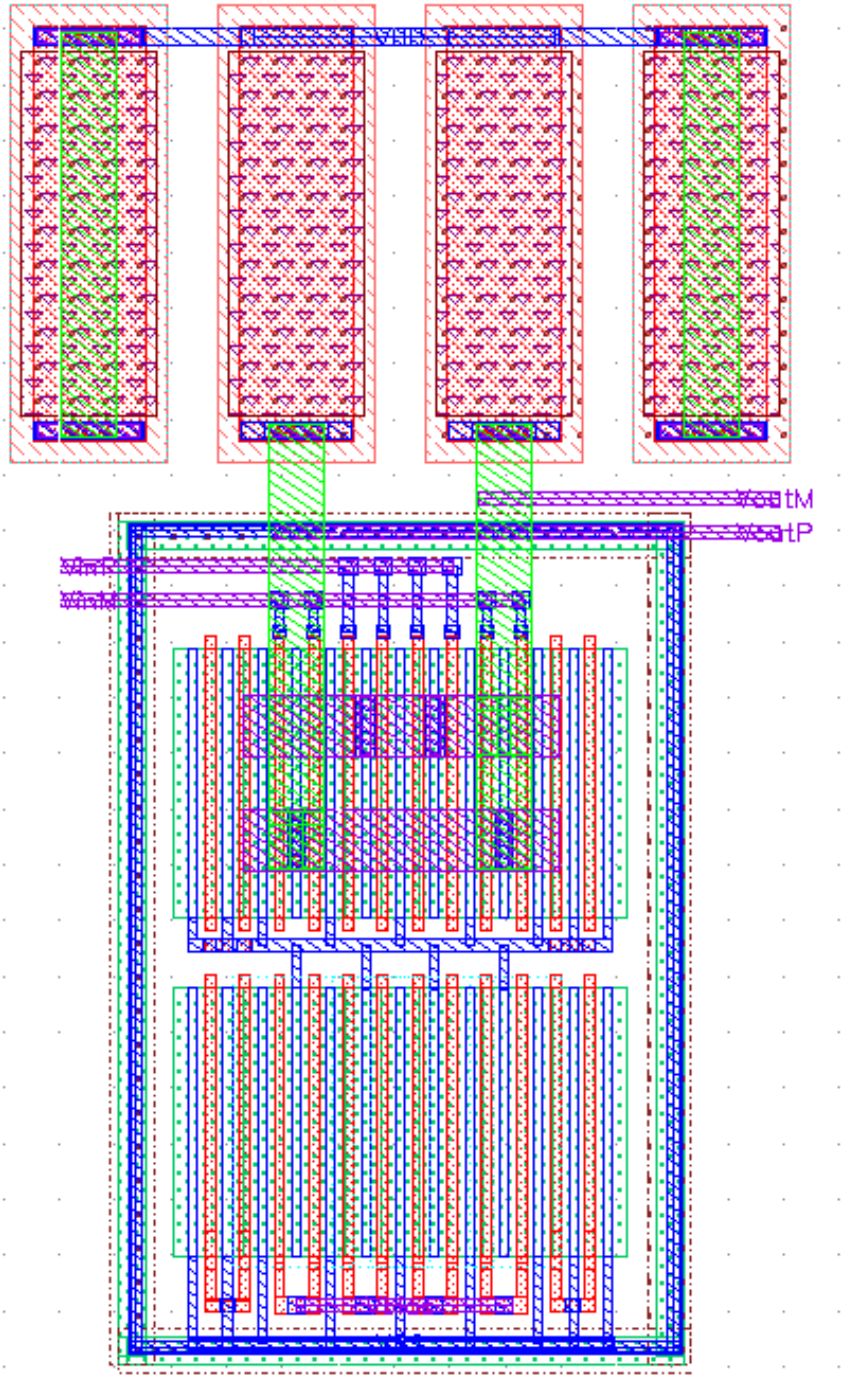

Figure 6-2: HS-OTA Single Stage Optimized Layout.

6.1.2. Differential to Single-Ended Optimized Layout

Figure 6.3 shows the differential to single-ended schematic with dummy transistors; the same approach was taken as the HS-OTA improvements. Figure 6.4 shows the final layout with dummy devices.

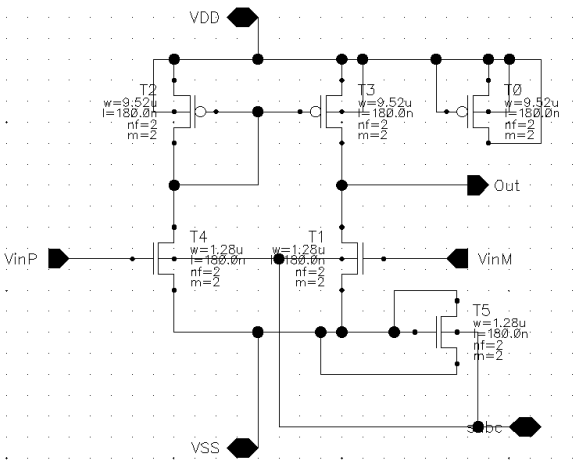

Figure 6-3: Differential to Single-ended schematic with dummy transistors.

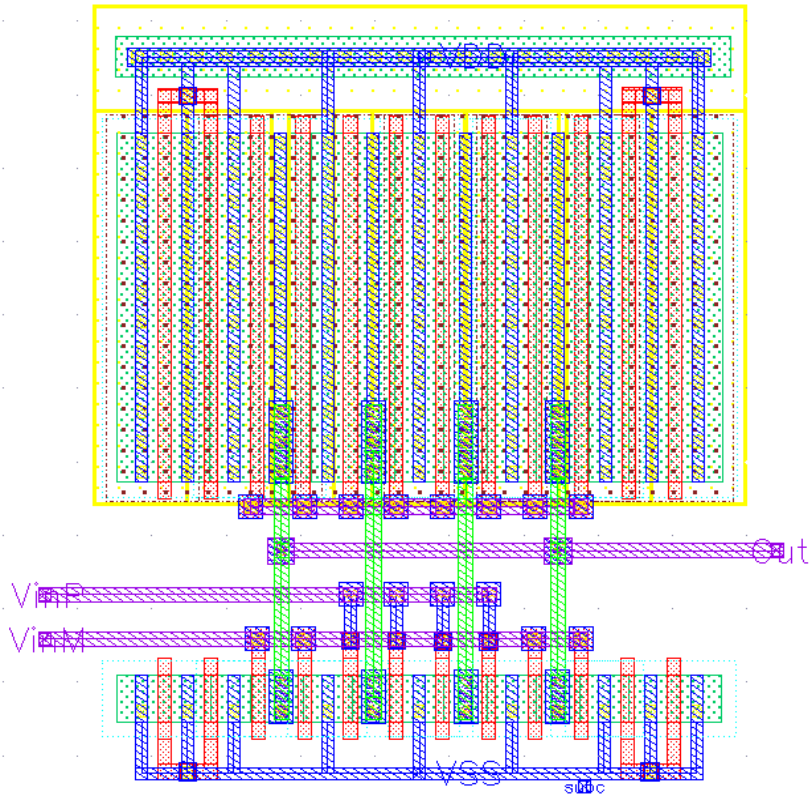

Figure 6-4: Differential To Single-Ended Optimized Layout.

6.1.3. Inverters Optimized Layout

Figure 6.5 shows the inverters with dummy transistors; the same approach was taken as the previous blocks. Figure 6.6 to 6.8 show the final layouts of the first, second and third inverter with dummy devices, the important thing to notice is that the nwell contact was removed and placed at the top level.

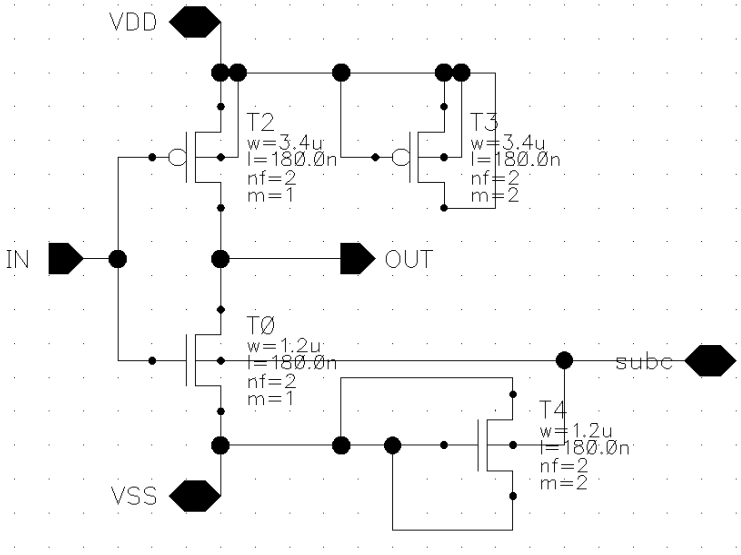

Figure 6-5: Inverter Schematic with dummy transistors.

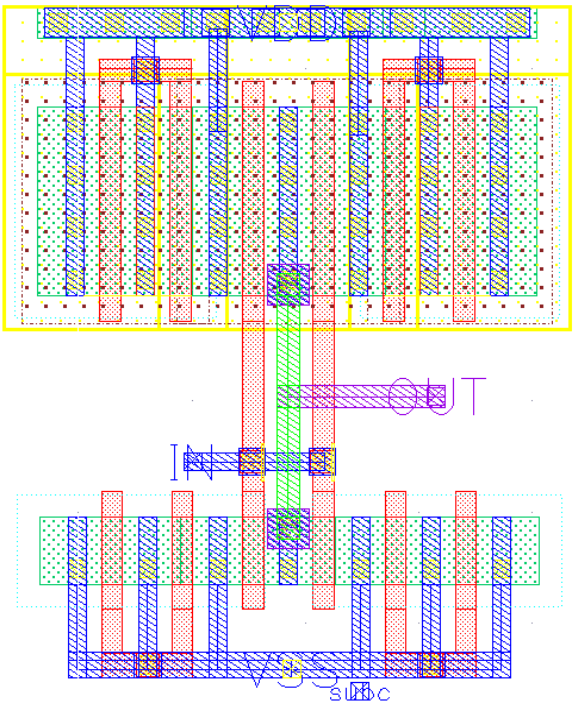

Figure 6-6: First Inverter Optimized Layout.

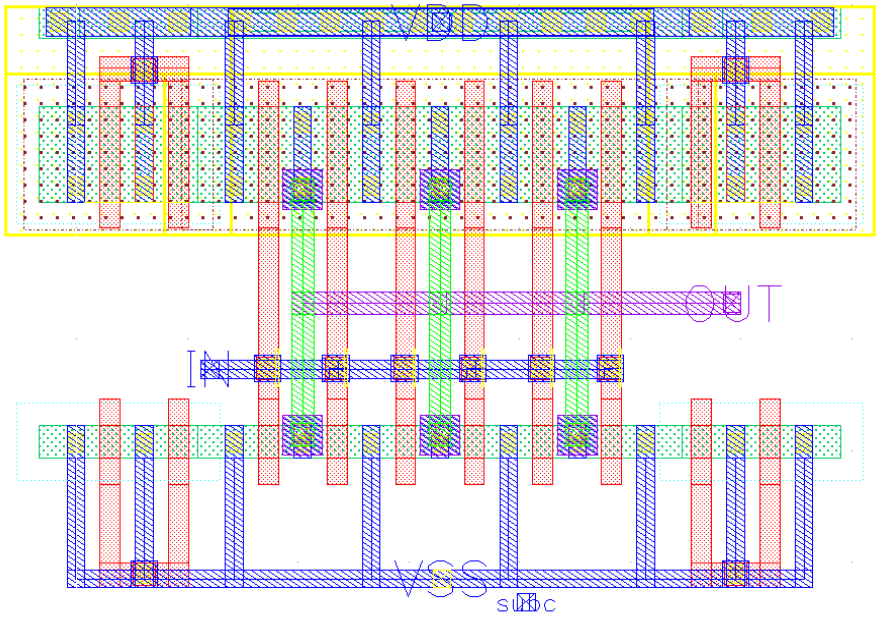

Figure 6-7: Second Inverter Optimized Layout.

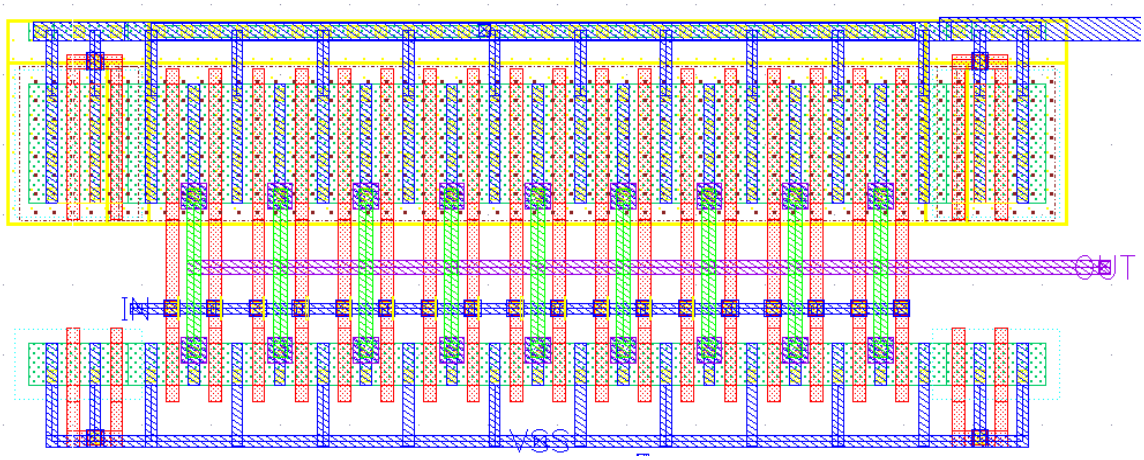

Figure 6-8: Third Inverter Optimized Layout.

6.1.4. High-Gain OTA Optimized Layout

Figure 6.9 show the final layout of the high-gain OTA improved, in this particular block dummy devices were not added only guard rings for NMOS and PMOS transistors. Hence the schematic was not updated; dummies could be added in future work.

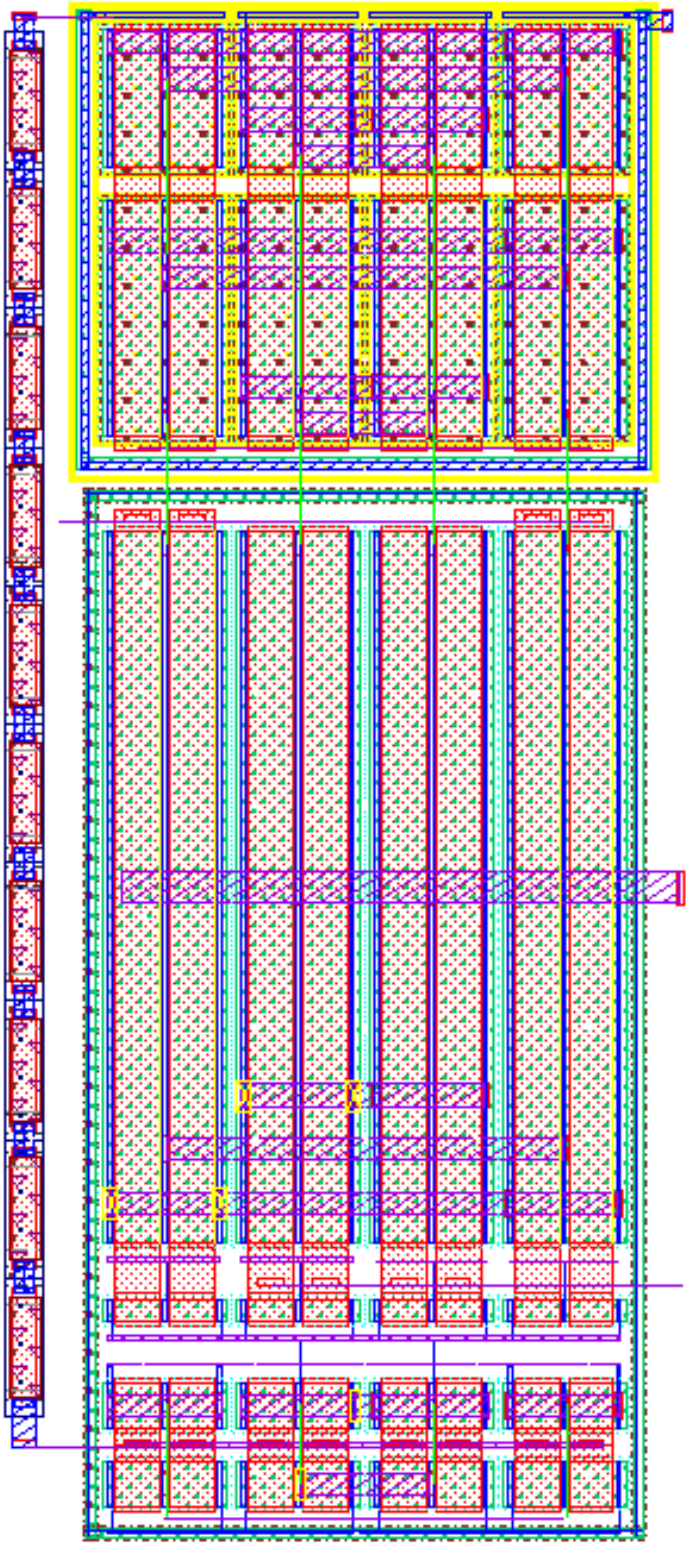

Figure 6-9: High-Gain OTA Optimized Layout.

6.1.5. Bias Circuit Optimized Layout

Figure 6.10 shows the bias circuit schematic with dummy transistors and resistor; the same approach was taken as the HS-OTA improvements.

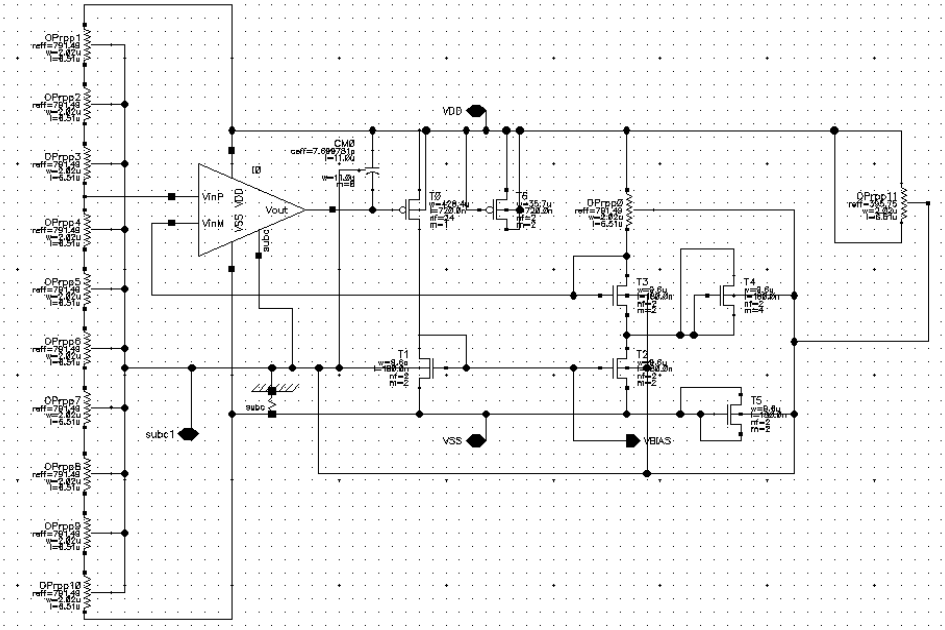

Figure 6-10: Bias Circuit Schematic with dummy transistors.

Figure 6.11 shows the final layout of the Bias circuit, at the top-right, the replica circuit is depicted, notice that it has two dummy resistors to avoid different boundary conditions and guard ring was also added to it. Notice that the PMOS transistor used for converting the voltage control signal to current also has dummy transistors and a guard ring. Guard rings were added to the capacitors as well.

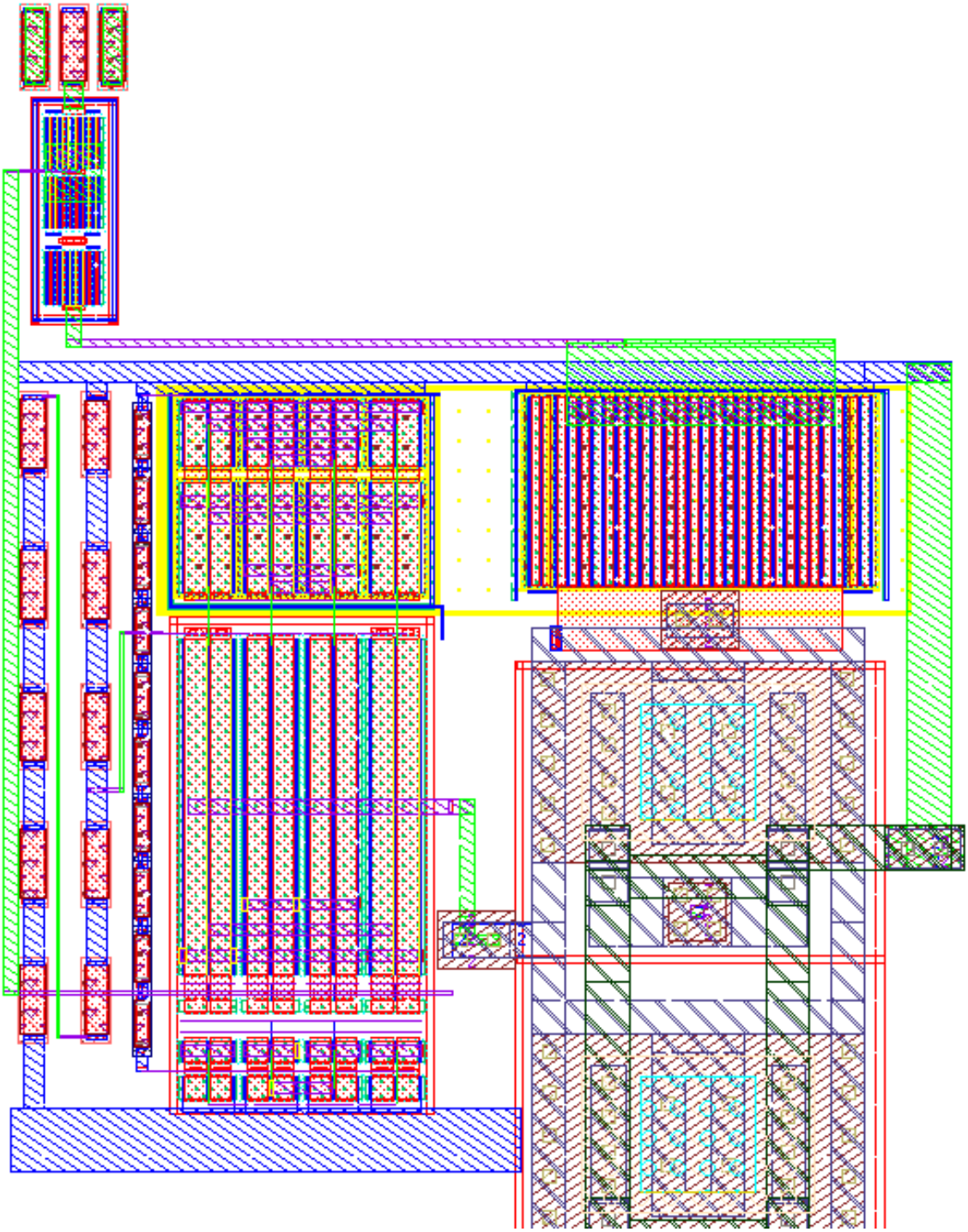

Figure 6-11: Bias Circuit Optimized Layout.

6.1.6. HSRX Path Optimized Layout

Figure 6.12 shows the optimized layout of the HSRX Path, at the left, we can see the HS-OTA, and at the right the inverters, minor changes were done such as changing the metal connections to VDD from metal 1 to metal 3, and some routing was optimized.

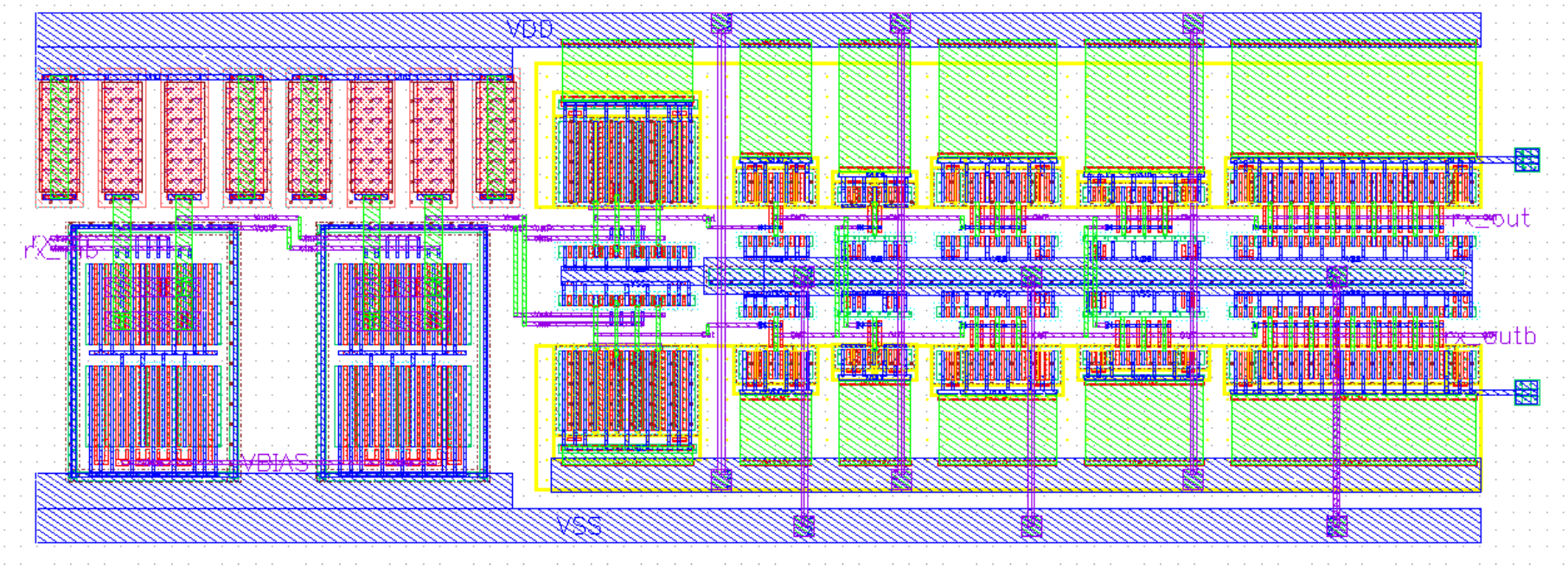

Figure 6-12: HSRX Path Optimized Layout.

6.1.7. Analog Receiver Top Optimized Layout

Figure 6.13 shows the analog receiver top optimized layout, notice that the total area of the design increased to accommodate the required optimizations, the final area 101.88 µm x 240.84 µm = 24,536.78 μm^2 = .024 mm^2 represents a 30.35% growth in area versus the previous implementation, this area increase is not an issue to the SerDes area requirements.

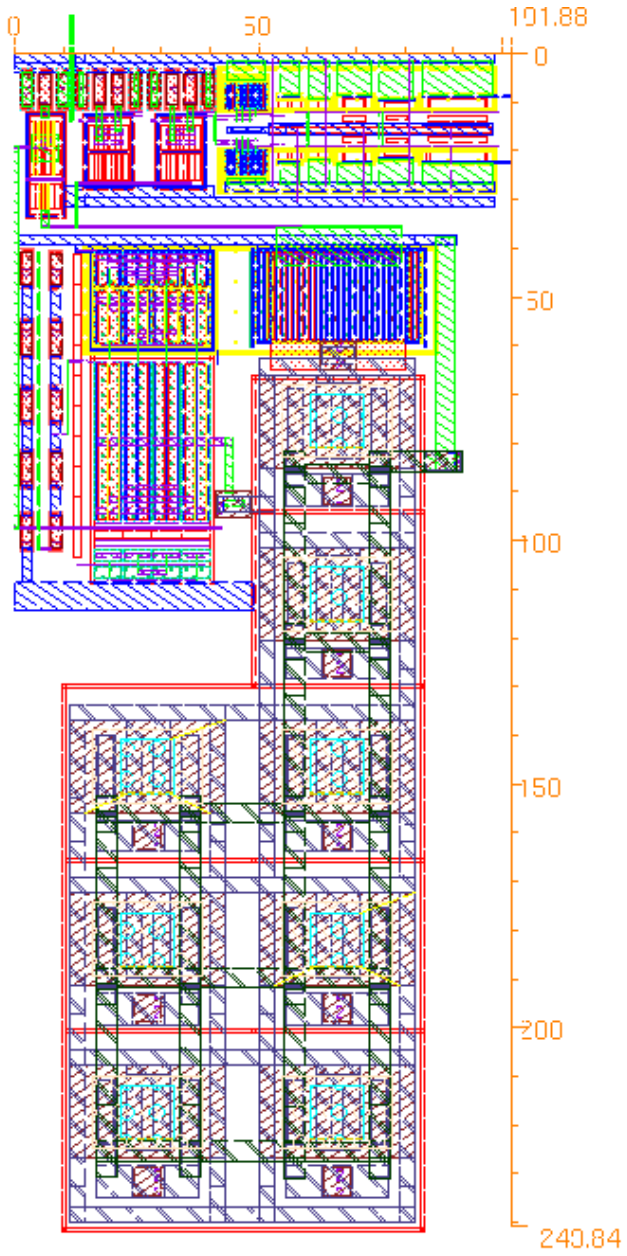

Figure 6-13 Analog Receiver Top Optimized Layout.

Figure 6.14 shows a close-up to the HSRX path of the analog receiver top optimized layout, at the left, we can see the replica circuit, a minor change was at the input signal routing from metal 2 to metal 3, this was done to avoid any noise coupling with the replica circuit.

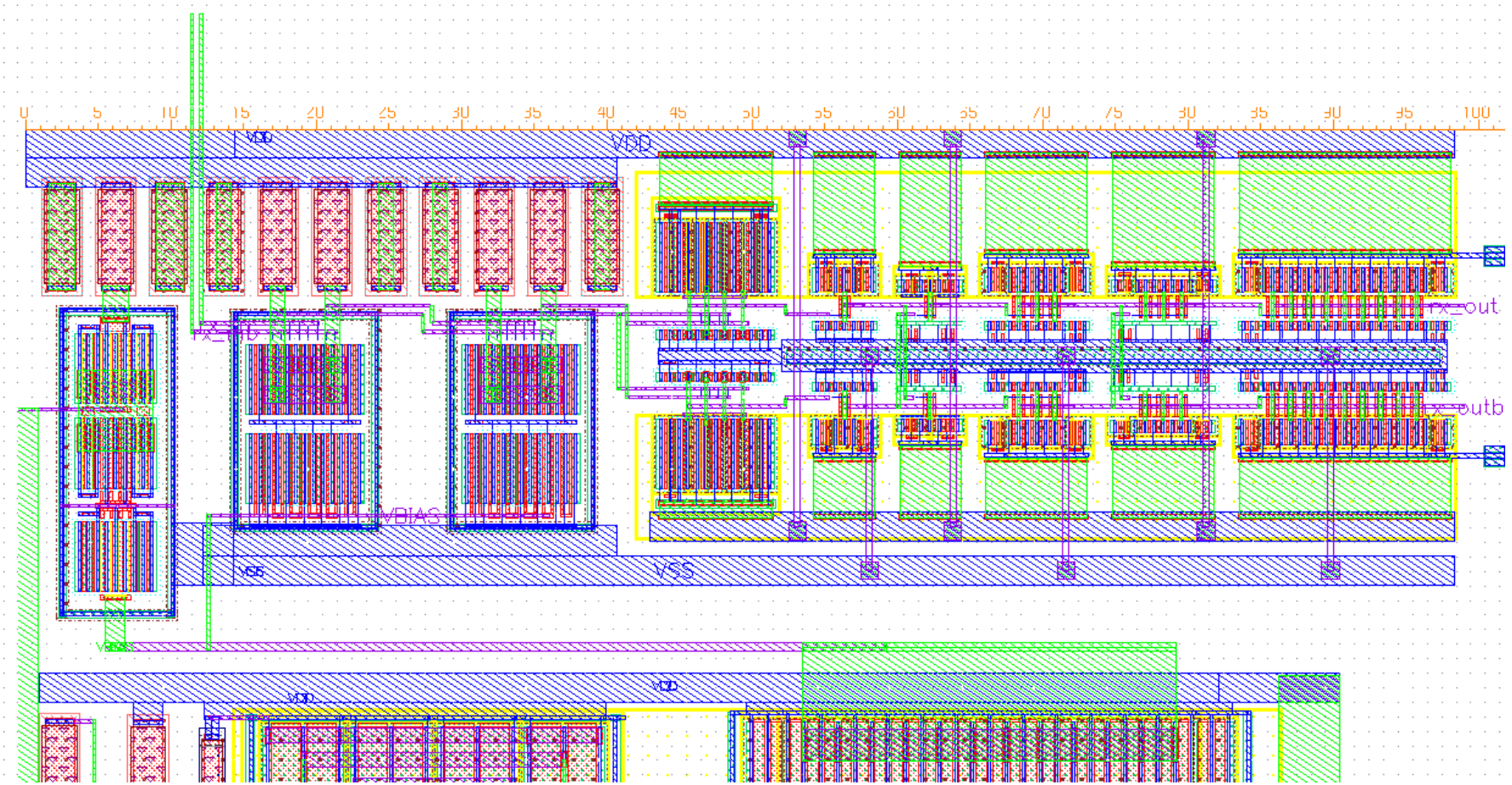

Figure 6-14: Analog Rx Top Optimized Layout Zoom to HSRX Path.

6.2. Analog Receiver Optimized Layout Verification

Once the layout optimizations were done, and the LVS and DRC verifications were clean, the second round of the audit is needed to assess the performance improvements due to this optimizations. The verification was bounded to the critical circuits only, the HS-OTA and the general system response.

6.2.1. HS-OTA Optimized Layout Verification

First verification carried out was an AC analysis to make sure that the 3 dB BW and the voltage gain are still within the specifications.

Figure 6.15 show the results, the 3 dB Bandwidth decrease by 1.36% (from ~2.4 GHz to 2.37 GHz) vs. previous post-layout simulations but interestingly the voltage gain increase by 29.25% (from ~20 dB to 26.74 dB) vs. previous post-layout simulations, these results indicate that most likely the g_m of the differential pair increased due to the layout optimizations.

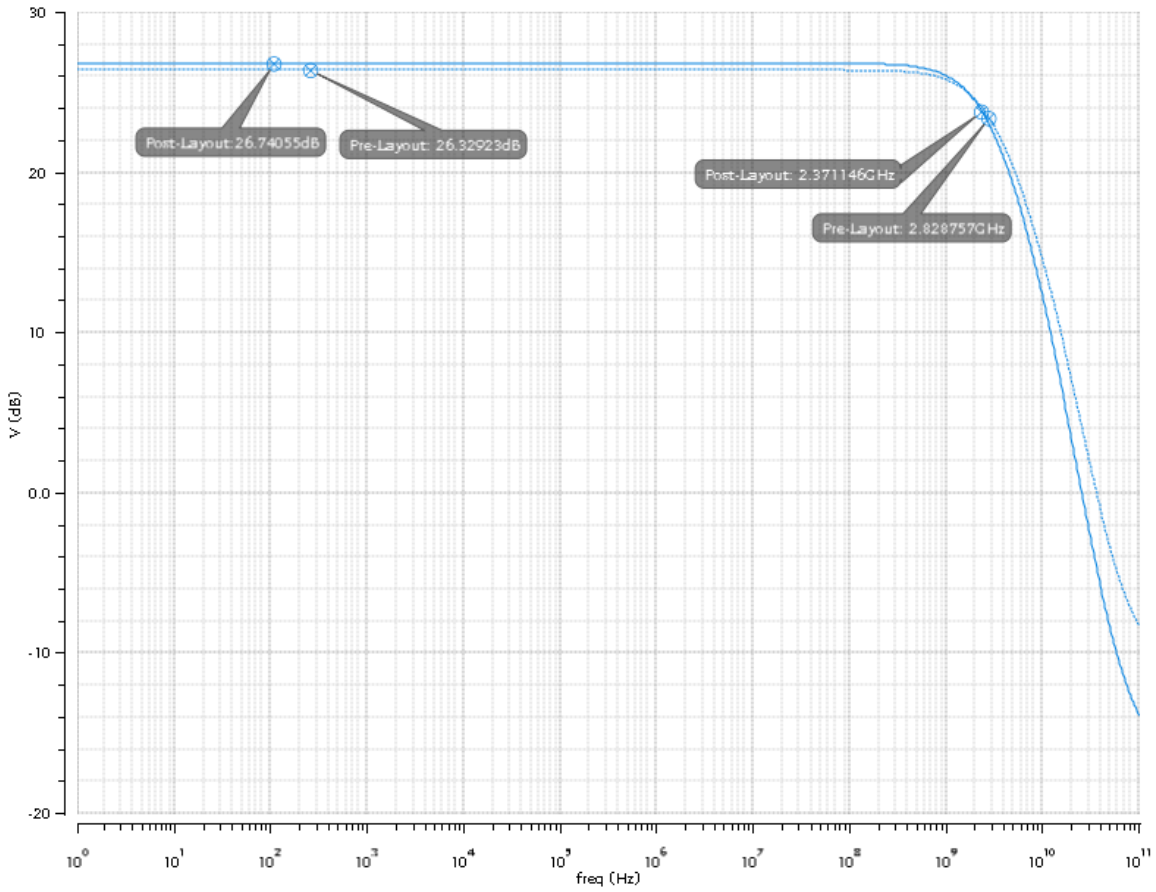

Figure 6-15: HS-OTA Optimized Layout AC response at Nominal PVT.

A DC analysis was carried out to see how the V_{ocm} of different stages of the HS-OTA behaved, figure 6.16 shows the HS-OTA schematic and variables that were analyzed, the results are presented in Table 6.1 (first stage) and 6.2 (second stage), as a reference the pre-layout results were added.

As it can be seen in Table 6.1, row 3 for the first stage the non-optimized layout gives a severe mismatch in the output voltage, 1.64% difference and the current has a 3.4% difference, the first stage mismatch is propagated to the second where is further exacerbated, table 6.2 row 2 shows that the output voltage difference goes up to 3.7%, this is a considerable mismatch impacting the desired performance.

Now in row 2 of both tables show an excellent improvement, the mismatch in the output voltage in the first stage is only 0.04% and in the second stage is only 0.1%. To better see the improvements a transient analysis was carried out, Figure 6.17 shows the post-layout response of the non-optimized layout; here the mismatch error can clearly be seen. Figure 6.18 shows the optimized layout response; the mismatch is imperceptible.

Notice that even with the optimizations the target of 840 mV of the common mode is not met, this is due to a higher tail current than the target.

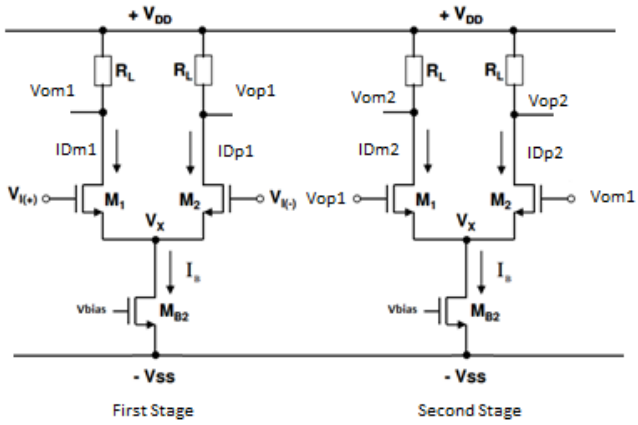

Figure 6-16: HS-OTA Schematic.

	First stage			
Design Stage	V_{op1} (mv)	V_{om1} (mv)	I_{Dp1} (A)	I_{Dm1} (A)
Pre-Layout	840	840	452.6E-3	452.6E-3
Post-layout optimized	832.8	833.2	461.9E-3	461.7E-3
Post-layout non-optimized	814.1	827.5	485.7E-3	468.9E-3

Table 6-1: HS-OTA First Stage DC Voltages at Nominal PVT.

	Second stage			
Design Stage	V_{op2} (mv)	V_{om2} (mv)	I_{Dp2} (A)	I_{Dm2} (A)
Pre-Layout	840	840	452.6E-3	452.6E-3
Post-layout optimized	834	833	459.5E-3	461.0E-3
Post-layout non-optimized	839.6	808.2	453.0E-3	492.8E-3

Table 6-2: HS-OTA Second Stage DC Voltages at Nominal PVT.

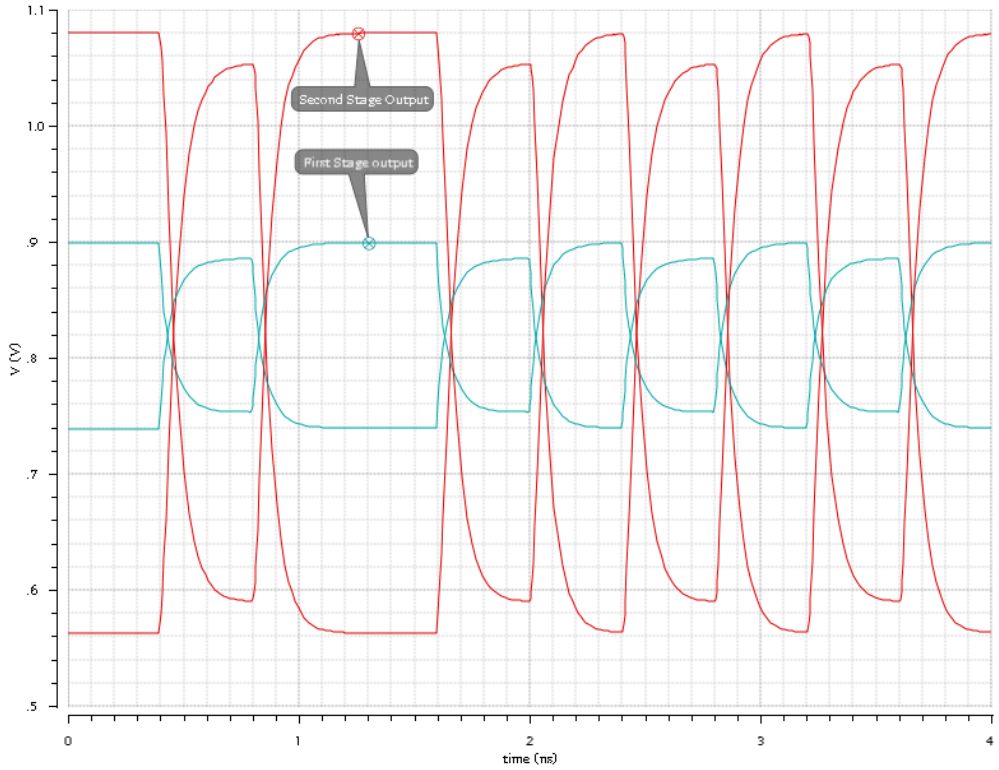

Figure 6-17: HS-OTA Unoptimized First and Second Stage Transient Response at Nominal PVT.

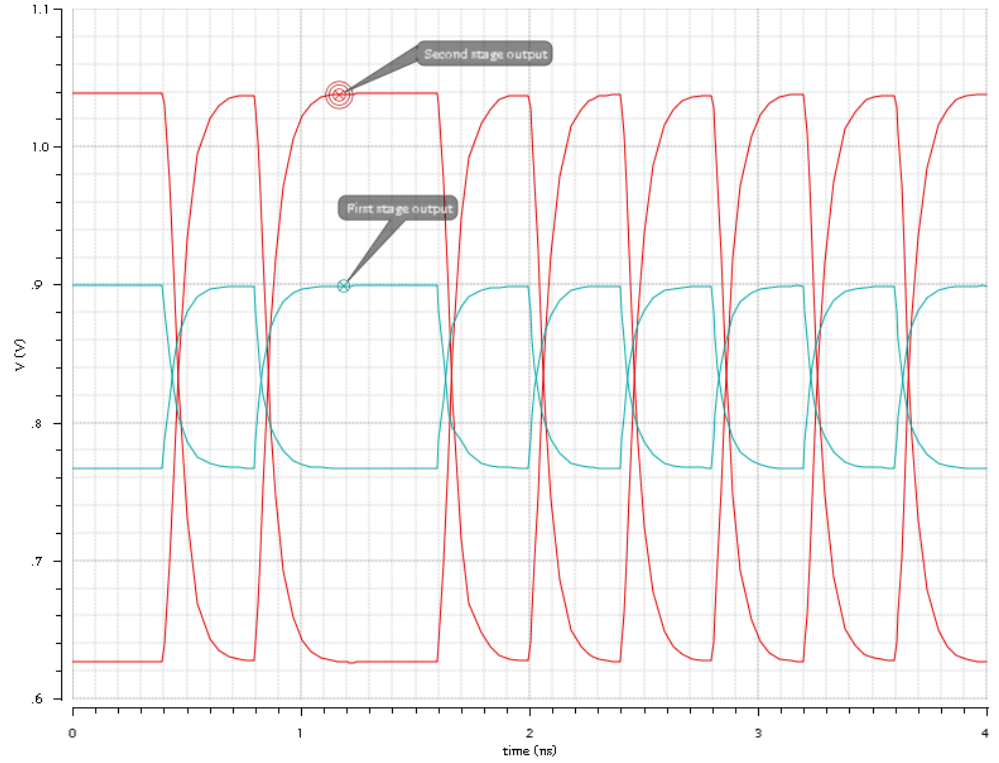

Figure 6-18: HS-OTA Optimized First and Second Stage Transient Response at Nominal PVT.

6.2.2. Analog Receiver top-level Optimized Layout Verification

Figures 6.19 shows the post-layout transient response of the top analog receiver with the optimized layout at nominal PVT conditions, as it can be seen, we have the same behavior as the non-optimized design, but the common mode improves from 620.202 mV seen in figure 5.11 to 618.0443 mV (0.34%) closer to the design target.

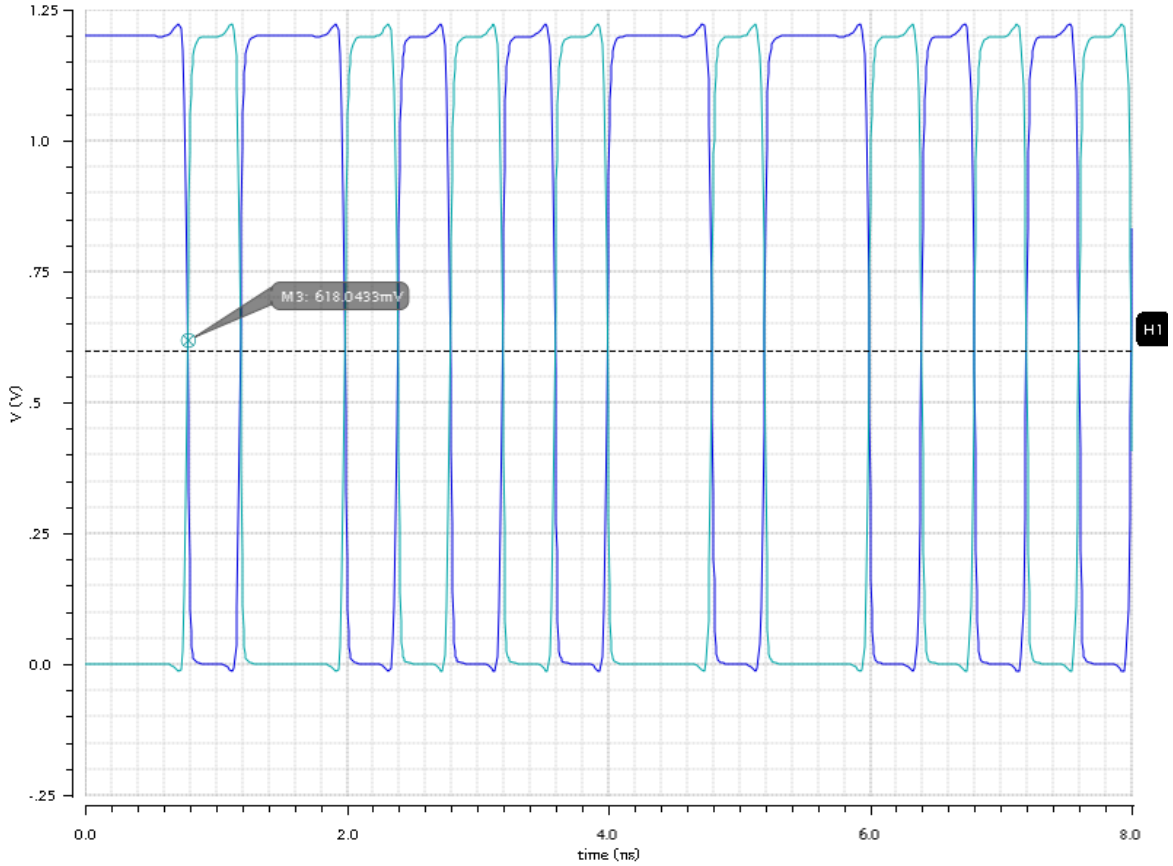

Figure 6-19: Analog Receiver Top Transient Response Optimized Layout.

6.3. Analog Receiver Final Design Figures of Merit

As a final remark, a comparison showing the design targets versus the last results of the critical parameters is presented in Table 6.3.

Figure of merit	Design Target	Final Results	Delta (%)
HS-OTA 3 dB Bandwidth	2.5 GHz	2.3711 GHz	-5.15%
HS-OTA Voltage Gain	20 dB	26.7405 dB	33.70%
High-Gain OTA Gain	40 dB	40.0715 dB	0.18%
High-Gain GBW	10 MHz	8.2968 MHz	-17.03%
Final Common mode output	600 mV	618.0433 mV	-0.35%

Table 6-3: Design Targets Versus Final Results.

It is worth noting that some parameters are under the target, the HS-OTA 3 dB BW is 5.15% off, but this is not a concern since the design is intended to work at a top rate of 1.25 GHz or 2.5 Gbps, this gives us still some margin (89.68 % margin).

Another parameter that looks bad is the High-Gain GBW, which is ~17% off, this instead of making the design worse it is making it better since the lower the bandwidth, the more stable the system is, the common mode voltage at the output difference is not critical to the circuit performance.

The remaining parameters are meeting the specifications, it is worth noting that the HS-OTA voltage gain is above the design target by ~33%, this means that our system is more sensitive, and it could potentially sense a smaller voltage swing than the required by the PCI Express Gen 1 protocol.

CONCLUSIONS

In this work the design, physical implementation and design verification of an Analog receiver module for a SerDes SoC in 130 nm CMOS process technology using GLOBALFOUNDRIES cmrf8sf Process design kit and Cadence Virtuoso were presented.

The design meets the specifications required to work at 2.5 Gbps for the PCI Express Gen 1 Protocol, extensive validation was carried out both pre-layout and post-layout covering PVT corners and mismatch analysis giving good results.

The layout LVS (Layout vs. Schematic) and DRC (Design Rule Checks) verifications were done with Mentors Graphics' Calibre software, passing all the required checkings.

The design presented is a good start, but certainly, there are many areas of opportunity for improvement. As a future work we have listed some features that will add more value to this design:

- Programmability features, such as tuning HS-OTA Bandwith, voltage gain & common mode output voltage. This architecture could potentially be used for other protocols that might need less data rate o different common mode input, by tuning these elements, power can be saved, giving a more attractive features for low-power devices and markets.
- Power gating features, currently the HS-OTA and High-Gain OTA are always on, dissipating power even when the link is idle, this feature could be implemented by disconnecting the tails of these circuits when the user indicates to save power.
- Equalization circuit such a CTLE (Continous time linear equalizer), current industrial designs have equalization features so different channel lengths and characteristics can be supported.
- Replace capacitors for active devices such as MOSCAPS; this enhancement will save silicon area that could be used for other circuits.
- Input impedance programmability, currently the input impedance control was out of the scope, but this feature could be added to improve signal integrity and to reduce the BOM of the board where this chip will be used
- Testability features (DFTs), our current design does not have any testing feature that could be utilized for post-silicon validation or BIST testing, some programmability features mentioned earlier could serve this purposes.
- IR Drop analysis, this was left out due to tool constraints, but certainly, this is a must to verify the connections are robust enough to handle the design's currents.

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APPENDIX A. Pre-Layout PVT Simulations

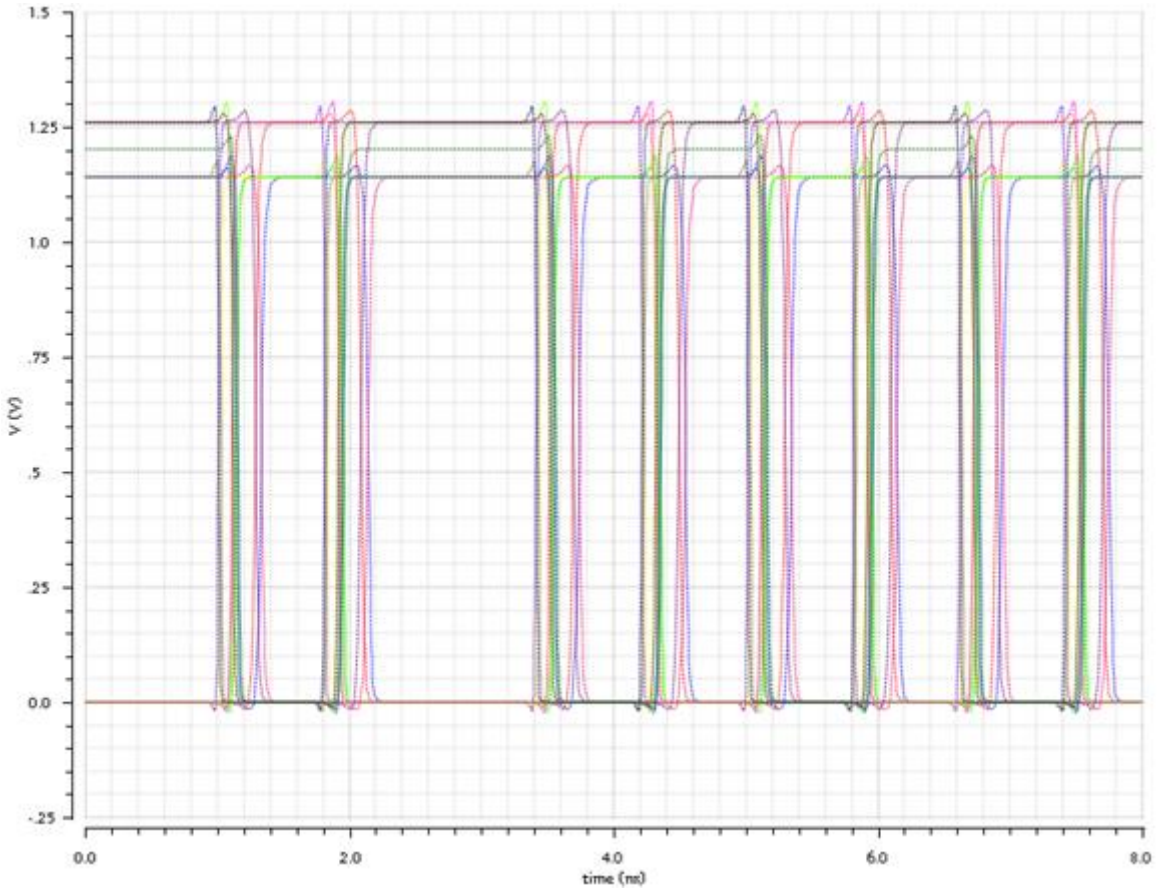

Figure 7-1: Analog Receiver Top Pre-Layout Transient Verification across PVT

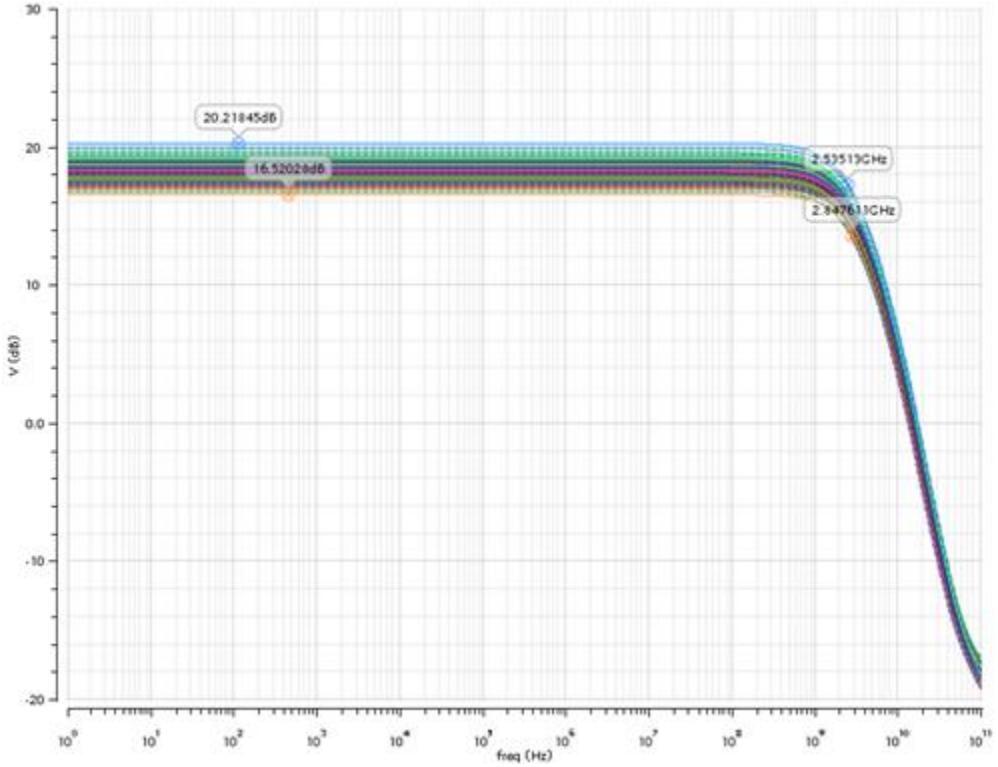

Figure 7-2: HS-OTA AC Response Under mismatch analysis at 1.26V 125C

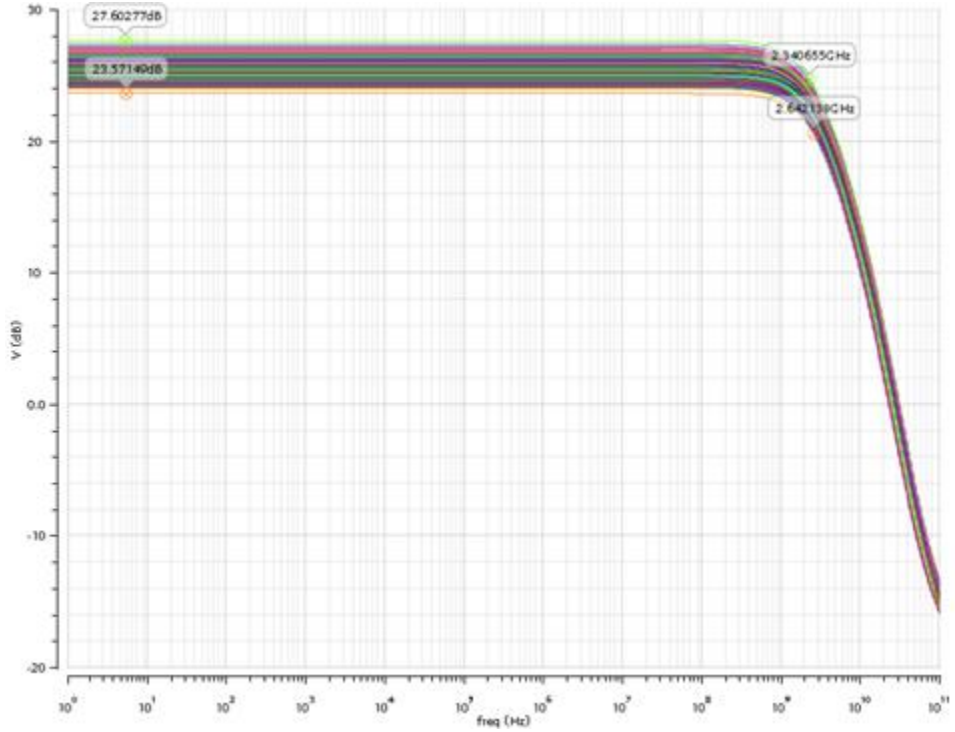

Figure 7-3: HS-OTA AC Response Under mismatch analysis at 1.14V -40C

APPENDIX B. Optimized Layout Simulations

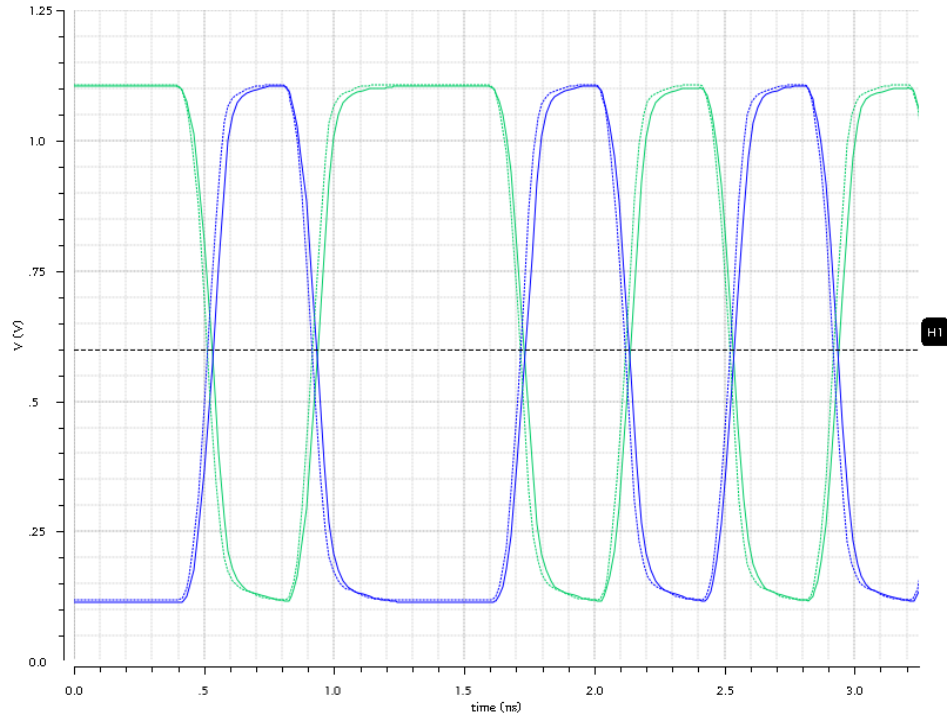

Figure 8-1: Differential to Single-Ended Pre-Layout vs Post-Layout Transient Response at nominal PVT.

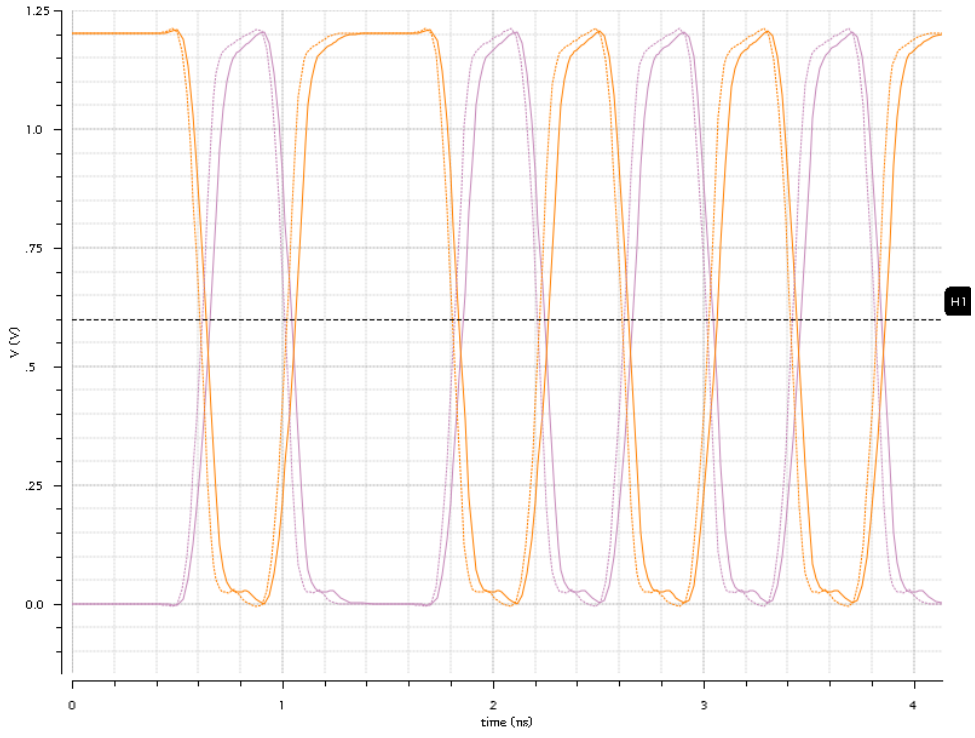

Figure 8-2: First Inverter Optimized Layout Pre-Layout vs Post-Layout Transient Response at nominal PVT.

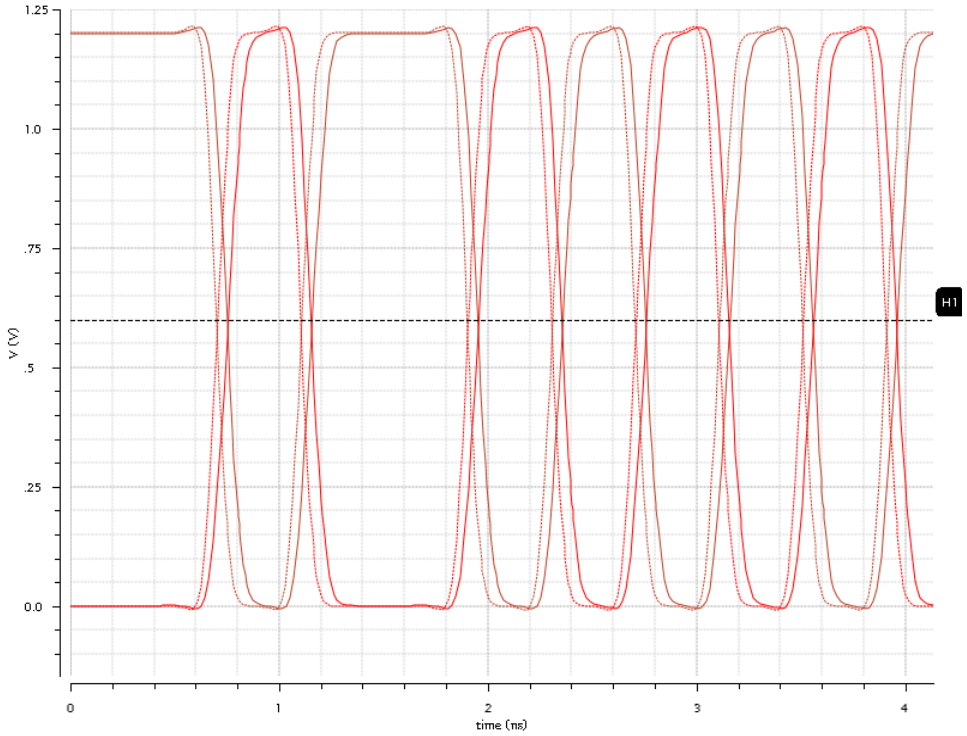

Figure 8-3: Second Inverter Optimized Layout Pre-Layout vs Post-Layout Transient Response at nominal PVT.

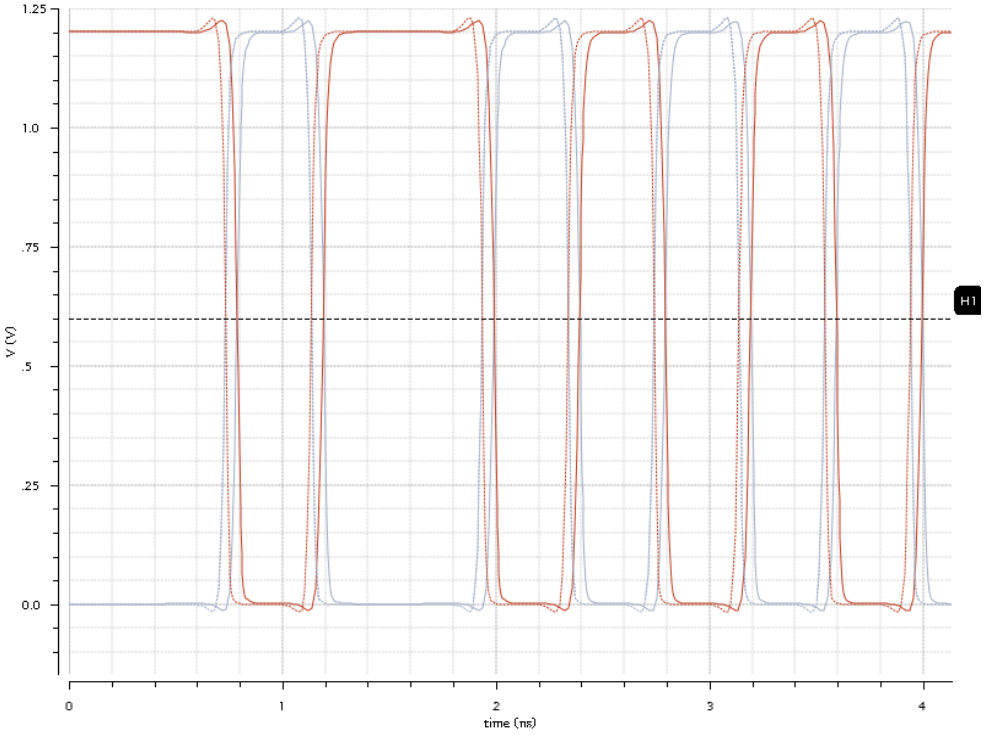

Figure 8-4: Third Inverter Optimized Layout Pre-Layout vs Post-Layout Transient Response at nominal PVT.

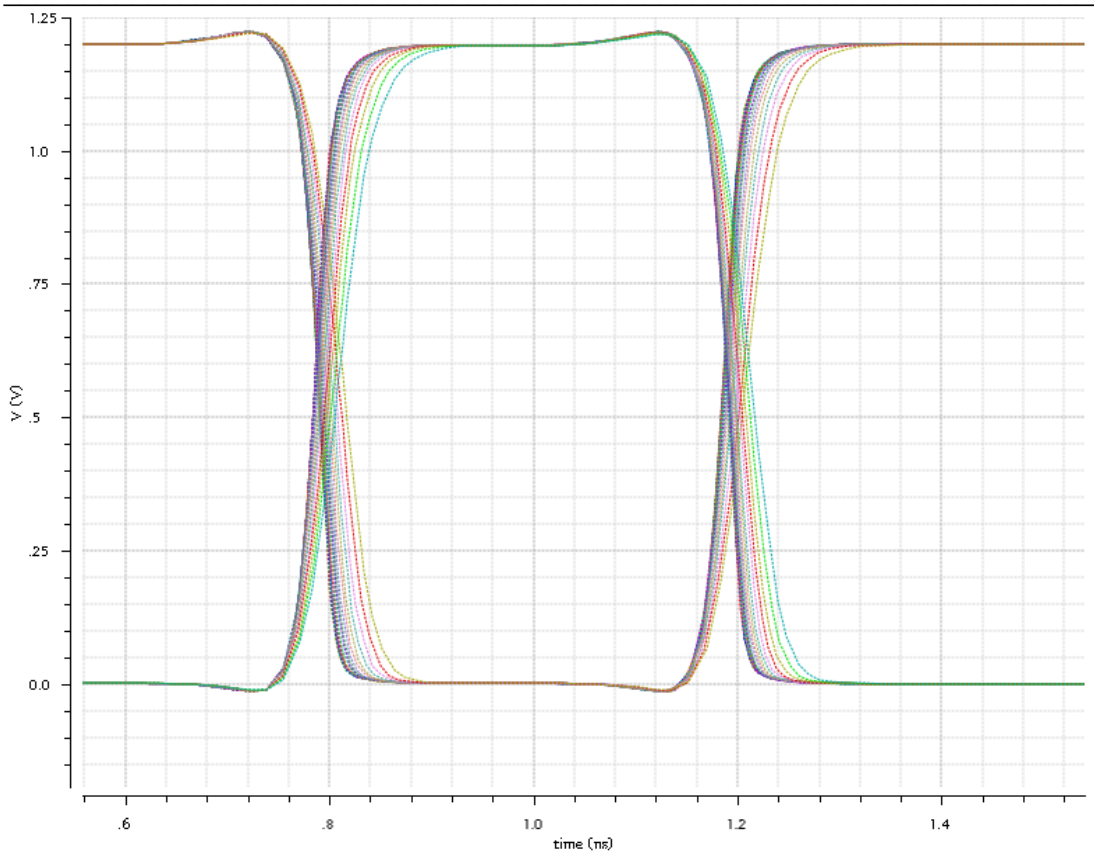

Figure 8-5: Analog Receiver Top Transient Response vs. Cload from 1fF to 100fF

APPENDIX C. Analog Receiver Data Base

Name of archive	Library	Views
1st_inverter_fingers_nosubc_v2	econde_work	Layout, schematic & symbol
2nd_inverter_nosubc_v2	econde_work	Layout, schematic & symbol
3rd_inverter_nosubc_v2	econde_work	Layout, schematic & symbol
1st_DCC_inverter_nosubc_v2	econde_work	Layout, schematic & symbol
2nd_DCC_inverter_nosubc_v2	econde_work	Layout, schematic & symbol
AMP_Diff_OTA_With_Tail_fingers_v2	econde_work	Layout, schematic & symbol
Diff_2_Single_converter_layout_nosunc_v2	econde_work	Layout, schematic & symbol
Bias_OPAMP_layout_post_v2	econde_work	Layout, schematic, caliber & symbol
HSRX_Path_subc_v2_2	econde_work	Layout, schematic, caliber & symbol
BIAS_circuit_with_cap_fingers_layout_subc_top_v2	econde_work	Layout, schematic, caliber & symbol
Analog_RX_Top_v2_2_final	econde_work	Layout, schematic, caliber & symbol
Analog_RX_Top_v2_2_nosubc_TB_AC	econde_sims	Config and schematic
Analog_RX_Top_v2_2_nosubc_TB_DC	econde_sims	Config and schematic
Bias_OPAMP_AC_DC	econde_sims	Config and schematic
Bias_circuit_TB_PostLayout	econde_sims	Config and schematic
BIAS_circuit_Open_Loop_Measurements_PMOS	econde_sims	Adexl and schematic

Table 9-1: Analog Receiver Module Cadence Data Base