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Departamento de Electrónica, Sistemas e Informática

DOCTORADO EN CIENCIAS DE LA INGENIERÍA


# DISEÑO Y DESARROLLO DE SOLUCIONES MINIATURIZADAS DE BAJO COSTO PARA UN DISPOSITIVO PORTÁTIL DE DIATERMIA POR RADIO-FRECUENCIA

Tesis que para obtener el grado de

DOCTOR EN CIENCIAS DE LA INGENIERÍA

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Director de tesis: Dr. Esteban Martínez Guerrero

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Department of Electronics, Systems, and Informatics

DOCTORAL PROGRAM IN ENGINEERING SCIENCES


# DESIGN AND DEVELOPMENT OF MINIATURIZED LOW-COST SOLUTIONS FOR A PORTABLE RADIO-FREQUENCY DIATHERMY DEVICE

Thesis to obtain the degree of

DOCTOR IN ENGINEERING SCIENCES

Presents: Antonio Rafael Corres-Matamoros

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This work is dedicated to my wife Marcela, my son Antonio, my daughter Luciana,
my father Antonio, my mother María de los Ángeles, and God,
for their understanding, patience, and continuous loving
support they gave me during all the time that this
important project in my life lasted.

# Resumen

La diatermia por radio frecuencia (RFD por sus siglas en inglés) es una terapia usada en rehabilitación física para curar lesiones musculares y nerviosas causadas por accidentes o problemas congénitos en personas de cualquier edad. Por medio del calor generado por un campo electromagnético de radio frecuencia no ionizante, se produce una mayor vascularización en el área lesionada, la cual produce un proceso de cicatrizado más rápido y de mayor calidad. En México, varios factores limitan el uso de la RFD en rehabilitación física. Las personas no encuentran atractivo el uso de este tipo de terapia mayormente porque: (a) los tiempos de curación de lesiones son largos debido a que las sesiones de terapia se aplican en intervalos muy separados, (b) los aparatos de RFD son caros y voluminosos, por lo que los pacientes no pueden comprarlos ni tenerlos en casa, y (c) su uso requiere la ayuda de un técnico especializado para evitar riesgo de daño a los pacientes. Ante estas limitaciones, surge la necesidad de un aparato de RFD portátil, de bajo costo y fácil de manejar, lo que permitiría aplicar tratamientos RFD en forma continua, de modo que la curación de lesiones musculares sea en tiempos más cortos y de mayor calidad. En esta tesis doctoral se presenta el desarrollo de un aparato con estas nuevas características. Inicialmente se presenta el desarrollo de un prototipo de RFD portátil, diseñado e implementado con componentes discretos, con el fin de evaluar la efectividad de un tratamiento continuo de rehabilitación. El prototipo se valida mediante un estudio de campo de acuerdo con el protocolo médico de rehabilitación física. Posteriormente, y para facilitar portabilidad del equipo de RFD, se miniaturiza el circuito electrónico mediante la integración de los componentes en un solo *chip*, para lo cual se realiza el diseño de un *chip* en tecnología CMOS de 0.5 μm para un segundo prototipo del equipo RFD. En la tesis doctoral propuesta se hace primero una introducción a la RFD, el principio de funcionamiento de este tipo de terapia, y el proyecto propuesto como oportunidad de desarrollo en México. Posteriormente se presenta el diseño y validación del prototipo de RFD con componentes discretos. En seguida se presenta el diseño del módulo oscilador del *chip* RFD, así como el diseño del módulo amplificador de voltaje. Finalmente, se describe el diseño físico del *chip* de RFD y su interconexión al anillo de *pads* para formar el *tape-out* del chip listo para fabricarse. Con base en esta tesis doctoral, ha sido oficialmente formalizada una solicitud de patente en México.

# Summary

Radio-frequency diathermy (RFD) is a therapy used in physical rehabilitation to heal muscle and nerve injuries caused by accidents or congenital disorders in people of all ages. By means of heat generated by a non-ionizing electromagnetic radio-frequency field, a greater vascularization of the injured area is produced, which stimulates a quicker and higher-quality scarring process. In Mexico, several factors limit the use of radio frequency diathermy in the physical rehabilitation field. People does not find attractive this therapeutic technique mainly due to: (a) the healing times are long because therapy sessions are applied in intervals largely separated, (b) RFD devices are bulky and very expensive, then patients cannot easily afford them and store them, and (c) its use requires a specialist technician to avoid hurting the patients. A clear need emerges of a low cost, portable, and easy to manage RFD device, which would allow continuously applied RFD treatments, such that the healing of muscle injuries is shorter and of higher quality. In this doctoral thesis, the development of an apparatus with these new features is presented. Initially the design of a prototype for a portable RFD is presented. This prototype is designed and implemented with discrete components to evaluate the effectiveness of continuous rehabilitation treatment. The prototype is validated through a field work according to a medical protocol of physical rehabilitation. Afterwards, and considering the RFD apparatus portability, an integration of the discrete components into a single-chip is implemented, for which a chip in 0.5 μm CMOS technology is presented for a second prototype of an RFD device for physical rehabilitation. This doctoral dissertation starts by making an introduction to RFD, the working principle of this kind of therapy, and the project proposal as a development opportunity in México. Next, the design and validation of a portable radio-frequency diathermy discrete prototype is presented. Afterwards, the design of the programmable oscillator module of the RFD chip, followed by the design of the voltage amplifier module, are described. Finally, the physical design of the RFD chip is presented, including its integration to the pads ring in order to complete the tape-out of the RFD chip. Based on this doctoral thesis, a Mexican patent application has been officially formalized.

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# Introduction

Nowadays, an important part of medicine is physical rehabilitation, because it has become a necessary step of therapy after every physical injury, produced either by accidents or by problems of genetic origin. There are electronic equipment specialized in physical rehabilitation for the treatment of different physical injuries. These devices have a wide variety of characteristics in terms of operation principle, applications, functions, portability, and cost. For example, electro stimulators are used for muscular re-education and pain; the ultrasonic stimulators are used for scaring process; therapeutic laser are used for anti-inflammation and pain; magnetic stimulation are used for bone scaring; and radio frequency diathermy apparatus are used for anti-inflammation and scaring process; to name a few. These therapeutic equipment aim at achieving health benefits in patients but with different operation principles.

Currently, physical rehabilitation sessions are applied in intervals largely separated. The intervals are dictated by the specialist´s availability, since they must schedule many patients and conduct different individualized therapy sessions. In addition, conventional units of electro-stimulators, therapeutic ultrasounds, therapeutic laser and electro-magnets are bulky, they need to be connected to a fixed AC source, and they need special manipulation and continuous supervision from the specialist during rehabilitation sessions in order to avoid damages to patients. There is a clear opportunity for developing radio-frequency equipment with the capacity to work continuously during the first days that physical injuries occur, to provide a more effective anti-inflammation and scaring process. In this doctoral dissertation, a design of a portable physical rehabilitation equipment based on radio-frequency diathermy is presented. First, a research is undertaken on radio-frequency diathermy (RFD) devices, to identify functional characteristics that the proposed new design must have. Then, the electrical characteristics of the electronic system are proposed, namely: shape of the output signal, output power, operating frequency, supply voltage, indicators of the equipment's battery status, energy consumption, cost of manufacturing process, and portability.

Before beginning to design the radio-frequency diathermy (RFD) chip, a macro modeling of electronic system is realized to get an overall idea of the system. With macromodeling we can generate a fairly good approximation of the system's functioning, enabling us to make quick

changes to each block's parameters. This makes it relatively simple to fine-tune the parameters, as many times as needed, to obtain the required results from the entire circuit. Simulations at behavioral level corroborate the appropriate functioning of each block separately and integrated. All of these tests provide the basis to begin designing each of the system blocks at the component level.

Afterwards, a prototype for a portable RFD equipment with commercially available components is designed, implemented, and tested, to give us information about the effectiveness of continuous rehabilitation treatment, proposed as an innovative way of applying RFD. The experimental measurements of frequency, amplitude, and current consumption in the output signal of the prototype show that the implemented prototype equipment generates the adequate RFD signal and fulfill the requirements for RFD standards. Having the portable RFD prototype makes it possible to draw up a fairly specific and defined work plan to obtain important information that allows to identify the minimum current needed for this circuit to achieve positive effects in the scarring of soft tissue in patients specified by specialist physicians.

In order to test the effectiveness of the RFD prototype previously designed and manufactured, a variety of medical tests were applied on a universe of patients with muscle or ligament injuries, which are the conditions that this RFD device is designed for quick and effective treatment. The work field was performed to make a comparative study between continuous mode and conventional of RFD treatments applied to patients with muscular diseases. With this study, it is possible to establish if the duration of exposure to RFD signals has a positive and measurable impact on healing affected muscles. This investigation in the RFD field allows us to validate the hypothesis that the continuous application of an RFD signal in patients with a recent injury is an effective and fast-acting measure for reducing inflammation or healing muscle, ligament, and nerve injuries. The conducted study will also confirm the effectiveness of the proposed RFD prototype for RF diathermy therapy in continuous mode.

After prototype validation, the design at the transistor level of each block of an integrated circuit for portable radio-frequency diathermy (RFD) is presented. The CMOS integrated RFD chip is composed by a low-frequency oscillator (LFO) implemented with 5-stages of current starved delay cells connected on a loop. This topology of LFO circuit handles very small currents in all of its operating stages, to ensure good functioning. A source-follower amplifier is placed at the LFO output in order to provide a gain in current and a good coupling with the next stage. Then,

the design of a voltage-controlled oscillator (VCO) is presented. The VCO is implemented with a 5 stage of differential delay cells with alternated connections. With this type of connection in the VCO circuit, a reduction of phase noise is achieved. Simulations corroborate a better performance in terms of frequency stability and layout area, as compared with a single-ended VCO. Finally, the design of a voltage amplifier circuit with a common-source configuration is presented. Through simulation results it is shown a limitation of CMOS technology to implement voltage amplifiers with inductive load for outputs above 40 V. Then the RFD chip is composed only by a signal generator and the second prototype will be implemented with the designed signal generator a power MOS transistor and a passive inductor.

An important innovation incorporated to the designed RFD apparatus is the programmability of frequency ranges. This feature was incorporated for the purpose of exploring other applications in medicine using the designed RFD apparatus. With this programmability feature, this RFD chip could be used for covering other medical therapies of physical rehabilitation, such as diabetic foot or superficial burns. The intention of this new feature is to provide a simple way to make accurate frequency selection in the RFD apparatus. The frequency selection is performed with a 2-bits control logic circuit (CLC). The CLC is implemented with simple NAND, NOR, XOR gates and inverters.

The design of all the circuit's layouts is described step by step, including the use of techniques such as inter-digitation for large-dimension transistors to achieve a symmetrical, uniform, and dense layout design. The process for achieving pre- and post-simulations is described, and the results obtained from these simulations are given.

Finally, the integration of all circuit's layouts, the connection to the pads ring, and the final manufacture files of the RFD chip are presented.

This thesis document is organized as follows. In Chapter 1, a brief introduction is given to radio-frequency diathermy (RFD), the working principle of this kind of therapy, and the project proposal for the detected development opportunity in México. In the second chapter, the design and validation of a portable radio-frequency diathermy prototype composed by commercially available components is presented. In Chapter 3, the design of the programmable oscillator module of the RFD chip is described. In Chapter 4, the design of the voltage amplifier module is presented, and finally, in Chapter 5, the physical design of the RFD chip is presented, its integration to the pads ring in order to complete the tape-out of RFD chip.

# 1. Radio-Frequency Diathermy (RFD) and Related Opportunities in Mexico

Radiofrequency diathermy (RFD) is a therapeutic technique that has been used for decades in the field of physical rehabilitation. A conventional RFD unit consists of a signal generator and an amplifier designed to deliver a constant or a pulsed RF wave at a single frequency and with an intensity capable of producing heat inside tissues. Many studies have shown a beneficial therapeutic effect with pulsed output, although the mode of action remains not explained enough. Some works indicate that therapeutic benefits depend not only upon the operating frequency and intensity of radiation, but also on the duration of exposure. In this chapter, basic concepts on RFD are presented, the current market of RFD in Mexico is described, its limitations, and a new approach to RFD apparatus for improving treatments based on the principle of RFD is described. The proposed RFD apparatus is a portable, comfortable, and easy to use unit for continuous RFD treatments.

## 1.1. Radio-Frequency Diathermy (RFD)

Radiofrequency diathermy (RFD) is a therapeutic technique that has been used for decades in the field of physical rehabilitation. RFD is used to heal muscle and nerve injuries caused by accidents or congenital disorders in people of all ages.

### 1.1.1 Classification of RF for Medical Uses by Frequency Range

Different frequency ranges in RF currents generate different electro-physical phenomena in the human body.

Table 1.1 shows some of the most common radio frequency ranges and their corresponding medical applications [Rodriguez-Martin-10].

### 1.1.2 The Working Principle of RFD

TABLE 1.1. RF RANGES AND THEIR MEDICAL APPLICATIONS

| Name | Frequency | Medical Application |
|---|---|---|
| D'Arsonval | 0.5-1 MHz | Anti-Inflammation |
| Diathermy | 1-10 MHz | Scarring Process |
| Short-Wave | 10-40 MHz | Scarring Process |
| Ultra-Short | 40-432 MHz | Superficial Scarring Process |
| Micro-Wave | 500-2450 MHz | Superficial Heating Process |

The application of a non-ionizing electromagnetic field on tissue raises the temperature and causes a greater vascularization of the injured area, which stimulates a quicker and higher-quality scarring process. This healing technique that uses heat generated by an electromagnetic radiofrequency field is called radiofrequency diathermy (RFD). Although heat may be delivered into tissues via several mechanisms, such as conduction (e.g., hot packs, paraffin dips, electric heating pads, microwavable rice-filled bags), convection (e.g., hydrotherapy, fluid therapy, cryotherapy), radiation (e.g., infrared lamps) [Allen-06], and conversion (e.g., sound, electricity, or a chemical agent). The last mechanism involves the changing of one form of energy into heat, for instance, in ultrasound therapy, mechanical energy produced by high-frequency sound waves is converted to heat energy at tissue interfaces and, in RFD, electromagnetic energy is converted into heat. With both ultrasound and RFD techniques heat is produced deeper in the tissues [Reid-17] compared with conduction, convection or radiation based techniques.

Typically, a RFD unit consists of a signal generator and amplifier designed to deliver a constant or a pulsed RF wave at a single frequency and with an intensity capable of producing heat inside tissues. The electromagnetic field is applied by means of 2 circular metallic electrodes as it can be seen in Fig. 1.1a [Vescica-11] [Teckra-11] [Sixtus-12] [EPS-14] [Neutec-12]. RFD units are usually bulky and cord supplied.

When the human body is exposed to a non-ionizing radio-frequency electromagnetic field (RF-EMF), the RF energy is attenuated as it penetrates body tissues. Energy absorption depends on the kind of exposed tissue and the radiation frequency. Water in tissues has a high dielectric constant, so it regulates the penetration of frequency- specified EMF. Fig. 1.2 shows an example of the dielectric properties of the human muscle [Gabriel-96].

The rate of energy absorbed by or deposited per unit mass per unit time is the specific

a) b)

Fig. 1.1 a) Resistive RFD equipment of Cormat Company. b) Electrodes Application in the RFD therapy. Figures taken from www.cormat.mx.

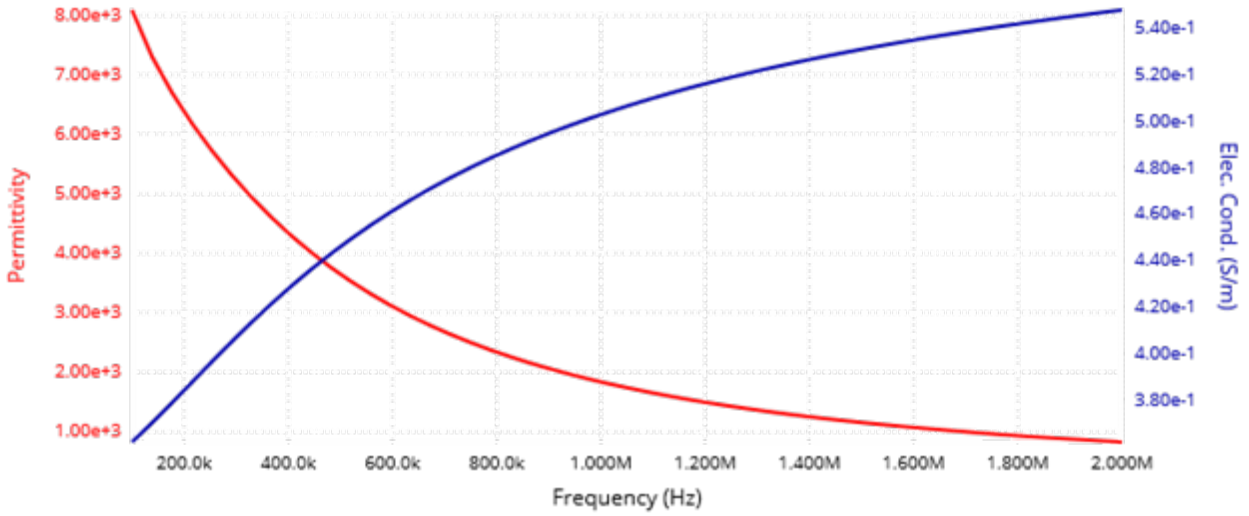



Fig. 1.2 Dielectric properties of the human muscle [Gabriel-96].

absorption rate (SAR) [IARC-13], the value is calculated by

$$SAR = [E]^2 \times \frac{\sigma}{\rho} \tag{1-1}$$

where $E$ is the induced electrical field, $\sigma$ is the electrical conductivity and $\rho$ is the tissue density.

The impedance of biologic tissues is given by the Cole-Cole model [Grimnes-00] as follows

$$Z = R + \frac{R}{1 + jw\left(\frac{1}{2\pi f_c}\right)^{1-\alpha}} \tag{1-2}$$

where $R$ is the tissue resistance, $f_c$ is the stimulating signal frequency and α is a dispersion constant in the model.

To estimate the heat generated in the tissue in terms of calories, we use the Joule´s law as follows

$$Calories = ZI^2 t \times 0.24 \tag{1-3}$$

where $Z$ is the tissue impedance calculated with (1-2), $I$ is the current through the tissue, $t$ is the time of exposition, and 0.24 is the constant to convert Joules in Calories [Rodriguez-Martin-10].

In the context of pain management, potential therapeutic benefits of heat are due to its effects on metabolic, neuromuscular, and hemodynamic activity [Allen-06]. Although heat in physical therapy can produce tissue healing and nociceptive pain, RFD may have utility in the treatment of chronic pain. With the increases in tissue temperature, there is more oxygen available for tissue repair. Increases in enzymatic activity increase oxygen uptake by the cell, thus enhancing healing [Allen-06].

Studies like the ones presented in [Chung-99] and [Rodriguez-Martin-10] reveal that typical sessions with RFD last about 20 minutes, and the physiotherapist establish the appropriate parameters for initialize each therapy.

Contraindications to RFD include applying heat over regions of acute injury, inflammation, malignancy, thrombophlebitis, in pregnant women, or patients with cutaneous problems. Precautions should be taken when applying heat over areas with impaired circulation, edema, or superficial metal implants or open wounds; with patients manifesting poor thermal regulation, cardiac insufficiency, or acute inflammatory disorders, also with hypotensive patients or patients prone to syncope when heating large body areas [Allen-06].

Standards and guidelines for limiting human exposure to RF fields are regulated by 2 principal organizations; The International Commission on Non-Ionizing Radiation (ICNIRP) and the Institute of Electrical and Electronic Engineers (IEEE). ICNIRP published its present RF guidelines in 1998 (ICNIRP, 1998) and restated them in 2009 (ICNIRP, 2009a). IEEE published its present guidelines in 2005 (IEEE, 2005), but its 1999 guidelines are still used in some countries (IEEE, 1999) [IARC-13].

## 1.2. Development of the RFD in Mexico

TABLE 1.2. RFD EQUIPMENTS AVAILABLE IN THE MEXICAN MARKET

| Manufacturer | Price | Features |
|---|---|---|
| Vescica | 48,930 M.N. | Capacitive RF Diathermy |
| Tekra | 200,000 M.N. | Capacitive and resistive RF Diathermy |
| Sixtus.it | 280,000 M.N. | Capacitive and resistive RF Diathermy |
| EPS Global company | 50,000 MN | Resistive RF Diathermy |
| Indiba | 67,000 MN | Capacitive and resistive RF Diathermy |

Current commercial RFD equipment typically operates with power outputs ranging from 1 to 80 mW, and operating frequencies ranging from 500 KHz to 3 MHz [Vescica-11] [Teckra-11] [Sixtus-12] [EPS-14] [Neutec-12]. In México only 2 companies develop RFD equipment; Vescica for an aesthetic medicine market, and Cormat for physical rehabilitation market. Other companies like Teckra, Sixtus, EPS and Neutec, bring import equipment for physical rehabilitation. Fig. 1.1b shows an example of a RFD device manufactured by the Mexican company Cormat[1].

Table 1.2 presents an overview of these devices.

### 1.2.1 Current Limitations of the Use of RFD in Mexico

The main limitations detected in RFD treatments with current RFD equipment include the following: Physical rehabilitation therapy sessions generally are insufficient and ineffective because they are applied in intervals largely separated. In Mexico, typically RFD treatments are given once or twice a week, in approximately 10 sessions [Vescica-11] [Teckra-11] [Sixtus-12] [EPS-14] [Neutec-12]. According to the effect on human tissues described in Section 1.1.2, to be effective, sessions should be at least 20 minutes long for periods of 10 consecutive days. Large intervals of RFD treatments are dictated by the specialist´s availability, since they must schedule many patients and conduct different individualized therapy sessions.

On the other hand, current RFD devices in the market are very expensive. Most RFD equipment is imported, and their price vary from roughly $15,000 to $60,000 Mexican pesos (Table 1.2) [Vescica-11] [Teckra-11] [Sixtus-12] [EPS-14] [Neutec-12], thus patients who only

[1] Cormat is a Mexican Company with 20 years of experience designing physical rehabilitation equipment. http://www.cormat.mx

need up to 20 therapy sessions cannot afford them.

In addition, almost RFD devices are difficult to operate and require the help of another person to place electrodes on injured area into a correct position.

Finally current RFD devices available on the market operate with high power outputs and its use require the advice or the help of a specialist technician to avoid hurting the patients during RFD application.

## 1.3. Project Proposal

In this doctoral dissertation, it is intended to verify that the application of RFD in continuous mode can cure in a shorter time and in a more efficient way compared with the traditional applications at widely spaced intervals (see Section 1.2.1). To do this, first a prototype with a single frequency range is designed and implemented to test our hypothesis, then we design an integrated electronic circuit for a portable, low price and easy to manage RFD apparatus. With the purpose of exploring other applications in medicine, the integrated electronic circuit is designed with four options of frequency ranges for a second RFD prototype. With this programmability, the RFD apparatus could be used for covering other medical therapies of physical rehabilitation, such as the diabetic foot superficial burns and others. It is important to mention that the author has a certain degree of mastery prior the development of the intended apparatus.

The proposed RFD electronic system must be portable, compact and low energy consumption. The electronic system must be supplied with a rechargeable battery and it must provide the appropriate waveform of an RFD system. The electrical characteristics of the proposed electronic system are: a time-varying output waveform of 8 mW power output (53 μA output current and 150 Volt output voltage), an operating frequency from 500 KHz to 1 MHz which are within the specifications of RFD apparatus [Rodriguez-Martin-10]. The RFD apparatus must be supplied by 5 Volt rechargeable batteries with 10 mAh current. Other characteristics of the finished portable apparatus are: a) low-cost manufacturing process, b) comfortable, and c) easy to manipulate.

Fig. 1.3 shows the block diagram of the electronic system to be developed during the PhD studies. This topology is designed to integrate all components of a RFD device in a single chip.

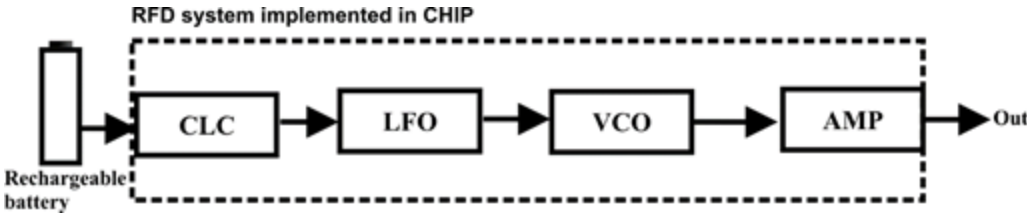



Fig. 1.3 Block diagram for the RFD prototype.

The control logic circuit (CLC), the low-frequency oscillator (LFO) together with the voltage controlled oscillator (VCO) blocks (Fig. 1.3) generates of 5 Vpp of amplitude with a variable frequency in the range of 500 KHz to 1 MHz. The VCO output signal is applied to a voltage amplifier to generate a signal of 150 Vpp with the same frequency range of VCO.

Due to its compactness, low risk of damage, ease to handling and low cost it is expected that this innovated RFD equipment could be used by any patient with muscular problems.

## 1.4. Conclusions

In this chapter we have presented the working principle of radiofrequency diathermy, and its uses in therapy of physical rehabilitation to heal muscle and nerve injuries caused by accidents or congenital disorders in people of all ages.

We have presented an overview of the current commercial RFD equipment in Mexico; their electrical specifications, the main limitations detected in RFD treatments with current RFD equipment, like the way the treatments are currently applied, the cost of the devices in Mexican market, and the difficulty in its operation and power control to avoid hurting the patients.

Finally, we have proposed the design of an integrated electronic system for radiofrequency diathermy (RFD) applications. The system fulfills the compactness and low energy consumption requirements of a portable apparatus. The electronic circuit is composed by a control logic circuit (CLC), a low frequency oscillator (LFO), a voltage controlled oscillator (VCO), and a voltage amplifier. With the CLC, LFO and VCO circuits it is possible to select four different frequency sweeps within 500 KHz to 1 MHz. The amplifier circuit rises the VCO output from 5 Vpp to 150 Vpp with an alternative output waveform of 8 mW power output with a frequency sweep from 500 KHz to 1 MHz.

# 2. Design and Validation of a Portable Radio-Frequency Diathermy Prototype

Before designing a chip for the RFD apparatus, a design and implementation of a prototype for radio-frequency diathermy (RFD) using commercial electronic components is done. This design is made to validate the hypothesis that continuous RFD helps damaged muscles to heal in a shorter time and in a more effective way. Although this prototype does not fulfill the requirements of compactness and low power consumption as compared with the features that can be achieved with a system integrated in a chip, it gives us information about the effectiveness of continuous rehabilitation treatment, proposed as an innovative way of applying RFD (Section 1.3). The RFD prototype is designed to generate a voltage of 150 Vpp and a varying frequency in the range from 500 KHz to 1 MHz, with the capability to repeat this sweep every second. The prototype is validated with a work field applied to a universe of 20 patients with lumbago problem. The work field shows that regardless of the patient's skin properties, the longer the duration of radiation exposure, the greater the amount of energy that will be absorbed by the tissue, and thus, a better healing muscle in a short time is obtained. This chapter is based on [Corres-Matamoros-17b].

## 2.1. Macro Modeling of RFD System

Before beginning the design of radiofrequency diathermy (RFD) prototype, it is important to get an overall idea of the system's behavior. Simulation of the complete system at component level is a titanic task and demands considerable computing resources and time. Macro modeling can generate a fairly good approximation of the system's functioning in a very short time. Macromodeling enables us to make changes in block's parameters in a simple way to fine-tune the parameters as many times as needed in order to obtain the required results from the entire system [Fitz-03]; then simulation of the system can be performed at behavioral level in order to assess its response as a whole.

As indicated in the Section 1.2, the RFD system is made up of 3 main blocks: a) a control

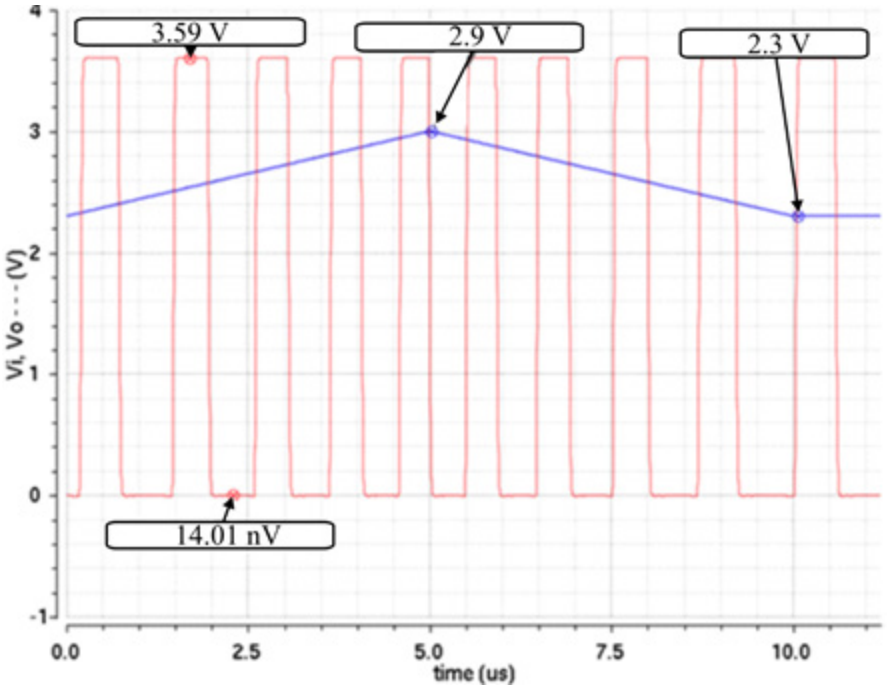



Fig. 2.1 Transient response of behavioral model based VCO stage.

logic circuit (CLC), b) a low frequency oscillator (LFO), c) a voltage-controlled oscillator (VCO), and d) a voltage amplifier. The macro modeling of the last 2 blocks and the simulation results are outlined below. The CLC is not macro-modeled but design as part of RFD chip.

### 2.1.1 Voltage Controlled Oscilator (VCO)

At the beginning of this project it was thought to use a 3.6 V battery as power supply, so the macro modeling was made using this value. The voltage-controlled oscillator (VCO) block is in charge of generating a square signal with an amplitude of 3.6 Vpp in the 500 KHz to 1 MHz frequency range, which are the frequencies needed in the signal of the RFD chip [Rodríguez-Martín-10]. The circuit is required to have a frequency accuracy of 3%, which is a typical figure of merit in commercial oscillators [TI-15]. The signal generated by the oscillator is applied to the voltage amplifier to activate it. The name given to this block is VCO_va and its code in Verilog A language is presented in Appendix 3, this code was adapted from [SIMETRIX-10] to the design specifications of the RFD prototype. Once the VerilogA code of the VCO block is implemented, we proceed to assess its behavior by running a simulation in the time domain. The simulations results are presented in Fig. 2.1. This figure shows that when the input voltage is 2.9 V, the VCO's

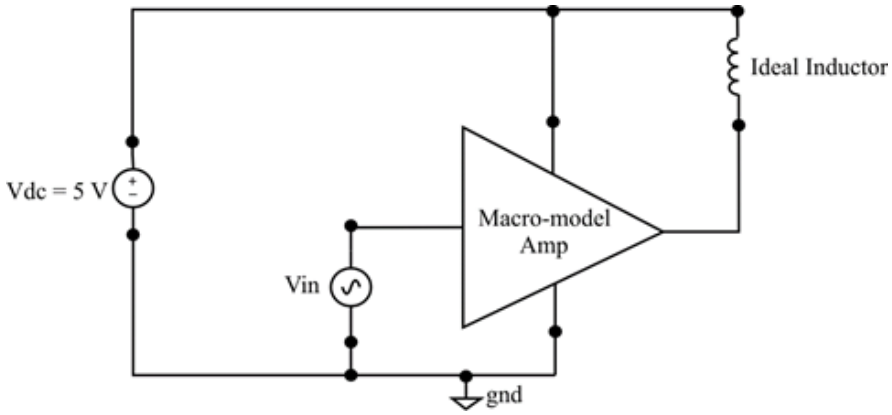



Fig. 2.2 Testbench of voltage amplifier with ideal inductor implemented in Virtuoso-Cadence.

output frequency is 1 MHz, and when the VCO input voltage decreases to 2.3 V, the output frequency drops to 500 KHz, meaning that the circuit's operational frequency can be set using these two voltage levels.

### 2.1.2 Voltage Amplifier

The amplification block named AMP_va is in charge of amplifying the signal provided by the VCO block. With the 3.6 Vpp input signal amplitude provided by VCO, and the 150 Vpp required for the RFD treatment (Section 1.2), it follows that the amplifier's voltage gain is 42 V/V. Notice when a 5 V of input amplifier is used the voltage gain must be 30 V/V. In Appendix 2 we define the Verilog A code of a current amplifier, this code was also adapted from [SIMETRIX-10]. The behavioral model of the current amplifier is combined with an ideal inductor to generate voltage amplification stage. The entire circuit was simulated at the behavioral level; to do this, the circuit schematic was captured at symbol level in Virtuoso-Cadence (Fig. 2.2).

The voltage generated by an inductive load is given by

$$V_O = V_L = L\frac{di}{dt} \tag{2-1}$$

where $L$ is the value of the inductance's coil and $di/dt$ is the change in current through the coil with respect to time.

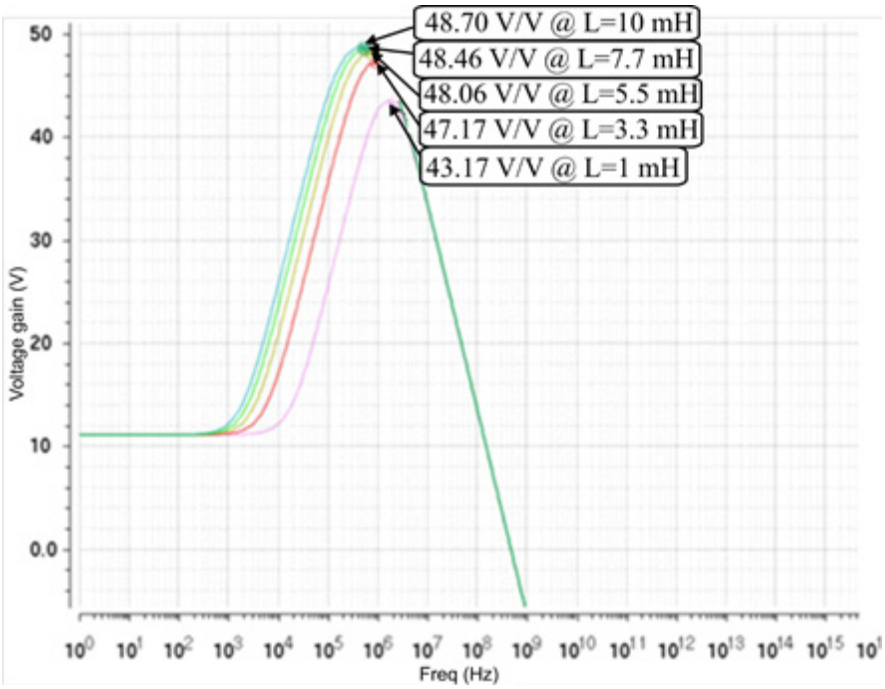



Fig. 2.3 Frequency response of the behavioral model based amplifier varying the value of the inductance from1 mH to 10 mH.

To achieve an output voltage of 150 Vpp, from (2-1) it is evident that for a given inductance value, a large current variation with respect to time (*di/dt*) is needed, from which we can conclude we must use a square waveform signal as input of voltage amplifier. In order to evaluate the appropriate inductance value required in the voltage amplifier circuit, a parametric sweep was performed in the voltage amplifier circuit. A testbench (Fig. 2.2) is implemented with a square input signal having a frequency of 1 MHz and 3.6 Vpp of amplitude, a rise time ($t_r$) and a fall time ($t_f$) of 1 nS; the parameter $L$ is varied in the range from 1 mH to 10 mH. Fig. 2.3 shows simulation results, from which one can note that with an inductance value of 1 mH, one achieves a specification of gain of 43.17 V/V at frequencies close to 1 MHz. Thus, it is concluded that we need an inductance of at least 1 mH to implement the voltage amplifier with inductive load for the RFD chip.

The next step is to observe the effect of the amplifier's gain in the amplification stage. The output current in the behavioral model is $I_{out} = g_m V_{in}$ (see Appendix 3), so for this analysis we vary $g_m$ in the range of 100 µA/V < $g_m$ < 10 mA/V, with an inductance value of $L$ = 1 mH. The simulation results are shown in Fig. 2.4, and the voltage gain of the amplifier was proportional to $g_m$ in the behavioral model. Thus, it was concluded that we needed a $g_m$ of 10 mA/V to obtain a voltage gain close to 42 V/V when $L$ =1 mH and $V_{in}$ = 3.6 Vpp.

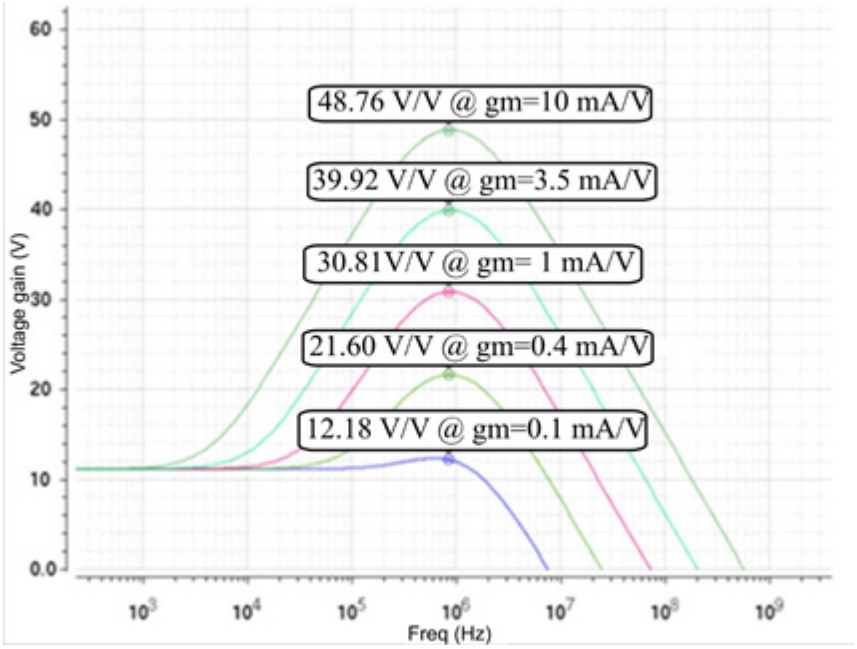



Fig. 2.4 Frequency response of the behavioral model based amplifier varying the value of the $g_m$ from 100 µA/V to10 mA/V.

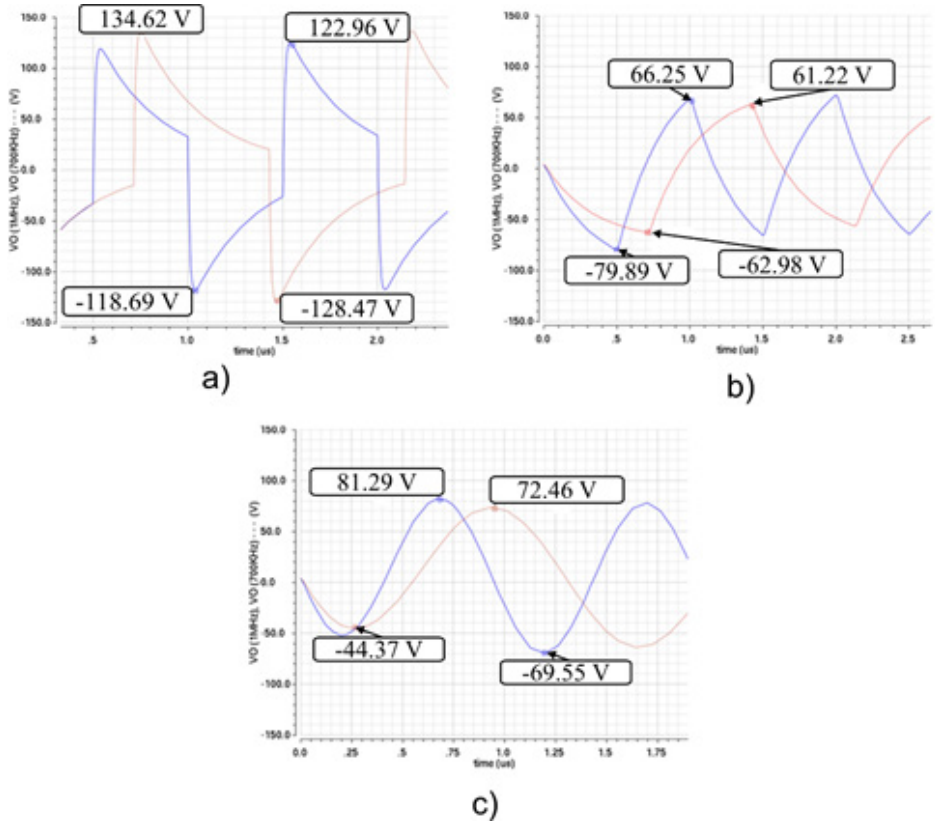



Fig. 2.5 Output voltage of the behavioral model based amplifier with $L$ = 1 mH, using a) a square input signal, b) a ramp input signal, and c) a sine input signal.

For the analysis in the time domain, a testbench (Fig. 2.2) was made up of 3 input signal

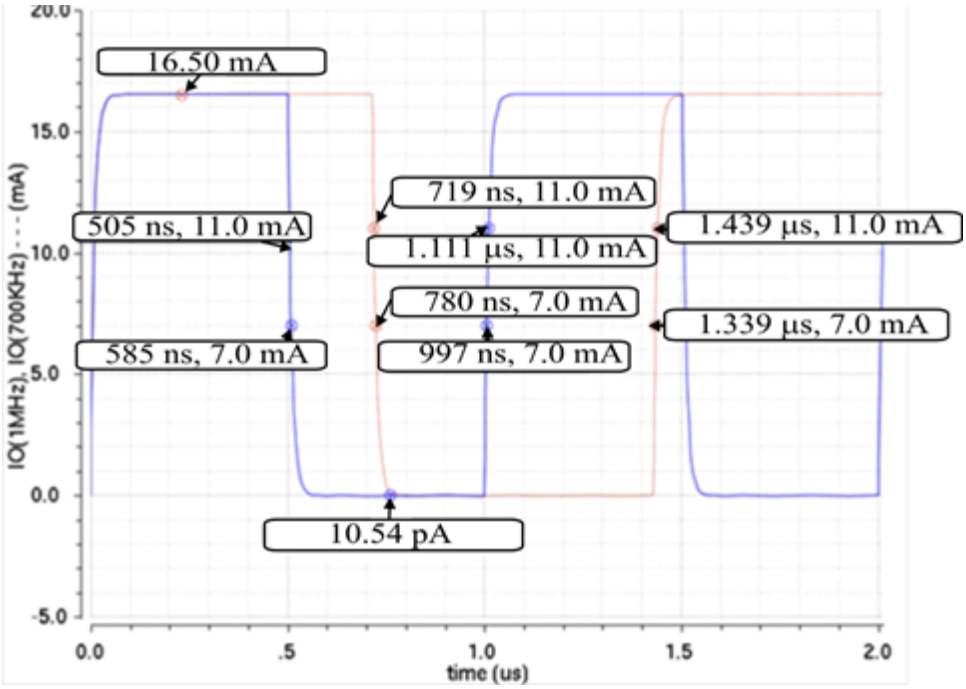



Fig. 2.6 Output current of the behavioral model based amplifier with an ideal inductance. In blue 1 MHz and in red 500 KHz.

sources: one square, one sinusoidal and one ramp signal with operational frequencies of 500 KHz and 1 MHz. For the square voltage signal source, a rise-and-fall time of 1 ns respectively was set, with a pulse width of 500 nS and a period of 1 µS, which produces a signal of frequency of 1 MHz and amplitude of 3.6 V. To generate the 500 KHz frequency, we simply change the pulse width to 1 uS and a period of 2 µS. This square signal generates a current wave in the amplifier's output node with the same shape and frequency as the input signal. The response in the time domain using this type of input source is shown in Fig. 2.5a. One observe from this figure, that in the three cases of input signal, a voltage around 100 V in the amplifier output node. Fig. 2.5b shows simulation results with a ramp signal as an input source with an amplitude of 3.6 Vpp and operational frequencies of 500 KHz and 1 MHz. Fig. 2.5c. shows the simulation results of the testbed with a sinusoidal signal with an amplitude of 3.6 Vpp and with operating frequencies ranging from 500 KHz and 1 MHz. Fig. 2.6 shows the value of *di/dt* slope of square waveform current signal at the amplifier's output node: we observe when using the 500 KHz square signal, the downward slope is $m_f = 65\times10^3$ and the upward slope is $m_r = 40\times10^3$. When we use an input signal with a frequency of 1 MHz, the downward slope is $m_f = 50\times10^3$ and the upward slope is $m_r = 35\times10^3$. For this macro modeling, using (2-1), $L = 1$ mH, and $di/dt = m_f$ we obtained a maximum output voltage of 208 Vpp for an operation frequency of 1 MHz, and a maximum output voltage of 160 Vpp for 500

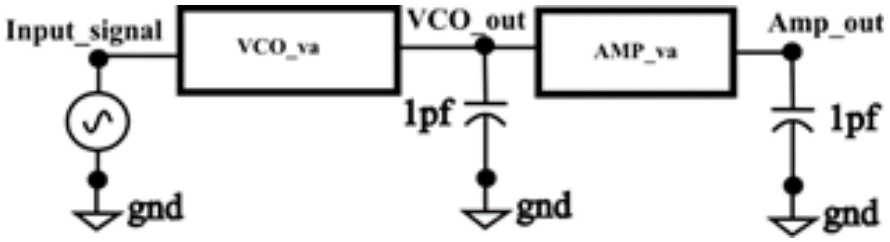



Fig. 2.7 Testbench of the RFD system to simulate in Virtuoso-Cadence.

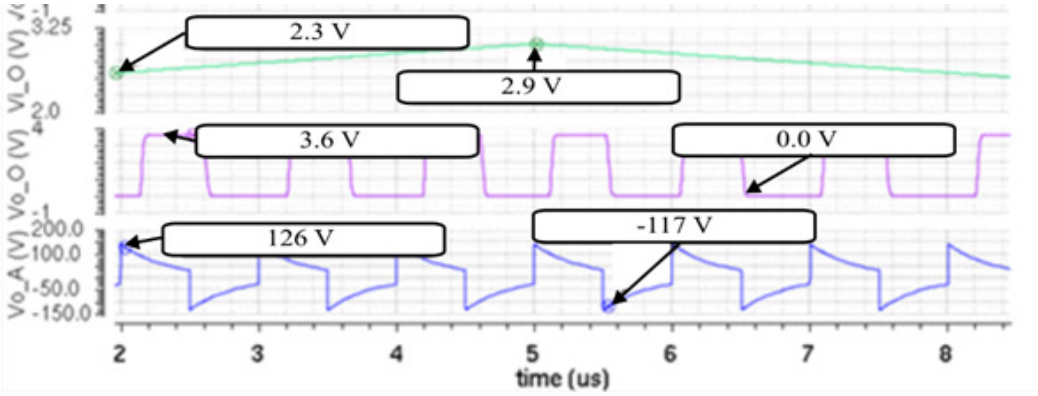



Fig. 2.8 System level simulation of the RFD chip.

KHz.

With all the results from macromodeling, we can conclude that to use an amplifier with inductive load, a square signal input signal must be used because it is the signal that enables us to achieve an output voltage that meets the specifications for this project.

### 2.1.3 System Level Simulation of RFD System

For the overall-system simulation, the schematic of the two RFD system´s building blocks is captured in Virtuoso-Cadence (Fig. 2.7). Then a simulation in time domain is performed using a PWL-type input source for the VCO to generate an upward ramp of 2.3 to 2.9 V in 3 µS and a downward ramp between 2.9 V and 2.3 V in 3 more µS. Fig. 2.8 shows the response in the time domain of each of the stages described above.

## 2.2. Prototype Design with Commercial Components

The block diagram of the RFD prototype is presented in Fig. 2.9. The LFO and VCO

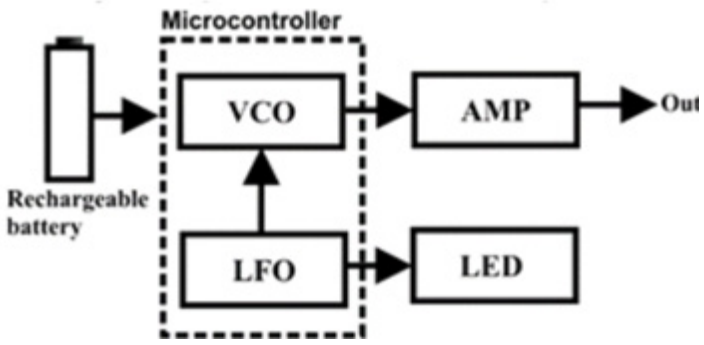



Fig. 2.9 Block diagram proposed for the radio frequency diathermy (RFD) system. Figure taken from [CORMAT-06].

modules are implemented with a microcontroller. The voltage amplifier is implemented with a power MOSFET and a passive inductor.

### 2.2.1 The Oscillator Module

The LFO and VCO circuits were implemented with a microcontroller from Microchip Company, we use an 8-bit PIC10F200-I/P component which operates at a frequency of 4 MHz and 384 bytes of flash memory which in addition is small size component [MICROCHIP-14]. All these features allow a compact design in the printed circuit board, which is a requirement for the portable RFD prototype. The internal timer of this microcontroller is used to generate the time references needed to produce a signal with an amplitude tuned in the range from 0 to 5 V and a frequency sweep from 500 KHz to 1 MHz. A subroutine having a variable delay is used to change every cycle the value of an output pin in the microcontroller. Every certain time this variable delay is increased until the minimum output frequency is reached. Next, a reset in the value of the variable delay produces the maximum output frequency in the output pin of the microcontroller.

### 2.2.2 The Voltage Amplifier Module

The voltage amplifier block is in charge to convert the signal from the microcontroller into a signal with a maximum amplitude of 150 Vpp. Design specification of this circuit were obtained as follows: the required output voltage amplitude is 150 Vpp, and $V_{in}$ = 5 V (from microcontroller) then $|A_v| = V_o/V_{in}$ = 30 V/V.

A common-source amplifier was chosen to implement the voltage amplifier. This configuration is the adequate in terms of input/output impedance, and voltage gain. In the common-source amplifier with source degeneration the small-signal voltage gain $A_V$ is given by

$$A_V = \frac{-g_m R_{out}}{1 + g_m R_s} \tag{2-2}$$

where $R_{out}$ is the parallel combination of $R_L$ and $r_{ds}$, $R_L$ is the resistance of the inductor used, $r_{ds}$ is the drain-source resistance, $g_m$ is the transistor transconductance, $R_s$ is a resistor used in the source degeneration configuration. Since linearity is not important for this application, we have opted for $R_s = 0$. On the other hand, taking into account that $R_L << r_{ds}$, (2-2) can be simplified as $A_v = -g_m R_L$.

The reactance of the inductor is given by

$$R_L = X_L = 2\pi f L \tag{2-3}$$

where $f$ is the operation frequency of the amplifier and $L$ is the inductance value of the inductor. For a $f$ = 500 KHz and $L$ = 1 mH, we obtain an $X_L$ = 3140 Ω, and for a $f$ = 1 MHz we obtain a $X_L$ = 6,280 Ω.

Using the simplified version of the voltage gain, $g_m$ is given by

$$g_m = \frac{|A_v|}{R_L} \tag{2-4}$$

from (2-4) we obtain for an $R_L$ = 3140 Ω a $g_m$ = 7.64 mS and for an $R_L$ = 6280 Ω a $g_m$ = 3.82 mS. The $g_m$ value is used to calculate the maximum current $I_D$ in the amplifier through

$$g_m = \frac{2I_D}{V_{eff}} \tag{2-5}$$

where $V_{eff} = V_{GS} - V_{Th}$ = 3 V, is the transistor overdrive voltage, we find the required minimum $I_D$ of 5.73 mA. Thus, to ensure proper operation, we select a power MOSFET with much larger $I_D$ than the previously calculated. A commercial MOSFET with such features is the IRF640[2] [LTC-

[2] This transistor is TO-220AB package, $V_{DSS}$ = 200 V and $I_D$ = 11 A.

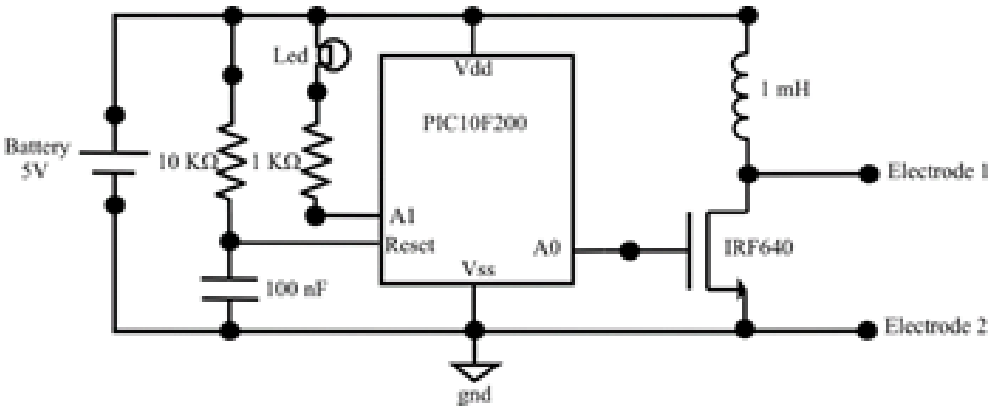
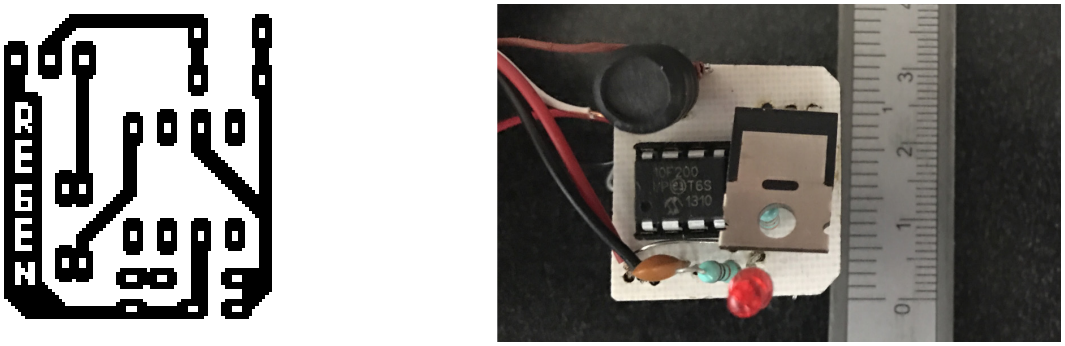



Fig. 2.10 Schematic of the RFD prototype using a PIC10F200 microcontroller and discrete components.



a) b)

Fig. 2.11 a) Prototype PCB layout. b) RFD prototype implemented with commercial components.

10], that has a $V_{Th}$ = 2 V and can manage an $I_{Dmax}$ = 11 A.

As load for the common-source voltage amplifier we use a Bourns inductor[3] [BOURNS-10] of 1 mH.

On the microcontroller's A1 pin, we connect in series a LED and a 1 kΩ resistance toward the power supply. The LED is used to indicate the user that the equipment is turned on. In this prototype, the power supply is a rechargeable Steren-brand MOV-102 battery, with a charge capacity $C_{bat}$ = 2000 mAh and an output voltage of 5 $V_{DC}$. Fig. 2.10 shows the schematic of the RFD prototype with discrete components.

The next step in the prototype design is the design of the printed circuit board (PCB) layout. The PCB layout was generated with Eagle V7 CAD tool. The PCB was designed to achieve as much as possible circuit miniaturization considering the size of all circuit components (Fig. 2.11a).

[3] Dimensions of this inductor is 8 mm (high), 11.2 mm (diameter), and $I_{max}$ = 150 mA.


Fig. 2.12 Cabinet and wires with metal electrodes used for the RFD prototype.

Fig. 2.11b shows the assembled RFD prototype, in which we can observe a compact RFD circuit. Fig. 2.12 shows the plastic cabinet in which the RFD apparatus described above is enclosed, together with the wires with metal electrodes that are in contact with the patient's skin to deliver the signal from the portable RFD apparatus.

## 2.3. Prototype Characterization

After assembling the circuit, we have characterized the RFD prototype. The electrical signals generated by the prototype were measured with a Tektronix TBS 1102B oscilloscope.

In Fig. 2.13 we observe a pulsed voltage signal at 679 KHz, and 84 V peak to peak amplitude. As explained in Section 1.2, this waveform of the RFD system is close to the expected one for a common-source amplification stage with inductive load. This signal was measured in the terminal *Electrode 1* of Fig. 2.10.

The measured average current consumption of the entire circuit working connected to the skin of one patient was $I_{bat}$ = 23 mA (see Fig. 2.14). This signal was measured in the positive pole of the battery in Fig. 2.10. Considering that the battery voltage is 5 V, the calculated power consumption is 115 mW.

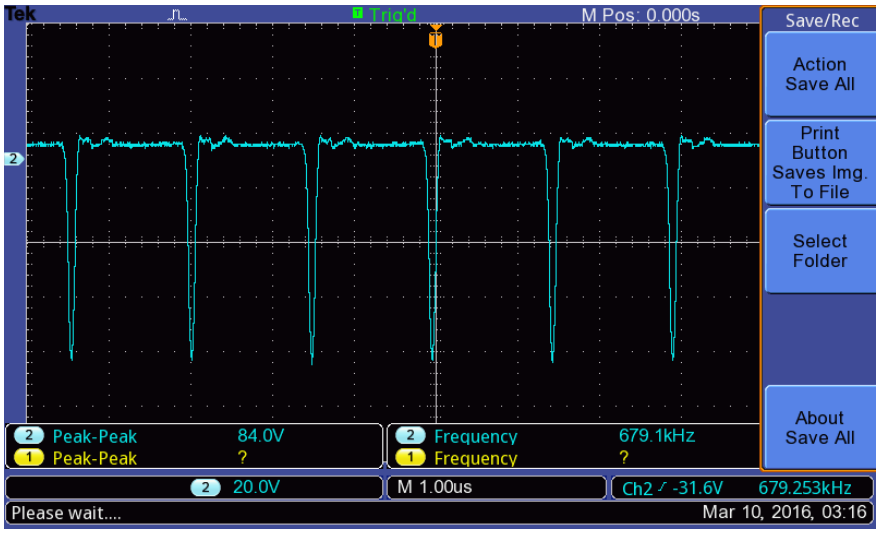



Fig. 2.13 Output voltage of the RFD prototype measured with a Tektronix TBS 1102B oscilloscope.

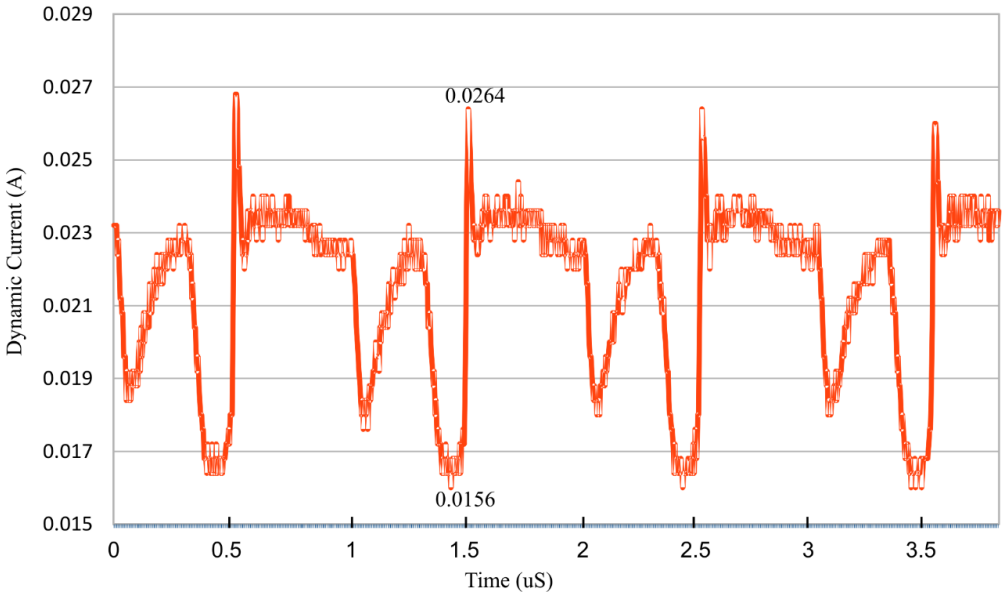



Fig. 2.14 Instantaneous current consumption of the radio-frequency diathermy (RFD) prototype measured during treatment of one patient.

The time $T_o$ in which the prototype can remains continuously turned on is given by

$$T_o = 0.7\frac{C_{bat}}{I_{bat}} \tag{2-6}$$

Considering at least 48 hours of continuous operation and a total current consumption $I_{bat}$ = 23 mA, from (2-6) a $C_{bat}$ = 1,577 mAh is needed.

## 2.4. Prototype Validation

In order to test the effectiveness of the RFD signal applied in continuous mode using the prototype designed (Section 2.2), a variety of medical tests were applied on patients with muscle or ligament injuries [Corres-Matamoros-17b].

The fieldwork was conducted by two students from the Bachelor's Degree Program in Physical Therapy at the *Universidad Autónoma de Guadalajara* (UAG), under the advice of Dr. José Antonio Rojas, who is a specialist in physical rehabilitation. Students from the final semesters of the above program were carefully chosen so that they would have enough experience to reliably run the required field tests.

In this fieldwork, we involve a universe of 20 patients with a lumbago problem[4]. Lumbago usually manifests itself after the person engages in physical activities, sudden movements, or when they lift heavy objects [Frenier-81]. One of the most common causes of acute lumbago is muscle or ligament strain in the back. These kinds of problems can be produced by lifting a heavy object, twisting, or making a sudden movement.

The level of pain from a lumbar muscle strain can vary from slight discomfort to strong incapacitating pain; it depends on the degree of strain and the lumbar muscle spasms caused by the injury [Frenier-81]. This kind of injury is difficult to treat with other electrotherapy devices, inasmuch as it is a spinal injury. This area of the human body is close to the surface and full of ligaments, nerves, and bones.

### 2.4.1 Physical Rehabilitation Protocol Description

As part of the medical protocol, first a brief clinical history is written up for each patient who will participate in the fieldwork, with the following information: name, age, weight, height, number of children, occupation, marital status, hereditary medical history, and personal medical history. Once the records are taken, the patients are divided into similar pairs, for example, two patients with obesity, two elderly patients, or two female patients, and so on, until two groups are formed, with each member corresponding to a similar member in the other group.

[4] Lumbago is one of the most common ailments found in physical medicine, occurring in people between the ages of 30 and 60 with sharp or dull pain in the lower back.

TABLE 2.1. CLINICAL HISTORY OF CONTROL PATIENTS (GROUP A)

| Patient´s ID | Age (years) | Weight (Kg) | Height (m) | Occupation | Civil condition | Familiar background | Personal background |
|---|---|---|---|---|---|---|---|
| 1A | 37 | 65 | 1.68 | Home | Married | Hypertension + Diabetes + overweight | Scoliosis + Cervical distension |
| 2A | 84 | 80 | 1.64 | Attorney | Widower | Hypertension + Cancer | Diabetes Mellitus type 2 |
| 3A | 31 | 82 | 1.82 | Traumatology doctor | Single | Hypertension + DM | Smoker |
| 4A | 54 | 74 | 1.60 | Nurse | Married | Hypertension | 2 Cesaris |
| 5A | 49 | 65 | 1.50 | Home | Married | Diabetes + Cancer | Hypotension |
| 6A | 17 | 60 | 1.75 | Student + acrobat | Single | Hypertension + diabetes + Vein insufficiency | Falange distal surgery in a finger |
| 7A | 32 | 58 | 1.67 | Student + home | Married | Tiroidal cancer + Diabetes | Ovarium tumor + Muscular debility |
| 8A | 51 | 100 | 1.80 | Engineer | Married | Hypertension + Colon cancer | Litiasis + Overweight + Hypercolesterolemia |
| 9A | 21 | 75 | 1.87 | Student | Single | --- | Ankleintesti fracture + Lazy intestine |
| 10A | 19 | 65 | 1.78 | Student | Single | Diabetes | --- |

From 20 patients to be treated, 10 patients have received conventional treatment (it is called group A), while the other 10 patients have received continuous application of RFD during the first 2 weeks of therapy using this prototype (this is called group B). The conventional treatment consists of the application of 1 MHz of ultrasound at an intensity of 2.4 W/cm$^2$ during 10 minutes, followed by another 10 minutes of electro-stimulation with a “Pulse Train” electrical current at an intensity of 40 mA. This treatment is applied with commercial RFD device COMBOCORMAT CE-131 from Cormat Co. [Cormat-06]. Following ultrasound and electro-stimulation treatments, the patients perform flexion, extension, lateralization, and rotation exercises in the treated area. Group B is provided starting at the first session with an RFD device placed by the therapists specifically on the injured area for continuous treatment until the patient returns for the following therapy session in two days. At that time, the RFD device is removed during conventional therapy, and at the end of the session, the device is put in place once again. These same steps are followed

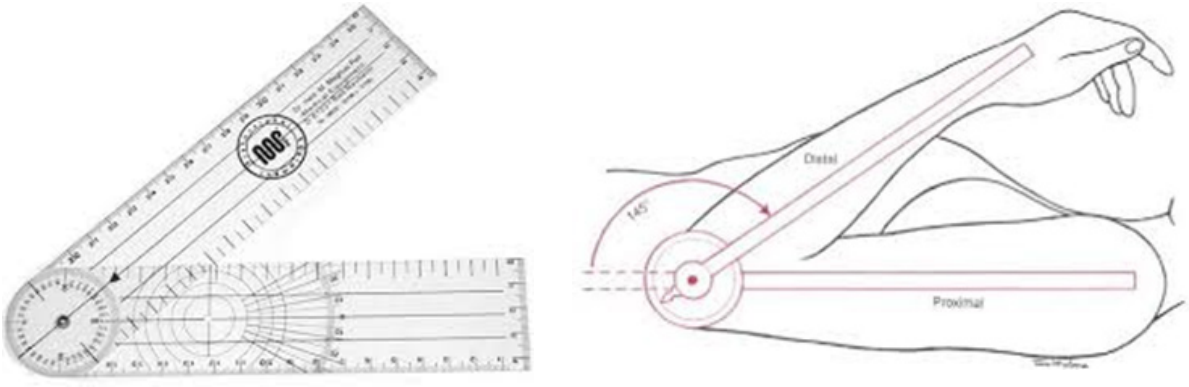
TABLE 2.2. CLINICAL HISTORY OF PATIENTS (GROUP B)

| Patient´s ID | Age (years) | Weight (Kg) | Height (m) | Occupation | Civil condition | Familiar background | Personal background |
|---|---|---|---|---|---|---|---|
| 1B | 62 | 57 | 1.27 | Attorney | Widow | Hypertension + Diabetes | Laparotomy + Falopy Desertion + Bladder ligature |
| 2B | 70 | 68 | 1.52 | Home | Widow | Hypertension | Gastritis + Colitis + Kcidney stone |
| 3B | 56 | 70 | 1.20 | Business | Widow | Diabetes | Diabetes + Frozzen shoulder |
| 4B | 63 | 73 | 1.57 | Doctor | Married | Hypertension + Diabetes | Amygdalotomy + Sistecolestomy |
| 5B | 59 | 56 | 1.60 | Business | Married | Cancer | Hypotension + Osteoporosis |
| 6B | 22 | 54 | 1.63 | Student + pole dancer | Single | Breast cancer + diabetes + hard attack | Gastritis |
| 7B | 18 | 93 | 1.72 | Student + bicyclist | Single | Diabetes + Hypertension | --- |
| 8B | 23 | 70 | 1.67 | Student | Single | Diabetes + Hypertension | Dysplasia |
| 9B | 22 | 72 | 1.73 | Student | Single | Hypotension + diabetes + tiroidal cancer | Falange amputation of a finger |
| 10B | 23 | 110 | 1.90 | Student | Single | Alzheimer | Nose surgery |

during 4 sessions in a row, which take approximately 2 weeks. The results of the improvement in each patient's injury are recorded weekly, in order to obtain an idea of the gradual evolution. Once the 4 sessions are over, the results of Group A and Group B are compared to see whether the RFD device offers an advantage when used in this type of therapy with different types of patients.

Table 2.1 shows the data of each of the patients taking part in this fieldwork to validate the RFD prototype. From Table 2.1 we can see that 80% are women with ages ranging from 22 to 70 years, while the other 20% are men with ages ranging from 17 to 84 years. We can also see different ailments that their closest relatives have had. This information is important to take into account because it gives an idea of each patient's genetic problems, as well as their current ailments, which are very important for determining whether they are candidates for this type of therapy.

Table 2.2 shows the control group, which consists of the subset of patients that underwent traditional therapy without using the continuous-use RFD device. This group's results served for




a) b)

Fig. 2.15 a) Goniometer. b) Goniometry example. Figures taken from [Cameron-09].

comparison purposes, to determine whether the continuous-use RFD prototype makes a difference for these types of ailments.

### 2.4.2 Techniques to Measure the Evolution of Patient´s Injuries

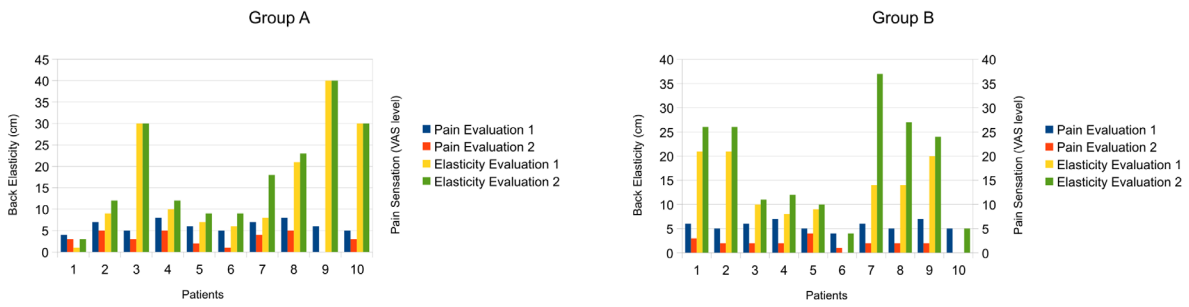
To measure the way patients' condition gradually improved in both Group A and Group B, two techniques were used. The first one is called Shober goniometry[5] technique [Cameron-09] [Godges-10]. The main objectives of this technique are to evaluate the position of the joint in space; to evaluate the arc of movement of a joint in each of the three planes of space; and to describe the presence of misalignments of the osteoarticular system for diagnostic, prognostic, therapeutic, and research purposes. In physical rehabilitation, goniometry is used to determine the initial point of a treatment, to evaluate its progress over time, to motivate the patient, to establish a prognosis, to modify or terminate the treatment, and finally, to evaluate the results. This technique is also used to quantify the evolution of athletes' training.

In order to take the measurements with these techniques, a goniometer[6] is used [Arana-13]. This is a practical, economic, portable and easy-to-use instrument.

The second technique for measuring the pain parameter in patients is called the Visual Analogue Scale (VAS) [Rivas-10]. This technique consists of a very simple test in which patients

[5] Goniometry is a discipline that studies the measurement of angles.

[6] This instrument is generally made either of plastic (usually transparent) or metal (stainless steel). Goniometers have a body and two arms, one fixed and the other mobile (see Fig. 2.15a) and Fig. 2.15b). The body of the goniometer is actually a 180º or 360º transporter.




a) b)

Fig. 2.16 a) Pain and elasticity evolution (group A) from first to fourth visit. b) Pain and elasticity evolution (group B) from first to fourth visit.

indicate the intensity of a certain symptom on a scale from 1 to 10. Studies show that the value of the scale reflects in a reliably way the pain intensity and its evolution [Rivas-10]. Thus, this technique provides a reference for assessing the intensity of a person's pain over time, but it does not allow a comparison of two different people's pain. VAS techniques can also be applied to other quality-of-life measurements such as happiness and comfort.

### 2.4.3 Results of the Applied Therapy

Fig. 2.16a and Fig. 2.16b show the evolution of pain reduction and the recovery of lower-back elasticity in patients of Group A and Group B, respectively. It is clear from both figures that the pain relieving and increased elasticity was better for the Group B.

The results of Fig. 2.16a and Fig. 2.16b are quantified and they are summarized in Fig. 2.17, in which one can observe a decrease of 80 % of pain in patients who have used the RFD device continuously, as compared to 50 % improvement in the patients who received traditional therapy. Regarding elasticity, a 22 % of increased elasticity is estimated in the patients who have used the RFD device continuously, as compared to a 7 % improvement in the patients who receive traditional therapy. Although these results are still not concluding, this study clearly indicates a more effective muscle healing by applying a continuous-mode RFD signal. These results can be explained by considering that the amount of energy absorbed by tissues from electromagnetic radiation depends not only on the skin properties of patients, the operating frequency, the intensity

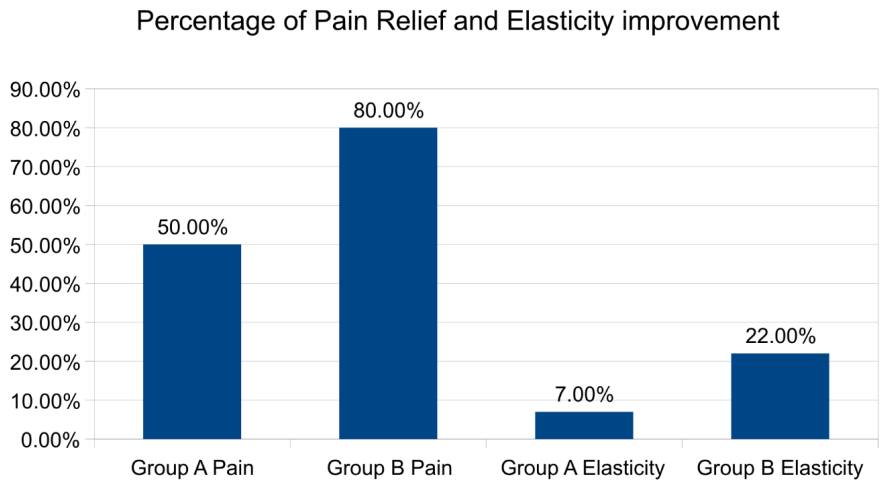



Fig. 2.17 Percentage of improvement in pain relief and elasticity improvement of Group A and Group B.

of radiation, but also on the duration of exposure [Habash-06]. Hence, this study confirms our initial hypothesis that regardless of the patient's skin properties, the longer the duration of radiation exposure, the greater the amount of energy that will be absorbed by tissue, and thus, a better healing muscle in a short time is obtained. In other words, this study demonstrates the effectiveness of the designed RFD prototype for diathermy therapy in continuous mode.

## 2.5. Conclusions

The full-system behavioral modeling developed in this chapter has allowed us to define the design specifications for each of the blocks making up the RFD chip, i.e., each block's signal type, voltage levels, and operational frequencies. First, simulations were run to corroborate the appropriate functioning of each block separately. Then a simulation was run of all the blocks interconnected among themselves, corroborating the correct functioning of the entire system. All these tests provided a basis to begin designing each of the system blocks at the component level.

The design of a prototype using commercial components and assembled on a one-layer PCB board was presented. Characterization of the prototype was performed, i.e., its power consumption, and the waveform of its output signal in order to evaluate whether the equipment generates the adequate RFD signal and whether its operating autonomy with a battery would surpass 48 hours. Having the portable RFD prototype made possible to draw up a fairly specific

and defined work plan to obtain important information that will enable us to identify the minimum current needed for this circuit to achieve positive effects in the scarring of soft tissue in a universe of patients specified by specialist physicians.

Finally, in this chapter, we have presented a comparative study on continuous mode and conventional of RFD treatments applied to patients with muscular diseases. This study showed that the duration of exposure to RFD signals has a positive and measurable impact on healing affected muscles. This investigation in the RFD field allowed us to validate that the continuous application of an RFD signal in patients with a recent injury is an effective and fast-acting measure for reducing inflammation or healing muscle, ligament, and nerve injuries. The conducted study also confirmed the effectiveness of the proposed RFD prototype for RF diathermy therapy in continuous mode.

# 3. Design of the Oscillator Module of the RFD Chip

One option to miniaturize the RFD system is the integration of all modules in a single chip. Among CMOS technologies available at ITESO, the 0.5 μm CMOS technology shows good performance at 10 MHz for digital circuits. Since the maximum operation frequency of the RFD system is 1 MHz, the 0.5 μm CMOS technology is selected to design the RFD chip. This chapter describes the design process, at the transistor level, of the oscillator module composed by a low-frequency oscillator (LFO), a voltage-controlled oscillator (VCO), and a control logic circuit (CLC). The oscillators are designed with a ring oscillator topology. The control logic circuit is designed with an array of logic gates. The main specifications of the oscillator module are: symmetrical transitions, low power consumption, low leakage current, and small layout area. Simulations show that the oscillation module generates a signal of 5 Vpp in the range of 500 KHz to 1 MHz, with the option of repeating the sweep in 4 different frequency sub-ranges. The maximum power consumption of VCO is 22 mW. This Chapter is based on the work in [Corres-Matamoros-17a].

## 3.1. The Control Logic Circuit

The proposed control logic circuit (CLC) allows 4 different frequencies to be selected for operating the LFO circuit in a similar way as a decoder circuit. The CLC inputs are placed in a defined initial logical state, which generates a fixed voltage at the output, thus defining a specific frequency operation of the LFO circuit, namely 0, 1 Hz, 5 Hz, and 12 Hz. As part of the design

TABLE 3.1. LOGIC OF THE FREQUENCY CONTROL CIRCUIT

| *A* | *B* | *X*1 | *X*2 | *X*3 | *X*4 |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

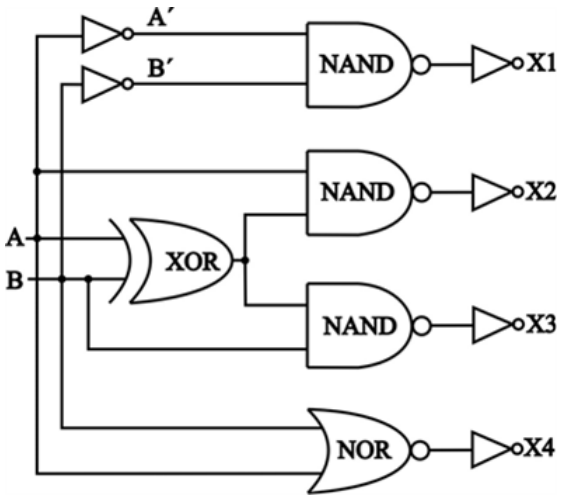



Fig. 3.1 Gate diagram of the logic control circuit of LFO circuit.

flow, first a truth table is defined with bits *A* and *B* as input, from which one of the 4 output bits *X*1, *X*2, *X*3 and *X*4 will be chosen (see

Table 3.1). According to this table, *X*1 = 1 only when *A* = 0 and *B* = 0. This is achieved with a two inputs AND gate; *X*2 = 1 only when *A* = 0 and *B* = 1, this is implemented with an XOR gate; output *X*3 is obtained using the output of XOR gate and input *B* as the inputs of second AND gate; *X*4 = 1 only when *A* = 1 y *B* = 1; this output is achieved with an OR gate. The gate-level array of CLC is shown in Fig. 3.1.

To implement this circuit in CMOS technology we define transistor sizes of each gate of CLC to provide the gate with current-driving capability in both directions similar to that one of the basic inverter.

One can find in the technical literature that digital circuits designed in 0.5 µm CMOS technology presents good performance at frequencies higher than 1 MHz, so we use parameters of OnSemi C5N process to design all circuits of RFD chip. Since the transconductance of the pMOS transistors is approximately 2 times smaller than the transconductance of nMOS transistors in the 0.5 µm CMOS technology [Baker-10], the transistors' aspect ratio $(W/L)_p/(W/L)_n$ was set at 2:1 in the pull-up and pull-down networks. This was done for ensuring symmetrical logical state transitions (i.e. same time for charging and discharging) of digital circuits.

Another design specification in digital circuits to be considered is the leakage current. Leakage current or subthreshold current is given by [Carusone-12]

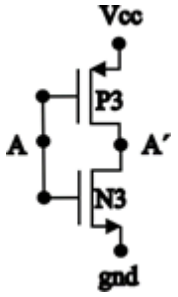



Fig. 3.2 Schematic of inverter circuit.

$$I_{D(sub\_th)} \cong I_{D0}\left(\frac{W}{L}\right)e^{(qV_{eff}/nkT)} \tag{3-1}$$

where

$$n = \frac{C_{ox} + C_{j0}}{C_{ox}} \approx 1.5 \tag{3-2}$$

and

$$I_{D0} = (n-1)\mu_n C_{ox}\left(\frac{k_B T}{q}\right)^2 \tag{3-3}$$

where $q$ is the electron's charge (1.602 x $10^{-19}$ C), $C_{ox}$ is the gate capacitance per unit of area, $C_{j0}$ is the depletion capacitance per unit of area, $k_B$ is the Boltzmann constant (1.38 x $10^{-23}$ $JK^{-1}$), and $T$ is the temperature in Kelvin degrees (≈ 300 °K at room temperature). In accordance with (3-3), the leakage current is directly proportional to transistor size. So keeping in mind the low leakage current, we use small-size transistors of each gate of CLC. Small size transistors also leads to small layout area which is another desirable feature of this design. Finally, we aim at keeping power consumption to a minimum without sacrificing functional effectiveness.

The static power consumption of a CMOS circuit is defined as [TI-97]

$$P_s = V_{DD} I_{D(sub\_th)} \tag{3-4}$$

and the dynamic power consumption is given by [Chandrakasan-15]

$$P_d = C_{pd}(V_{DD})^2 f_i \tag{3-5}$$

where

$$C_{pd} = \frac{I_{CC}}{V_{DD} f_i} - C_{L(eff)} \tag{3-6}$$

here $I_{CC}$ is the total current through transistor ($I_{CC} \approx I_D = \mu_n C_{ox}(W/L)(V_{GS}-V_{th})V_{DS}$), $f_i$ is the input

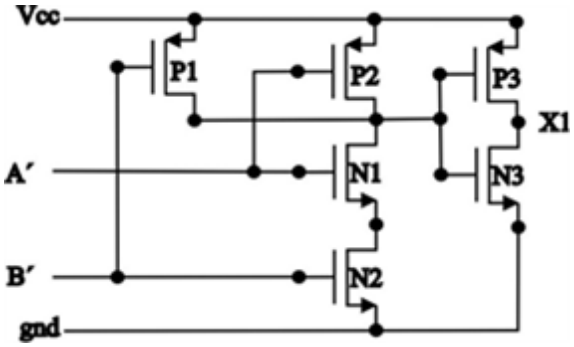



Fig. 3.3 Schematic of a two inputs AND circuit implemented to generate output *X*1.

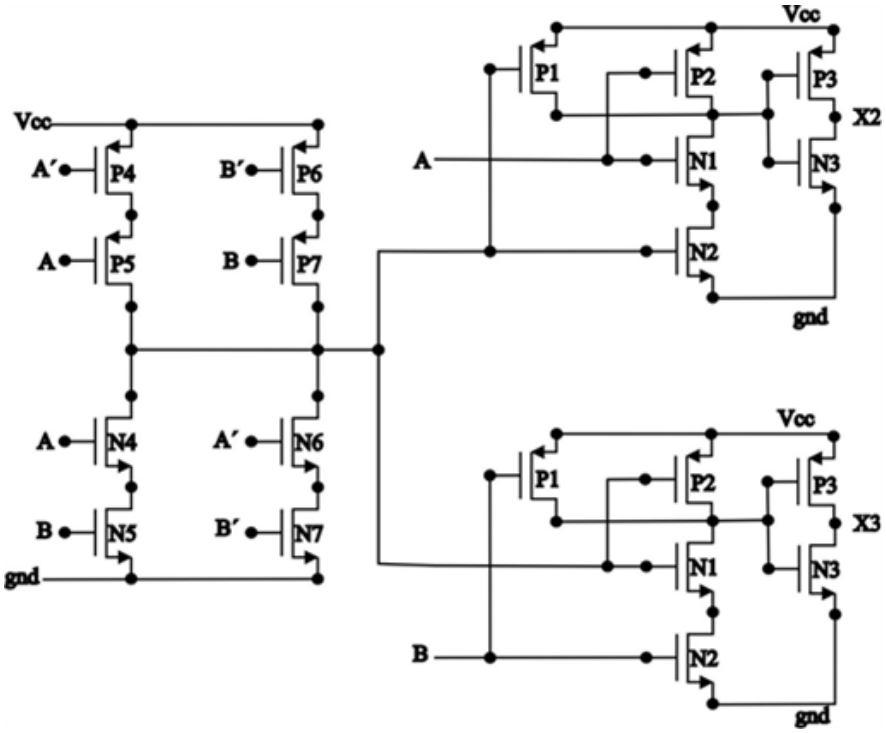



Fig. 3.4 Schematic of XOR and NANDs circuits implemented to generate outputs *X*2 and *X*3.

signal frequency, and $C_{L(eff)}$ is the effective load capacitance.

In order to get a good tradeoff between symmetrical transition levels, minimum leakage current, minimum power consumption, minimum layout area, but at the same time to minimize geometrical variations in the chip manufacturing process, almost all transistors of the CLC must have dimensions lightly superior to the minimal dimensions defined in the 0.5 μm CMOS technology, hence, for inverter cell (Fig. 3.2): $W_{p\text{-}inv} = 2.4$ μm and $W_{n\text{-}inv} = 1.2$ μm while $L = 2L_{min} = 1.2$ μm in all transistors of CLC.

As far as the AND gate (Fig. 3.3) to generate X1 output, dimensions of transistors' were

defined applying classical theory of sizing CMOS logic gates described in [Sedra-04], hence for the parallel pMOS transistor we have $W_{p\text{-}AND}$ = 1.2 μm, while for the two series connected nMOS transistor we have $W_{n\text{-}AND}$ = 1.2 μm.

Fig. 3.4 shows the schematic of XOR gate cascaded with two AND gates to generate the X2 output. According with the rule of transistor series connection, the pMOS dimensions should double those of the nMOS due to the transconductance differences, then dimensions for pMOS transistors of the XOR gate are: $W_{p4,\ 5,\ 6,\ 7\text{-}XOR}$ = 4.8 μm, and for nMOS transistors, the dimensions are $W_{n4,\ 5,\ 6,\ 7\text{-}XOR}$ = 2.4 μm. Dimensions of AND gate transistors of the *X*2 output is identical to that one used for output *X*1. The XOR gate to generate the output *X*3 is the same used to generate the output X2.

The same procedure described for sizing transistors of the previous gates was applied to the OR gate to generate output X4 (Fig. 3.5) [Baker-10]. Thus $W_{p7,\ 8\text{-}OR}$ = 4.8 μm, and $W_{n7,8\text{-}OR}$ = 1.2 μm.

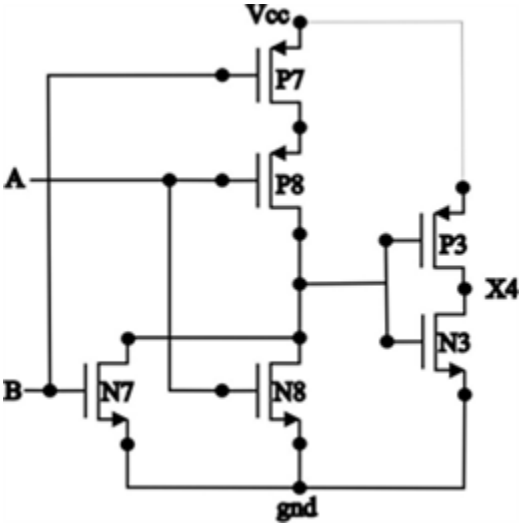



Fig. 3.5 Schematic of NOR circuit implemented to generate output *X*4.

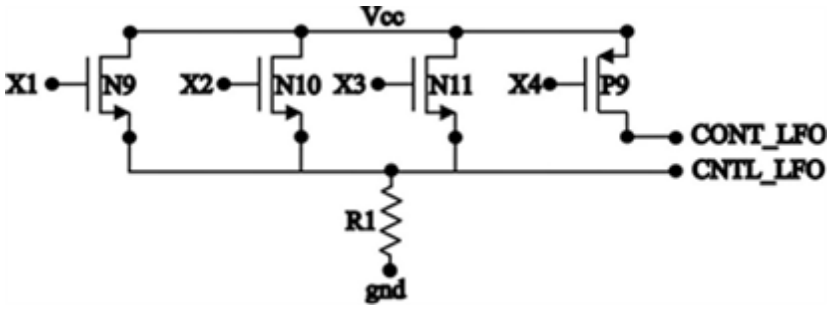



Fig. 3.6 Schematic of voltage divider circuit for the digital control circuit.

Finally, to convert the CLC outputs $X1$-$X4$ into a control voltage to modify the LFO circuit's operation frequency, a voltage divider circuit was designed with a 260 Ω passive resistance and an active resistance formed by three parallel connected transistors (transistors N9, N10 and N11), as illustrated in Fig. 3.6. The output of voltage divider circuit depends on which transistor is turned on. Each transistor is activated with the voltage level at the CNTL_LFO node. The size of transistors N9, N10 and N11 are fine-tuned to obtain precise magnitudes of voltage that allow for calibration of the LFO circuit frequencies at the desired values. The resulting sizes are: $W_{n9}$ = 12 µm; $W_{n10}$ = 11 µm and $W_{n11}$ = 8 µm, and for all transistors $L_n$ = 10 µm. As observed in Fig. 3.6, the 3 nMOS transistors have their gates connected to the outputs $X1$, $X2$, and $X3$ respectively. This connection is implemented in this way so that the CLC can choose which transistor turns-on by putting only the corresponding active resistance and the desired voltage value into the voltage divider. Transistor P9 acts as a switch that closes or opens the LFO's feedback loop to $V_{CC}$. This is the reason to connect the $X4$ output to the gate of P9. This switch is used to turns-on/turns-off the LFO. The transistor size is $W_{p9}$ = 10 µm and $L_p$ = 0.6 µm. Once the design was completed, the circuit's functionality was tested at the schematic level.

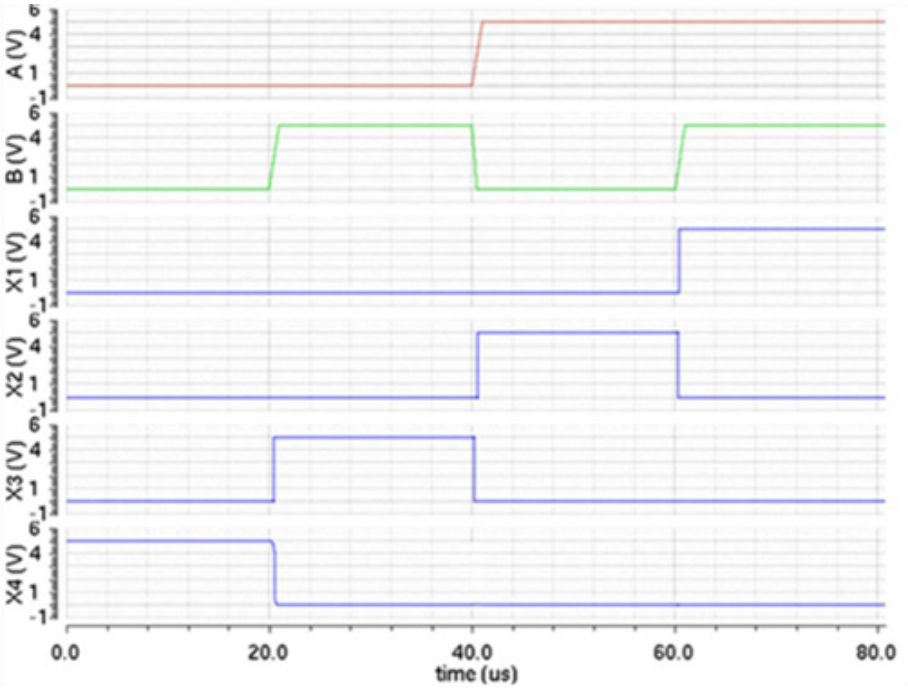



Fig. 3.7 $X1$, $X2$, $X3$ and $X4$ output signals of digital control circuit generated with inputs $A$ and $B$. Simulated in Virtuoso of Cadence.

### 3.1.1 Simulation Results for the CLC Circuit

In Fig. 3.7, the transient response of logic part of the CLC circuit is shown. Notice the layout of CLC was designed. The parasitics of layout were extracted and then a simulation was performed. Fig. 3.8 shows the pre- and post-layout of 4 voltage values that the CLC circuit generates, i.e. 0 V, 497 mV, 637 mV and 679 mV. These voltage values were specially chosen to calibrate the LFO circuit with output frequencies of 0 Hz (continuous mode), 1 Hz, 5 Hz, and 12 Hz. One can observe that the pre- and post-layout responses are quite similar, and the CONT output remains active only when the *X*4 is active to put the LFO into continuous mode. Finally, Fig. 3.9 presents the current consumption of the CLC circuit (pre-layout and post-layout), from which we can observe that the maximum current consumption is of 2.49 mA, with the first operation mode. From (3-4) we can deduce a maximum power consumption of 12.45 mW.

## 3.2. The Oscillator Circuit

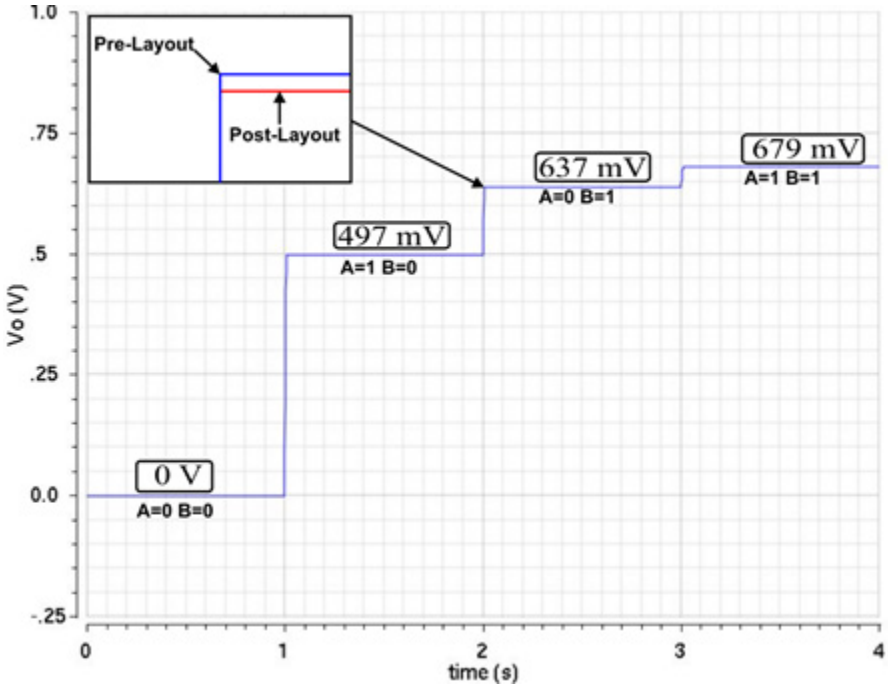



Fig. 3.8 CNTL_LFO output for the different values of *A* and *B*. Simulated in Virtuoso of Cadence.

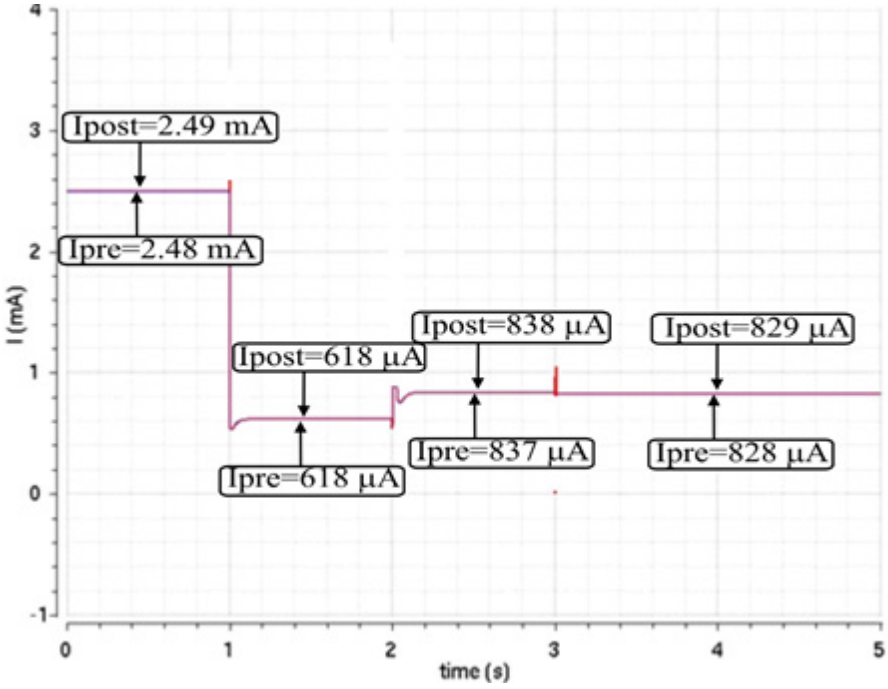



Fig. 3.9 Dynamic current of the CLC circuit, pre-layout (blue line) and post-layout (red line) simulation obtained in Virtuoso-Cadence.

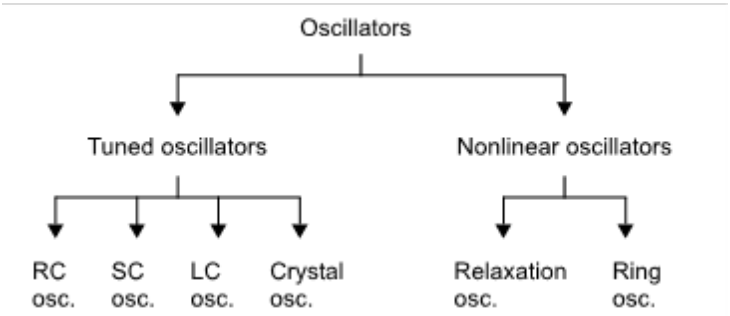



Fig. 3.10 Classification of oscillators [Carusone-12].

In the technical literature one can find sine wave and square wave oscillators. Sine-wave oscillators are designed with tunable-frequency circuits together with a feedback loop; these oscillators can be implemented with RC, LC, multiplexed capacitor, and crystal circuits. Non-linear circuits with a feedback loop are used to implement square-signal oscillators. Square-signal oscillators include ring and relaxation structures. Fig. 3.10 summarizes the oscillator's classification. Ring oscillators (RO) and LC oscillators (LCO) are the ones used most often in integrated circuits [Carusone-12].

In [Michal-12] we find a useful oscillator structure of 3-stage RO with frequencies close to the required ones for the intended design of RFD chip. In addition, this structure of RO presents

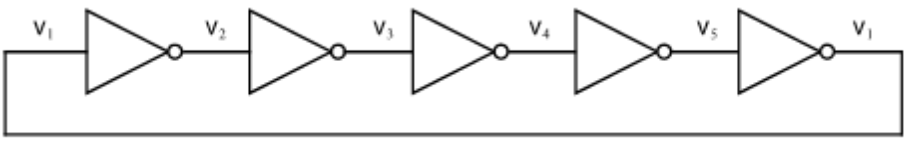



Fig. 3.11 Ideal implementation of a Ring Oscillator [Carusone-12].

reduced power consumption. In [Van-Der-Tang-02] a broader overview of the potential applications of this kind of RO oscillator is presented. [Hershenson-99] presents a method for the calculation and optimization of transistor sizes in a LC oscillator (LCO). The design of an LCO with quadrature output is described in [Rofougaran-96], which is used in the design of a more complete circuit, such as a PLL. The main advantage of this design is its large output voltage swing, at frequencies that are relatively close to the frequencies we are desired for this project.

### 3.2.1 Ring Oscillators

This type of oscillator (Fig. 3.11) consists of an odd number of serially connected inverters, with the output and input connected by a feedback loop. The task of each inverter is to change the logical state coming from the previous inverter, but with a certain delay, so that if we set an odd number of inverters and add up the delay times of each one, we obtain an oscillation with a frequency that is inversely proportional to the number of inverters we use. The oscillation frequency is given by [Carusone-12]

$$f_0 = \frac{1}{T_0} = \frac{1}{2NT_d} \tag{3-7}$$

where $T_0$ is the period of signal, $T_d$ is the delay time of each inverter and $N$ is the number of inverters used in the circuit. The delay time is given by

$$T_d = NT_f + NT_r \tag{3-8}$$

The delay time $T_d$ value depends upon transition times of inverter circuit, namely, transition time from the transistor's high logic level to its low logic level $T_f$, and transition time from the transistor's low level to its high level $T_r$. These transition times are given by [Michal-12]

$$T_f = \frac{2C_{ox}L^2(k+1)\left[V_{DD} - V_{T,n} + \left|V_{T,p}\right|\right]}{K_n\left(V_{DD} - \left|V_{T,n}\right|\right)^2} \tag{3-9}$$

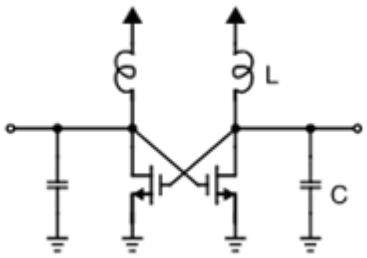



Fig. 3.12 CMOS implementation of the LC oscillator [Carusone-12].

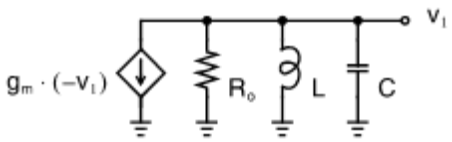



Fig. 3.13 Small signal model of the LC oscillator circuit [Carusone-12].

$$T_r = \frac{2C_{ox}L^2(k+1)\left[V_{DD} - V_{T,n} + \left|V_{T,p}\right|\right]}{kK_P\left(V_{DD} - \left|V_{T,p}\right|\right)^2} \tag{3-10}$$

where $K_{P,N}$ are the transconductance parameters, $k = W_p/W_n$ is the aspect ratio of transistors, $V_{Tp,n}$ are the threshold voltages, $C_{ox}$ is the thin oxide capacitance of transistors, and $V_{DD}$ is the supply rail.

Power consumption of the RO circuit can be calculated with (3-5) but in this case $C_{pd} = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + NC_{load}$. Each of these capacitances depends on transistor dimensions of inverter cell.

### 3.2.2 LC Oscillators

LCO circuits are used for applications where high frequencies and a high spectral purity are required. Fig. 3.12 shows the equivalent circuit of a complementary cross-coupled-type oscillator. The output frequency for these kind of oscillators is given by [Carusone-12]

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{3-11}$$

where $L$ and $C$ are the circuit's inductance and capacitance values, respectively.

Fig. 3.13 shows the electrical equivalent of the small-signal model from the middle of the

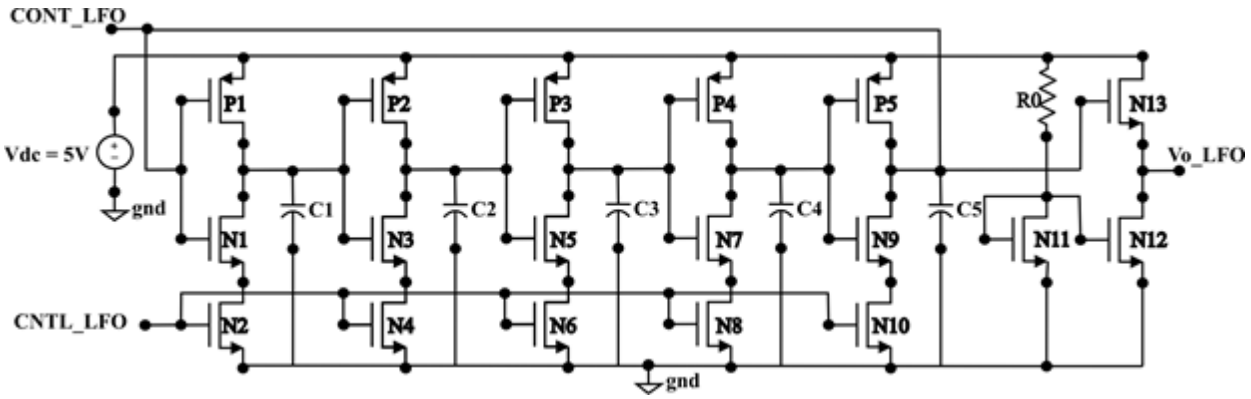



Fig. 3.14 Electrical equivalent of the LFO circuit implemented in Virtuoso-Cadence.

LCO circuit, from which we can determine that the following condition is essential for the circuit to oscillate

$$g_m > \frac{1}{R_0} \tag{3-12}$$

where $R_0$ represents the output resistance of each transistor together with any loss associated with the circuit's inductor or capacitor and $g_m$ is the transistor transconductance.

## 3.3. The Low-Frequency Oscillator (LFO) Block

As mentioned above, the LFO circuit controls the change of frequency sweep of VCO from 500 KHz to 1 MHz each second. As described below, design of LFOs with classic CMOS-circuit topologies involves large passive-element values [Vita-07] [Todani-12] [LTC10-b] [Cayuela-12] [Ravi-15] [Michal-12], which limit its implementation in integrated-circuit technology.

Keeping in mind that the oscillation frequency RO circuits is inversely proportional to the delay time, we look for RO structures with high $T_d$. A LFO topology that could be enabled to operate at frequencies in the Hz range without degrading the signal stability neither increasing power consumption or silicon area is presented in Fig. 3.14. This LFO topology is like a classical 5-stage ring oscillator with the delay inverters and capacitors described in Section 3.2.1, but this time, on each inverter an extra NMOS transistor is placed in cascade with a discharge NMOS. The design of this LFO topology for the current project was adapted from the one described in [Maymandi-Nejad-03]. In this structure one can adjust the impedance on the discharge of the delay capacitor with the help of CNTL signal.

In the LFO circuit (Fig. 3.14), transistor N2 connected to the source of transistor N1 is the element that controls the delay time ($T_d$) of the basic cell through its drain-current in the saturation region, and the overall capacitance at drain node of N1 in the inverter [Maymandi-Nejad-03].

The oscillation frequency of the LFO is given by (3-7) but in this case, $T_d$ is given by [Retdian-02]

$$T_d = \frac{V_{osc} C_L}{I_{cntl}} \tag{3-13}$$

where $V_{osc}$ is the oscillation amplitude, $I_{cntl}$ is the current controlled by transistor N2 working in saturation region, and $C_L$ is the overall parasitic capacitance at drain node ($C_L = C_{gsp1} + C_{dsp1} + C_{dbp1} + C_{dsn1} + C_{gdn1} + C_{dbn1} + C_{dgn2} + C_{dsn2} + C_{dbn2} + C_{gdp2} + C_{gsp2} + ...$). Combining (3-7) and (3-13) we obtain

$$f_{osc} = \frac{I_{cntl}}{2NV_{osc}C_L} \tag{3-14}$$

in which $I_{cntl}$ is given by

$$I_{cntl} = \frac{\beta}{2}\left(V_{gs} - V_T\right)^2\left(1 + \lambda V_{DS}\right) \tag{3-15}$$

where $\beta = k_n W/L$;

Although the LFO circuit (Fig. 3.14) handles very small currents, to ensure good functioning, a source-follower amplifier is placed at the LFO output (see transistors N11, N12, N13 and R0 of Fig. 3.14), in order to provide a gain in current and a good coupling with the VCO stage (Section 1.2).

For the RO's output buffer design we calculate the dimensions of the corresponding transistors as follows. We know that the voltage gain for this buffer is given by

$$A_v = \frac{V_O}{Vi} = \frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}} = g_{m1}\left(\frac{1}{g_{m1}} \| \frac{1}{g_{s1}} \| r_{ds1} \| r_{ds2}\right) \tag{3-16}$$

where $g_{m1} = \sqrt{2\beta I_D}$ and considering that the body-effect parameter $g_{s1}$, and conductance $g_{ds1}$ and $g_{ds2}$ are of the order of more than one tenth of $g_{m1}$, the gain with this type of configuration is close to one.

We also have $r_{ds}$ defined by

$$r_{ds1} = r_{ds2} = \frac{1}{\lambda I_D} \tag{3-17}$$

### 3.3.1 Implementation of a LFO with a Starved Current-Topology

According to (3-14), the oscillation frequency can be controlled by varying $I_{cntl}$, as long as the number of stages $N$ and $C_L$ are fixed. It is also evident from (3-4) and (3-14) a tradeoff between frequency oscillation and power consumption: low frequencies require large $C_L$ values, and low power consumption requires smaller $C_L$ values. Notice however, at very low frequencies power consumption (static and dynamic) is insignificant, so we can use large values of $C_L$. Nevertheless, parasitic capacitance at output node of an inverter is relatively small (<< 1 pF), then to get the required $T_d$ (8.3 ms – 100 ms) for a frequency range of 1 Hz to 12 Hz, we connect an external capacitor $C_{delay}$ = 6 pF, that becomes in the new dominant capacitance $C_L$ at each output node of inverters. The size ratio of transistors of delay cell in LFO circuit were calculated to get a discharge ramp much slower than the charge ramp, so that the sweep of frequencies was much more gradual. Using (3-8), (3-9) and (3-10) and the process parameters of 0.5 µm CMOS technology ($k_n$ = 120

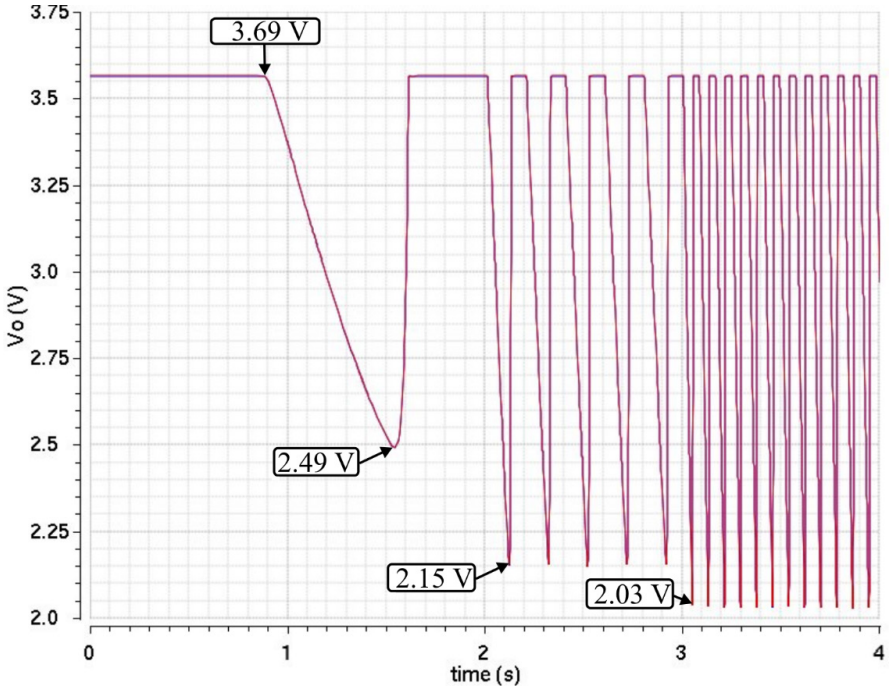



Fig. 3.15 Output signal ($Vo$) of the LFO circuit for a $V_C$ = 0 V, 497 mV, 637 mV and 679 mV. Obtained in Virtuoso-Cadence.

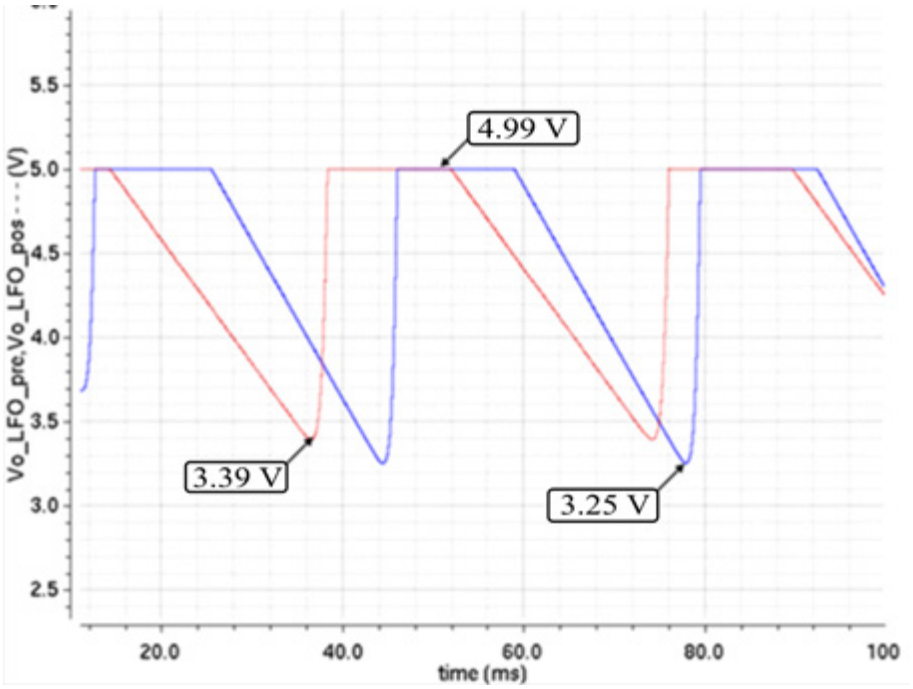



Fig. 3.16 Output signal of LFO circuit: pre-layout (blue line) and post-layout (red-line) responses.

µA/V, $k_p$ = 37 µA/V, $V_{Thn}$ = 0.72 V, $V_{Thp}$ = -0.9 V and $\lambda$ = 0.2 /V), and voltages $V_{gs}$ = 1.02 V and $V_{DS}$ = 0.48 V, the resulting values are $(W/L)_n$ = 1.5 µm/10.0 µm, and $(W/L)_p$ = 10.0 µm/0.6 µm. For the voltage buffer at the output of the LFO, *R0* = 1 KΩ, $(W/L)_{n11,n12}$ = 1.5 µm /0.6 µm and $(W/L)_{n13}$ = 100 µm/0.6 µm Fig. 3.15 shows the output signal for this circuit: with an operation frequency of $f$ = 0 Hz for a $V_C$ = 0 V, a $f$ = 1 Hz for a $V_C$ = 497 mV, a $f$ = 5 Hz for a $V_C$ = 637 mV, and $f$ = 12 Hz for a $V_C$ = 679 mV. These frequencies are the required ones for enable sweeps of VCO circuit.

### 3.3.2 Simulation Results of the LFO Circuit

Once the circuit response was validated at schematic level, we designed the layout of LFO circuit, layout parasitics extraction was performed with Calibre-PEX from Mentor Graphics and then the post-layout analysis was performed; simultaneous pre- and post-layout simulation were performed. Fig. 3.16 shows the comparison between the LFO circuit's output voltage for pre- and post-layout simulation. In this figure, we can see some differences between pre and post-layout responses: both signals have a voltage of 4.99 V in the upper level, however, in the lower level the

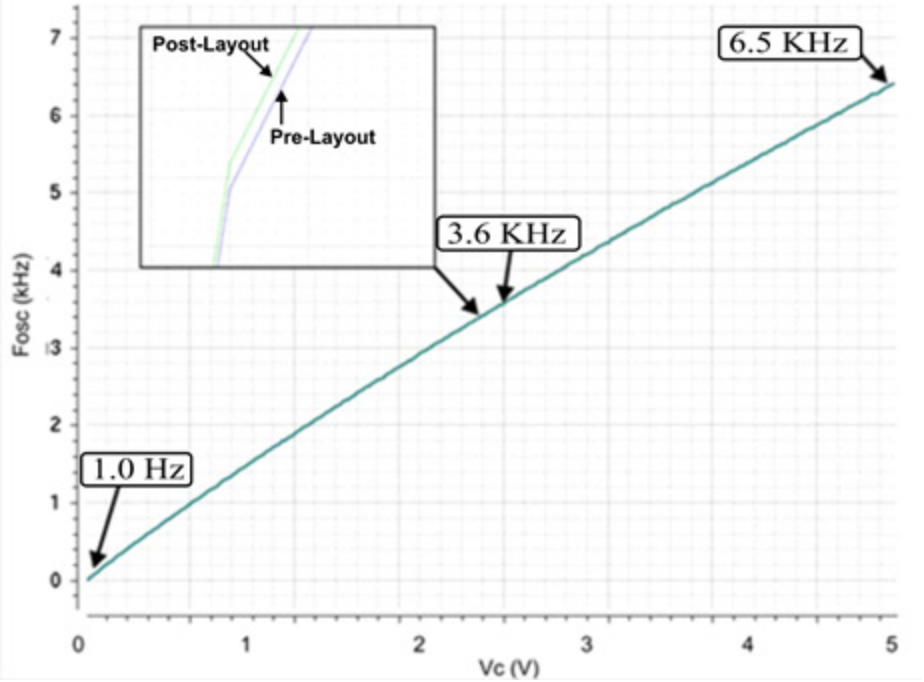



Fig. 3.17 Tuning range of the LFO circuit, pre-layout (blue line) and post-layout (red-line) simulation obtained in Virtuoso-Cadence.

pre-layout response presents a voltage of 3.25 V while the post-layout response presents a voltage of 3.39 V. This difference in the discharge levels of both responses is due to the resistance added for the routing of the layout in the post-layout simulation. With respect to oscillation frequency, pre-layout response is 29 Hz and post-layout response is 26 Hz. This frequency difference can be attributed to the parasitic capacitances of LFO layout. However, the effect of this frequency difference on the circuit's performance is not very significant, on one hand, because we are dealing with low-frequency circuits (1 Hz < $f$ < 12 Hz), and on the other hand, because we can adjust the operation frequency of the circuit with an extra control voltage input. Fig. 3.17 shows the tuning range of the LFO circuit in both pre-layout and the post-layout responses. We found that for a $V_C$ = 0 V, an output signal with an operation frequency $f$ = 1 Hz is obtained, and for a $V_C$ = 5 V, an output signal with an operation frequency $f$ = 6.5 KHz is obtained. These are the oscillation frequencies required for the LFO circuit. Fig. 3.18 presents the dynamic current consumption of the LFO circuit (pre-layout and post-layout), from which we can observe that the maximum current consumption is of 949 µA for all frequencies, but for 1 Hz the minimum consumption is 938 µA, for 5 Hz is 928 µA, and for 12 Hz is 922 µA. From (3.5) and (3.6) we can deduce an average dynamic power consumption for 1 Hz of 4.71 mW, for 5 Hz was 4.69 mW, and for 12 Hz was 4.67

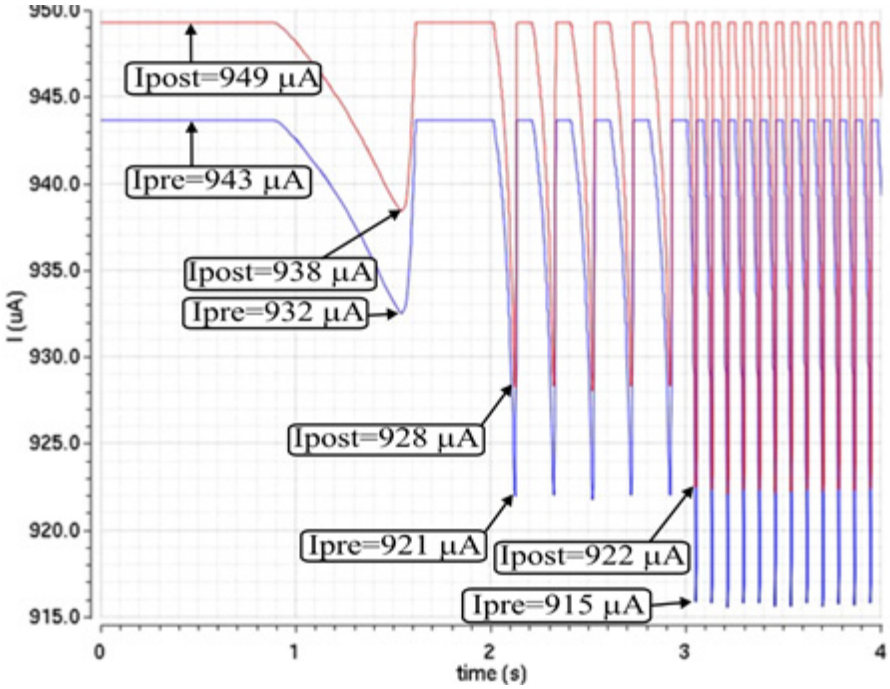



Fig. 3.18 Dynamic current of the LFO circuit, pre-layout (blue line) and post-layout (red line) simulation obtained in Virtuoso-Cadence.

mW. The static power consumption in a continuous mode ($f$ = 0 Hz) was 4.74 mW.

## 3.4. The Voltage-Controlled Oscillator (VCO) Block

For this block, the main design specifications is a stable frequency tuned in the range of 500 KHz to 1 MHz and a maximum power consumption of 25 mW (Section 1.3). Other desirable design specifications are: small layout area and low phase noise (less than 150 dBc/Hz). According to the technical literature, VCO architectures based on LC tank show good performance for high frequency applications, however, the ring VCO topologies are preferred because they are more reliable and suitable for the wide tuning range, smaller layout area, lower dissipated power, and less design complexity than LC tank counterpart [Savoj-01], [Xuemei-13], [Saini-13], but they are more prone to noise [Saini-13]. However, the low phase noise performance of ring oscillators can be improved by using differential VCO structures [Saini-13], as will be shown below.

### 3.4.1 Design of a Differential VCO

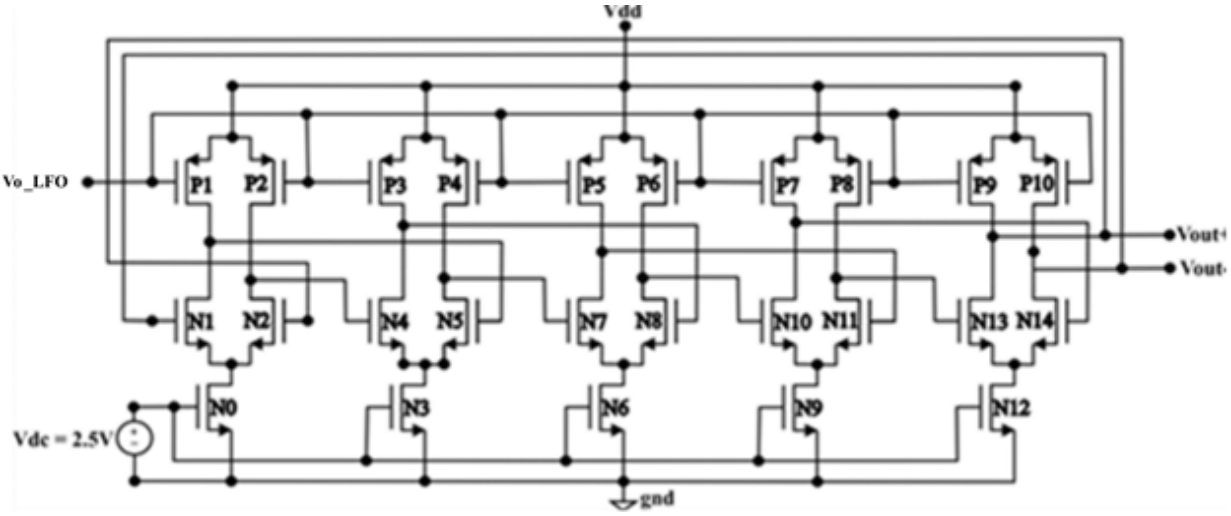



Fig. 3.19 Electrical equivalent of the DVCO circuit implemented in Virtuoso-Cadence.

As far as the differential VCO (DVCO) concerns, the design is adapted from topology presented in [Saini-13].

In the basic delay cell of DVCO (Fig. 3.19), P1 and P2 are pMOS transistors that operates from deep triode region to saturation region when its gate to source voltage ($V_O$_LFO) is varied to get the desired output frequency of oscillation. N1 and N2 are nMOS transistors whose input voltage produces operation in triode region and saturation region, N0 is the nMOS transistor used to provide a constant current source, so it operates in a saturation region. P1 and P2 are sized to act as a variable resistor controlled by $V_O$_LFO input. As the $V_O$_LFO become more positive the resistance of P1 and P2 transistor increases, thus raising the time constant at the output and lowering the operating frequency at the output.

The frequency oscillation is also given by (3-17) described in Section 3.3, and the delay time is defined in terms of the equivalent RC circuit of the delay cell as follows [Saini-13]

$$T_d = \frac{C_L}{K_p (W/L)_{1,2} (V_{DD} - V_{o\_LFO} - |V_{Thp}|)} \tag{3-18}$$

where $K_p$ is a transconductance parameter, $V_{Thp}$ is threshold voltage, $(W/L)_{1,2}$ is the aspect ratio of pMOS transistors, and $V_{DD}$ is power supply. From (3-18) it is evident that for getting high values of $T_d$, $(W/L)_{p1,p2,n1,n2} < 1$. Here we have used $(W/L)_{p1,p2} = 1.5\ \mu m/10.0\ \mu m$, $(W/L)_{n1,n2} = 1.5\ \mu m/10.0\ \mu m$, and $(W/L)_{n0} = 1.5\ \mu m/10.0\ \mu m$ to achieve $T_d = 0.2\ \mu s - 0.1\ \mu s$ (for each stage) corresponding to 500 KHz – 1 MHz frequency range of DVCO circuit.

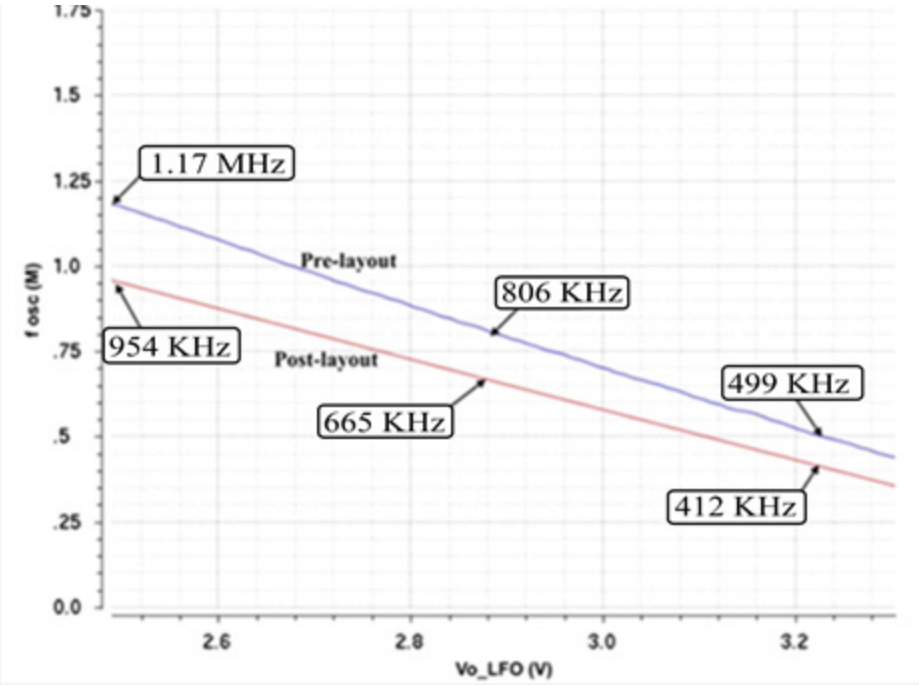



Fig. 3.20 Tuning range of the DVCO circuit: pre-layout (blue line) and post-layout (red line) responses. Obtained in Virtuoso-Cadence.

### 3.4.2 Simulation Results for the VCO Circuit

Similar to the LFO circuit, once the circuit response was validated at schematic level, we designed the layout; the layout parasitics were extracted using Calibre tool, and then the simulations were performed. Fig. 3.20 shows the tuning range of the DVCO circuit (pre-layout and post-layout) from 412 KHz to 954 KHz. This frequency tuning is achieved with a Vo_LFO voltage varying from 2.25 V to 3.69 V. These results indicate that the DVCO satisfies the operation frequencies for RFD chip.

Fig. 3.21 presents an example of the output signal of the DVCO circuit (in both pre-layout and post-layout responses) in the time domain, with a frequency sweep from 500 KHz to 1 MHz.

Fig. 3.22 presents the dynamic current consumption of the DVCO circuit (pre-layout and post-layout), which is the same for both 500 KHz and 1 MHz, from which we can calculate an

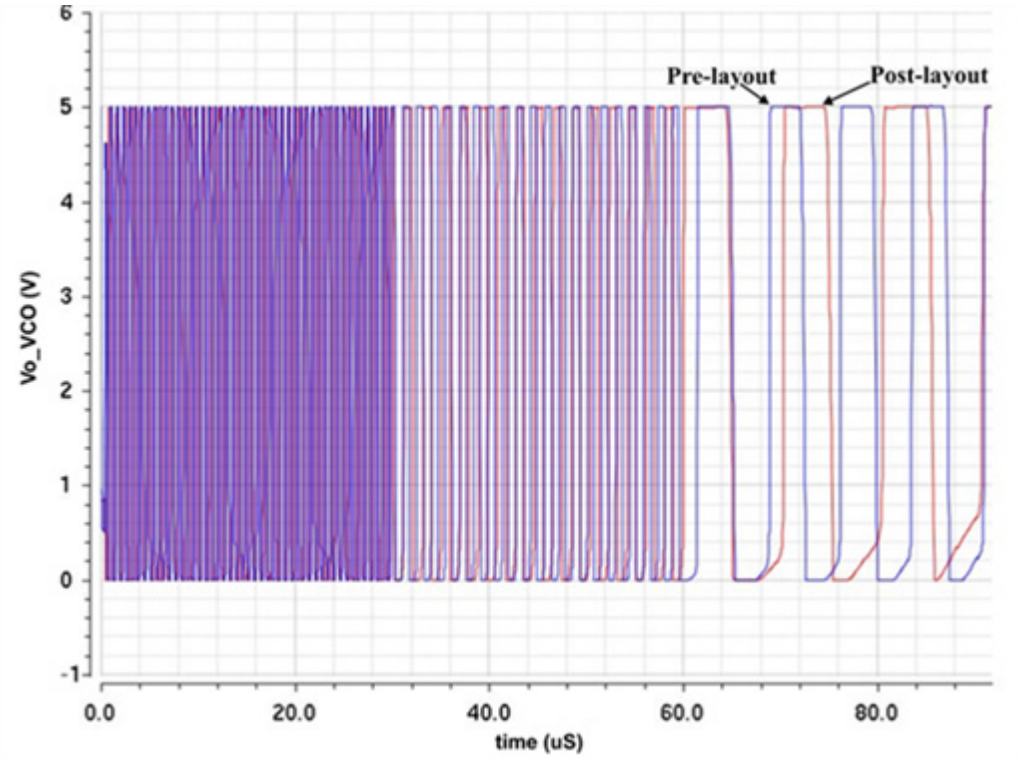



Fig. 3.21 Output signal of DVCO circuit: pre-layout (blue line) and post-layout (red line)

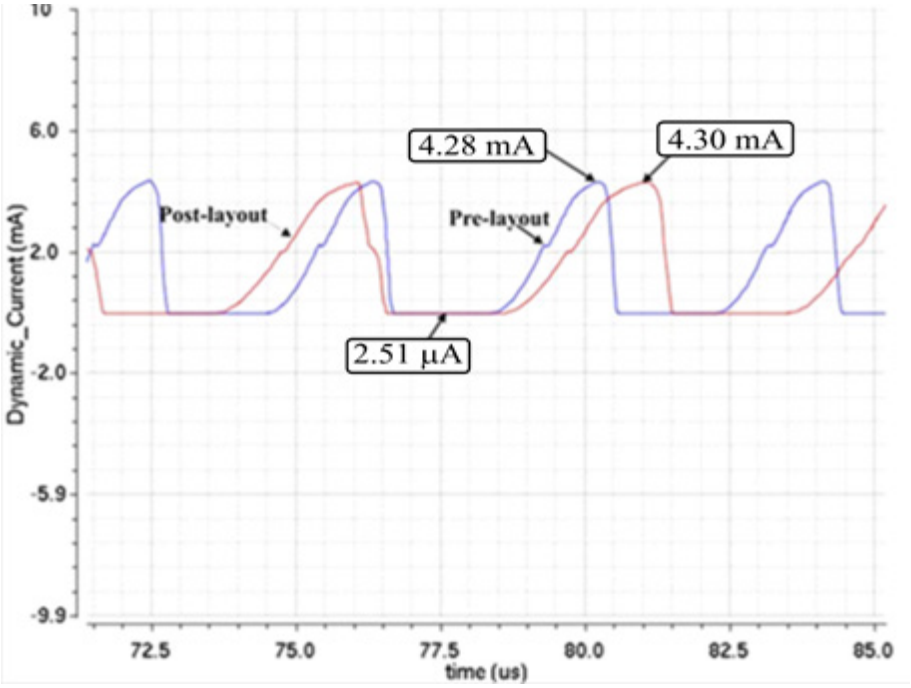



Fig. 3.22 Dynamic current of the DVCO circuit, pre-layout (blue line) and post-layout (red line) simulation obtained in Virtuoso-Cadence.

average current of 1 mA. Once again, using $P = V_{DD}I_{ave}$, we calculate an average power

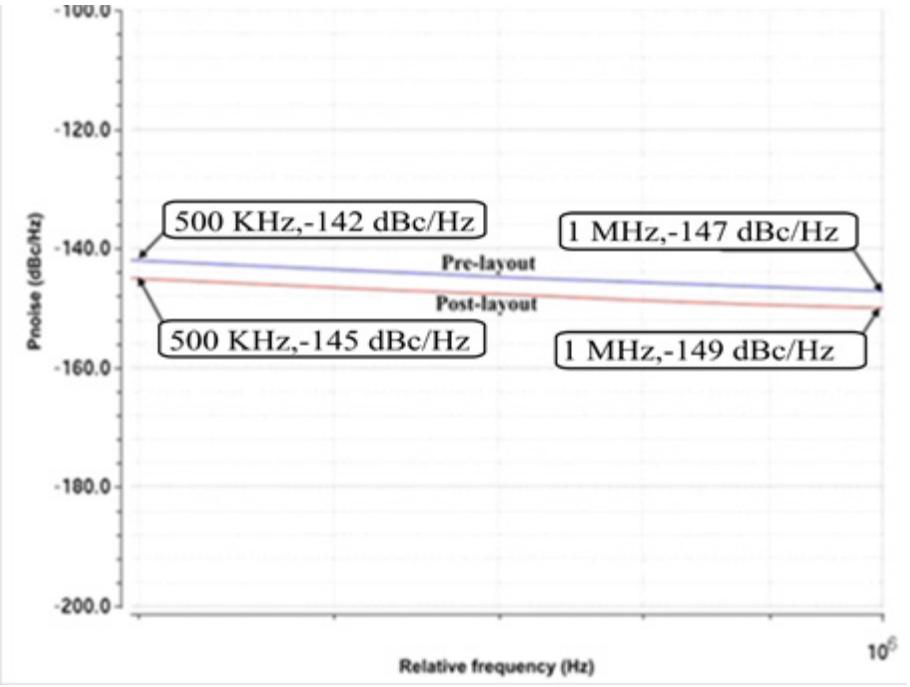



Fig. 3.23 Phase noise of the DVCO circuit, pre-layout (blue line) and post-layout (red line) simulation obtained in Virtuoso-Cadence.

consumption of 5 mW. This level of power consumption meets the requirements generating signal block of RFD chip.

In Fig. 3.23 we can see a phase noise decreasing linearly from of −145 dBc/Hz at 500 KHz to −149 dBc/Hz at 1 MHz of useful frequency range (post-layout response). This phase noise curve indicates that the designed DVCO circuit generates a stable signal in frequency domain that satisfy the requirements for medical therapy equipment [Guo-11].

## 3.5. Conclusions

The design process at the transistor level of the oscillation module for RFD chip was presented. This module is composed by a control logic circuit (CLC), a low-frequency oscillator (LFO), and a voltage-controlled oscillator (VCO). The 2-bits CLC circuit was designed with an array of logic gates, to generate 4 different dc voltages, which allows 4 different frequencies to be selected for operating the LFO module. The main specifications of this module were: 2 inputs, and 1 output with 4 different dc voltages (0 V, 497 mV, 637mV and 679 mV). The resulting power consumption of the CLC circuit was 12.45 mW.

Next, it was described the design of a low-frequency oscillator (LFO), with a topology of 5 stages current starved delay cells, this circuit had an extra buffer stage to get a current gain and voltage levels at the output of 0 to 5V. This module had 4 different oscillation frequencies: 0 Hz (continuous mode), 1 Hz, 5 Hz and 12 Hz. Simulations showed a maximum power consumption of 4.74 mW for this module.

Finally, the design of a voltage-controlled oscillator (VCO) with 5 stages of differential ring oscillator topology was presented. The circuit presented a maximum power consumption of 5 mW, a maximum phase noise of −149 dBc/Hz, and a frequency tuning range of 500 KHz to 1 MHz.

# 4. Design of the Voltage Amplification Module

One important part of the radiofrequency diathermy (RFD) chip is the amplifier module, since it is the block that provides the power needed to achieve enough electrical stimulation to increase the temperature of a localized part of the human body. This chapter describes the design of the voltage amplifier circuit in 0.5 μm CMOS technology; design specifications are those defined in Chapter 1, namely: a gain of 30 V/V (to achieve an output voltage of about 150 Vpp), and a current load of around 26 mA. The amplifier is implemented in a common-source topology with active-inductance load. The active inductance is a gyrator structure implemented with 4 OTAs and a grounded capacitor. Simulation results at schematic level show that the gyrator circuit achieves an inductance value around 2.4 mH in the frequency range of 500 KHz – 1 MHz. Simulation results also show that the voltage amplifier develops short voltage pulses of about 170 Vpp (at schematic level). However, the post-layout simulations show a 38 Vpp as maximum output voltage of the voltage amplifier; the reason of this limitations are discussed inside this chapter. The limitations found in 0.5 μm CMOS technology, pushed us to make the decision to leave the voltage amplifier module off the chip, then this block will be implemented with discrete components.

## 4.1. Design Requirements of the Voltage Amplifier Module

This section outlines the design of the voltage amplifier with active inductance load in 0.5 μm CMOS technology, according to configuration and specifications defined in Chapter 1, namely: high input impedance, a gain of 30 V/V, and a maximum drain current of around 26 mA. As discussed in Chapter 2, on one hand, an inductance value of around 1 mH in the range of 500 KHz to 1 MHz is required to develop 150 Vpp at the output node of the voltage amplifier and, on other hand, we need the simplest circuit possible in order to minimize the layout area in the chip. The proposed amplifier attempts to fulfill both the above requirements.

### 4.1.1 On-chip Passive Inductors

Passive on-chip inductors, such as bond wire inductors and spiral inductors, are available in standard silicon CMOS process. The most widely used type of passive on-chip inductors are the planar spiral inductor, and the square shaped spiral inductor. Usually, the planar spiral is implemented on the top metal layer of determined CMOS technology to reduce the spiral-to-substrate oxide capacitance and other parasitics. In those geometries, both frequency operation and structural parameters such as the outer dimension, number of turns, the distance between the centers of lines (or pitch), and substrate property are all important factors that determines the value and performance of on-chip inductors. The most popular geometry is the square spirals because of the ease of their layout. The inductance value of a square planar inductor (see Fig. 4.1) can be calculated using an empirical formula given by [Crols-96]

$$L = 1.3x10^{-4}\left(\frac{d^3{}_{out}}{w^2}\right)\eta_a^{\frac{5}{3}}\eta_w^{\frac{1}{4}} \tag{4-1}$$

where $d_{out}$ is the outer diameter of metal wire, $w$ is the metal width, $\eta_a$ is the ratio of wire area to total area, and $\eta_w$ is the ratio of wire width to turns pitch, i.e., $\eta_w = (w + s)$. Typical values of monolithic inductors in CMOS technology are in the range of hundreds of nH and use considerable layout area. As indicated in Chapter 2, the required value of $L$ for the voltage amplifier is at least 1 mH, such that the passive integrated inductor is discarded as load of the intended design of voltage amplifier.

### 4.1.2 On-chip Active Inductors

On-chip active inductors are active networks with the inductive impedance emulated. Active inductors can be constructed by loading an OTA-based array (which is called gyrator) with

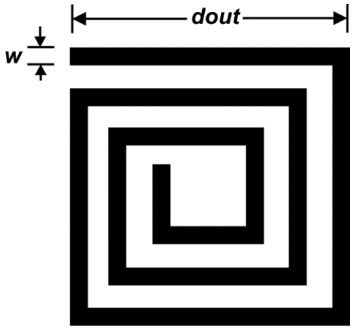



Fig. 4.1 Implementation of square planar inductor.

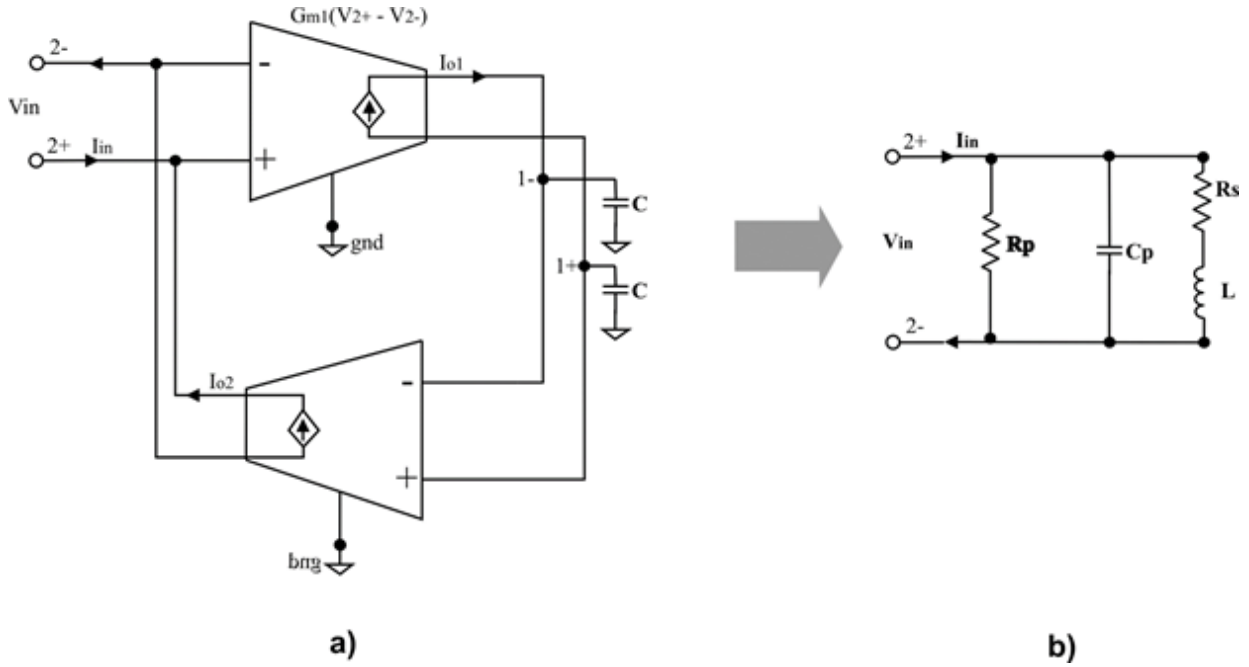



Fig. 4.2 a) Ideal implementation of the gyrator-C active inductance topology. b) RLC equivalent circuit of the gyrator-C active inductance topology. Figure taken from [Yuan-08].

a capacitance [Yuan-08], as shown in Fig. 4.2, or by using other structures such as regulated cascade array [Sabaghi-12], [Wu-06], digitally programmable active inductor [Alzaher-06] and others (see Table 4.1).

In order to prove the feasibility of using of active inductances in this project, the first step was the study of their principle of operation and figures of merit of main topologies with which inductance values can be reached in the range of 500 KHz to tens of MHz. Table 4.1 shows the summary of published works on active inductors. From Table 4.1, it seems that with simple transistor structures of active inductors it is not possible to get inductance values more than hundreds of nano-henry. It is also noted that with gyrator structures one could achieve higher inductance values, then, a gyrator structure is selected to implement the active inductor to be used in the voltage amplifier.

A basic gyrator-C network circuit consists of two transductors connected back-to-back and a capacitor connected to the input ports of one transconductor (Fig. 4.2a) [Yuan-08]. This type of gyrator has no losses when the impedances of the transductors are infinite and the transconductances are constant. The inductance for this type of circuit is given by [Yuan-08]

TABLE 4.1. COMPARISON BETWEEN ACTIVE INDUCTANCES REPORTED IN THE LITERATURE

| Reference | Inductance (H) | Frequency (Hz) | Topology | Power consump. (mW) | CMOS technology (μm) |
|---|---|---|---|---|---|
| [Kumar-89] | 22 | 100 K - 100 M | OPAMP | ---- | 0.5 |
| [Joshua-06] | 22 n | 1 M - 100 G | Gyrator-C | ---- | 0.18 |
| [Xiaolang-11] | 6.27 m | 500 K - 50 M | Gyrator-C | ---- | 0.13 |
| [Ming-Jeui-06] | ---- | 1.3 G | Gyrator-C | 18 | 0.25 |
| [Mishra-13] | 6.7 n | 6 G | Yodprasit | 6 | 0.18 |
| [Takahashi-09] | ---- | 10 M | Hara | ---- | 1.2 |
| [Yuan-08] | 144 n | 2 G - 7 G | Gyrator-C | 1 | 0.13 |
| [Ugur-07] | 0.68 n | 5.7 G | Gyrator-C | 19 | 0.18 |
| [Chun-Hsueg-09] | 4.3 n | 6 G | Carreto | ---- | 0.35 |
| [Yanxiao-14] | 30 n | 2.5 G | Carreto | 5 | ---- |
| [Ghorbel-14] | 3.8 n | 2.5 G | OPAMP | ---- | ---- |
| [Stornelli-13] | ---- | 4.5 G | Gyrator-C | 4 | 0.18 |
| Ma-13 | 8 n | 1 G - 10 G | Carreto | 10 | ---- |
| Hara-02 | 4 n | 10 G | Gyrator-C | ---- | 0.18 |
| Banchuin-10 | 13 m | 1 k - 100 k | Gyrator-C | ---- | 0.35 |
| Zheng-10 | ---- | 1 M | Gyrator-C | 20 | 0.18 |
| Muhammed-12 | 110 n | 0.1 M - 1 G | Gyrator-C | 21 | 1.2 |
| Katageri-14 | 1.08 m | 49.8 k- 305 k | Gyrator-C | ---- | ---- |

$$L = \frac{2C}{g_{m1}g_{m2}} \tag{4-2}$$

When we speak of a floating gyrator-C active inductance, its equivalent RLC is similar to that one shown in Fig. 4.2b. Each of its components is defined by

$$L = \frac{C_1/2}{g_{m1}g_{m2}} \tag{4-3}$$

$$R_s = \frac{G_{o1}/2}{G_{m1}G_{m2}} \tag{4-4}$$

$$R_p = \frac{2}{G_{o2}} \tag{4-5}$$

$$C_p = \frac{C_2}{2} \tag{4-6}$$

where $C_1$, $G_{o1}$, $C_2$ and $G_{o2}$ are the capacitances and conductances of nodes 1 and 2 in Fig. 4.2b.

When the transconductor's input and output conductances are considered, the gyrator-C network performs like a lossy inductor that is modeled through its parasite resistor $R_p$, its capacitance $C_p$, and its resistance $R_s$. Thus, to reduce the ohmic losses, $R_p$ must be maximized while $R_s$ must be minimized. The finite impedance input and the output impedances of the gyrator-C network's transconductors have no effect on the active inductor's inductance.

$R_p$ and $C_p$ are determined only by $G_{o2}$ and $C_2$, while $G_{o1}$ and $C_1$ affect only $R_s$ and $L$. According to (4-3), basic gyrator-C structure implies the use of large capacitor to achieve high $L$ values. With structures of floating inductance based on 3, 4, and 5 OTAs it is possible to achieve larger inductance values [Katageri-14]. [Banchuin-06] has reported that the 4-OTA-based floating inductors present a better bandwidth and noise performance than its 3-OTA counterpart. Based on this information, we decided the use a 4-OTA with single grounded capacitor (Fig. 4.3) as inductive load of the voltage amplifier. The equivalent inductance for this kind of topology is given by [Katageri-14]

$$L = \frac{C_1}{g_m^2} = \frac{4V_T^2 C_1}{I_B^2} \tag{4-7}$$

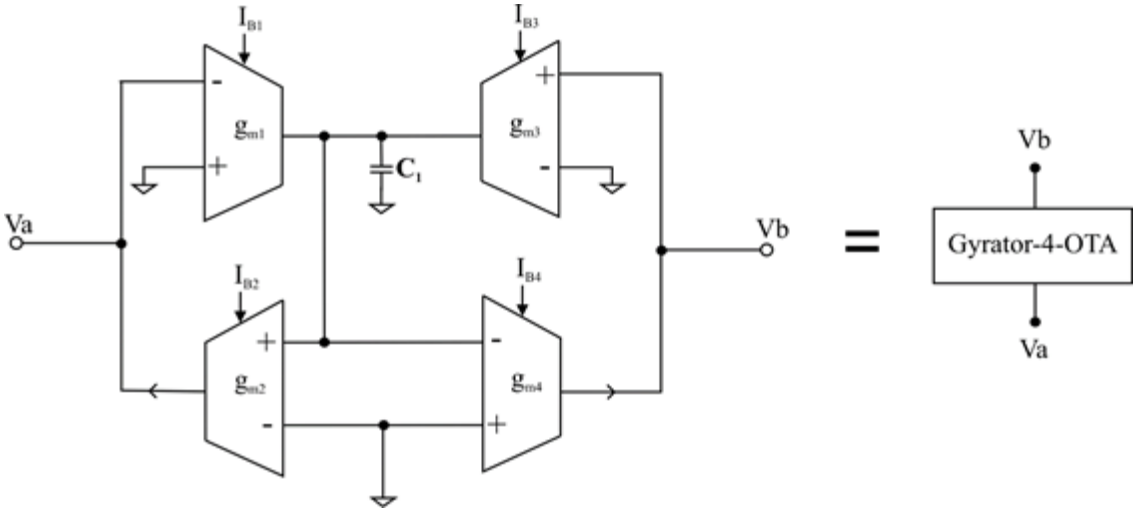



Fig. 4.3 Ideal implementation of the 4-OTA with grounded capacitor gyrator-C active inductance topology. Figure taken from [Katageri-14].

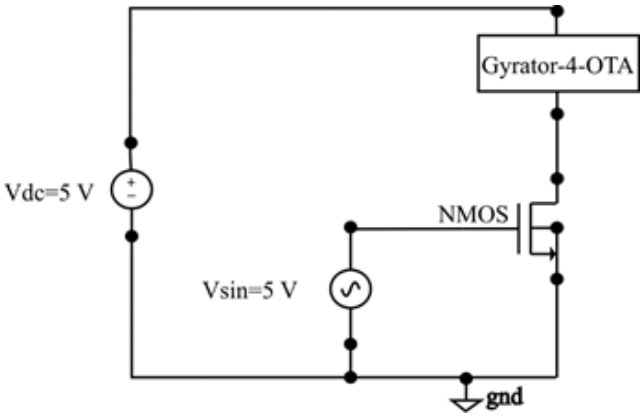



Fig. 4.4 Common-source amplifier with active load implementation for macromodeling in Virtuoso-Cadence.

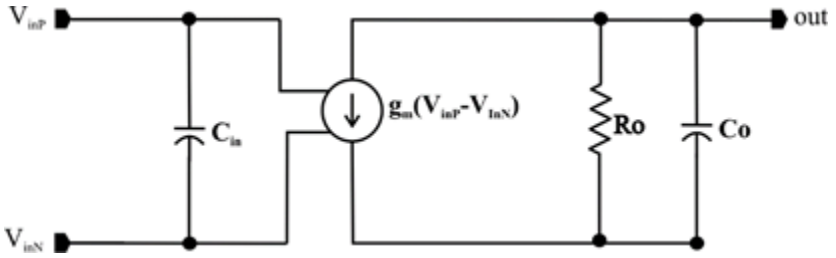



Fig. 4.5 Macromodel of single-ended OTA.

where $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_m$.

## 4.2. Voltage Amplifier Response with a 4-OTA Based Gyrator using the Macromodel of OTA

According to (4-7), in the 4-OTA based gyrator we have three dependent variables, namely: $L$, $g_m$, and $C_1$. To extract the adequate values of $g_m$ and $C_1$ to achieve a $V_o$ = 150 Vpp in the voltage amplifier with the gyrator structure of 4-OTAs as load, we have performed a parametric sweep using Virtuoso Tool and the testbench shown in Fig. 4.4. The dimension of the NMOS input transistor in the testbench is $W$ = 600 µm and $L$ = 4.95 µm (according with the $g_m$ and $I_D$ calculated in Section 2.2.2) and the input signal is a square voltage signal of 5 V of amplitude at 500 KHz. In that analysis we used the macromodel of the OTA shown in Fig. 4.5, in which we have used typical values of OTAs with basic structures designed in 0.5 µm CMOS technology, that is $C_{in}$ = 100 fF,

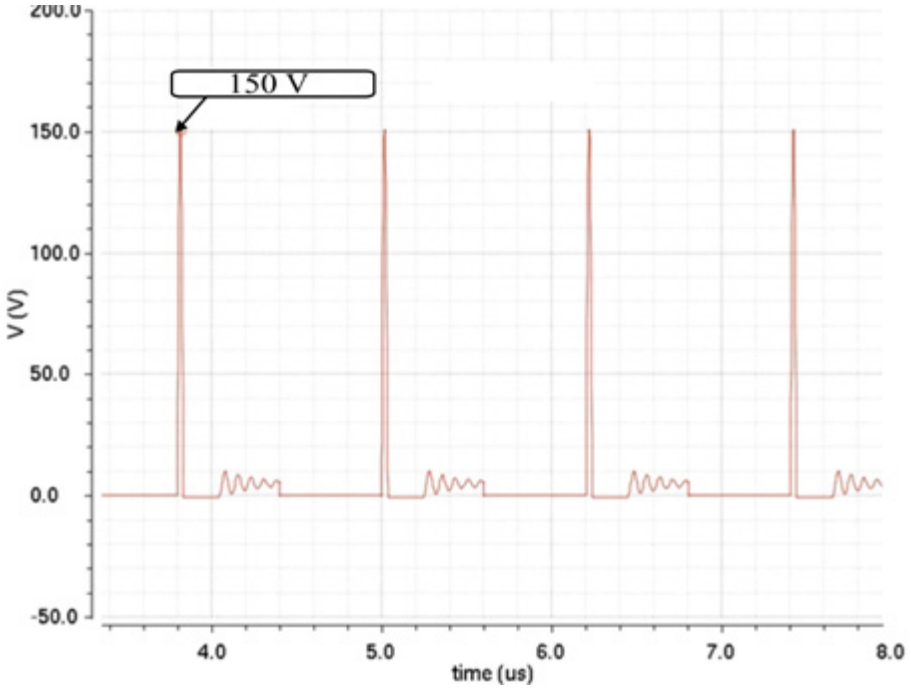



Fig. 4.6 Output voltage of the common-source amplifier implemented for macro modeling in Virtuoso-Cadence.

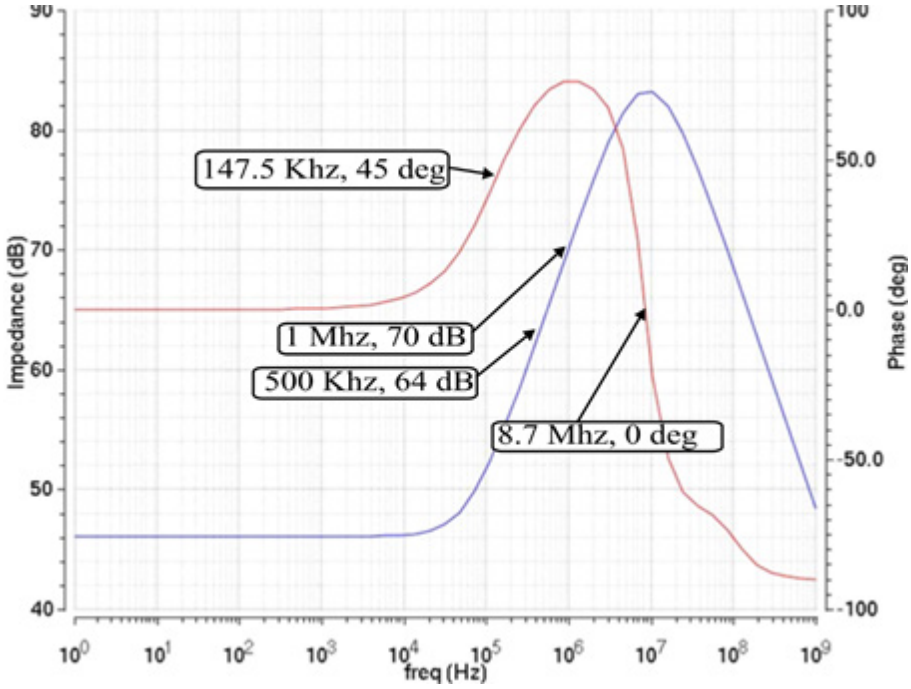



Fig. 4.7 Impedance magnitude (blue line) and phase (red line) of the 4-OTA Gyrator active inductance.

a $R_o$ =100 KΩ, and a $C_o$ = 16.5 pF; $g_m$ and $C_1$ were left as variables that are adjusted for the required value of $L$. To obtain 150 Vpp (Fig. 4.6) at the output node of voltage amplifier, we need OTAs

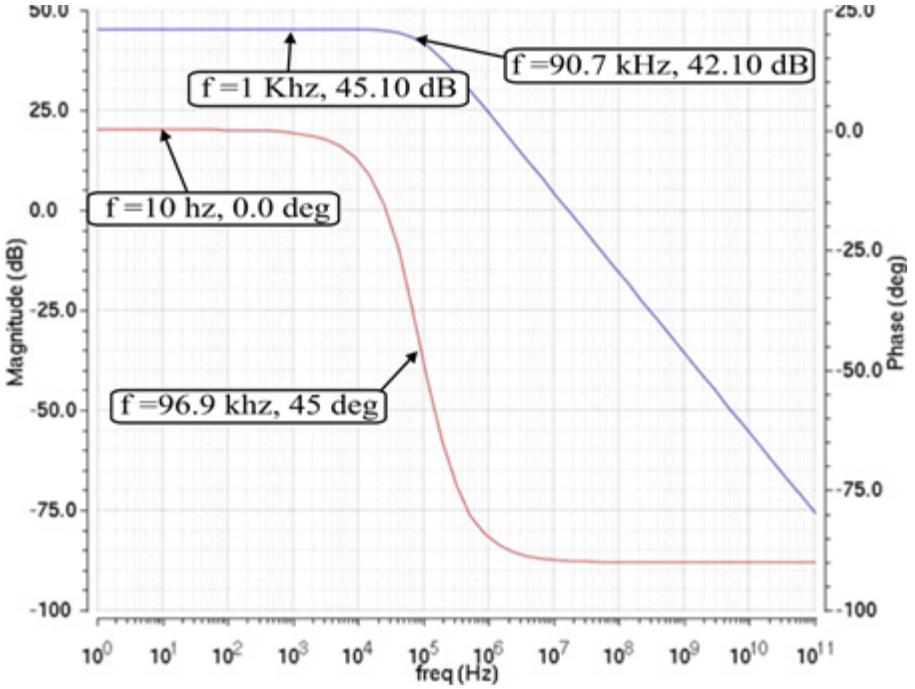



Fig. 4.8 Bode diagram of the OTA using the macromodel depicted in Fig. 4.4.

with a $g_m$ = 315µA/V and $C_1$ = 16.5 pF in the 4-OTAs based gyrator.

To verify the inductor behavior of circuit depicted in Fig. 4.3, its impedance behavior in the range of 1 Hz to 1 GHz (Fig. 4.7) is analyzed. One can note from Fig. 4.7 that gyrator impedance increases linearly with frequency, following equation $Z_L = 2\pi fL$ in the range from 500 KHz to 1 MHz: $Z_L$ vary from 64 to 70 dB, and the phase angle confirms that the range where the circuit behaves as an inductor is from 147.5 KHz to 8.7 MHz. From simulation results presented in Fig. 4.7, one can estimate the inductance value $L = Z_L/2\pi f$ = (0.5 - 1.2) mH in the frequency range (750 KHz - 1 MHz) which is the required for achieving 150 Vpp at the out node of the voltage amplifier.

The frequency response of the OTA macromodel with $C_{in}$ = 100 fF, $R_o$ =100 kΩ, $C_o$ = 16.5 fF and $g_m$ = 315 µA/V shows a DC gain of 45.10 dB and a bandwidth of 90.7 KHz (Fig. 4.8); an analysis of the effects of DC gain and BW over gyrator performance demonstrates that a BW can be of 90.7 KHz and gain 42.10 dB. Then, the 4-OTA based Gyrator is designed for Av(DC) = 45 dB and cutoff frequency of 90.7 KHz. These specifications can be achieved with a simple structure of OTA in 0.5 µm CMOS technology. We have opted for a balanced-OTA structure (Fig. 4.9). In this circuit, the DC gain voltage is given by [Peterson-86] [Kaewdang-11]

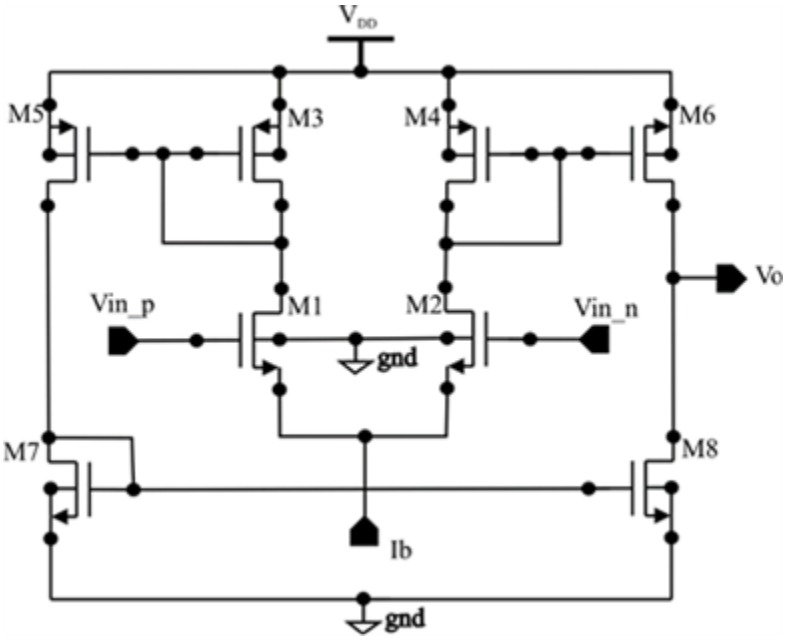



Fig. 4.9 Schematic of balanced-OTA used in 4-OTAs gyrator structure.

$$A_{VDC} = \frac{\alpha g_{m1}}{g_{ds6} + g_{ds8}} \tag{4-8}$$

where $\alpha$ is the ratio of the dimension between the M3 and M5 (or M4, M6) transistors, $g_{m1}$ is the transconductance of M1 or M2, $g_{ds6}$ is the gate-source conductance of M6, and $g_{ds8}$ is the gate-source conductance of M8. The bandwidth is given by

$$BW = \frac{1}{R_o C_o} \tag{4-9}$$

where *Ro* and *Co* are the resistance and the net capacitance at the out node (Fig. 4.5). The gain-bandwidth product is given by

$$GBW = \frac{\alpha g_{m1}}{C_L} \tag{4-10}$$

where $C_L$ is a load capacitance at the output of the balanced OTA. The approximate phase margin is

$$PM \cong 180^0 - \tan^{-1}\left(\frac{w}{w_{p1}}\right)\Bigg|_{w=w_T} - \tan^{-1}\left(\frac{w}{w_{p2}}\right)\Bigg|_{w=w_T} - \tan^{-1}\left(\frac{w}{w_{p3}}\right)\Bigg|_{w=w_T} \tag{4-11}$$

where $w_{p1}$, $w_{p2}$, $w_{p3}$ are the approximate location for poles. The slew rate is given by

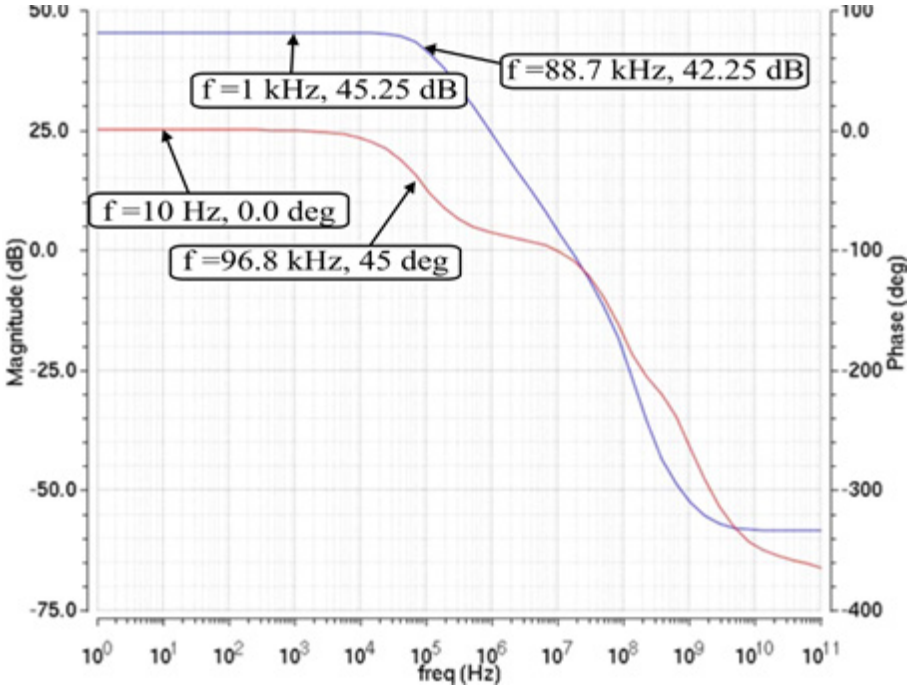



Fig. 4.10 Bode diagram of the transistor based OTA implemented.

TABLE 4.2. TRANSISTOR SIZES OF THE BALANCED OTA

| Transistor | Width (μm) | Large (μm) |
|---|---|---|
| M1 | 39.2 | 0.6 |
| M2 | 39.2 | 0.6 |
| M3 | 68 | 1.2 |
| M4 | 68 | 1.2 |
| M5 | 27.8 | 1.2 |
| M6 | 27.8 | 1.2 |
| M7 | 6.0 | 1.2 |
| M8 | 6.0 | 1.2 |

$$SR = \frac{\alpha I_B}{C_L} \tag{4-12}$$

The relationship between the branch currents are

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_B}{2}, I_{D5} = I_{D6} = I_{D7} = I_{D8} = \alpha\left(\frac{I_B}{2}\right) \tag{4-13}$$

and finally the dc voltage at out node $V_o$ is given by

$$V_o = V_{GS7} = V_{T7} + \sqrt{\frac{\alpha I_B}{K_N (W/L)_7}} \tag{4-14}$$

Using (4-8), (4-9) and (4-12) to (4-14) the OTA circuit is designed with an iterative procedure to meet the above mentioned design specifications of 45 dB and a $BW$ = 90 KHz with a capacitive load of $C_L$ = 16.5 pF and an $I_B$ = 20 μA. The resulting values of transistor sizes are summarized in

Table 4.2. The frequency response at transistor level is verified by plotting the Bode diagram and then, the layout is designed. The parasitic extraction was performed using the Calibre CAD tool. Fig. 4.10 presents the post-layout frequency response of the designed OTA for the 4-OTA based gyrator. One can note from Fig. 4.10 that the DC gain is 45.25 dB and the BW is 88.7 KHz.

## 4.3. Design of the 4-OTA Based Gyrator

The implementation of the 4-OTA gyrator in the Virtuoso simulator is shown in Fig. 4.11. Notice that we have added four voltage dividers connected to the inputs of the OTAs (Fig. 4.11)

TABLE 4.3. TRANSISTOR SIZES OF VOLTAGE DIVIDERS ADDED TO THE 4-OTA GYRATOR

| Transistor | Width (μm) | Large (μm) |
|---|---|---|
| M1 | 3.0 | 3.0 |
| M2 | 11.0 | 3.0 |
| M3 | 3.0 | 3.0 |
| M4 | 11.0 | 3.0 |
| M5 | 3.0 | 3.0 |
| M6 | 11.0 | 3.0 |
| M7 | 3.0 | 3.0 |
| M8 | 11.0 | 3.0 |

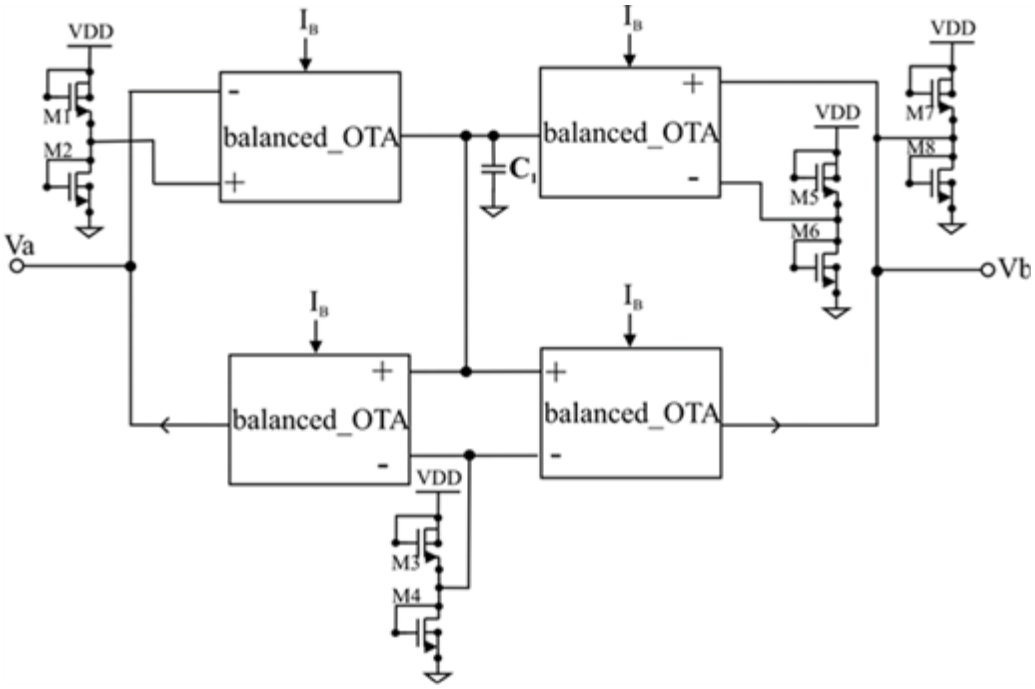



Fig. 4.11 Schematic of the 4-OTA gyrator active inductor implemented in Virtuoso-Cadence.

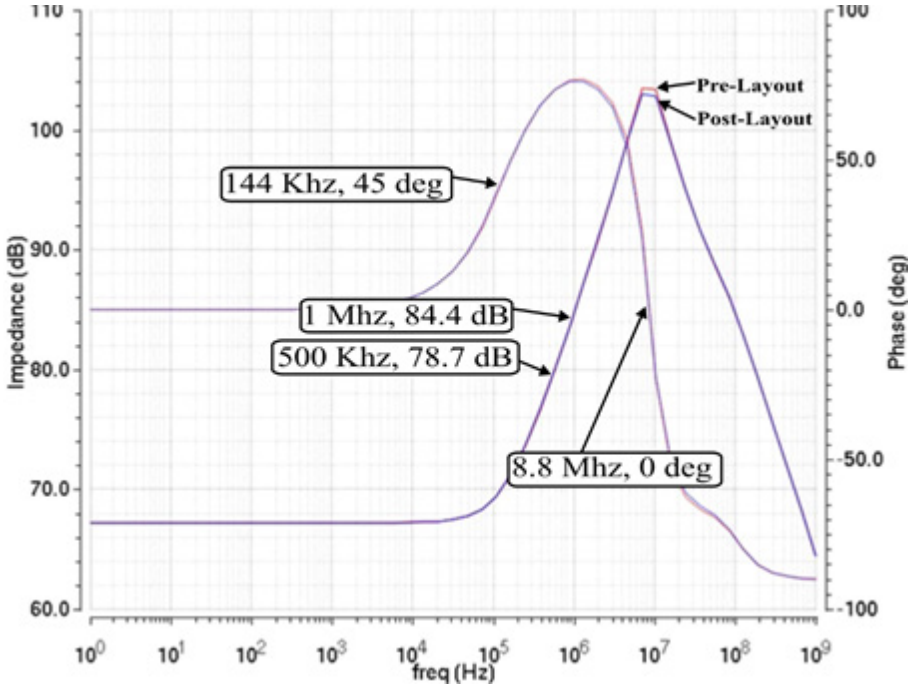



Fig. 4.12 The inductive behavior of the designed 4-OTA gyrator active inductor implemented in Virtuoso-Cadence.

in order to provide a dc voltage to balance the branch currents of OTAs and to ensure that all OTAs work in the saturation region. The resulting values of transistor sizes are summarized in Table 4.3.

TABLE 4.4. TRANSISTOR SIZES OF CURRENT SOURCE AND ACTIVE RESISTANCE (M5) ADDED TO VOLTAGE AMPLIFIER

| Transistor | Width (μm) | Large (μm) |
|---|---|---|
| M1 | 4.0 | 12.0 |
| M2 | 15 | 3.0 |
| M3 | 15 | 3.0 |
| M4 | 600 | 60 |
| M5 | 3.0 | 3.0 |

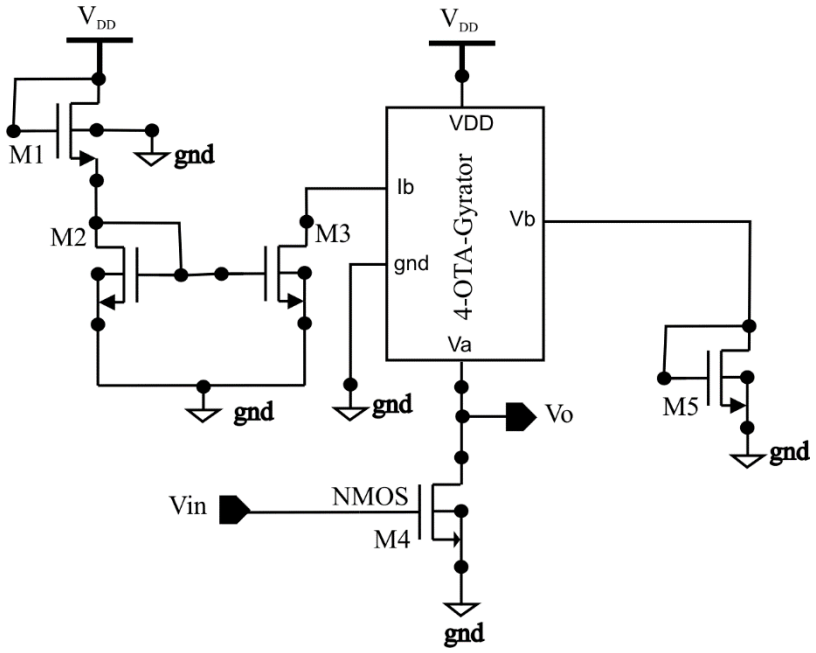



Fig. 4.13 Schematic of common source amplifier with the 4-OTA gyrator active load.

The layout is implemented using the hierarchical technical layout technique by assembling OTA blocks (see Appendix). After verifying (DRC and LVS) the layout, we extracted the parasitics using Calibre tool. The inductive function of designed 4-OTAs based gyrator is verified with a simulation in the frequency domain at schematic and post-layout levels. Fig. 4.12 shows the impedance of the 4-OTA based gyrator. As can be noticed in that figure, the impedance increases linearly in the range from 500 KHz to 1 MHz, and the phase angle confirms that the range where the circuit behaves as an inductor is from 144 KHz to 8.8 MHz. Using $Z = 2\pi fL$, the estimated inductance at 750 KHz is $L$ = 2.38 mH. Differences between calculated $L$ value using the theoretical model and extracted value from layout can be attributed to the parasitics from layout.

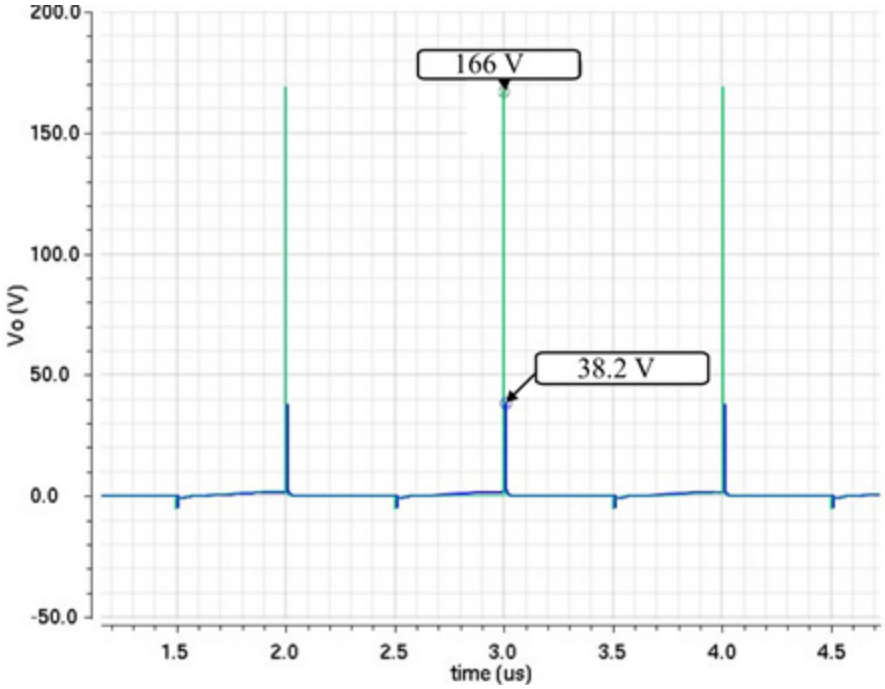



Fig. 4.14 Time response of the common source amplifier with a 4-OTA gyrator active load implemented in Virtuoso-Cadence.

Simulation results in Fig. 4.12 also show that the pre- and post-layout responses are almost identical in the range of frequency of interest for this project.

## 4.4. Simulation Results of the Voltage Amplifier with a 4-OTA Based Gyrator Load

Fig. 4.13 shows the implementation of the common-source amplifier with the 4-OTA gyrator active load. In order to implement all the circuit at transistor level, we added a current mirror, formed by M1, M2 and M3 (Fig. 4.13) to provide an $I_B$ = 80 µA to the four OTAs of the active inductor. Also, an active resistance formed by a diode-connected transistor (M5) is added to the gyrator circuit as a reference to ground. The corresponding resistance of this active resistance is 100 kΩ. The input transistor M4 complete the voltage amplifier. Table 4.4 summarizes the values of the transistor sizes of the voltage amplifier with active inductance load at transistor level.

The voltage amplifier response, shown in Fig. 4.13, is measured in time domain; we used the same testbench to test the RFD prototype, i.e. a square waveform input signal with a period of 1 µs (or 1 MHz), a rise and fall time of 1 ps, and an amplitude of 5 V; these rise time an fall time


Fig. 4.15 Warning results of the transient simulation of the post-layout circuit implemented in Virtuoso-Cadence.

values are chosen to ensure a correct voltage amplification in the active load. The simulation results are shown in Fig. 4.14. One can note in this figure sharp voltage pulses of 168 V in the pre-layout response, however, in the post-layout response the maximum amplitude reached is 38 V. We searched for causes to this low voltage in the amplifier; it seems that the transistor in the signal path reaches its breakdown voltage in the conduction interval, hence the maximum voltage that can be developed at the out node of the voltage amplifier is 38 V. Fig. 4.15 shows an example of report generated by Virtuoso tool after simulations; in this figure one can note warnings related to the breakdown voltage of 40 V is exceeded. With this study one can postulate that the design of this kind of high voltage circuits are not feasible in 0.5 μm CMOS technology (OnSemi C5N process). Therefore, the voltage amplifier module cannot be integrated to the VCO module to have all components of RFD system in a single chip. From here, the oscillator module of the RFD chip and the amplifier block should be implemented using discrete components.

## 4.5. Conclusions

This chapter presented the design of the voltage amplifier circuit with a common-source

topology with inductive load in 0.5 μm CMOS technology. A brief analysis of on-chip passive inductors and on-chip active inductors in CMOS technology was done. We have explored the possibility to implement a small layout area circuit using a 4-OTA based gyrator as a load of voltage amplifier. The design of 4-OTA based gyrator shows proper inductive function in the range of 500 KHz to 1 MHz with an inductance value slightly larger than 2.38 mH. Simulations results at pre-layout level of the voltage amplifier with inductive load show the expected response of an output voltage around 168 V. However, the post-layout response was limited to a maximum output voltage of 38 V. This reduced output voltage is attributed to the fact that transistor in the signal path of voltage amplifier circuit reaches the breakdown voltage in the time interval where they conduct. This implies *a priori* that the design of this kind of high voltage circuits are not feasible in 0.5 μm CMOS technology (OnSemi C5N process) and puts a technology limitation to implement all modules of RFD system in a single chip. Then, the voltage amplifier module must be implemented with discrete components to complete the RFD system proposed in this dissertation work.

# 5. Physical Design of the RFD Chip

In this chapter, the oscillator module layout of the RFD chip is presented. It includes the control logic circuit (CLC), which allows 4 different modes to be selected for operating the RFD chip, the low-frequency oscillator (LFO), which controls the change of frequency sweep of VCO from 500 KHz to 1 MHz each second, and the voltage-controlled oscillator (VCO), which generates a stable frequency signal tuned in the range from 500 KHz to 1 MHz. The layout of all these blocks were designed using the custom technique with pCells of 0.5 µm CMOS technology from process OnSemi C5N PDK provided by MOSIS. The integration of the oscillator module in a single core and its routing to the pads ring is also described.

## 5.1. Floorplan

The floorplan for this chip is designed to use the shortest lengths of interconnects between all layout modules in order to minimize the effect of parasitics [Zhou-11], such that the final circuit meets the required performance. This floorplan was manually designed. Fig. 5.1 shows the proposed floorplan of the RFD chip. It is seen from Fig. 5.1 that all the RFD modules are connected in cascade: at the left we find the logic inputs *A* and *B* of the CLC circuit, then the outputs *Cntl* and *Cont* are connected to the LFO module, the output *LFO_out* is connected to the VCO module, and the output *VCO_out* connected to the output signal of the RFD chip.

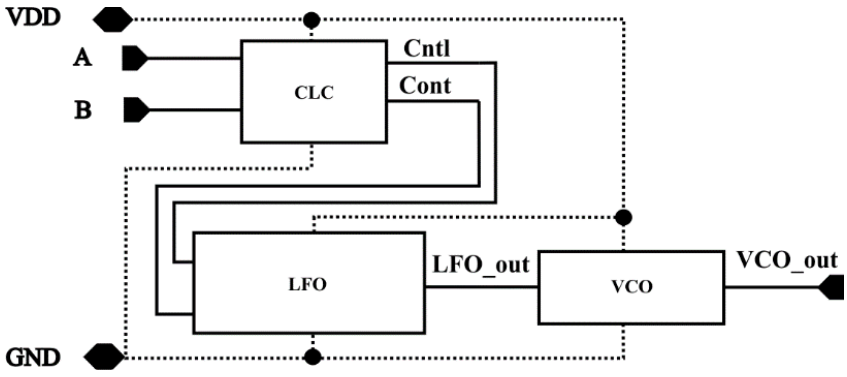



Fig. 5.1 Floorplan of the RFD chip.

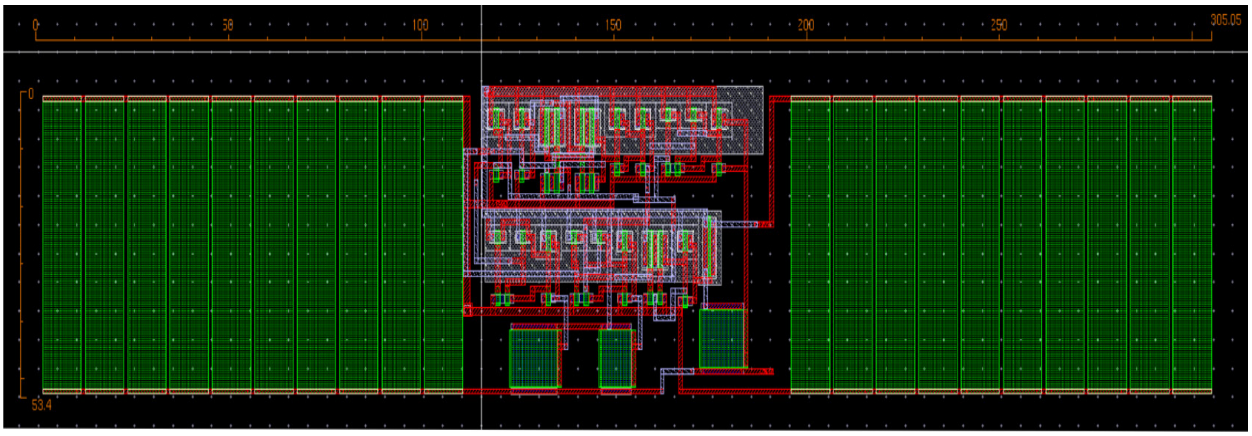



Fig. 5.2 Layout of the digital control and the voltage divisor circuits. Implemented in Virtuoso-Cadence.

## 5.2. Layout of the CLC Block

The layout of CLC is shown in Fig. 5.2; the digital logic circuitry and the voltage divider are placed in the middle and the circuit's R1 resistance is placed on the left and right sides. The width of $V_{DD}$ and *GND* interconnections are 2 µm and 2 µm, respectively. The width of these

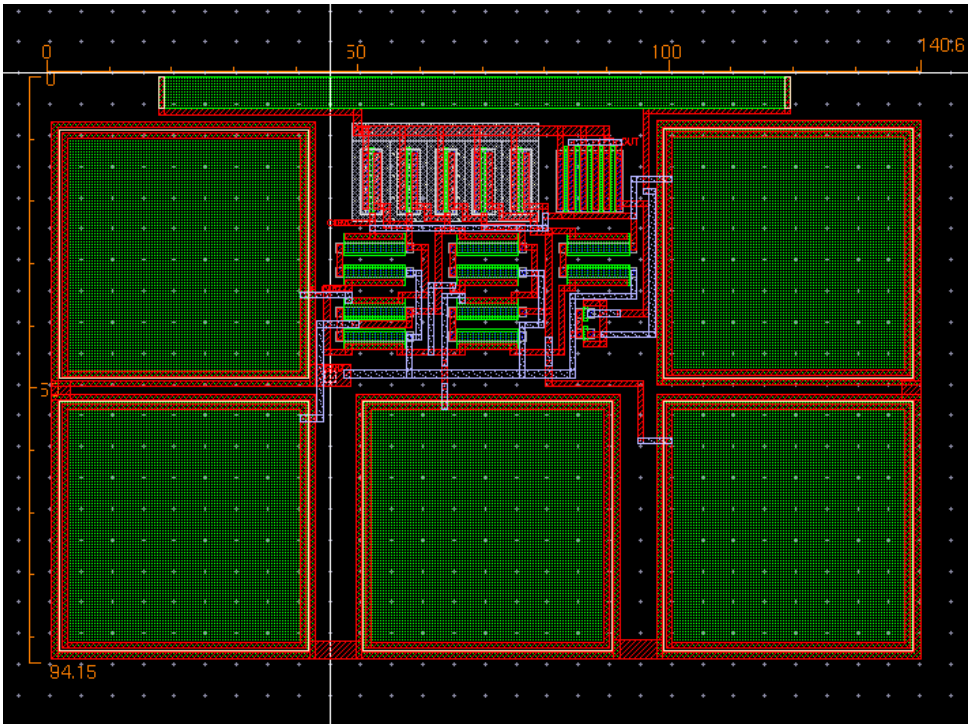



Fig. 5.3 Layout of the LFO circuit obtained in Virtuoso-Cadence.

interconnects are calculated considering electro-migration rules for this PDK [OnSemi-16]. The resulting layout area is 55 µm × 305 µm. This placement of components in the layout is defined according to the floorplan in the integration blocks' stage of the project. The DRC and LVS checks were verified using Calibre tool, then the extraction of parasitic layout was performed using PEX-tool from Calibre.

## 5.3. Layout of the LFO Block

Fig. 5.3 shows the circuit layout designed for this block using techniques like those proposed in [Hastings-01]. In Fig. 5.3, the exterior geometries correspond to the LFO's larger capacitors, while in the center are placed the group of transistors of this circuit. The width of $V_{DD}$ and *GND* interconnections dictated by electro-migration rules are 2 µm and 3 µm, respectively. The layout area of LFO block is 94 µm × 140 µm and it fulfills the project's layout area requirement. The Calibre tool from Mentor Graphics, along with the suite of Cadence design tools, are used to debug DRC and LVS errors, as proposed in [Martínez-Guerrero-16]. The layout passed all the above checks and then parasitic extraction from layout was performed.

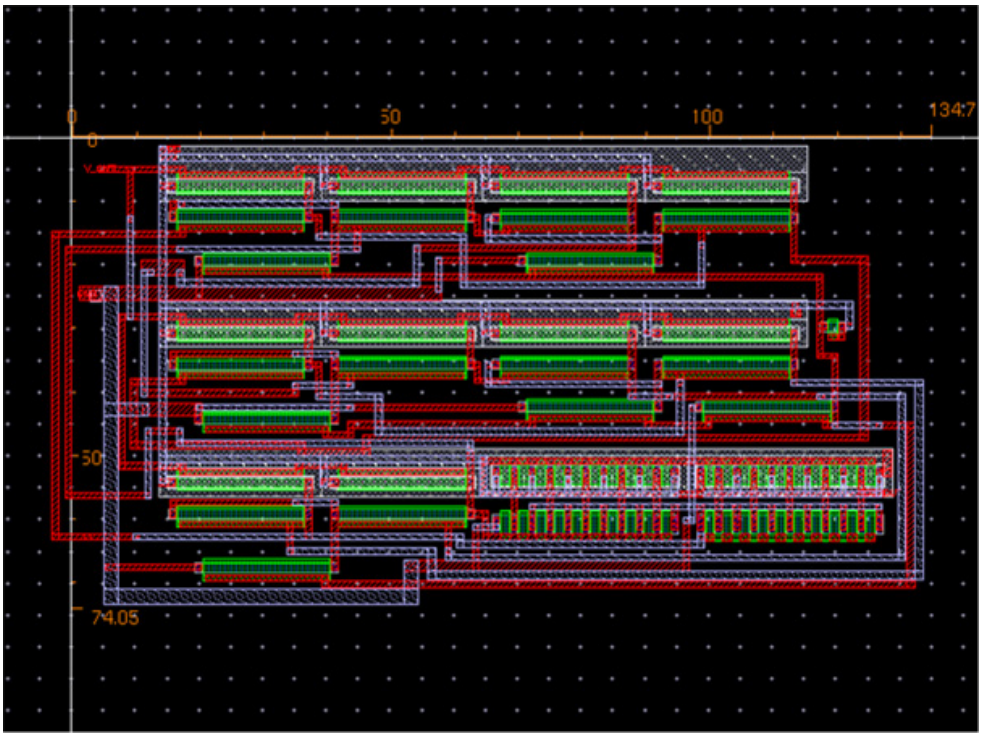



Fig. 5.4 Layout of the DVCO circuit obtained in Virtuoso-Cadence.

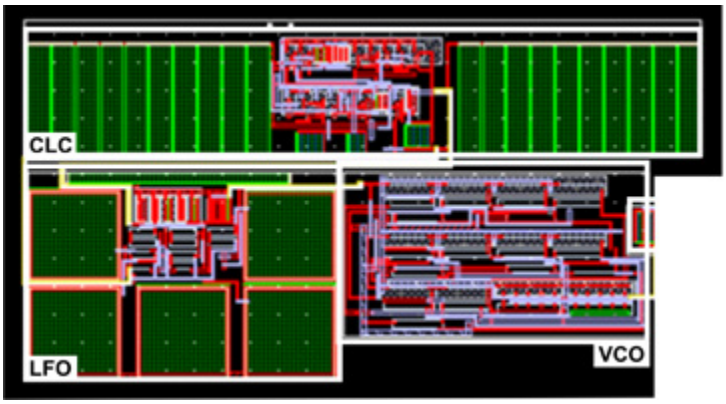



Fig. 5.5 Integration of all the layouts in the RFD chip. Implemented in Virtuoso-Cadence.

## 5.4. Layout of the VCO Block

Fig. 5.4 shows the circuit layout designed for VCO block. The transistors of this circuit are arranged in this way in order to avoid the induction of noise into the circuit. The width of $V_{DD}$ and *GND* interconnections dictated by electro-migration rules are 2 µm and 2 µm, respectively. The layout area of DVCO block is 74 µm × 134 µm and it is defined according to the area of VCO block in the floorplan of the RFD chip.

## 5.5. Integration of Oscillator Blocks' of RFD Chip

Fig. 5.5 shows the layout of the 4 blocks of the signal generator of the RFD chip joined in a single block; on the top we find the CLC layout connected to the LFO layout positioned on the left, then the LFO layout connected to the VCO layout on the center, and finally the VCO connected to the output of the circuit.

All the layouts modules (CLC, LFO, and VCO) are interconnected with metal 1, metal 2 and metal 3 to break long routing paths. The resulting layout area for the circuit core is 150 µm × 320 µm.

The pad-ring is constructed with pCells like: *iosana3* for input/output analog pad, the *ana_gns_clamp* for the GND analog pad, the *ana_pwr_clamp* for the VDD analog pad, the *inline_clamp* for the straight line filling pad, and the *corner_clamp* for the corner filling pad, all from OnSemi C5N process. The pads were placed in the following order: first the *A* and *B* input

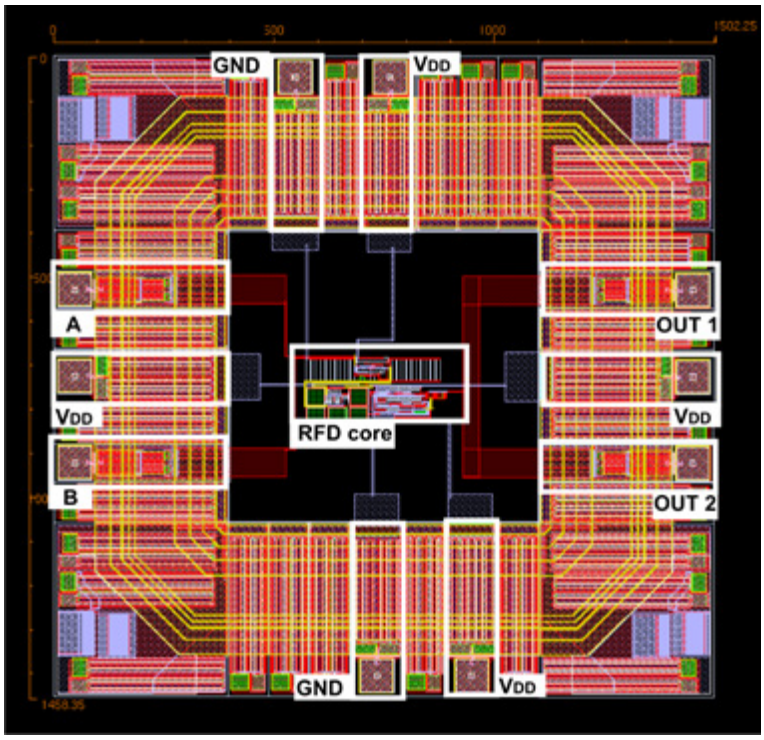



Fig. 5.6 Tapeout of the signal generator module of the RFD chip implemented in 0.5 µm CMOS technology.

ports, then the $V_{DD}$ and GND ports, and finally the OUT1 and OUT2 ports.

Fig. 5.6 shows the assembled layout with the pads ring of the signal generator of RFD chip. The assembled layout was verified with checks DRC, and LVS using Calibre tool. The layout area of the whole signal generator of RFD chip is 1460 µm × 1500 µm.

## 5.6. Conclusions

This chapter presented the integration of all layouts of the modules that conform the RFD chip. First, the layout design of the control logic circuit (CLC) is implemented, where the resulting layout area was 55 µm × 305 µm. Then, the layout design of the low-frequency oscillator (LFO) was presented, where the resulting layout area was 94 µm × 140 µm. Finally, the voltage-controlled oscillator (VCO) layout design was presented, where the resulting layout area was 74 µm × 134 µm. The width of all interconnections were defined by applying electro-migration rules from OnSemi C5N process.

All the blocks of the signal generator of the RFD chip were assembled in a single core

using the hierarchical technique according to the floorplan defined for this chip. Finally, the core layout was routed to the pads ring of the RFD chip. The Calibre tool from Mentor Graphics, along with the suite of Cadence design tools, was used to debug the tape-out from DRC and LVS errors. The final layout area of the RFD chip was 1460 µm × 1500 µm.

# General Conclusions

This thesis presented the design of a radiofrequency diathermy integrated system intended for physical rehabilitation application. The electronic system is composed of a programmable low-frequency oscillator (LFO), a voltage controlled oscillator (VCO), and a common-source voltage amplifier.

First, the full-system was macro-modeled to define the design specifications for each of the blocks making up the RFD chip, i.e., each block's signal type, voltage levels, and operational frequencies; simulations were performed to corroborate the appropriate functioning of each block separately. Then, a simulation was run of all the blocks interconnected among themselves, corroborating the correct functioning of the entire system. All of these tests provided a basis to begin designing each of the system blocks at the schematic level.

A prototype of the RFD system using discrete components assembled on a one-layer PCB board was designed, implemented, and tested to validate the hypothesis that shorter time to heal damaged muscles can be achieved with continuous RFD application. Characterization of the prototype was performed, i.e., its power consumption, and the waveform of its output signal in order to evaluate whether the equipment generates the adequate RFD signal and whether its operating autonomy with a battery would surpass 48 hours. Having the portable RFD prototype made it possible to draw up a fairly specific and defined work plan to obtain important information that enabled us to identify the minimum current needed for this circuit to achieve positive effects in the scarring of soft tissue in a universe of patients specified by specialist physicians. Next, we performed a comparative study on continuous mode versus conventional RFD treatments applied to patients with muscular diseases. This study showed that the duration of exposure to RFD signals has a positive and measurable impact on healing affected muscles. This investigation in the RFD field allowed us to validate that the continuous application of an RFD signal in patients with a recent injury is an effective and fast-acting measure for reducing inflammation or healing muscle, ligament, and nerve injuries. The conducted study also confirmed the effectiveness of the proposed RFD prototype for radio frequency diathermy therapy in continuous mode. Similarly, and as a future work, it would be necessary to perform additional medical studies to confirm the effectiveness of the integrated circuit designed for the portable radio-frequency diathermy.

The design process of two modules of the RFD chip, i.e., the signal generator and the voltage amplifier at the transistor level, was also presented. The signal generator module was implemented with a 2-bits control logic circuit (CLC), which allows 4 different frequencies to be selected for operating the RFD chip. A low-frequency oscillator (LFO) was described, with a topology of 5 stages current starved delay cells and an extra buffer stage to get a current gain and voltage levels at the output of 0 to 5V, and a frequency tuning range of 1 Hz to 12 Hz. A voltage-controlled oscillator (VCO) with differential ring oscillator topology was detailed. The post-layout simulations of signal generator of the RFD chip presented a maximum power consumption of 22.19 mW, a maximum phase noise of −149 dBc/Hz, and a range of operation frequency from 500 KHz to 1 MHz.

The common-source voltage amplifier with active inductive load in integrated circuit technology was also presented. This block was designed with a voltage gain of 30 V/V, and a maximum drain current of around 26 mA. The active-inductor load was designed for an $L$ = 1.2 mH. The active inductance was implemented with a 4-OTA Gyrator-C. Post-layout simulations of voltage amplifier with active inductance load showed a maximum output voltage of 40 V. The reduced output is attributed to the breakdown voltage and the current limits for the transistor in 0.5 µm CMOS technology. This established a limitation to assemble the two modules in a single core of the RFD chip. Then, the only module to be implemented in integrated circuit is the generator signal, while the voltage amplifier must be implemented with discrete components.

The physical synthesis of internal blocks of signal generator module of the RFD chip was performed using Layout Virtuoso tool and pCells of 0.5 µm CMOS technology. Blocks of signal generator were placed according to a proposed floorplan which was conceived to use the shortest interconnects and hence minimize the effects of layout parasitics. The CLC block consumed an area of 94 µm × 140 µm; the layout area of the LFO circuit was 94 µm × 140 µm, and finally the layout area of the VCO circuit was 74 µm × 134 µm. The total area of signal generator module was 1460 µm × 1500 µm.

The pads ring was implemented with pCells like: *iosana3* for input/output analog pad, *ana_gns_clamp* for the GND analog pad, *ana_pwr_clamp* for the VDD analog pad, *inline_clamp* for the straight line filling pad, and *corner_clamp* for the corner filling pad, all from OnSemi C5N process. The layout of signal generator core was routed manually to the pads ring of the RFD chip. Calibre tool from Mentor Graphics along with the suite of Cadence design tools used to verify the

layout showed that the final tape out of RFD chip was free of DRC and LVS errors, thus it is ready to be fabricated.

# Conclusiones Generales

Esta tesis presentó el diseño de un sistema integrado de diatermia de radiofrecuencia enfocado en aplicaciones de rehabilitación física. El sistema electrónico está compuesto de un oscilador programable de baja frecuencia (LFO), un oscilador controlado por voltaje (VCO), y un amplificador de fuente- común.

Primero el sistema completo fue macro modelado para definir las especificaciones de diseño de los bloques que componen el chip de RFD, por ejemplo: el tipo de señal de cada bloque, los niveles de voltaje, y las frecuencias de operación; las simulaciones fueron corridas para corroborar el funcionamiento apropiado de cada bloque de forma separada. Después, fueron corridas simulaciones con todos los bloques conectados entre sí, corroborando el buen funcionamiento del sistema completo. Todas estas pruebas dieron las bases para poder comenzar el diseño de los bloques del sistema a nivel esquemático.

Se diseñó un prototipo usando componentes comerciales y ensamblados en una tarjeta PCB de una capa, implementado y probado para validar la hipótesis de que se puede acortar el tiempo de sanación de una lesión muscular con una aplicación continua de RFD. Fue conformada la caracterización del prototipo, incluyendo: su consumo de potencia, la forma de onda de señal de salida con la finalidad de evaluar si el equipo genera la señal de RFD adecuada con una autonomía de operación con batería mayor a las 48 horas. Una vez teniendo el prototipo de RFD, fue posible esbozar un plan de trabajo para obtener información importante que permitiera deducir la corriente mínima necesaria para que el circuito provoque efectos positivos en el cicatrizado de tejidos blandos en un universo de pacientes especificado por especialistas en terapia física.

También se presentó un estudio comparativo entre el modo continuo y el modo convencional de tratamientos de RFD aplicados en pacientes con problemas musculares. Este estudio mostró que la duración en exposiciones a señales de RFD tiene un impacto positivo y medible en el cicatrizado de músculos dañados. Esta investigación en el campo de RFD nos permitió validar que la aplicación continua de RFD en pacientes con lesiones recientes es una medida efectiva y rápida para reducir la inflamación y la cicatrización en músculos, ligamentos y nervios dañados. El estudio confirmó la efectividad del prototipo de RFD para terapia con diatermia de RF en modo continuo. Similarmente, y para un trabajo futuro, sería necesario realizar

estudios extras que confirmen la efectividad del circuito integrado diseñado para la diatermia de radiofrecuencia portable.

También se presentó el proceso de diseño a nivel de transistor de los dos módulos del chip de RFD: el generador de señal y el amplificador de voltaje. El generador de señal fue implementado con un circuito de control lógico de 2 bits (CLC), que permite la selección de 4 diferentes frecuencias de operación del chip de RFD. Se describió un oscilador de baja frecuencia (LFO), con topología *current starved delay* de 5 etapas, con una etapa extra de buffer para obtener una ganancia de corriente y niveles de voltaje de 0 a 5 V, y un rango de sintonizado de frecuencia de 1 Hz a 12 Hz. Se describió un oscilador controlado por voltaje (VCO) con topología de oscilador diferencial de anillo. Las simulaciones de *post-layout* del generador de señal del chip RFD presentaron un consumo de potencia máximo de 22.19 mW, un ruido de fase máximo de -149 dBc/Hz, y un rango de frecuencias de operación de 500 KHz a 1 MHz.

También fue presentado el diseño de un amplificador de fuente-común con carga activa inductiva. Este bloque fue diseñado con una ganancia de voltaje de 30 V/V, y una corriente en *drain* máxima de 26 mA. La inductancia activa fue implementada con un 4-OTA *Gyrator-C*. Las simulaciones *post-layout* del amplificador con carga activa de inductancia mostraron un voltaje de salida máximo de 40 V. La salida de voltaje reducida es atribuida al voltaje de rompimiento y los límites de corriente de los transistores en tecnología 0.5 µm CMOS. Esto coloca una limitación para ensamblar los 2 módulos en un solo *core* del chip de RFD. Así, el único módulo que se va a implementar en el circuito integrado es el generador de señal, mientras que el amplificador de voltaje debe ser implementado con componentes discretos.

La síntesis física de los bloques internos del módulo generador de señal fue realizada usando la herramienta de *layout* de Virtuoso y las *pCells* de la tecnología CMOS 0.5 µm. Los bloques del generador de señal fueron colocados de acuerdo al *floorplan* propuesto que fue realizado para lograr las interconexiones más cortas y minimizar los efectos parásitos del *layout*. El bloque CLC consumió un área de 94 µm × 140 µm, el área de *layout* del circuito LFO fue de 94 µm × 140 µm, y el área de *layout* del circuito VCO fue de 74 µm × 134 µm. El área total para el circuito generador de señal fue 1460 µm × 1500 µm.

El anillo de *pads* fue implementado con *pCells* como: *iosana3* para el *input/output analog pad*, *ana_gns_clamp* para el GND *analog pad*, *ana_pwr_clamp* para el VDD *analog pad*, *inline_clamp* para el *straight line filling pad*, y finalmente *corner_clamp* para el *corner filling pad*,

todas del proceso OnSemi C5N. El *core* del *layout* del generador de señal fue ruteado manualmente al anillo de *pads* del chip de RFD. La herramienta Calibre de Mentor Graphics junto con las herramientas de diseño de Cadence que se usaron para verificar el *layout* mostró que el *tapeout* final del chip de RFD no tuvo errores ni de DRC ni de LVS, así que está listo para ser fabricado.

# Appendix

# A. LIST OF INTERNAL RESEARCH REPORTS

1) A. Corres-Matamoros and E. Martínez-Guerrero, "Fundamentals of electromyography," Internal Report *PhDEngScITESO-13-02-R*, ITESO, Tlaquepaque, Mexico, Dec. 2013.
2) A. Corres-Matamoros, E. Martínez-Guerrero, and I. Padilla-Cantoya, "Macro modeling of an electromyography acquisition system," Internal Report *PhDEngScITESO-14-06-R*, ITESO, Tlaquepaque, Mexico, Aug. 2014.
3) A. Corres-Matamoros, E. Martínez-Guerrero, and I. Padilla-Cantoya, "Design of an electronic system for physical rehabilitation," Internal Report *PhDEngScITESO-14-12-R*, ITESO, Tlaquepaque, Mexico, Dec. 2014.
4) A. Corres-Matamoros and E. Martínez-Guerrero, "Macro modeling of a RFD chip and simulation of a common-source amplifier," Internal Report *PhDEngScITESO-15-15-R*, ITESO, Tlaquepaque, Mexico, Dec. 2015.
5) A. Corres-Matamoros and E. Martínez-Guerrero, "Fundamentals of active inductances, gyrator-c and Carreto-Castro topologies," Internal Report *PhDEngScITESO-15-18-R*, ITESO, Tlaquepaque, Mexico, Dec. 2015.
6) A. Corres-Matamoros and E. Martínez-Guerrero, "Design of a voltage-controlled oscillator (VCO)," Internal Report *PhDEngScITESO-16-04-R*, ITESO, Tlaquepaque, Mexico, Apr. 2016.
7) A. Corres-Matamoros and E. Martínez-Guerrero, "Design of a low-frequency oscillator (LFO) for a radio-frequency diathermy (RFD)," Internal Report *PhDEngScITESO-16-16-R*, ITESO, Tlaquepaque, Mexico, Nov. 2016.
8) A. Corres-Matamoros and E. Martínez-Guerrero, "Design of a portable radio-frequency diathermy prototype," Internal Report *PhDEngScITESO-16-28-R*, ITESO, Tlaquepaque, Mexico, Dec. 2016.
9) A. Corres-Matamoros and E. Martínez-Guerrero, "Layout design of a signal generator for radio-frequency diathermy," Internal Report *PhDEngScITESO-16-29-R*, ITESO, Tlaquepaque, Mexico, Dec. 2016.
10) A. Corres-Matamoros and E. Martínez-Guerrero, "Re-design of a low-frequency oscillator (LFO) in AMI 0.5 μm technology," Internal Report *PhDEngScITESO-17-11-R*, ITESO, Tlaquepaque, Mexico, May. 2017.

11) A. Corres-Matamoros and E. Martínez-Guerrero, “Design of a voltage controlled oscillator in AMI 0.5 μm technology,” Internal Report *PhDEngScITESO-17-12-R*, ITESO, Tlaquepaque, Mexico, May 2017.
12) A. Corres-Matamoros and E. Martínez-Guerrero, “Prototype validation for radio-frequency diathermy applications,” Internal Report *PhDEngScITESO-17-20-R*, ITESO, Tlaquepaque, Mexico, Jun. 2017.
13) A. Corres-Matamoros and E. Martínez-Guerrero, “Design of a 2-bits control logic for a low-frequency oscillator (LFO) and a common-source amplifier (CSAMP),” Internal Report *PhDEngScITESO-17-26-R*, ITESO, Tlaquepaque, Mexico, Jul. 2017.

# B. LIST OF PUBLICATIONS AND INTELECTUAL PROPERTY

## B.1. CONFERENCE PAPERS

1) A. Corres-Matamoros, E. Martínez-Guerrero, and J. E. Rayas-Sánchez, "A programmable CMOS voltage controlled ring oscillator for radio-frequency diathermy on-chip circuit," in *Int. Caribbean Conf. Devices, Circuits, and Systems (ICCDCS-2017)*, Cozumel, Mexico, Jun. 2017, pp. 65-68. (e-ISSN: 2165-3550; p-ISBN: 978-1-5386-1963-6; e-ISBN: 978-1-5386-1962-9; INSPEC: 16996077; DOI: 10.1109/ICCDCS.2017.7959721)
2) A. Corres-Matamoros, E. Martínez-Guerrero, and J. E. Rayas-Sánchez, "Design and validation of a portable radio-frequency diathermy prototype," in *Int. Caribbean Conf. Devices, Circuits, and Systems (ICCDCS-2017)*, Cozumel, Mexico, Jun. 2017, pp. 93-96. (e-ISSN: 2165-3550; p-ISBN: 978-1-5386-1963-6; e-ISBN: 978-1-5386-1962-9; INSPEC: 16996066; DOI: 10.1109/ICCDCS.2017.7959710).

## B.2. PATENTS

1) A. Corres-Matamoros and E. Martínez-Guerrero, "*Dispositivo portátil de diatermia por radiofrecuencia para terapia médica en rehabilitación de lesiones*," Mexican Patent Application MX/A/2017/003153 (IMPI), March 17, 2017.

# C. MACROMODEL FILES IMPLEMENTED

## C.1 MACRO MODEL CODE OF THE VCO BLOCK

```
// VerilogA for ACORRES, VCO_va, veriloga
//Archivo compu : Ejemplos Verilog_A.pdf pag.23
`include "constants.vams"
`include "disciplines.vams"

module VCO_va( va, vb );

      input  va;
      output vb;

      electrical va, vb;

      parameter real amplitude = 3.3;
      parameter real centre_frequency = 850000;
      parameter real gain = 1000;
      parameter integer steps_per_cycle = 200;
      localparam real omegac = 500.0 * `M_PI * centre_frequency,
                  omega_gain = 500.0 * `M_PI * gain;

      analog
      begin : main
            real vin, instantaneousFreq;
            vin = V(va);
            V(vb) <+ amplitude*sin(idt(vin*omega_gain+omegac, 0.0));
            instantaneousFreq = centre_frequency + gain * vin;
            $bound_step(1.0 / instantaneousFreq / steps_per_cycle);

      end

endmodule
```

## C.2 MACRO MODEL CODE OF THE AMP BLOCK

```
// VerilogA for ACORRES, AMP_va, veriloga

`include "constants.vams"
`include "disciplines.vams"

module AMP_va(in,out,gnd);

input in,gnd;
output out;

real gm;
parameter real r1=15000;

electrical in,out,gnd;

analog begin
```

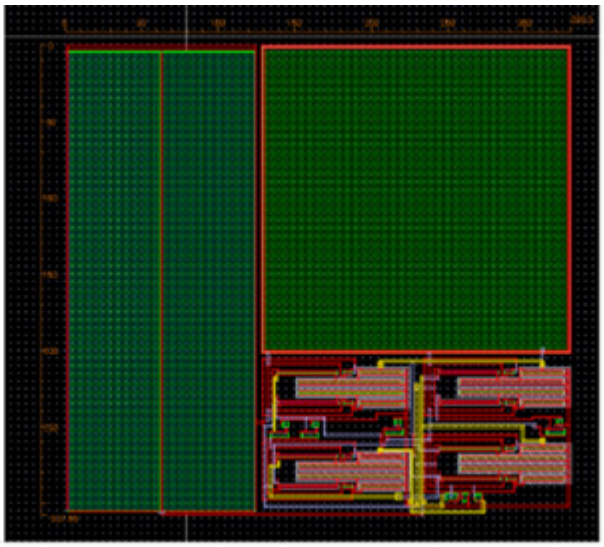
```
gain=1;

I(in,gnd)<+V(in,gnd)/r1;
I(out,gnd)<+gm*(V(in,gnd));

end

endmodule
```

## C.3 LAYOUT OF THE AMPLIFIER WITH THE 4-OTA GYRATOR-C ACTIVE LOAD



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# Author Index

# Subject Index

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