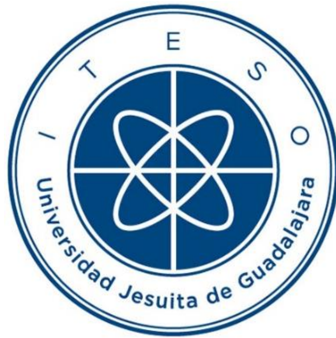
INSTITUTO TECNOLÓGICO
Y DE ESTUDIOS SUPERIORES DE OCCIDENTE

Reconocimiento de validez oficial de estudios de nivel superior según acuerdo secretarial 15018, publicado en el Diario Oficial de la Federación el 29 de noviembre de 1976.

Departamento de Electrónica, Sistemas e Informática

DOCTORADO EN CIENCIAS DE LA INGENIERÍA



METODOLOGIAS DE OPTIMIZACION PARA ECUALIZADORES TRANSMISOR Y RECEPTOR DE ENLACES DE ALTA VELOCIDAD EN LA VALIDACION POST-SILICIO INDUSTRIAL DE PLATAFORMAS COMPUTACIONALES

Tesis que para obtener el grado de

DOCTOR EN CIENCIAS DE LA INGENIERÍA

presenta: Francisco Elías Rangel Patiño

Director de tesis: Dr. José Ernesto Rayas Sánchez

Co-director de tesis: Dr. Nagib Hakim

Tlaquepaque, Jalisco. Julio de 2018

DOCTOR EN CIENCIAS DE LA INGENIERÍA (2018) ITESO, Tlaquepaque, Jal., México

TÍTULO: **Metodologías de Optimización para Ecualizadores Transmisor y Receptor de Enlaces de Alta Velocidad en la Validación Post-Silicio Industrial de Plataformas Computacionales**

AUTOR: Francisco Elías Rangel Patiño

Ingeniero en Comunicaciones y Electrónica (Universidad Veracruzana, México)

Maestro en Electrónica y Telecomunicaciones (CICESE, México)

Maestro en Ciencias Computacionales (TecNM, México)

DIRECTOR DE TESIS: José Ernesto Rayas Sánchez

Profesor Numerario del Departamento de Electrónica, Sistemas e Informática, ITESO

Ingeniero en Electrónica (ITESO, México)

Maestro en Sistemas Electrónicos (ITESM Campus Monterrey, México)

Doctor en Ingeniería Eléctrica (Universidad McMaster, Canadá)

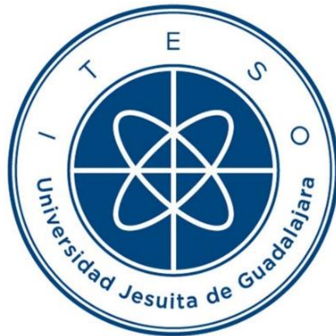
Senior, IEEE

NÚMERO DE PÁGINAS: xxx, 168

ITESO – The Jesuit University of Guadalajara

Department of Electronics, Systems, and Informatics

DOCTORAL PROGRAM IN ENGINEERING SCIENCES



TRANSMITTER AND RECEIVER EQUALIZERS OPTIMIZATION METHODOLOGIES FOR HIGH-SPEED LINKS IN INDUSTRIAL COMPUTER PLATFORMS POST-SILICON VALIDATION

Thesis to obtain the degree of

DOCTOR IN ENGINEERING SCIENCES

Presents: Francisco Elías Rangel-Patiño

Thesis Director: Dr. José Ernesto Rayas-Sánchez

Thesis Co-director: Dr. Nagib Hakim

Tlaquepaque, Jalisco, Mexico
July 2018

PHD IN ENGINEERING SCIENCES (2018) ITESO, Tlaquepaque, Jal., Mexico

TITLE: **Transmitter and Receiver Equalizers Optimization Methodologies for High-Speed Links in Industrial Computer Platforms Post-Silicon Validation**

AUTHOR: Francisco Elías Rangel-Patiño
Bachelor’s degree in electronics engineering (Universidad Veracruzana, Mexico)
Master’s degree in electrical engineering (CICESE, Mexico)
Master’s degree in computer sciences (TecNM, Mexico)

THESIS DIRECTOR: José Ernesto Rayas-Sánchez
Department of Electronics, Systems, and Informatics, ITESO- The Jesuit University of Guadalajara
Bachelor’s degree in electronics engineering (ITESO, México)
Master’s degree in electrical engineering (ITESM, México)
Ph.D. degree in electrical engineering (McMaster University, Canada)
Senior, IEEE

NUMBER OF PAGES: xxx, 168

To my loving wife, Alma Delia, whose patience and understanding
have made this achievement possible

Resumen

A medida que el diseño de microprocesadores se escala a tecnologías nanométricas, las técnicas tradicionales de validación post-silicio resultan inadecuadas para lograr una cobertura funcional completa del sistema. Complejidades físicas del diseño, y variaciones extremas en los procesos tecnológicos, crean grandes desafíos para garantizar que el sistema funcione adecuadamente en las variantes condiciones de proceso de manufactura, voltaje y temperatura (PVT). Adicionalmente, cada vez hay un número mayor de circuitos de señal mixta en los microprocesadores. Una parte importante de ellos corresponde a los enlaces de entrada/salida de alta velocidad (HSIO; por sus siglas en inglés). Mejoras en el diseño de circuitos, en el procesamiento de señales y en los procesos de manufactura, han permitido que las velocidades de las interfaces HSIO rebasen los 10 Gb/s. Los efectos de ruido no deseado pueden crear múltiples problemas de integridad de señal, lo cual se agrava por el continuo incremento de las velocidades de canal al pasar de una generación tecnológica a la siguiente. Resulta evidente que los retos de la validación post-silicio están en constante aumento, aunados a una alta presión por mantener calendarios agresivos de lanzamiento al mercado. Con todos estos elementos, la validación post-silicio de los enlaces HSIO es complicada y extensa, además de ser crítica en la toma de decisión para el lanzamiento de un producto al mercado. Uno de los mayores desafíos radica en el proceso de sintonización de la capa física, donde se utilizan técnicas de ecualización para cancelar efectos indeseados inducidos por los canales. Ajustar la ecualización del transmisor (Tx) y del receptor (Rx) en PVT, considerando diferentes interconexiones de canal, es una tarea demandante en la validación post-silicio. Las prácticas industriales actuales para sintonización de la capa física requieren mediciones de laboratorio masivas, ya que se basan en métodos de enumeración exhaustiva, convirtiendo el proceso de ecualización en una tarea prolongada y prácticamente prohibitiva bajo las restricciones de lanzamiento al mercado. En esta tesis doctoral se proponen métodos de optimización directa, de modelaje sustituto y mapeo espacial, combinados con funciones objetivo apropiadas, para sintonizar eficientemente los ecualizadores del Tx y Rx. La evaluación de los métodos es realizada mediante mediciones de laboratorio en plataformas industriales realistas. Los resultados obtenidos demuestran la eficacia de los métodos propuestos, así como una mejora sustancial en desempeño, con respecto a la práctica industrial actual.

Summary

As microprocessor design scales to nanometric technology, traditional post-silicon validation techniques are inappropriate to get a full system functional coverage. Physical complexity and extreme technology process variations introduce design challenges to guarantee performance over process, voltage, and temperature (PVT) conditions. In addition, there is an increasingly higher number of mixed-signal circuits within microprocessors. A significant portion of them corresponds to high-speed input/output (HSIO) links. Improvements in signaling methods, circuits, and process technology have allowed HSIO data rates to scale beyond 10 Gb/s. Undesired noise effects can create multiple signal integrity problems. This problem is aggravated by the fact that channel speeds keep increasing from one generation bus technology to the next one. It is evident that challenges of post-silicon validation are continuously increasing, along with a high pressure of maintaining aggressive launch schedules. With all of these elements, post-silicon validation of HSIO links is tough and time-consuming, and can be critical for making a product release qualification decision. One of the major challenges in electrical validation of HSIO links lies in the physical layer (PHY) tuning process, where equalization techniques are used to cancel undesired effects induced by the channels. Adjusting the transmitter (Tx) and receiver (Rx) equalization across PVT and different interconnect channels can be a very time-consuming task in post-silicon validation. Typical current industrial practices for PHY tuning require massive lab measurements, since they are based on exhaustive enumeration methods, making the equalization process too lengthy and practically prohibitive under current silicon time-to-market commitments. In this doctoral dissertation, direct and surrogate-based optimization methods, including space mapping, are proposed based on suitable objective functions to efficiently tune the Tx and Rx equalizers. The proposed methodologies are evaluated by lab measurements on realistic industrial post-silicon validation platforms, demonstrating the efficiency of the proposed methods and substantial performance improvements as compared with those achieved by current industrial practices.

Acknowledgements

The author wishes to express his sincere appreciation to Dr. José Ernesto Rayas-Sánchez, professor of the Department of Electronics, Systems, and Informatics at ITESO, and director of research in the Computer-Aided Engineering of Circuits and Systems (CAECAS) group at ITESO, for his encouragement, expert guidance, and keen supervision as doctoral thesis director throughout the course of this work. The author offers his gratitude to Dr. Nagib Hakim, Principal Engineer from Intel Corporation, for his support as doctoral thesis co-director during the development of this work. He also thanks Dr. Zabdiel Brito-Brito, Dr. Arturo Veloz-Guerrero, Dr. José Rodrigo Camacho-Pérez, and Dr. Manuel Salim-Maza, members of his Ph.D. Thesis Committee, for their interest, assessment, and suggestions.

The author has greatly benefited from working with MATLAB, developed by The MathWorks Inc.

Special thanks are due to Dr. Zabdiel Brito-Brito, from CAECAS research group at ITESO, and Mr. Edgar A. Vega-Ochoa, from Intel Corporation, for fruitful cooperation and helpful technical discussions.

It is the author's pleasure to acknowledge fruitful collaboration and stimulating discussions with his colleagues of CAECAS research group at ITESO – The Jesuit University of Guadalajara: Andrés Viveros-Watcher, Felipe de Jesús Leal-Romo, José Luis Chávez-Hurtado, and Rafael del-Rey-Acuña, as well as with colleagues at Intel Corp.: Alejandro Cortez-Ibarra, Brenda M. Marcial-Camacho, Carolina Olea-Gutierrez, Carlos Galindo-Meza, Carlos Rivas-Parra, Jesus Gomez-Lopez, Miguel Davalos-Santana, Ricardo Chavez-Cuadras, Ricardo Baca-Baylon, Rodrigo Camacho-Perez, and Vicente Penney.

The author gratefully acknowledge the financial assistance through a scholarship granted by the *Consejo Nacional de Ciencia y Tecnología* (CONACYT), Mexican Government, as well as the financial support provided by Intel Corporation.

Finally, special thanks are due to my family: my wife Alma Delia, and my children Perla and Yasmin, for their understanding, patience, and continuous loving support.

Contenido

Resumen ..... **vii**

Summary ..... **ix**

Reconocimientos ..... **xi**

Contenido ..... **xiii**

Contents ..... **xix**

Lista de Figuras ..... **xxv**

Lista de Acrónimos ..... **xxix**

Introducción **1**

1. Validación Post-Silicio **7**

1.1. INTRODUCCIÓN 7
1.2. VALIDACIÓN DE SILICIO 9
1.2.1 Pre-Silicio y Post-Silicio 9
1.2.2 Disciplinas de Validación Post-Silicio 11
1.2.3 Validación Eléctrica Post-Silicio 12
1.3. VALIDACIÓN DE LOS MÁRGENES DEL SISTEMA – EL CONCEPTO SMV 12
1.4. RETOS EN LA VALIDACIÓN POST-SILICIO 14
1.4.1 Desarrollo de Silicio 14
1.4.2 Tiempo para Calificación 14
1.4.3 Limitado Número de Pruebas 16
1.4.4 Limitado Número de Partes 17
1.4.5 Interacción Compleja con Circuitos Circundantes 17
1.4.6 Reproducción de Fallas 17
1.4.7 Simulación a Nivel Sistema 17

1.4.8 Sintonización en Post-Silicio 18
1.5. OPORTUNIDADES EN LA VALIDACIÓN ELÉCTRICA POST-SILICIO 18
1.5.1 Conectando Verificación Pre-Silicio y Validación Post-Silicio 19
1.5.2 Compensaciones entre Tiempo de Validación y Calidad 19
1.5.3 Integrando Múltiples Fuentes de Datos 20
1.5.4 Conectando Simulación con Validación 20
1.6. CONCLUSIONES 21

2. Ecualización de Canal para Enlaces Seriales de Alta Velocidad 23

2.1. INTRODUCCIÓN 23
2.2. INTERFERENCIA ENTRE-SÍMBOLOS (ISI) 24
2.3. CONCEPTO DE ECUALIZACIÓN 25
2.4. ECUALIZACIÓN EN EL TRANSMISOR 27
2.5. ECUALIZACIÓN EN EL RECEPTOR 29
2.5.1 Ecualizador Lineal de Tiempo Continuo (CTLE) 29
2.5.2 Ecualizador de Decisión Retroalimentada (DFE) 30
2.6. ALGORITMO PARA ECUALIZADORES ADAPTIVOS 31
2.7. CONCLUSIONES 32

3. Validación de los Márgenes del Sistema 35

3.1. INTRODUCCIÓN 35
3.2. MARGEN DE OPERACIÓN 37
3.3. INSTRUMENTOS EMBEBIDOS 37
3.4. PRUEBAS DE LAZO CERRADO 39
3.5. PRUEBAS DE INTERCONEXIÓN A NIVEL SISTEMA 40
3.5.1 Pruebas de Interconexión con Escaneo de Limites 41
3.5.2 Pruebas de Interconexión con Escaneo de Limites en Alta Velocidad 41
3.5.3 Autodiagnóstico de Interconexión 42
3.6. PRUEBA FUNCIONAL UTILIZANDO INSTRUMENTOS EMBEBIDOS 44
3.6.1 Prueba de Márgenes 46
3.7. CONCLUSIONES 48

4. Ecualización del Receptor HSIO por medio de Optimización con Modelo Sustituto 51

4.1. INTRODUCCIÓN 51
4.2. SISTEMA DE MEDICIONES 53
4.2.1 Márgenes del Sistema 54
4.2.2 Pruebas de Tolerancia al Ruido 54
4.3. FORMULACIÓN DE LA FUNCIÓN OBJETIVO 58
4.3.1 Función Objetivo de Márgenes del Sistema 58
4.3.2 Función Objetivo de Márgenes del Sistema y Tolerancia al Ruido 61
4.4. MODELO SUSTITUTO Y OPTIMIZACIÓN 62
4.4.1 Diseño de Experimentos 62
4.4.2 Sucesión de Baja Discrepancia 63
4.4.3 Secuencia Sobol 64
4.4.4 Modelo Sustituto Kriging 65
4.4.5 Optimización usando Modelo Sustituto 67
4.5. CASOS DE PRUEBA 68
4.5.1 Caso de Prueba 1: USB3 69
4.5.2 Caso de Prueba 2: SATA3 71
4.5.3 Caso de Prueba 3: PCIe 73
4.6. CONCLUSIONES 73

5. Ecualización del Transmisor Ethernet por medio de Optimización Directa 75

5.1. INTRODUCCIÓN 75
5.2. BANCO DE PRUEBAS DEL SISTEMA 77
5.3. SISTEMA DE MEDICIONES 78
5.4. FORMULACIÓN DE LA FUNCIÓN OBJETIVO Y OPTIMIZACIÓN 79
5.5. RESULTADOS 81
5.6. CONCLUSIONES 82

6. Ecualización del Transceptor PCIe por medio de Optimización Directa . 85

6.1. INTRODUCCIÓN 85

6.2. ECUALIZACIÓN PCI EXPRESS 88
6.2.1 Ecualizadores Tx y Rx 88
6.2.2 Proceso de Ecualización........ 89
6.3. MATRIZ DE COEFICIENTES DE ECUALIZACIÓN EN EL TRANSMISOR 90
6.4. FORMULACIÓN DE LA FUNCIÓN OBJETIVO Y OPTIMIZACIÓN 92
6.5. BANCO DE PRUEBAS DEL SISTEMA 95
6.6. RESULTADOS 96
6.7. CONCLUSIONES 98

7. Modelado Sustituto Burdo del Receptor HSIO 99

7.1. INTRODUCCIÓN........ 99
7.2. MÁQUINA DE APRENDIZAJE EN VALIDACIÓN POST-SILICIO 101
7.3. CONCEPTOS BÁSICOS DE REDES NEURONALES ARTIFICIALES........ 103
7.3.1 Neuronas Artificiales 103
7.3.2 Topologías de ANN 104
7.4. MODELADO DEL RECEPTOR POR MEDIO DE ANN 105
7.4.1 Topología ANN 106
7.4.2 Modelado por Descomposición 107
7.4.3 Modelado y Entrenamiento de ANN 108
7.5. CONFIGURACIÓN DEL SISTEMA EXPERIMENTAL Y MÉTODOS DOE........ 110
7.6. RESULTADOS DEL MODELADO NEURAL 113
7.7. CONCLUSIONES 115

8. Ecualización del Receptor HSIO por Medio de Optimización de Mapeo Espacial 117

8.1. INTRODUCCIÓN........ 117
8.2. MAPEO ESPACIAL BASADO EN BROYDEN........ 119
8.2.1 Modelo Fino........ 119
8.2.2 Modelo Burdo 120
8.2.3 Función Objetivo 121
8.3. OPTIMIZACIÓN ASM 121
8.4. RESULTADOS DE OPTIMIZACIÓN........ 123
8.5. CONCLUSIONES 124

General Conclusions **.......... 127**

Conclusiones Generales 131

Apéndice 137

A. LISTA DE REPORTES INTERNOS DE INVESTIGACIÓN 139

B. LISTA DE PUBLICACIONES 141

B.1. Artículos de Revista 141

B.2. Artículos de Congresos 141

B.3. Artículos de congresos INTEL 143

Bibliografía 145

Índice de Autores 159

Índice de Términos 165

Contents

Resumen vii

Summary ix

Acknowledgements xi

Contenido xiii

Contents xix

List of Figures xxv

List of Acronyms xxix

Introduction 1

1. Post-Silicon Validation 7

1.1. INTRODUCTION 7
1.2. SILICON VALIDATION 9
1.2.1 Pre-Silicon and Post-Silicon 9
1.2.2 Post-Silicon Validation Disciplines 11
1.2.3 Post-Silicon Electrical Validation 12
1.3. SYSTEM MARGINALITY VALIDATION – THE SMV CONCEPT 12
1.4. POST-SILICON VALIDATION CHALLENGES 14
1.4.1 Silicon Development 14
1.4.2 Time-to-Qualification 14
1.4.3 Limited Number of Tests 16
1.4.4 Limited Parts 17
1.4.5 Complex Interaction with Surrounding Circuits 17
1.4.6 Failure Reproduction 17
1.4.7 System-Level Simulation 17

1.4.8 Post-Silicon Tuning 18
1.5. POST-SILICON ELECTRICAL VALIDATION OPPORTUNITIES 18
1.5.1 Bridging Pre-Silicon Verification and Post-Silicon Validation 19
1.5.2 Trade-off between Validation Time and Quality 19
1.5.3 Integrating Multiple Sources of Data 20
1.5.4 Connecting Simulation with Validation 20
1.6. CONCLUSIONS 21

2. Channel Equalization for High-Speed Serial Links 23

2.1. INTRODUCTION 23
2.2. INTER-SYMBOL INTERFERENCE (ISI) 24
2.3. EQUALIZATION CONCEPT 25
2.4. EQUALIZATION AT THE TRANSMITTER 27
2.5. EQUALIZATION AT THE RECEIVER 29
2.5.1 Continuous Time Linear Equalizer (CTLE) 29
2.5.2 Decision Feedback Equalizer (DFE) 30
2.6. ALGORITHMS FOR ADAPTIVE EQUALIZERS 31
2.7. CONCLUSIONS 32

3. System Marginality Validation 35

3.1. INTRODUCTION 35
3.2. OPERATING MARGIN 37
3.3. EMBEDDED INSTRUMENTS 37
3.4. LOOPBACK TESTING 39
3.5. SYSTEM-LEVEL INTERCONNECT TESTING 40
3.5.1 Interconnect Testing with Boundary Scan 41
3.5.2 Interconnect Testing with High-Speed Boundary Scan 41
3.5.3 Interconnect Built-In Self-Test 42
3.6. FUNCTIONAL TESTING BY USING EMBEDDED INSTRUMENTS 44
3.6.1 Margin Testing 46
3.7. CONCLUSIONS 48

4. HSIO Receiver Equalization by Surrogate-Based Optimization................51

4.1. INTRODUCTION... 51
4.2. SYSTEM MEASUREMENTS... 53
4.2.1 System Margins 54
4.2.2 Jitter Tolerance Testing.. 54
4.3. OBJECTIVE FUNCTION FORMULATION... 58
4.3.1 Objective Function for System Margining 58
4.3.2 Objective Function for System Margining and Jitter Tolerance......................... 61
4.4. SURROGATE MODEL AND OPTIMIZATION 62
4.4.1 Design of Experiments.. 62
4.4.2 Low-discrepancy Sequences 63
4.4.3 The Sobol Sequence.. 64
4.4.4 Kriging Surrogate Model 65
4.4.5 Optimization using the Surrogate Model 67
4.5. TEST CASES.. 68
4.5.1 Test Case 1: USB3 69
4.5.2 Test Case 2: SATA3 71
4.5.3 Test Case 3: PCIe... 73
4.6. CONCLUSIONS 73

5. Ethernet Transmitter Equalization by Direct Optimization.......................75

5.1. INTRODUCTION... 75
5.2. SYSTEM TEST SETUP 77
5.3. SYSTEM MEASUREMENTS... 78
5.4. OBJECTIVE FUNCTION FORMULATION AND OPTIMIZATION 79
5.5. RESULTS... 81
5.6. CONCLUSIONS 82

6. PCIe Transceiver Equalization by Direct Optimization.............................85

6.1. INTRODUCTION... 85
6.2. PCI EXPRESS EQUALIZATION.. 88
6.2.1 Tx and Rx Equalizers.. 88

6.2.2 Equalization Process 89
6.3. TRANSMITTER EQUALIZATION COEFFICIENT MATRIX 90
6.4. OBJECTIVE FUNCTION FORMULATION AND OPTIMIZATION 92
6.5. SYSTEM TEST SETUP 95
6.6. RESULTS 96
6.7. CONCLUSION 98

7. HSIO Receiver Coarse Surrogates Modeling 99

7.1. INTRODUCTION 99
7.2. MACHINE LEARNING IN POST-SILICON VALIDATION 101
7.3. BASIC CONCEPTS ON ARTIFICIAL NEURAL NETWORKS 103
7.3.1 Artificial Neurons 103
7.3.2 ANN Topologies 104
7.4. ANN-BASED RECEIVER METAMODELING 105
7.4.1 ANN Topology 106
7.4.2 Decomposed Modeling 107
7.4.3 ANN Modeling and Training 108
7.5. EXPERIMENTAL SYSTEM CONFIGURATION AND DOE APPROACHES 110
7.6. NEURAL MODELING RESULTS 113
7.7. CONCLUSION 115

8. HSIO Receiver Equalization by Space Mapping Optimization 117

8.1. INTRODUCTION 117
8.2. BROYDEN-BASED INPUT SPACE MAPPING 119
8.2.1 Fine Model 119
8.2.2 Coarse Model 120
8.2.3 Objective Function 121
8.3. ASM OPTIMIZATION 121
8.4. OPTIMIZATION RESULTS 123
8.5. CONCLUSION 124

General Conclusions 127

Conclusiones Generales **131**

Appendix **137**

A. LIST OF INTERNAL RESEARCH REPORTS 139
B. LIST OF PUBLICATIONS 141
B.1. Journal Papers 141
B.2. Conference Papers 141
B.3. INTEL Conference Papers 143

Bibliography **145**

Author Index **159**

Subject Index **165**

List of Figures

Fig. 1.1 Example of SMV functional eye diagram. 14

Fig. 1.2 Design and validation product lifecycle. Figure taken from [INTEL-03]. 15

Fig. 2.1 Diagram of a typical backplane communication between two chips. 24

Fig. 2.2 Inter-symbol interference effect. 25

Fig. 2.3 Basic idea of equalization: the equalizer frequency response approximates the inverse of the channel frequency response to flatten out the overall response. a) channel response, b) equalizer response, c) equalized response. 26

Fig. 2.4 Graphical concept of the EQ process. 27

Fig. 2.5 Transmit pre-emphasis FIR filter. 28

Fig. 2.6 Continuous time linear equalizer and typical transfer function. 29

Fig. 2.7 Decision feedback equalizer. 30

Fig. 2.8 Simultaneously employing Tx and Rx equalizers, combining different EQ topologies. 31

Fig. 2.9 Typical continuous-time adaptive equalizer. 32

Fig. 3.1 Specification window and characterization window for electrical validation. Figure taken from [Gizopoulos-06]. 38

Fig. 3.2 IBIST as applied for high-speed serial testing at the board level. Figure taken from [Nejedlo-03]. 43

Fig. 3.3 Loopback mode testing. 45

Fig. 3.4 SMV's on-die instrumentation architecture. 46

Fig. 3.5 Functional eye diagram based on multiple margin points. 47

Fig. 4.1 Architecture of a typical SerDes PHY. 53

Fig. 4.2 Jitter classification and their relationships. Figure taken from [Wang-08]. 54

Fig. 4.3 Jitter sources in an HSIO link. 55

Fig. 4.4 Relationship between jitter and BER in the Rx. Figure taken from [Fan-09]. 56

Fig. 4.5 Rx jitter tolerance threshold for testing. Figure taken from [Wang-08]. 57

Fig. 4.6 A generic test setup for Rx jitter testing. 58

Fig. 4.7 JTOL testing setups: a) PCIe setup, b) USB setup, c) SATA setup. 59

Fig. 4.8 Eye diagram: a) graphical objective function representation, b) example of asymmetries on 3 test cases of EQ. 60

Fig. 4.9 Post-Silicon industrial validation platform. 68

Fig. 4.10 Bock diagram of the platform controller hub. 68
Fig. 4.11 USB3 Rx channel topology. 69
Fig. 4.12 The holistic methodology test setup for USB system margining and JTOL optimization. 70
Fig. 4.13 USB3 results comparing the proposed methodology against the initial design and the trade-off approach: a) eye width versus eye height, b) JTOL testing results. 70
Fig. 4.14 SATA Rx channel topology. 71
Fig. 4.15 SATA results comparing the proposed methodology against the initial design and the trade-off approach: a) eye width versus eye height, b) JTOL testing results. 71
Fig. 4.16 PCIe Gen3 Rx channel topology. 72
Fig. 4.17 PCIe results comparing the proposed methodology against the initial design and the trade-off approach: a) eye width versus eye height, b) JTOL testing results. 72
Fig. 5.1 Block diagram of a 3-tap transmit FIR filter. 76
Fig. 5.2 Test setup for SFP transmitter optimization. 77
Fig. 5.3 Eye diagram and SFP+ Tx mask. 78
Fig. 5.4 SFP eye diagram over mask before optimization. 80
Fig. 5.5 SFP FIR normalized coefficients responses and function values across iterations. 81
Fig. 5.6 SFP eye diagram over mask after optimization. 82
Fig. 6.1 PCIe switched architecture. Figure taken from [PCISIG-17]. 86
Fig. 6.2 A PCIe channel with Tx and Rx equalizers. 89
Fig. 6.3 PCIe Tx/Rx adaptive equalization. 90
Fig. 6.4 PCIe EQ map coefficients search space for optimization. 91
Fig. 6.5 PCI Express test setup: an Intel server post-silicon validation platform. 94
Fig. 6.6 PCIe objective function values across iterations. 96
Fig. 6.7 PCIe normalized coefficients responses across iterations. 96
Fig. 6.8 PCIe eye diagram results: comparing the proposed methodology ($\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}^*)$) with three different seeds against the exhaustive method ($\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}^*_{\mathrm{exhaustive}})$). 97
Fig. 6.9 PCIe eye diagram results: comparing the proposed methodology ($\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}^*)$) against the initial design ($\boldsymbol{R}_{\mathrm{f}}^{(\boldsymbol{x}0)}$) and the exhaustive method ($\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}^*_{\mathrm{exhaustive}})$). 98
Fig. 7.1 Neural representations: a) simplified diagram of a biological neuron, b) inner-product artificial neuron (modified from [Rayas-Sánchez-15]). 103
Fig. 7.2 ANN topologies: a) feedforward, b) recurrent. Figure taken from [Suzuki-11]. 104
Fig. 7.3 ANN modeling concept. Figure modified from [Rayas-Sánchez-04]. 106

Fig. 7.4 A 3-layer perceptron including the scaling process. Figure modified from [Rayas-Sánchez-04]. 107

Fig. 7.5 ANN decomposed modeling. Figure modified from [Rayas-Sánchez-04]. 109

Fig. 7.6 Algorithm for training the ANN with controlled generalization performance. 111

Fig. 7.7 HSIO server post-silicon hardware configuration for Rx metamodeling. 112

Fig. 7.8 Comparison of SATA neural model generalization performance for different DoE techniques: a) eye height error; b) eye width error. 113

Fig. 7.9 Learning and testing errors during SATA neural training using Sobol50, for a) eye width and b) eye height. 113

Fig. 7.10 Neural model generalization performance using Sobol50 for a) SATA eye width; b) SATA eye height. 114

Fig. 7.11 Neural model generalization performance using Sobol50 for a) USB width; and b) USB eye height. 114

Fig. 8.1 HSIO link reconfiguration in post-silicon server validation to cancel out the effects of system channels' variability. 118

Fig. 8.2 Test setup for SM optimization: an Intel server post-silicon validation platform. 119

Fig. 8.3 Pseudo-code for the Broyden-based input space mapping optimization. Figure taken from [Rayas-Sánchez-11]. 122

Fig. 8.4 Normalized SATA coefficients and objective function values across SM optimization iterations. 123

Fig. 8.5 Comparison between the system fine model responses at the initial Rx EQ coefficients, $\boldsymbol{x}_c^{(0)}$, at the optimal coarse model solution, $\boldsymbol{x}_c^*$, and at the space-mapped solution found, $\boldsymbol{x}^{SM}$. 124

List of Acronyms

3LP	3-Layer Perceptron
ANN	Artificial Neural Networks
ASIC	Application-Specific Integrated Circuit
ASM	Aggressive Space Mapping
ATE	Automatic Test Equipment
BER	Bit-Error Rate
BIOS	Basic Input Output System
BMF	Bayesian Model Fusion
CAD	Computer-Aided Design
CDR	Clock Data Recovery
CMOS	Complementary Metal–Oxide–Semiconductor
CPU	Central Processing Unit
CTAE	Continuous-Time Adaptive Equalizer
CTLE	Continuous Time Linear Equalizer
CV	Compatibility Validation
DAC	Digital to Analog Converter
DFE	Decision-Feedback Equalization
DFT	Designed For Test
DFx	Design-For-x
DIMM	Dual In-Line Memory Module
DMA	Direct Memory Access
DMI	Direct Media Interface
DoE	Design of Experiments
DUT	Device-Under-Test
EM	Electromagnetic
EQ	Equalization
EV	Electrical Validation
FFE	Feed-Forward Equalizer
FIR	Finite Impulse Response
FM	Frequency Modulated
FS	Full Swing
HSIO	High-Speed Input/Output
HVM	High Volume Manufacturing
IBIST	Interconnect Built-In Self-Test
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IJATG	Internal Joint Test Action Group
IL	Insertion Loss
ISI	Inter-Symbol Interference
JIM	Jitter Injection Module
JTOL	Jitter Tolerance

LF	Low Frequency
LMS	Least Mean Squares
MAC	Medium Access Control
MLP	Multilayer Perceptrons
MSE	Mean-Square Error
OS	Operating System
PCH	Platform Controller Hub
PCIe	Peripheral Component Interconnect Express
PDF	Probability Density Functions
PHY	Physical Layer
PI	Phase-Interpolator
PLL	Phase-Locked Loop
PRBS	Pseudo-Random Bit Sequence
PRQ	Product Release Qualification
PSM	Polynomial-based Surrogate Modeling
PVT	Process, Voltage, and Temperature
RC	Root Complex
RF	Radio Frequency
RJ	Random Jitter
Rx	Receiver
SATA	Serial Advanced Technology Attachment
SBO	Surrogate-Based Optimization
SerDes	Sserializer-Deserializer
SFF	Small Form Factor
SFP	Small form-Factor Pluggable
SFP+	Enhanced SFP
SJ	Sinusoidal Jitter
SM	Space Mapping
SMA	SubMiniature version A
SMV	System Marginality Validation
SNR	Signal-to-Noise Ratio
SoC	Systems on Chip
SV	System Validation
T&M	Test and Measurement
TAP	Test Access Port
TL	Transmission Lines
TTM	Time-To-Market
Tx	Transmitter
UI	Unit Interval
USB	Universal Serial Bus
VGA	Variable Gain Amplifier
VT	Voltage/Temperature
ZF	Zero Forcing

Introduction

A computer-aided design (CAD) tool based on electromechanical relays was programmed in the very early 1950's to solve the algebraic equilibrium-condition equations of a linear electrical network in the sinusoidal steady state [Graham-53]. Quickly it was possible to employ optimization techniques to achieve excellent designs of electric filters [Aaron-56]. From this fairly remote start from the perspective of digital computers, there has been a gradually increasing use of computers in the analysis, evaluation, testing, and optimization of electric and electronic circuits and systems [Aaron-56].

From the early 1950's, engineers and researchers on circuit and systems have always been interested in the theoretical problems of CAD circuit analysis, optimization, and automated design. In many cases, results from applied physics and mathematics have been identified and used to advantage. At many locations around the world, in both industrial and academic environments, circuit and system researchers have been working extensively on new advances on CAD and have contributed significantly with outstanding results being documented in many scientific publications.

Modern CAD optimization techniques can now utilize most types of models, including multidimensional physical models. Space mapping (SM) [Bandler-94], [Koziel-08], offers a particularly powerful means of linking multidimensional numerical simulations (both physics-based and electromagnetic (EM) simulations) to CAD applications.

Trends for the future show that flexible macromodeling of devices and components will be created through SM models to replace central processing unit (CPU) intensive EM models [Snel-01]; and develop a design environment to work on large mixed-signal systems with the utilization of the Internet to incorporate manufacturing process requirements.

Furthermore, optimization software engines are appearing for wireless and microwave circuit design, which exploit both full-wave EM simulators and fast, empirical, coarse or surrogate models. It can be expected that commercial implementations of optimization-ready EM simulators incorporating exact or adjoint sensitivities [Alessandri-93], [Chung-00], [Ureel-96] will appear in the next decade, as well as robust algorithms for EM optimization fully exploiting SM and surrogate models. Similarly, knowledge-based artificial neural networks (ANN) techniques

[Rayas-Sánchez-04] are expected to play a significant role in future CAD.

The search for accurate models of active devices and passive components continues to be an imperative task. Advanced CAD technologies, such as SM and surrogate modeling, offer promising methodologies to address some of these challenges.

In the area of silicon validation, CAD techniques provide a means for designers to validate the design before physical implementation. Compared to traditional post-silicon validation, simulations (behavioral simulation) are much cheaper and faster to run. However, simulation results can deviate from the post-silicon measurements to some extent, due to inaccuracies of device models (components, channels, interconnects, etc.) and simplifications in behavioral models (e.g., in silicon transmitter and receiver circuits). Given such gaps between simulation and post-silicon validation measurements, there is an interest in how to use simulation to help post-silicon validation, and how post-silicon validation results can be used to calibrate pre-silicon CAD models. In addition to the inaccuracies in simulation, special techniques might be needed to integrate them with other post-silicon measurements considering industrial variations (i.e. silicon manufacturing process, voltage, temperature).

Nowadays, technologies such as formal verification, simulation acceleration and FPGA-based emulation allow covering much larger portions of the validation plans than traditional validation based on regular simulation. However, to really approach the overall verification and validation challenge holistically, a more unified verification infrastructure is needed to carry on from pre-silicon to post-silicon, but unfortunately this is where current methodology often breaks apart. In order to transform the post-silicon validation from an engineering art, practiced by few experienced engineers, to a technical discipline with solid foundations and systematic methodologies, new approaches and CAD techniques are required. Some approaches may include reliable system design, embedded systems, software test and verification, and simulation in post-silicon by using concepts like SM.

In 1965, Gordon Moore, Intel’s cofounder, predicted that the number of transistors integrated per square inch on a die would double every year [Moore-65]. In subsequent years, the pace slowed, but the number of transistors has continued to double approximately every 18 months for the past three decades. Most experts expect that Moore’s law will hold for at least two more decades. Die size will continue to grow larger, but, at the same time, minimum feature size will continue to shrink. As the manufacturing technology continues to advance, precise control of the

silicon process is becoming more challenging. As microprocessor design moves into the nanometer age and in order to keep up with Moore's law, many new nanotechnologies and circuit design techniques must be developed and adopted, all of which pose new test challenges that must be addressed concurrently. Otherwise, the cost of test would eventually surpass the cost of silicon manufacturing.

Undesired effects such as jitter, inter-symbol interference (ISI), crosstalk and others, can create multiple problems on the signal integrity of high-speed I/O's (HSIO) circuits, making maximum bus speeds difficult to achieve in practice. This problem is aggravated by the fact that channel speeds keep increasing from one generation bus technology to the next one. With each step upward to a higher speed and higher signaling frequencies, an HSIO circuit becomes more susceptible to distortions and anomalies which can effectively disrupt bus traffic and stall system throughput. In general, the higher the frequency of the signaling, the more susceptible the interconnect becomes to errors, re-transmissions and other anomalies. This is of particular concern for serial I/O's interfaces, such as Peripheral Component Interconnect Express (PCIe), Serial Advanced Technology Attachment (SATA), Universal Serial Bus (USB), and Ethernet interfaces.

During silicon validation, a failure (e.g., a too small eye diagram at the receiver) may be observed, or it may be concluded that the percentage of dies that may fail is too high for high volume production. In either situation, debugging is required. Ideally, the bug is root-caused, and fix it by re-designing. However, this approach is inefficient and costly. In practice, instead of re-designing the circuit, many link failures can be fixed by reconfiguring the I/O links through modifying the underlying training algorithm and/or by tuning knob settings.

Training algorithms and physical layer (PHY) tuning are two important components in modern HSIO links. Training of a link is performed when the system boots, and it determines an optimal setting of sampling point (time and voltage) as well as transmitter (Tx)/receiver (Rx) coefficients, such as equalization (EQ) coefficients. This is usually an empirical algorithm given by expert knowledge of how the eye diagram is shaped. Obviously, the training algorithm has a very significant impact on eye margins, and is critical for I/O links to work properly.

PHY tuning is another important feature in mixed-signal systems. PHY tuning knobs are usually embedded in the I/O links, and can be digitally tuned to appropriate values. With transistor size keeping shrinking, there can be large die-to-die process variations. Besides, depending on the operating conditions (such as voltage supply and temperature), board impedance, different channel

loss, different add-in cards/DIMMs, the performance of I/O links can exhibit large variation. The PHY tuning provide a way to reconfigure I/O links in post-silicon to cancel out various fluctuations. Therefore, failures observed under one PHY tuning knob configuration might disappear under another knob configuration. However, it is usually unknown in pre-silicon which configuration gives the overall best performance. In other words, it is post-silicon validation's responsibility to search for "optimal" PHY tuning knob configurations that results in a good performance across all operating conditions. In the worst case, this means sweeping all possible combinations of all PHY tuning knobs – nearly prohibitive in the post-silicon validation time frame [Gu-12]. Therefore, CAD research directions are needed for reducing validation time/cost and improving validation accuracy/confidence [Keshava-10].

Within the computer server segment, there are conditions that further increase system complexities. These include nonflexible form factors, which implies that the channel physical designs remain unchanged. Therefore, PHY tuning based on EQ techniques are used to cancel any undesired effect [Rangel-Patiño-16]. The current industrial practices to perform PHY tuning consist of an exhaustive enumeration method, turning them into the most time-consuming processes in post-silicon validation [Rangel-Patiño-17b].

This doctoral dissertation presents several optimization techniques based on novel objective functions to optimize the Tx and Rx equalizers in a server post-silicon validation platform. This doctoral dissertation is organized as follows.

In Chapter 1, a description of post-silicon validation is provided; the convergence between post-silicon and pre-silicon is discussed along with key challenges in post-silicon HSIO validation. Some opportunities to overcome the current post-silicon challenges are discussed and potential solutions to improve efficiency and quality of HSIO validation are proposed.

Chapter 2 makes a review of basic concepts on equalization, as well as a review of some of the most popular Tx and Rx equalizer topologies in HSIO links is realized. The ISI phenomenon and its impact on HISO links is explained, and the concept of equalization is outlined.

Chapter 3 is devoted to HSIO links testing, at both chip and system levels, by using a design-for-testability (DFT) approach for the emerging equalization and compensation circuits used in modern I/O links, known as system marginality validation (SMV).

In Chapter 4, a holistic optimization approach is described, that merges system margining and jitter tolerance measurements to optimize the Rx analog circuitry during industrial post-silicon

validation. The methodology concurrently optimizes Rx system margins and jitter tolerance (JTOL), by defining an objective function that combines both type of measurements, and by using a Kriging surrogate-based modeling approach to efficiently perform optimization.

In Chapter 5, an efficient optimization methodology is proposed to find out the optimal coefficients for a reconfigurable finite impulse response (FIR) filter used for the Tx of an Ethernet interface. The procedure implies developing an effective objective function and by using direct numerical optimization in a post-silicon validation platform.

In Chapter 6, a new optimization methodology is proposed to find out the optimal subset of coefficients for the Tx and Rx in a PCIe equalization process. The procedure implies defining an effective objective function, and then applying a direct numerical optimization method using lab measurements in a post-silicon validation platform. To overcome the problem of multiple local minima in the measurement-based objective function, an efficient combination of pattern search and Nelder-Mead methods is employed.

In Chapter 7, coarse surrogate models of an HSIO link are developed based on actual measurements of a server post-silicon validation platform. Several surrogate modeling techniques combined with different design of experiments (DoE) approaches are compared to find the best coarse model. A metamodeling approach is also proposed, based on ANN, to efficiently simulate the silicon equalizer Rx circuitry. The model is generated by using a frugal set of training data exploiting several DoE approaches to reduce the number of test cases.

In Chapter 8, the Broyden-based input space mapping algorithm is exploited to efficiently optimize the PHY tuning Rx equalizer settings for an HSIO interface. A good-enough surrogate model is used as the coarse model, and a post-silicon validation physical platform as the fine model. A map between the coarse and the fine model Rx equalizer settings is built, yielding an accelerated SM-based optimization of the PHY tuning process.

In the General Conclusions, the most relevant remarks about this doctoral dissertation are summarized, discussing the overall results of the proposed optimization techniques and the novel objective functions to optimize the Tx and Rx equalizers in a server validation platform. Some opportunities for future research are briefly outlined.

Finally, Appendix A shows the reference list of the thirteen internal research reports developed during the doctoral studies, and Appendix B shows the list of papers published during this same period of time.

1. Post-Silicon Validation

There is an increasingly higher number of analog/mixed signal circuits in microprocessors and in Systems on Chip (SoC). A significant portion of those mixed-signal circuits are HSIO links. Improvements in signaling methods, circuits and process technology have allowed HSIO data rates to scale beyond 10 Gb/s over several legacy channels. It is evident that challenges of post-silicon validation are continuously increasing, along with a big pressure of maintaining aggressive launch schedules. With all these elements, post-silicon validation of HSIO links is hard and time-consuming, and can be critical for making a product release qualification decision. Therefore, in order to overcome these challenges, new post-silicon approaches are required. In this chapter, a description of post-silicon validation is provided; the convergence between post-silicon and pre-silicon is discussed along with key challenges in post-silicon HSIO validation. Some opportunities to overcome the current post-silicon challenges are discussed and potential solutions to improve efficiency and quality of HSIO validation are proposed.

1.1. Introduction

Complexity of new embedded systems has grown to an amazing level. Today's most advanced processors and SoC incorporate millions of transistors, and must be compatible with dozens of operating systems, hundreds of platform components and thousands of hardware devices and software applications. To ensure leading performance, reliability and compatibility in this complex environment, companies like Intel invests over hundreds of millions of dollars annually in component and platform validation [INTEL-03].

This internal processor complexity creates a huge number of possible test sequences, and this complexity is just one parameter to assess the validation challenges. Each component will be used in an enormous variety of platform configurations, and it will have to interoperate with many different motherboards, components, peripherals, operating systems and applications. It will also face various extremes of temperature, voltage and clock frequency. This variability of configurations and operating environments increases extremely the number of tests.

The combined effects of increased product complexity, performance requirements and

time-to-market (TTM) commitments have added tremendous pressure on validation, which is usually the last step prior to volume manufacturing. This challenges the validation teams to continuously assess their methods and processes, and look for opportunities to make validation faster and cheaper [Keshava-10].

The interfaces coming out from the new microprocessors, SoC and chipsets are now a lot faster, and there are many more of them. Additionally, the increase in the number of cores and threads and the inclusion of advanced power management and virtualization drive additional complexity, as well as new boundary conditions and bus requirements. Therefore, post-silicon validation is undertaking fundamental transformations, from radically changing environmental conditions [Keshava-09], [Patra-07], [Tiruvallur-09].

Post-silicon validation of a microprocessor is performed at various so called disciplines, including System Validation (SV), Compatibility Validation (CV), and Electrical Validation (EV) [INTEL-03], [Keshava-10], [Shkolnitsky-10]. Different types of validation focus on different specifications and execute in parallel. Finally, the post-silicon validation purpose is to qualify a product over all process corners and operating conditions. At the end of post-silicon validation process, a Product Release Qualification (PRQ) decision is made based on the validation results according to the risk assessment of how many systems may fail specifications.

Among post-silicon validation disciplines, EV focuses on validating electrical parameters/behaviors, including those of I/O links, phase-locked loop (PLLs), power grid, clock network, analog/mixed-signal circuits, training algorithms optimization and PHY tuning knob settings. As an increasing number of HSIO interfaces are integrated on die, a large portion of EV is devoted to the validation of HSIO to include PCIe, SATA, USB and Ethernet interfaces.

The goal of post-silicon EV I/O validation is to predict from a small set of experiments, the distribution of HSIO performances in high volume and under various operating conditions. This goal itself poses the greatest challenge for I/O validation since in practice only a limited number of experiments is finished within the post-silicon validation time-frame. On top of that, complexity in EV is aggravated by the need to compensate for circuit non-idealities to reach the increasing speeds. These non-idealities include: process variability, noise, non-linear circuit behavior, the need to accommodate other components, etc. This complexity translates to increased compensation and adaptation loops. These circuits require Design-For-x (DFx) and programmability which need to be validated in the context of the entire usage space. In addition, with SoC, many components

and power management solutions are added that create uncertainty on the die and on the platform. To overcome these problems, some areas of improvement have been identified [Gu-12]:

a) Develop coverage metrics for I/O validation.
b) Develop specialized data mining and analysis techniques to discover correlations among various sources of data, which can be used to increase validation efficiency.
c) Maximize the usage of simulation and bridge the gap between simulation and validation results.

In this chapter, some key challenges in post-silicon validation of high-speed I/O links are presented and potential solutions to improve efficiency and quality of HSIO validation are reviewed.

1.2. Silicon Validation

The complexities of modern microprocessors have turned the validation of these components into an enormous task [Wile-05]. Silicon validation involves tens or hundreds of person-years and requires the computing power of large number of workstations. But even with all this effort, it is practically impossible to detect and fix all silicon bugs in the design before it tapes-out. Actually, statistics show that almost 50% of chips may require additional unplanned tape-outs because of functional bugs. Moreover, project plans may call for several planned tape-outs changes at intermediate stages before the final release of the silicon [Adir-11].

1.2.1 Pre-Silicon and Post-Silicon

Silicon validation techniques may be generally classified as pre-silicon and post-silicon. Pre-silicon validation refers to all of the validation activities performed before the first silicon is available. During the pre-silicon stage, the devices are tested in a virtual environment with complex simulation, emulation, and formal verification tools. However, the testing is done at the circuit level, not extending to the system-level. Therefore, after the first silicon is ready, post-silicon validation is done in a system environment looking for bugs missed in pre-silicon validation [Rotithor-00]. Post-silicon validation has been used for many years, and it can be attributed with the findings of many silicon bugs that escaped from pre-silicon validation. However, in general,

functional verification methodology for pre-silicon is still more mature than for post-silicon. Very few publications on post-silicon verification methodologies are available, and most research has centered on on-line checking and debugging capabilities of the validation platforms [Abramovici-06], [Chen-08], [Chang-07], [De Paula-08], [Wagner-08].

The objective of post-silicon validation is to ensure that the silicon design works properly under actual operating conditions while executing actual software, identifying and fixing bugs that may have been missed during pre-silicon validation. Therefore, post-silicon validation involves operating hundreds of manufactured silicon samples in actual customer application environments to validate a correct behavior over specified operating conditions. Due to the complexities of modern microprocessors, post-silicon validation is becoming significantly difficult and prohibitively expensive because existing techniques cannot manage with the total complexity of those systems [Abramovici-06], [Patra-07], [Yerramilli-06]. Post-silicon validation involves four major steps [Mitra-10]:

a) Detecting a problem by running a stress environmental test sequence to end-user applications.
b) Isolating the problem to a small region from the system failure.
c) Identifying the root cause of the problem.
d) Fixing or patching the problem, circuit editing or, as a last option, re-design.

Post-silicon validation has significant overlap with pre-silicon validation and high volume manufacturing (HVM) testing. Traditionally, most design bugs are detected during pre-silicon validation, and manufacturing defects are targeted by HVM testing. While both HVM testing and pre-silicon validation continue to be critical, post-silicon validation is becoming extremely important because of several unique aspects [Mitra-10]:

a) Silicon health cannot just rely on pre-silicon validation to detect all design bugs. Circuit simulation is several orders of magnitude slower than actual silicon and then unacceptable under the new TTM challenges.
b) A silicon part will see more events in its first few minutes of power-up than it has in its entire prior existence in simulation and emulation.
c) Modern microprocessor designs are so large and complex that it is virtually impossible for any individual to know every aspect of the design, or even of a large circuit block.
d) Several interactions between a design and the electrical state of a system are becoming

significant, e.g., signal integrity (cross-talk and power-supply noise), thermal effects, and process variations. Such interactions can result in incorrect behavior (electrical bugs). Accurate modeling of all these electrical phenomenon is usually very difficult during pre-silicon validation.

e) It may be very difficult to create accurate and effective fault models for bugs may be caused by subtle interactions between a design and physical effects (electrical bugs) or by design errors (logic bugs).

f) Unlike manufacturing testing, where the primary objective is to detect defects, post-silicon validation involves localizing, root causing and fixing bugs. Bug localization generally dominates post-silicon validation effort and costs [Josephson-06]. Moreover, unlike defect diagnosis which targets manufacturing yield improvement, the presence of one or more bugs may prevent detection of errors caused by other bugs. Such bugs are also referred to as blocking bugs because they may slow down the design or validation cycle [Anis-08], [Keshava-10].

1.2.2 Post-Silicon Validation Disciplines

As mentioned before, the disciplines of post-silicon validation include SV, CV, and EV [Bentley-01], [INTEL-03]. SV is typically performed on custom validation boards using specially written tests. These boards are usually larger than commercial boards because they provide room for additional connections to probing, measurement, and debug tools, and allow interchangeability of components. The tests run the range of operating system (OS) level programs and random instruction tests, down to hardware-coded patterns and built-in self-tests. The tool sets involved in SV are quite different from that in the pre-silicon world and rely heavily on in-target probes, logic analyzers, hardware accelerators, and tools using system management interrupts to bound the problem and reproduce it in a simulation environment [Silas-03]. Tests include focused tests to stress one aspect of the die, random instruction tests, or even OS-level applications. In CV, silicon is tested using commercially available operating systems and applications with a focus on ensuring backward compatibility with existing software, and running additional tests in an environment more resembling the end user's own platform and applications. EV focuses on validating the part from an electrical perspective, analyzing its inherent performance and margin, and on its electrical

interaction with other components on the board. Tests here range from commercial applications, to specific patterns that stress the various components and platform interconnections. Speed-paths are usually confronted by a separate step in the overall validation, using both platform and high-speed testers [Gray-08]. While testers provide very good controllability of the voltage and temperature environment, they may not duplicate the environment of a real system and may produce optimistic results. Platform-level tests enable to reproduce this environment better, and even provide patterns for future high-volume tests [Keshava-10].

1.2.3 Post-Silicon Electrical Validation

The goal of post-silicon EV is to exercise the electrical characteristics of the system, components, and platform to ensure adequate electrical margin under worst-case operating conditions. The EV is performed with respect to various specification and platform requirements, and must cover the entire spectrum of operating conditions. The process starts from sampling the system response by using few sample parts, then identify the operating conditions under which the electrical behavior does not meet the specifications, and finally to optimize, redesign, and/or tuning the circuits as necessary to fix the problem. The ultimate goal is to statistically predict the I/O electrical behavior in a real system environment across different process corners and operating conditions – such a prediction leads to a reasonable PRQ decision which requires the average defect to be low, typically less than 50 parts per million.

For HSIO links, a major performance metric is the bit-error rate (BER). Besides, there are separated specifications for the Tx and the Rx, as well as specifications for the PHY circuit tuning knobs. The specifications are defined at different levels of granularity, and accordingly, the validation test setup and focus are different for different specifications.

1.3. System Marginality Validation – The SMV Concept

SMV [Gambill-08], [Shkolnitsky-10] is the most important electrical validation for I/O links. It measures Rx eye margins in a real system/platform environment, i.e., device-under-test (DUT) with a real board and add-in cards (usually in loop-back mode), such as graphics cards or dual in-line memory modules (DIMMs). The BER is then estimated from the margin

measurements. Such tests reflect I/O performance in systems similar to those of end users. Therefore, SMV results are the most important for making the PRQ decision. Note that the eye margining process is usually done using on-die hooks, rather than manual oscilloscope probing. Hence, SMV is semi-automatic, and is of relatively low cost as compared to other tests. However, due to time and resource constraints, only a very small portion of dies, configurations and operating conditions are validated in practice, and the prediction is made based on these measurements as well as on empirical experience [Gu-12].

SMV is based on sending data traffic through the DUT link, while monitoring reception errors which are predefined beforehand. This step is called "nominal position testing". The next step is to sweep predefined electrical knobs/hooks, in order to check the system's stability. These knobs are called margin parameters, and are usually designed for test (DFT) features. Additional stress tests, e.g., power, can be defined to run simultaneously on the DUT.

Some examples of swept margin parameters are:

a) Signal amplitude.
b) Timing parameters of the Rx circuit.
c) I/O buffer impedance.
d) I/O buffer voltage references.
e) Voltage supply level.
f) Temperature of the chips.

Errors are checked at each margin parameter setting. The resulting pass/fail matrix gives an engineer the solution space in which the system can operate without fault. By using the SMV method, worst case patterns can be identified.

A useful representation of the SMV results is a functional eye, also known as data-eye. It is a two-dimensional chart, where each axis represents a different margin parameter. An example of a functional eye can be seen in Fig. 1.1. When a test uses a single margin parameter, it is called one-dimensional test.

SMV is an approach used by engineers to indicate a system's health and stability, which, in turn, can be used to determine whether or not a product should be transferred into HVM phase.

The production yield will eventually reflect the quality and robustness of the design. In

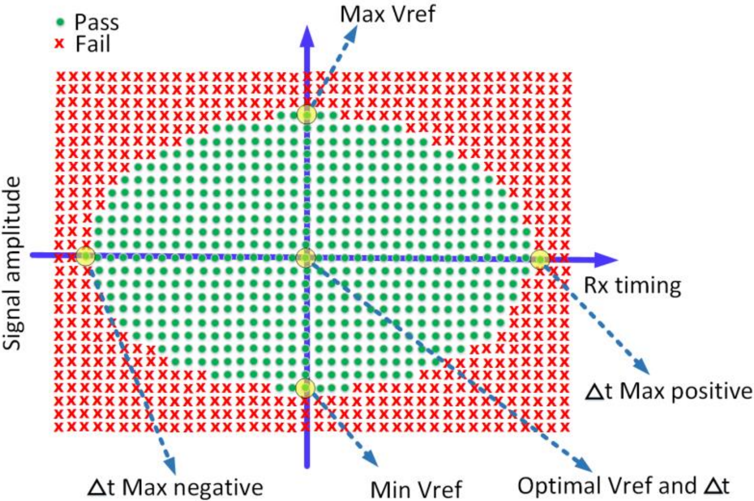


Fig. 1.1 Example of SMV functional eye diagram.

case of multiple failures or low SMV margin, an in-depth investigation has to be started to find the root cause. For example, this can be done by means of electrical probing and verifying that the electrical parameters meet their specifications. By testing a small number of DUTs, and using statistical techniques such as design of experiments (DoE), it is possible to make an estimation of the yield in the mass production phase. By using this methodology, design defects can be corrected before entering HVM.

1.4. Post-Silicon Validation Challenges

1.4.1 Silicon Development

If a problem is found in silicon that requires redesign and a silicon respin, several months to a year will be lost for next delivery. Given the current TTM aggressive schedules, waiting for silicon to check for problems is clearly a failing economic approach, even before considering the expense associated with testing silicon [Goodenough-10].

1.4.2 Time-to-Qualification

Qualification of the product is a judgment of product readiness at the end of validation, as illustrated in Fig. 1.2 at the PRQ milestone. While several coverage metrics have been developed

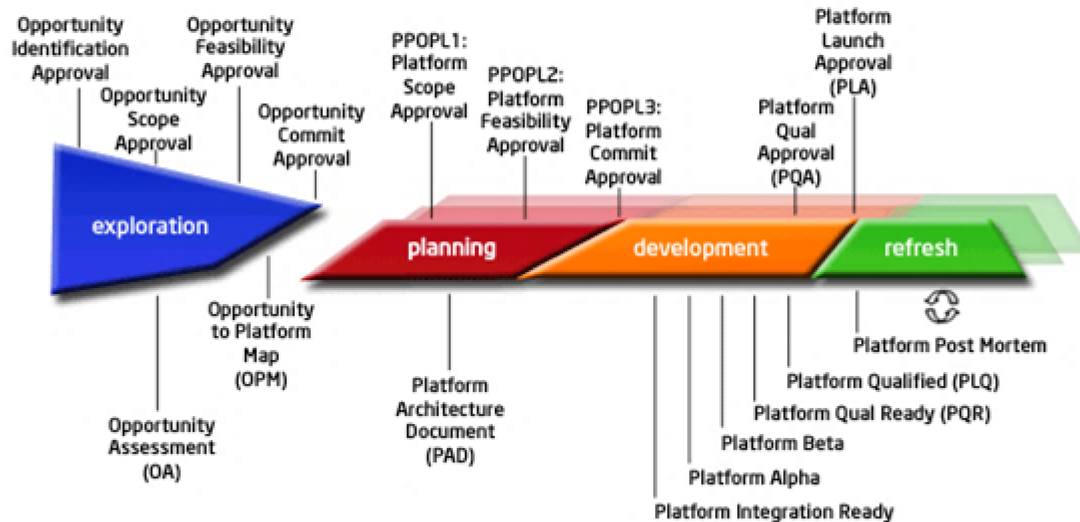


Fig. 1.2 Design and validation product lifecycle. Figure taken from [INTEL-03].

[Bojan-07], [Tasiran-01], their application to qualify a product relies on heuristic formulae involving the number of features, events, and states exercised, with an emphasis on newly introduced features and risky designs. Other metrics rely on the rate of bugs being found, and usually indicate a product readiness when a period of time passes without finding new issues [Bentley-01]. These traditional metrics are hard to obtain in post-silicon, as platform tests are often redundant and it is hard to observe the internal states of the machine. Furthermore, they require a historical perspective, subjective assessment, and a lot of expertise to convert them into a useful risk assessment which provides confidence in the goodness of a design. As a consequence, validation efforts tend to be overly conservative to minimize the risk of a bug escaping to the field.

Validation time also depends on the quality of the initial design [Bentley-01]. With the increase of design complexity, the simultaneous development of the product, the manufacturing technology, and the system boards, it is often the case that several product steppings are needed to eliminate all blocking bugs and achieve the level of performance required for the product. These steppings are quite costly to the validation as they imply dead time while bugs are fixed in the design and new masks are being manufactured.

The nature and impact of bugs is also changing with the designs [Gray-08], [Patra-07]. The increased complexity of analog and mixed-signal circuits necessary to meet challenging performance and interconnection targets also requires special flows to validate these circuits in the context of their digital control and platform environment. The scope of silicon mixed-signal

validation is greatly augmented by silicon process variation as well as by voltage and temperature fluctuations. The complexity of verifying the electrical performance and its impact at the platform level in pre-silicon is a strong limiter, and renders the bugs that are found harder to debug due to the lack of system-level accurate electric simulation.

With all these effects becoming more pronounced with every new generation of products, it is imperative that validation tools and methodologies stay ahead to manage the added requirements.

1.4.3 Limited Number of Tests

The fundamental question to be answered in validation is whether the I/O link works over all process corners, configurations and operating conditions. However, there are simply too many corner cases to be covered during the post-silicon time frame. A few common corners have been categorized to be considered in HSIO validation, as follows [Gu-12]:

a) Parametric variations, such as process variation, different types of packages, board impedance, trace length, variations of third-party cards and DIMMs.
b) Environmental variations, such as voltage supply, temperature, clock jitter, cross-talk.
c) Input stimuli variations, such as input pattern, frequency, magnitude.
d) System configurations, such as number of DIMMs, different combinations of DIMMs from different vendors.
e) Tuning knobs, such as Tx and Rx equalization coefficients.

It is obvious that there is a multi-dimensional space to sample, and in practice, it is impossible to perform tests on every die and under every configuration. Instead, only a few dies are selected to represent millions of dies, and only a few corner cases (in terms of process, voltage, temperature, DIMM configuration, etc.) are selected to perform tests and measurements. Moreover, for some hard to validate corners (such as humidity, trace length, etc.), usually due to SMV margin specifications, this implies a possible over-pessimistic validation. Over-validation, just like over-design, increases the cost of a new design. Given the limited number and kind of measurements, the prediction/projection of I/O link performance distribution in high volume is a hard problem.

1.4.4 Limited Parts

EV looks to mimic a real system environment, including the DUT, board and devices (third-party cards). However, either of these components might be unavailable at the time of post-silicon validation, due to various practical reasons like limited silicon samples due to new process technology, validation platforms with different trace lengths, devices available only in the late stage of post-silicon validation, etc.

1.4.5 Complex Interaction with Surrounding Circuits

Power supply noise, clock jitter and link training algorithms/finite-state-machines directly affect the eye diagram margins. Therefore, when a bit error is observed, it is sometimes hard to tell whether the error is caused by the I/O interface at DUT or the I/O interface at a third-party card. Such complex interactions make it hard to root-cause a bug in I/O validation. On the one hand, the bug might be caused by software/algorithm, power supply noise, cross-talk, third-party cards, etc., and therefore it usually requires different validation teams to review the bug sighting together and brainstorm root causes and fixes. On the other hand, in rare cases where there is a circuit bug in the I/O link, it is needed to reproduce the bug in a debugging or simulation environment. However, the bug might not be excited in the debugging environment, due to interactions with boards and oscilloscope probes.

1.4.6 Failure Reproduction

Many electrical bugs are very hard to reproduce. The problem of bug reproduction is aggravated by the presence of asynchronous I/Os, and multiple clock domains. Techniques to make failures reproducible [Heath-04], [Sarangi-06], [Silas-03] are often intrusive to system operation, and may not expose bugs.

1.4.7 System-Level Simulation

Running system-level simulation can be 7-8 orders of magnitude slower than actual silicon.

Moreover, expensive external logic analyzers are required to record all signals that enter and exit the system through external connectors [Silas-03]. Therefore, a functional bug typically takes hours to days to be localized vs. electrical bugs that require days to weeks and more expensive equipment [Josephson-01].

1.4.8 Post-Silicon Tuning

As process technologies scale down, traditional circuit design methodologies are challenged by the problem of silicon process variation. Different techniques exist to maximize the parametric yield based on statistical design for analog circuits, and these techniques usually fall into two categories: design-time optimization and post-silicon tuning [Yao-09].

Design-time optimization techniques explore the design space at system-level and device-level to maximize the yield for analog circuits. However, accurate simulations for non-linear circuits, which are dominant in digital CMOS circuits, are computationally very expensive given the complexity of the system involved. Transistors are coupled with the IC interconnects, whose electrical properties cannot be ignored in deep submicron design [Wang-03]. On the other hand, post-silicon tuning in analog design has been widely adopted to confront the silicon process variation [Rangel-Patiño-17b]. Tunable elements are proposed to adjust the analog circuit performance after chip fabrication [H.Huang-01], [Miller-03]. These tunable elements provide a way to reconfigure I/O links in post-silicon to cancel out the effects of system channels' variability [Rangel-Patiño-16]. PHY tuning settings include: parameters of an equalizer at the Tx, Rx, or both; the clock and data recovery circuit settings; the variable gain amplifier; baud-spaced feed-forward equalizer (FFE) in the Tx, and the bias voltages or currents values, among others [Gu-12]. A typical system may have hundreds of combinations of just equalization parameter values. Finding the optimal PHY settings that guarantee the BER required by an industrial specification is called PHY tuning. In the worst case, this means sweeping all possible combinations of all PHY settings, which is prohibitive in the post-silicon validation time frame [Gu-12], [Rangel-Patiño-17b].

1.5. Post-Silicon Electrical Validation Opportunities

As seen in previous sections of this chapter, the post-silicon validation domain has certain

unique advantages and limitations over traditional pre-silicon simulation-based validation. Post silicon validation is performed at target platform speeds (in the gigahertz range) and contains the real system components. In contrast, pre-silicon validation includes limited platform level interactions and runs in the hertz or tens of hertz range. However, visibility and ability to control the system are much reduced in post-silicon validation and failure analysis requires significantly more effort [Keshava-10].

There is evidence that pre-silicon and post-silicon validation cannot achieve their goals on their own; pre-silicon, in terms of finding all the bugs before tape-out, and post-silicon, in terms of finding the bugs that escaped pre-silicon. This creates an increasing need to connect the gap between these two areas by sharing methodologies and building a bridge allowing easier integration between these areas. It is needed CAD research directions for reducing validation time/cost and improving validation accuracy/confidence [Keshava-10].

1.5.1 Bridging Pre-Silicon Verification and Post-Silicon Validation

Technologies such as formal verification, simulation acceleration and FPGA-based emulation allow covering much larger portions of the validation plans than traditional validation based on regular simulation. However, to really approach the overall verification and validation challenge holistically, a more unified verification infrastructure is needed to carry on from pre-silicon to post-silicon, but unfortunately this is where current methodology often breaks apart. In order to transform the post-silicon validation from an engineering art practiced by few experienced engineers to a technical discipline with solid foundations and methodologies, new validation approaches and CAD techniques are required.

1.5.2 Trade-off between Validation Time and Quality

As time progresses during post-silicon validation, more tests are performed and more data is collected. It should be expected that with more data a better estimate and confidence of statistics of HSIO performance in high volume should be obtained. However, in practice, there is limited time for post-silicon validation. On the other hand, at some PVT corners, there might be over-validated parts by running too many experiments. Then, it is required a trade-off or strategy to

reduce the validation time, but having the most effective experiments for validation purpose. The strategy should be to develop a coverage metric (as a function of post-silicon tests and measurements) that defines the quality of validation. Such metric can help to decide when it is "safe" to stop validation without impairing product quality, and use it as a guidance to design new experiments to maximize the coverage.

1.5.3 Integrating Multiple Sources of Data

In a product life-cycle, various data are collected at different stages. For HSIO links, there should be available simulation data (SPICE-level for individual modules, and behavioral simulation for statistical eye analysis [Balamurugan-09]), on-die test structures data that monitor process variations [Panganiban-02], tester data [K.Cheng-10], [Friedman-01], and so on. During validation, it may also read out a few key run-time parameters such as equalization coefficients.

These simulation and tests are designed by different teams for different purposes. However, it is believed that some of them may have good correlation to validation results. For example, the on-die test structure measurements characterize process variations, and may be correlated to the margins that are dominated by process impacts. To extract useful information from these data, techniques developed in the statistical learning and data mining community [Bishop-06], [Friedman-01] may be used. Applications of state-of-the-art correlation mining, classification, clustering and regression algorithms may discover useful and interesting information that are hard to be identified manually. Such correlations, once found, can greatly help increasing validation efficiency. For example, if correlation is identified between an early-stage measurement and a late-stage measurement, we may eliminate or reduce the number of late-stage tests to reduce validation time. If correlation is identified between an easy-to-measure parameter to a key circuit performance (e.g., BER), it can be used to quickly identify the problematic/worst-case dies, and more validation efforts can be spent on these "bad" dies [Gu-12].

1.5.4 Connecting Simulation with Validation

Simulation provides a means for designers to validate the design before physical implementation. However, simulation results can deviate from the post-silicon measurements to

some extent, due to inaccuracies of device models and simplifications in behavioral models. Given such gaps between simulation and post-silicon validation measurements, there is an interest in how to use simulation to help post-silicon validation, and how post-silicon validation results can be used to calibrate pre-silicon CAD models. For example, while simulation results may deviate from the post-silicon measurements, they should give a rough idea of the sensitivity with respect to various parameters, and the sensitivity information may help post-silicon optimization. As another example, simulation may be used to validate cases that are impossible or too expensive to cover in post-silicon, such as different trace lengths. However, due to the inaccuracies in simulation, special techniques might be needed to integrate them with other post-silicon measurements at other PVT corners. An example of such techniques could be Space-Mapping Optimization [Bandler-94], [Cheng-08], [Koziel-08] through a simulator and actual validation platform to obtain the optimal PHY knob settings to reduce the number of experiments at post-silicon validation. Finally, simulation results can be viewed as a prior knowledge before any post-silicon experiment is performed. Statistical inference techniques [Bishop-06] might be applied to estimate post-silicon distributions using simulation results as a prior. If simulation renders a good prior, the number of experiments may greatly reduce, while still being able to extract accurate statistics from limited measurements.

1.6. Conclusions

Over the past decade, HSIO data rates have scaled from a few hundred Mb/s to more than 10 Gb/s. This has been possible due to improvements in link architecture (e.g., point-to-point instead of multi-drop), signaling methods (e.g., transmit pre-emphasis), circuits (e.g., low noise receivers and precision clocking), and semiconductor process technology. This increased speed and complexity has required significant improvements in link modeling and analysis techniques to enable design optimization and validation. It is clear that the challenges of post-silicon validation are continuously increasing together with aggressive launch schedules. In order to overcome these challenges, new post-silicon approaches are required.

In this chapter, a detailed description of post-silicon validation was presented. The key challenges in post-silicon of HSIO links were listed. The idea of connecting simulation with validation has been discussed as a potential solution to overcome the current post-silicon

challenges to improve efficiency and quality of HSIO links validation. It is concluded that bringing CAD methodologies into post-silicon can improve validation efficiency, and one potential direction could be using space-mapping optimization concepts through a simulator and an actual validation platform to obtain the optimal knob settings, and then reducing the number of experiments required for this optimization at post-silicon electrical validation.

2. Channel Equalization for High-Speed Serial Links

A common method to mitigate the ISI in high-speed serial links consists of using a linear finite impulse response (FIR) filter as equalizer. This equalizing method can mitigate unwanted effects of the channel and improve the signal at the Rx. Advanced equalization techniques include a mix of linear feed-forward and feedback filters, called decision-feedback equalization (DFE). Equalization (EQ) at the Rx is usually preferred because of the Rx equalizer can be adapted to the channel characteristics. However, power and speed constraints in HSIO links require different EQ topologies. This chapter provides an overview of the existing EQ topologies to mitigate the ISI in HSIO links.

2.1. Introduction

New high speeds on digital communication have led to higher attenuation, reflections, and undesired coupling. HSIO links through a backplane now reach the bandwidth limitations of the physical interconnects [TEKTRONIX-14], [M.Li-07]. Fig. 2.1 shows a diagram of a typical backplane, where the Tx sends a signal to the Rx, and the ideal objective is to deliver an error-free electrical signal at the highest data rate possible. However, the signal must go through several discontinuities from Tx to Rx (i.e. I/O card traces, I/O card connectors, backplane traces, etc.), causing significant distortions to the original signal [ALTERA-13].

At sufficiently high data rates, signal degradation through the channel will simply close the eye diagram. To solve the problem of signal degradation through a backplane or other high-speed interconnects, modern Rx designs use a circuit compensator called equalizer, for compensating or reducing mainly the ISI in the received signal. Various EQ topologies have been developed. They aim at exploiting the inverse response of the channel to flatten out the overall frequency response.

The EQ can be implemented either in the Tx or in the Rx. The Tx equalizer implementation is relatively easier than the Rx equalizer because the required FIR filter deals with the digital data

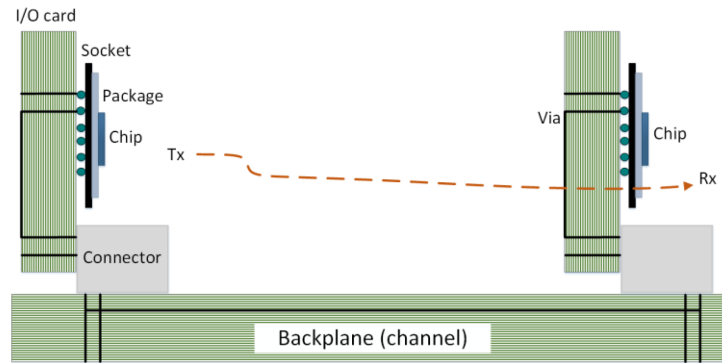


Fig. 2.1 Diagram of a typical backplane communication between two chips.

at the Tx, rather than the received analog data at the Rx, however, the channel information may not available at the Tx. Therefore, several adaptive algorithms have also been developed to adjust the overall response depending on the channel characteristics when they are unknown in advance or they are time variant. There are many types of signal conditioning, or compensation/equalization techniques, each of which has their own advantages and disadvantages, and they may be combined based on the design application.

In this chapter, basic concepts on equalization are revisited and a review of some of the most popular EQ topologies in HSIO links is realized. It is organized as follows. The ISI phenomenon and its impact on HISO links is explained in Section 2.2. The concept of equalization is outlined in Section 2.3. Tx and Rx equalizer topologies are discussed in Sections 2.4 and 2.5, respectively. Section 2.6 discusses the adapting equalizers, and finally, conclusion are given in Section 2.7.

2.2. Inter-Symbol Interference (ISI)

Among the different types of distortions in the HSIO links, the ISI is a phenomenon that causes a high data loss in the communication link. When transmitting data across the channel, typically the data from the Tx will be in a square waveform representing 1's and 0's, but when this square waveform mixes with the noise and is deformed due to other non-idealities in the channel, the waveform spreads out and merges with the adjacent symbol sequence, causing the data at the Rx to be unreadable. In this context, a symbol is defined as a state or significant condition of the communication channel that persists for a fixed period of time. Hence, the effects of the past and future symbols on the current symbol is the ISI. Pre-cursor ISI is caused by the past symbol and

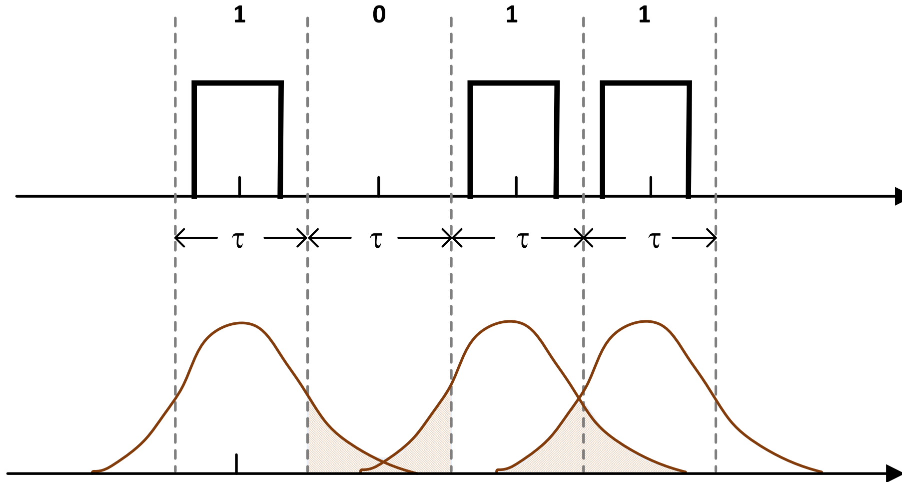


Fig. 2.2 Inter-symbol interference effect.

post-cursor ISI is caused by the future symbol. This phenomenon is not desirable because it distorts the signal, decreasing the reliability of the communication link by increasing the overall bit error rate. ISI increases with channel loss and can completely close the received data eye diagram. Fig. 2.2 shows a graphical representation of ISI.

2.3. Equalization Concept

The objective of an equalizer is basically to compensate for any signal distortions or any general losses caused by the channel characteristics. The transmission medium is a linear system, which corresponds to some transfer function in the frequency domain. A basic linear equalizer ideally reproduces the inverse of such a transfer function:

$$T_E(f) = \frac{1}{C(f)} = \frac{1}{|C(f)|} e^{-j\theta_C(f)} \tag{2-1}$$

where $C(f)$ contains the channel characteristics as a transfer function in frequency domain, $\theta_C(f)$ is the corresponding channel phase response, $T_E(f)$ is the equalizer transfer function, and f is the operating frequency (Hz). Ideally, the amplitude response of the equalizer is $|T_E(f)| = 1/|C(f)|$ and its phase response is $\theta_E(f) = -\theta_C(f)$. If the equalizer transfer function is equal to the inverse form of the channel transfer function, the equalizer completely eliminates ISI and other distortions caused by the channel.

An effective EQ technique compensates for the frequency-dependent channel loss

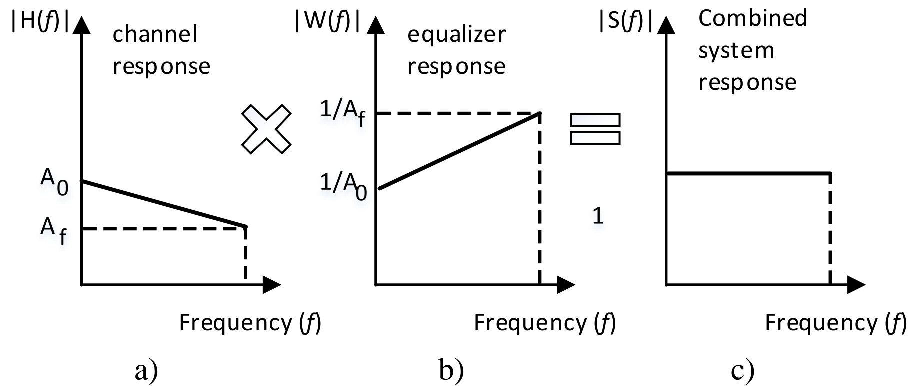


Fig. 2.3 Basic idea of equalization: the equalizer frequency response approximates the inverse of the channel frequency response to flatten out the overall response. a) channel response, b) equalizer response, c) equalized response.

characteristics as illustrated in Fig. 2.3. The band-limited channel typically has a low-pass frequency response as shown in Fig. 2.3a, with larger losses at high-frequencies than those in the low-frequency range. Fig. 2.3b shows how the frequency response of the equalizer has larger gain at high frequencies than at low frequencies. After EQ, the combined frequency response becomes flat through the desired frequency range, as shown in Fig. 2.3c. This new combined transfer function ideally has a unitary gain over the complete frequency band of interest.

The traditional physics-based methods to solve the HSIO links issues, such as replacing the channel with low-loss material, incorporating repeaters in the channel, reducing the transitions and discontinuities, or reducing the channel length, can be also very effective but they are usually much more expensive and cumbersome to implement. In contrast, EQ is a well-established system approach technique used to overcome many non-idealities introduced by the channel. A conceptual diagram illustrating the way of performing EQ is shown in Fig. 2.4. In summary, EQ is used to improve the received signal to get the system achieving a lower bit error rate.

Since the assumption is a linear system, the signal conditioning performed by the equalization process can be applied before or after the channel. In the case the equalizer is placed at the Tx, the signal is pre-distorted, thus, after it goes through the channel, the resulting signal is recovered at the Rx. This type of signal conditioning is called "emphasis," and there are two types: pre-emphasis [Dally-97], [Farjad-Rad-99] if it pre-shapes the transmitted data increasing the high-frequency components, or de-emphasis if it reduces the power of low-frequency components [Fiedler-97], [Foley-01]. Therefore, it is important to choose the right EQ method from the variety of available topologies and signal-conditioning techniques. Equalizing filters can be implemented

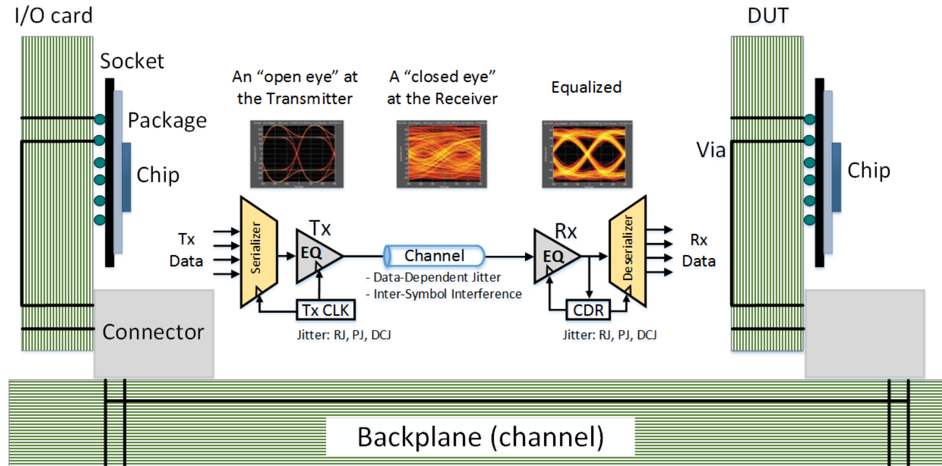


Fig. 2.4 Graphical concept of the EQ process.

in discrete-time or continuous-time at the Tx and/or Rx. Discrete-time implementations include transmit pre-emphasis, Rx Linear Equalizer and Rx DFE, while continuous-time implementations include Rx Continuous Time Linear Equalizer (CTLE), and passive elements in Tx/Rx termination network.

2.4. Equalization at the Transmitter

Tx pre-emphasis/de-emphasis is implemented at the Tx driver by pre-conditioning the signal before sending it through the channel. In this way, the high-frequency content of the signal is amplified (pre-emphasis) or the low-frequency content of the signal is reduced. The current and the past values of the received signal are linearly weighted with equalizer coefficients and combined to produce the output. This type of equalizer, which is also called FIR, compensates for ISI with adjustable tap-coefficients, as shown in Fig. 2.5. It consists of a delay line, gain cells, and a summing node. The transfer function of the equalizer is expressed by

$$y(t)=\sum_{i=0}^{n} A_i x(t-i\tau) \tag{2-2}$$

where y is the Tx output in time domain (t), x is the data input to the equalizer, A is the weight

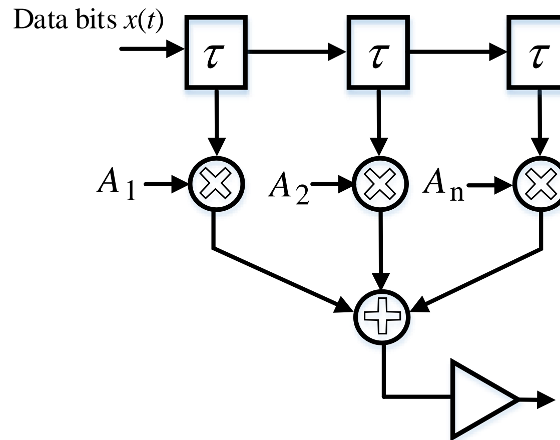


Fig. 2.5 Transmit pre-emphasis FIR filter.

from the gain cells, and τ is the delay of one delay cell. Tx equalizer can also be a de-emphasis filter, which reduces the power of low-frequency components. The simplest way consists of increasing the signal amplitude at each transition edge and reducing the signal amplitude when there is no transition.

Equalization using FIR filter is easier to implement at the Tx, however, there are several limitations to this approach:

a) Due to the signal attenuation, Tx pre-emphasis cannot improve the signal-to-noise ratio (SNR).
b) Tx pre-emphasis may even increase the amount of crosstalk in the system, because the signal is preconditioned on the Tx to have an excessive amount of high-frequency content [Zerbe-01].
c) High-resolution digital to analog converters (DAC) are required to implement pre-emphasis filters to equalize channels containing a large number of ISI terms [Zerbe-03].
d) Finally, even though the Tx pre-emphasis, there is even a considerable residual ISI, which results in reduction of both timing and voltage margins, particularly at higher data rates.

Both Tx and Rx implementations have some problems: peak power constraint in the Tx equalizer, and several non-idealities, such as limited bandwidth, noise enhancement, amplifier nonlinearity, in the Rx equalizer. By using both Tx and Rx implementations together, some of the problems can be alleviated.

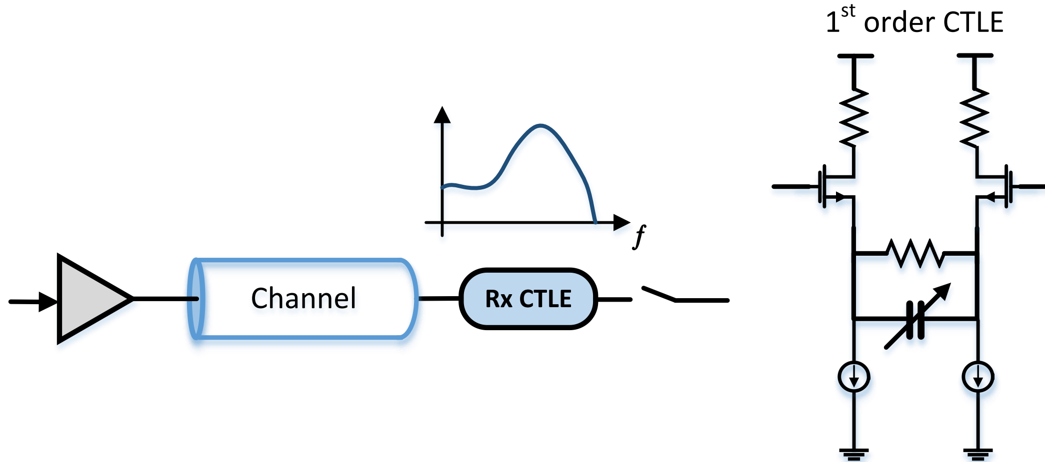


Fig. 2.6 Continuous time linear equalizer and typical transfer function.

2.5. Equalization at the Receiver

The EQ topologies at the Rx can be divided into two categories: 1) discrete-time EQ and 2) continuous-time EQ. A discrete-time equalizer, which is based on the FIR filter, can take advantage of various digital adaptive algorithms. However, because EQ is based on the samples captured by the Rx's recovered clock, there exists a cross-dependence between the equalizer and the clock recovery circuit. As the data rate increases, the power consumption would increase dramatically due to the large number of taps implemented in this EQ topology. On the other hand, a continuous-time equalizer does not require a sampling clock, and thus the equalizer would work independent of the clock recovery circuit. Therefore, a continuous-time equalizer at Rx offers a method to mitigate ISI without any peak power constraint. The loss in the channel is suppressed by boosting the high-frequency signal spectrum rather than attenuating the low-frequency content. The different Rx equalizer topologies are now described.

2.5.1 Continuous Time Linear Equalizer (CTLE)

A CTLE is a simple one tap continuous-time circuit with high-frequency gain boosting, whose transfer function can flatten the channel response. The topology is basically a simple RC network, as shown in Fig. 2.6. The differential-pair emitter resistor attenuates the low-frequency

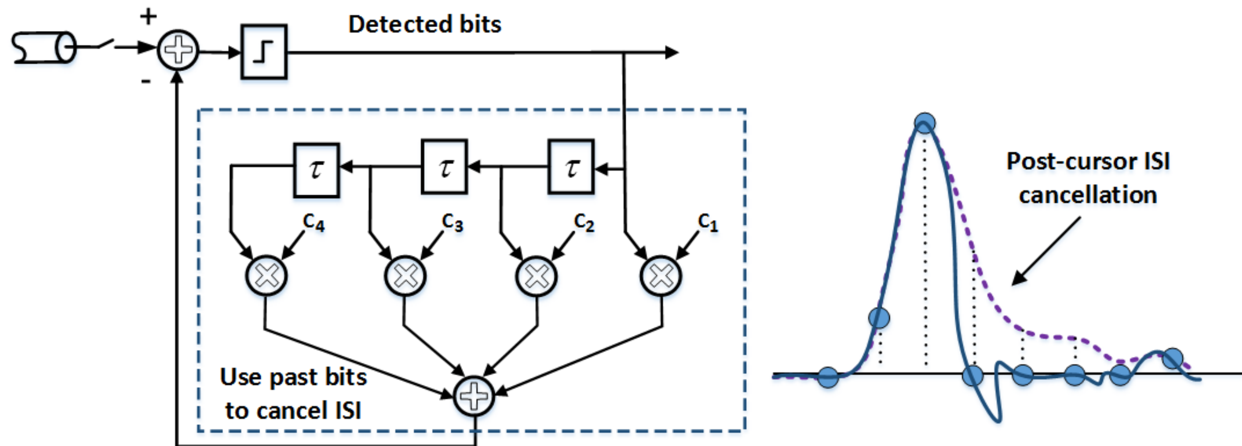


Fig. 2.7 Decision feedback equalizer.

signals while the capacitor allows the high-frequency signal content, thus resulting in high frequency gain boosting.

Similar to Tx pre-emphasis, the CTLE addresses pre-cursor and post-cursor ISI but in continuous time instead being limited to a pre-set number of Tx taps. This simple topology has a very low power consumption rate, and many equalizer stages can be added not only to increase the order of the resulting equalizer but also to increase the maximum boost achieved in a given frequency interval.

In a system with a CTLE topology, the crosstalk is not increased as it occurs with Tx emphasis, because of the reduced high frequency content at the Tx drive. The CTLE topology is well suited for real-time adaptation, since the signal information after the channel is readily available for processing and reconditioning at Rx.

There are two main disadvantages with simple passive RC equalizers. First, the RC network induce large impedance discontinuity at the channel and equalizer interface. Impedance matching networks [Lee-98], often employing inductors, can be used to reduce the discontinuity. However, large inductors make this approach less suitable for on-chip integration. Second, this method cannot improve SNR, since EQ is performed by attenuating low-frequency signal spectrum, much like transmit pre-emphasis. Due to these reasons, this technique has limited usage in HSIO links.

2.5.2 Decision Feedback Equalizer (DFE)

Unlike prior EQ topologies, DFE is a nonlinear system specifically designed to avoid noise

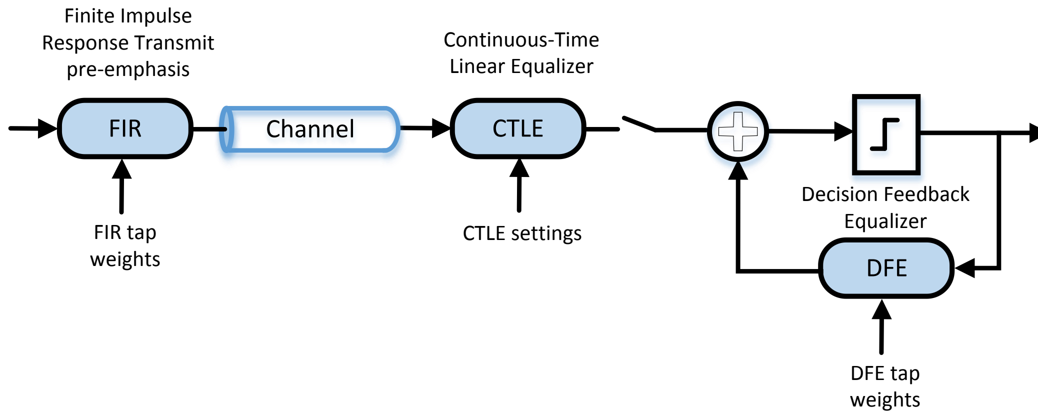


Fig. 2.8 Simultaneously employing Tx and Rx equalizers, combining different EQ topologies.

amplification. Fig. 2.7 shows the block diagram of this topology The gain-peaking transfer function of CTLE amplifies the high-frequency noise, degrading the noise margin, but this problem can be completely eliminated by using DFE [Goupil-10], [Le-02], [Sohn-03].

The major benefit of DFE is the improved immunity in the case of crosstalk. The effectiveness of ISI cancellation is based on the assumption that all previous decisions are correct, and therefore, bit errors can exacerbate ISI instead of cancelling it. This problem is referred to as error propagation. As a result, a CTLE type of EQ still is required in a DFE system to accommodate the pre-cursor ISI. But, in the case of serial links with required BER $<10^{-12}$, error propagation does not degrade the performance [Bala-04].

The DFE topology is the optimal option for systems in which noise limits the amount of EQ that can be done. However, because of the added complexity and the associated timing difficulties, the simpler feedforward equalizer should be used when the noise is not prohibitive. Some of these issues can be solved by using both Tx and Rx equalizers simultaneously, as shown in Fig. 2.8.

2.6. Algorithms for Adaptive Equalizers

In a practical transmission system, the exact characteristics of the channel are unknown and they can vary significantly. PVT conditions, properties of the material and the length of the channel, or other non-idealities in the channel can cause the channel to change its attenuation and bandwidth substantially [Hermans-06].

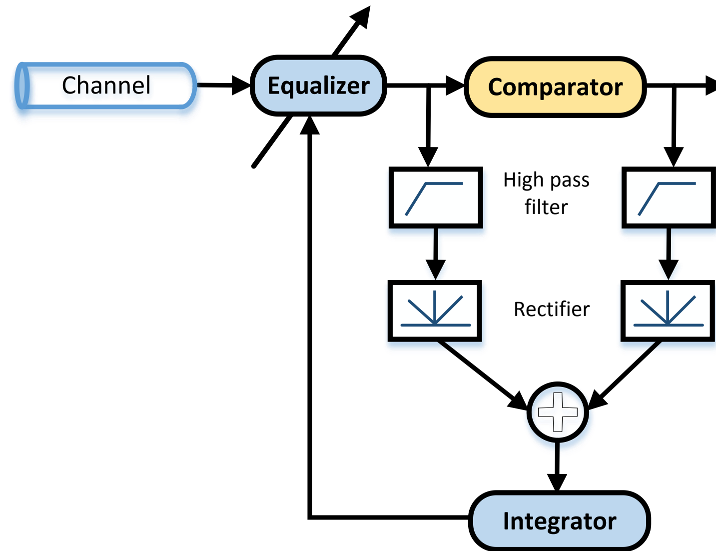


Fig. 2.9 Typical continuous-time adaptive equalizer.

Fig. 2.9 shows the architecture of a typical continuous-time adaptive equalizer (CTAE). The equalizing filter either boosts the high-frequency components or attenuates the low-frequency components of the signal at the Rx to compensate the high-frequency loss resulting from the channel. The adaptive servo loop, which adjusts the compensation gain of the equalizing filter, determines the control voltage by comparing the input and the output signals of the comparator.

There are several algorithms that can be used for adapting the equalizer. The mean-square error (MSE) calculated between the recovered signal and the training data in the time domain at sampling points [Abeysekera-05], the least mean squares (LMS) [Krall-08], and the zero forcing (ZF) [Abeysekera-05], or their variations. The LMS algorithm optimizes the filter coefficients based on minimizing the mean-squared error. It has a simple computational complexity but a slow convergence [Atef-13]. The ZF algorithm brings down the ISI to zero in a free-noise case. However, when the channel is noisy, the ZF equalizer will amplify the noise greatly [Atef-13].

2.7. Conclusions

At higher data rates, several EQ techniques can be used to compensate for jitter and noise and then maximizing the eye diagram before the Rx sampling fails to satisfy the required BER. In this chapter, an overview of the more popular existing EQ topologies to mitigate the effects of jitter and noise in HSIO links was presented. Tx pre-emphasis suffers from peak power constraints,

while Rx equalizer performance is limited by the amplifier bandwidth, therefore, design trade-offs are required between Tx and Rx implementations or a combination of both. However, many times the exact characteristics of the channel are unknown and they can change due to PVT conditions, and other non-idealities in the channel, and then techniques such as the continuous-time adaptive equalizer to adaptively determine equalizer settings are required to overcome these challenges.

3. System Marginality Validation

Over the last decades, the semiconductor manufacturing technology has advanced from 4 microns to 10 nanometers. The implied design complexity has made it almost impossible for engineers armed with legacy measurement technologies such as oscilloscopes to accurately measure the overall signal integrity on high-speed serial I/O, and then correlate this with the behavior of the system through the corner cases. In consequence, a new approach to design validation, known as SMV, has emerged and is compensating for the deficiencies of legacy methods with traditional instrumentation. SMV determines the marginality of the entire system while taking into account variations in silicon process, voltage, temperature, humidity, and other conditions. This chapter is devoted to HSIO link testing, at both chip and system levels, by using SMV as novel DFT approach for the emerging equalization and compensation circuits used in modern I/O links.

3.1. Introduction

In 1965, Gordon Moore, Intel's cofounder, predicted that the number of transistors integrated per square inch on a die would double every year [Moore-65]. In subsequent years, the pace slowed, but the number of transistors has continued to double approximately every 18 months for the past two decades. Most experts expect that Moore's law will hold for at least two more decades. Die size will continue to grow larger, but, at the same time, minimum feature size will continue to shrink.

As the manufacturing technology continues to advance, precise control of the silicon process is becoming more challenging. As the technology moves into the nanometer age and in order to keep up with Moore's law, many new nanotechnologies and circuit design techniques must be developed and adopted, all of which pose new test challenges that must be addressed concurrently. Otherwise, the cost of test would eventually surpass the cost of silicon manufacturing.

Undesired effects like jitter, ISI, crosstalk and others can create multiple problems on the signal integrity of HSIO circuits, making maximum bus speeds difficult to achieve in practice.

This problem is aggravated by the fact that channel speeds keep increasing from one generation bus technology to the next one. With each step upward to a higher speed and higher signaling frequencies, an HSIO circuit becomes more susceptible to distortions and anomalies which can effectively disrupt bus traffic and stall system throughput.

For serial I/O's interfaces like PCIe, SATA, USB, and Ethernet, the higher the frequency of the signaling, the more susceptible the interconnect becomes to errors, re-transmissions and other anomalies. To avoid potential problems with high-frequency bus traffic, the signal integrity on the bus must be validated during each of the major phases of a system's life cycle, including design, manufacturing and as an installed system in the field. Unfortunately, as the bus technology is moving to new generations, the signal integrity validation of HSIO has become more difficult due to the limitations of legacy probe-based test equipment. However, non-intrusive test methods based on embedded instrumentation are providing alternative validation solutions that are more cost-effective and deliver observed signal integrity data. These methods provide soft access to hard data. In addition, industry specifications such as the IEEE P1687 Internal Joint Test Action Group (IJTAG) standard for embedded instrumentation are emerging to simplify and streamline the adoption of signal integrity validation techniques based on embedded instruments [Caffee-12]

SMV is an innovative way of not only validating the signal integrity of a circuit board design, but also of assessing how much margin is in the design relative to silicon characteristics and processes that vary over time, including voltage, temperature, frequency, humidity, component aging and numerous other factors.

SMV has emerged as a viable means of measuring system operating margins in real world environments and in real time. Similar methodologies have been adopted by several semiconductor companies such as Intel, PLX, Altera, Xilinx, Broadcom, TI and others. This methodology has become the preferred means for measuring how much margin is in a chip design.

In this chapter, the HSIO link testing methods at both chip and system levels by using SMV as a DFT are presented. The organization of the chapter is as follows. Section 3.2 describes the specification window based on operating margin for post-silicon validation. A definition of embedded instruments is presented in Section 3.3. Loopback testing is explained in Section 3.4, and Section 3.5 describes the different types of interconnect testing and the Interconnect Built-In Self-Test which is the foundation for SMV. Functional testing by using embedded instruments is discussed in Section 3.6. Finally, conclusions are given in Section 3.7.

3.2. Operating Margin

There are two main portions of the silicon validation plan. The first one is the functional validation plan, which is usually done in systems called “platforms”, that are representative, or better yet, equivalent, to the actual system where the product will be used.

The second portion is the electrical validation plan. The intent of this second plan is to ensure that the silicon part meets the data sheet specifications, and that the device's operation is robust across frequency, voltage, temperature, and across the variation of parts coming out of the fabrication facility. Fig. 3.1 shows a simple two dimensional plot of the voltage versus frequency windows of a device. The device specification window is the range of voltages and frequencies across which the device is guaranteed to work. The characterization window is a superset of the specification window; the validation team will not consider the electrical validation complete until the device operation is clean across the entire characterization window. The difference between the two windows is the operating margin of the device. Margin accounts for any inaccuracy in the testing and characterization of the design [Gizopoulos-06].

3.3. Embedded Instruments

Historically, a variety of intrusive, probe-based test and measurement (T&M) devices and various kinds of testers have provided engineers the eye diagrams and other measurements they require to assess signal integrity. Unfortunately, this legacy test equipment is limited because of its reliance on placing a physical probe on a device or a test pad on a circuit board to extract test data without affecting the inherent performance. As signal frequencies increase on high-speed buses, placing a probe on the bus to monitor signal integrity becomes decreasingly feasible. Many designs prohibit the placement of test pads on high-speed buses because of the capacitive coupling effects that pads and probes have on the sensitive signaling. Pads and probes will introduce anomalies into the signaling at a time when operating margins on these buses are shrinking dramatically. As a result, today’s best practices in board design will typically prohibit test pads.

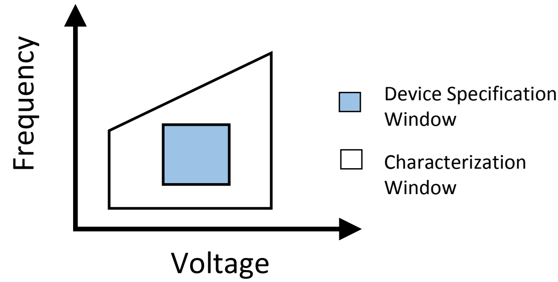


Fig. 3.1 Specification window and characterization window for electrical validation. Figure taken from [Gizopoulos-06].

Without access to the bus, intrusive probe-based testers, such as oscilloscopes or logic analyzers, cannot accurately monitor signal integrity.

Fortunately, non-intrusive tools based on instrumentation embedded in chips (embedded instruments), rather than physical probes, can be used in place of intrusive testers. Instead of extracting signaling data with the anomalies introduced by the probe and test pad, non-intrusive embedded instruments deliver the signal data that is actually seen by the receivers. In other words, soft access is provided to the hard data validation engineers by means of these embedded instruments and the tools that support them.

Several validation, test and debug instruments are being embedded into chips and re-used throughout the life cycle. These embedded instruments are typically accessed by way of standard technologies, such as the IEEE 1149.1 boundary-scan (JTAG) Test Access Port (TAP), which is present on practically all processors and many other types of digital devices.

For high-volume manufacturing test, typical testing of the I/O interfaces on an automatic test equipment (ATE) requires to match the performance of the DUT. HSIO's data rates can range from 1 GHz for parallel buses and more than 6 Gbps for serial links. ATE that meet these requirements are very expensive; in addition, test time and test programming complexities often mean delayed time-to-market. This combination can result in high product cost that may make the product noncompetitive. This becomes a problem when mass-market personal computers and consumer digital appliances increase their performance bandwidth and both high-speed parallel and serial I/O interfaces become the norm.

These trends and costs have motivated ways to test these products on mainstream test platforms with reasonable test time. There have been two trends: 1) making changes to the load-board; and 2) incorporating I/O-DFT into the design. These test methods are refer as DFT-assisted

testing in which the DFT circuits are embedded on the load-board or within the silicon itself. With this approach, no new or special equipment has to be purchased and time-to-market and product cost are better off to fit into the business requirements [Wang-08].

3.4. Loopback Testing

In the early 1990s, an I/O structural test methodology called I/O wrap [Gillis-98] was developed. More commonly called I/O loopback, this method involves applying a transition fault test methodology to I/O circuitry. By tying an output to an input, the output data are launched and latched back into the input buffer on the following clock. As most signal pads are I/O in nature, the I/O wrap (I/O loopback) methodology is convenient. Input-only or output-only pads can be connected with the DFT circuit or wires/relays present on the load-board. The main limitation of this method is that, because the delay path is tested with the clock, the delay cannot be characterized without overstressing the other peripheral circuits. This approach is limited to testing gross delay defects, and timing specifications cannot be measured. By the early 2000s, a test methodology known as AC I/O loopback testing had been proposed. This one uses the same loopback principle, but with a twist [Tripp-04]: rather than just using the clock to launch and capture the signal, the launch can be carried out by a delayed version of the clock or the capture be accomplished using an early version of the clock. By controlling the delay, the relative delay between the strobes and data can be actually measured without high precision timing measurements requirements from ATE.

Instrumentation-based testing is much more accurate than DFT-assisted loopback testing. However, it also requires special instruments to be set up, calibrated, and integrated into test platforms. The lengthy setup time, long test pattern sequence application, and data capture, which is typically followed by extensive numerical analysis, often require experienced personnel and longer testing time than would be desired in a high-volume manufacturing setting. As serial link technologies are deployed to an increasingly cost-sensitive commodity computing world, it is required to decrease testing costs.

Loopback testing has been around for as long as serial interfaces have been. However, simple loopback testing is just a simple functional test. All the required jitter and noise tests are not possible with this method, and there is no guarantee that the simple loopback test can

interoperate with other similar components in an extreme environment. Loopback also makes diagnosis difficult because, for instance, a defective component cannot be easily located, and there is also the probability of having a bad receiver covered up with an extremely good transmitter.

To improve the simple loopback testing, several approaches have incorporated jitter injection capabilities into the loopback to “stress” the signal and thus test the receiver’s jitter rejection or noise-tolerant capabilities [Cai-02], [Cai-05], [J.Huang-01], [Laquai-01], [Lin-05]. The last method, as proposed in [Makand-05], involves assessing data eye via margining as an approach to testing Gbps serial I/O’s. The approach assumes that defective components are relatively rare, and loopback is established with a data pattern streaming through the loopback path.

It is virtually impossible to generate all kinds of deterministic and random jitter required for the characterization of the serial link with all the necessary built-in DFT, particularly when a new interface is first designed and there is no way of knowing what the receivers are sensitive to; however, it is advisable for these jitter injection circuits to be programmable so that a richer or more diverse set of stimuli can be generated. The proper set of stimuli is defined only after extensive characterization of early samples to minimize both escapes and test time.

Similar techniques have also been reported in [Robertson-05]. These techniques may not fully test the Clock Data Recovery (CDR) circuit, as the same clock source may be used to generate the output data stream at the transmit side and simultaneously drive the receiver circuits.

3.5. System-Level Interconnect Testing

Even though silicon parts are tested at the manufacturing sites, the parts will then have to be soldered (or socketed) onto the board. Such a board assembly process has its own set of manufacturing defect issues, not to mention that the bare PCB fabrication also can introduce its own defects. Many of these defects are not easy for a bed-of-nails board tester to find, but the defects can affect system-level operation at the rated speed and worst-case environmental conditions (voltage, noise, etc.). Consequently, these interfaces have to be tested on the board as well as in the system and there is a spectrum of methodologies to choose from. It is, of course, possible to just put together the system and perform an end-user functional test of the whole system. However, the success rate of such a test is not high (because of the many components

mounted on a given board), and, even worse, there is no diagnostic information when the system fails to boot (or startup). Hence, the following methodologies are commonly developed and deployed in various kinds of board assembly and system-level manufacturing.

3.5.1 Interconnect Testing with Boundary Scan

The aim for this test method is to primarily identify board-level manufacturing problems, such as incorrectly placed devices, rotated devices, bent leads, cold solder joints, improper socketing (if sockets are used), cracked PCB and traces, via problems, etc. The IEEE 1149.1 boundary-scan standard [Robertson-05] is commonly used for interconnect testing of the above-mentioned manufacturing problems.

The basic concept of the IEEE 1149.1 standard is the addition of a boundary-scan cell for every input or output pad in the chip. Through the TAP, each boundary-scan cell can be set to 1 or 0 independently through the boundary-scan chain. When the net connected to both ends of two chips (chip 1 and chip 2) implemented per the IEEE 1149.1 standard, the data that are driven by one end of the net are captured by the receiving boundary-scan cell and subsequently shifted out through the boundary-scan chain for analysis. This can detect and locate permanent faults, such as stuck-at, open, and short faults on the nets. The IEEE 1149.1 boundary scan allows the designer or user to immediately pinpoint the errors to the defective interconnects or bad chips [Wang-08].

3.5.2 Interconnect Testing with High-Speed Boundary Scan

The IEEE 1149.1 boundary-scan standard has been the mainstay for board-level interconnect testing since the early 1990s. However, the world of chip-level interconnects has changed from tens to hundreds of Mbps to that of multiple Gbps data rate. The signaling technologies for transferring those data have also changed from single-ended signaling to that of differential, clock embedded, and in some situations, even AC-coupled. Although one can design the IEEE 1149.1 TAP controller to run faster for testing these modern high-speed buses and serial links, it is becoming ineffective because of the non-performance-driven nature of the IEEE 1149.1 architecture. Moreover, the nature of differential and AC-coupled (there is no DC path) signaling on high-speed serial links also makes it incompatible with the IEEE 1149.1 standard.

The IEEE 1149.6 standard [IEEE-03] is an extension of the IEEE 1149.1 standard to deal with this differential, AC-coupled interface. With this standard, independently controllable digital driver logic and digital receiver logic under the control of the IEEE 1149.1 TAP controller are now implemented on both ends of the differential pads of the serial link, such that interconnect tests can be applied on these differential pads to detect defects that may exist between the differential lines.

Because it is an extension of the IEEE 1149.1 standard and there is no change to the underlying TAP architecture, IEEE 1149.6 still basically runs at a relatively slow data rate. What this test method fails to address is that these new high-speed serial interfaces have to run billions of bits every second. Passing IEEE 1149.6 testing alone cannot guarantee the data rate nor transmission reliability, particularly when the system I/O is running at multiple Gbps data rate.

An important issue with serial signaling is that the pattern changes so fast that before the pattern has a chance to go from one state to the opposite state fully, it has to go back to the original state again because of fast data changes. This creates data waveforms that are more difficult to differentiate (whether it is a 1 or a 0). Additionally, a long series of 0 or 1 patterns also makes the signal saturated to one side, and when a single bit of data change comes along, the signal will take a longer time to ramp before it has to change again. This yields the worst-case data eye. This physical effect is called ISI as mentioned in Sub-subsection 2.2. In conclusion, data pattern is critical for board-level and system-level testing when the physical media plays a major role.

3.5.3 Interconnect Built-In Self-Test

Interconnect built-in self-test (IBIST) [Nejedlo-03] is based on the premise that high-performance interfaces have to be tested at high speed. In a board manufacturing environment, it is desirable to separate board assembly defects without running full board-level functional tests. These types of tests should be carried out before the system attempts to boot/start up to increase

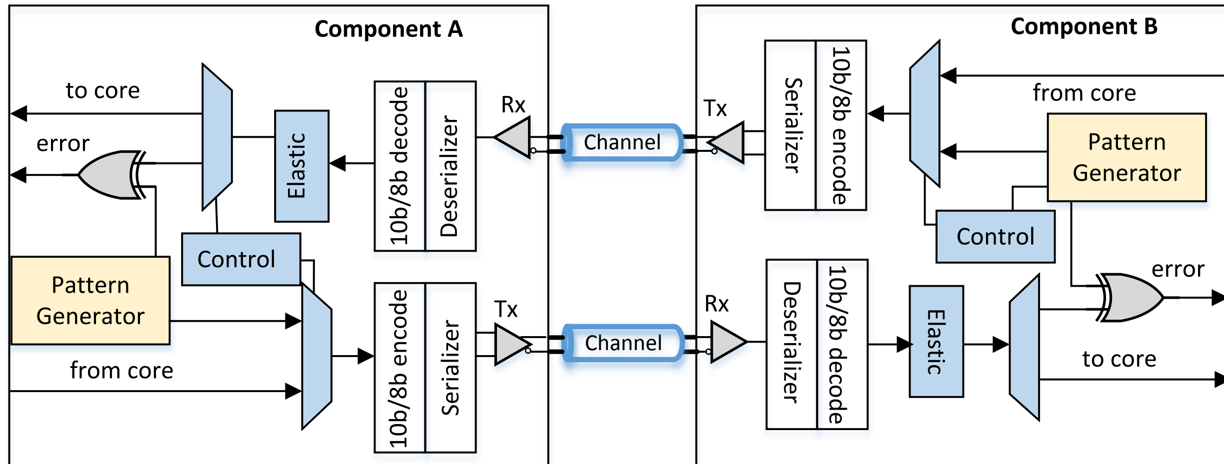


Fig. 3.2 IBIST as applied for high-speed serial testing at the board level. Figure taken from [Nejedlo-03].

the confidence level of the overall board manufacturing process.

Fig. 3.2 shows an IBIST example with two components as applied for high-speed serial testing at the board level. The two sides (components) of the I/O interface are named master and slave. On the transmit side, IBIST consists of a programmable pattern generator behind the Tx driver or transmitter of the I/O interface in the high-speed serial link. On the receive side, IBIST consists of logic to route the received data back to their own transmitter as well as error checking logic, which can check the pattern transmitted versus the received pattern. To further reduce the circuit requirement, the slave can simply implement the internal loopback circuit to support only the bounced back mode. With this reduced logic, it cannot independently send a pattern but will support the bounced back mode only. The independent pattern generator allows the interface to be tested independently of the core logic of the chip that has these high-speed interfaces. With this scheme, the master will take control of the whole test process. The included pattern generator on the master then drives a high-speed pattern to the slave side. Upon receiving it, the slave resends all the data that it has received (in bounce-back mode) immediately (bit-per-bit) through its own transmitter. The master's receiver receives this retransmitted pattern and checks it against the original transmitted pattern. Error checking is done on a symbol-by-symbol basis so that the error can be pinned down to the exact bits and further logic reasoning can be done to figure out what the cause of the error may be. A second stream of data can also be initiated from the slave side to aid with further diagnosis. Control registers keep track of when an error is first detected and can be examined after the test patterns are transmitted and received.

To stress the system under test, several data patterns can be supported, from pseudo-random pattern generation to specific preloaded patterns (some specific patterns may be needed for specific jitter and ISI requirements).

From the manufacturer standpoint, if such a system can be coupled with the electrical AC loopback system, in-system margin characterization is also possible, providing a much richer set of characterization data. This simply cannot be done with any of the aforementioned methods.

3.6. Functional Testing by Using Embedded Instruments

A general and brief introduction to SMV is realized in Sub-section 1.3. In this section, a more detailed description on the subject is discussed, emphasizing how margin testing is performed based on on-die instrumentation tools.

Many of today's chips already have instruments embedded in them by the device manufacturer. Rather than relying on external hardware-based measurements, simulation and user interpretation of specifications and results, embedded instruments can provide true, uncorrupted results observed at the receiver itself. Tests executed by embedded instrumentation use the same receiver that is employed in normal functional modes. There is no interpretation of results by the tester since the actual functional receiver is the test point.

Not only can this embedded instrumentation technology detect structural board faults on chip-to-chip interconnects, but it can also provide information about the performance and quality of the links (eye diagrams).

With Intel's embedded instrumentation, functional tests can be performed on HSIO links using pseudo-random bit sequence (PRBS) patterns as a foundation for pattern generation and checking (PG&C), BER testing and margining.

Basic PG&C tests can detect many structural faults, but high-speed serial nets like PCIe are designed to reject common mode noise and DC offsets. Some structural faults, such as shorts to ground or power, simply inject a DC offset which the receiver attempts to reject. In these cases, many types of test technologies may show that the links are operating normally and they could even work functionally, but the performance and margin available on the link will be degraded. Then more advanced capabilities of Intel's embedded instrumentation technology are required to detect performance degradation due to structural faults or variances in device, materials or process

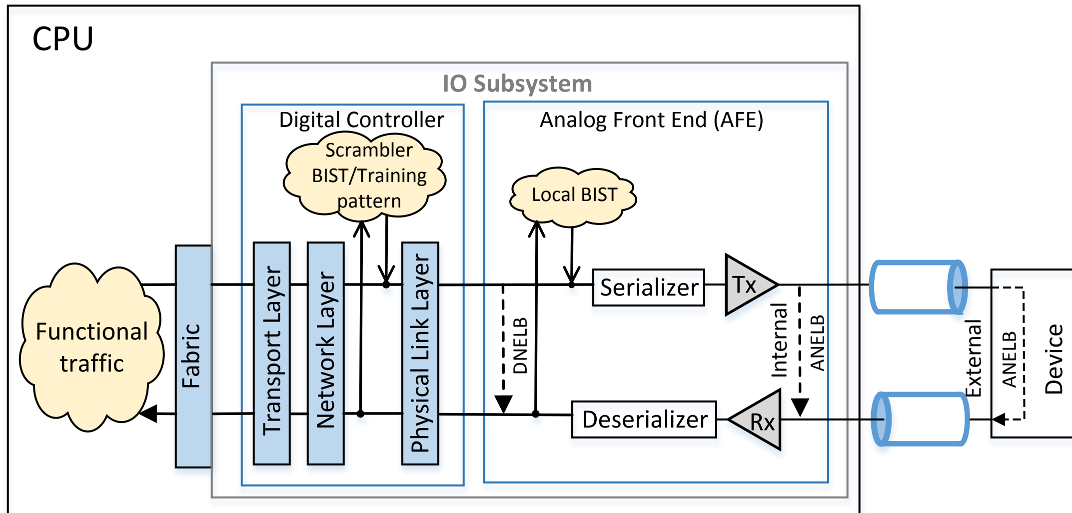


Fig. 3.3 Loopback mode testing.

changes. SMV is an approach used by engineers to indicate a system's health and stability, which, in turn, can be used to determine whether or not a product should be transferred into HVM phase [Shkolnitsky-10].

The production yield will eventually reflect the quality and robustness of the design. In case of multiple failures or low SMV margin, an in-depth investigation has to be started to find the root cause. For example, this can be done by means of electrical probing and verifying if the electrical parameters meet their specifications. By testing a small number of DUTs, and using statistical techniques from DoE, it is possible to make an estimation of the yield in the mass production phase. By using this methodology, design defects can be corrected before entering HVM.

SMV is based on sending data traffic through DUT link, while monitoring reception errors which are predefined beforehand. The next step is to sweep predefined electrical knobs/hooks, in order to check the system's stability. These knobs are called margin parameters, and are usually DFT features. Additional stress tests, e.g., power, can be defined to run simultaneously on the DUT. Some examples of swept margin parameters are: signal amplitude, timing parameters of the Rx circuit, I/O buffer impedance, I/O buffer voltage references, voltage supply level, and temperature of the chips.

A useful representation of the SMV results is a functional eye, which is a two-dimensional chart, where each axis represents a different margin parameter. An example of a functional eye can be seen in Fig. 1.1.

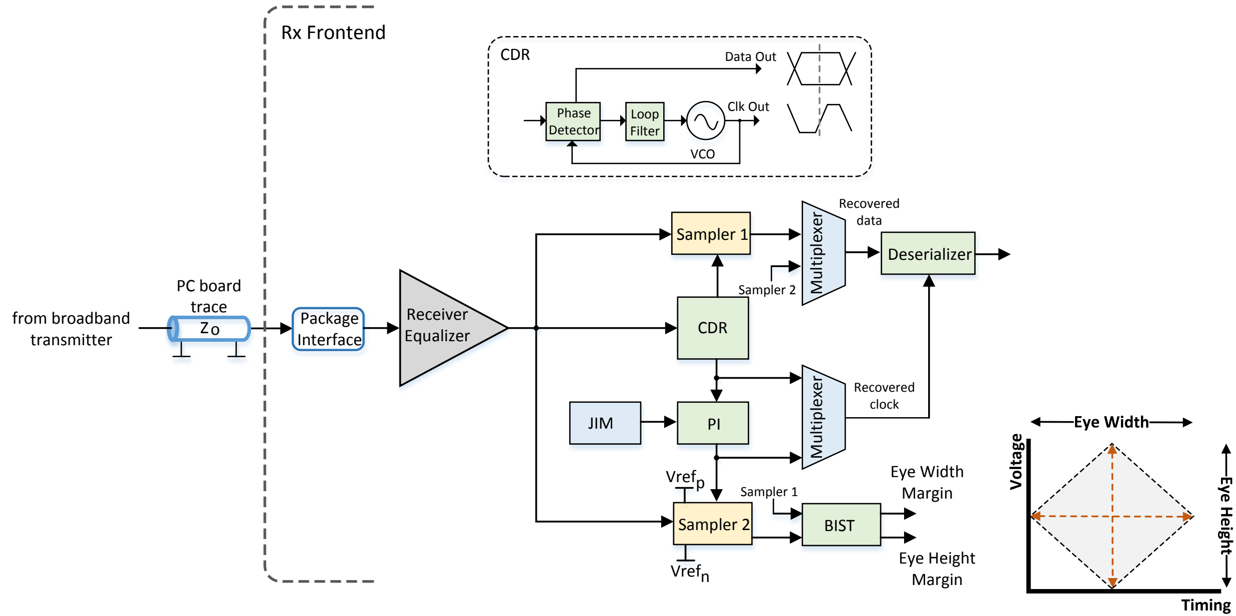


Fig. 3.4 SMV's on-die instrumentation architecture.

SMV is based on Intel IBIST, in this case, each link needs to be put into loopback as shown in Fig. 3.3. Loopback consists of a master IBIST device transmitting patterns from an internal buffer to a remote device. The remote device receives the patterns at the physical protocol layer and retransmits the data back to the master device without processing the data. For this to work, both devices have to be enabled and be able to send and receive data on the interconnect.

3.6.1 Margin Testing

SMV's on-die instrumentation tool provides measurement capability at various signal nodes within the transceivers. This cannot be easily achieved by external equipment, and it is a key feature for the Tx and Rx equalization, and debug as well as link characterization. The functionality and performance of SMV's on-die instrumentation tool are quite similar to those of an external instrument or a tester, but as it resides inside the transceiver the measurements are directly through internal signal nodes, and then it solves the high-speed interface issues when using external instruments at no additional cost. Fig. 3.4 shows the SMV on-die instrumentation architecture.

For margin testing the master varies the voltage threshold and the sampling point relative to time (phase interpolation) while errors are checked at each margin parameter setting. The

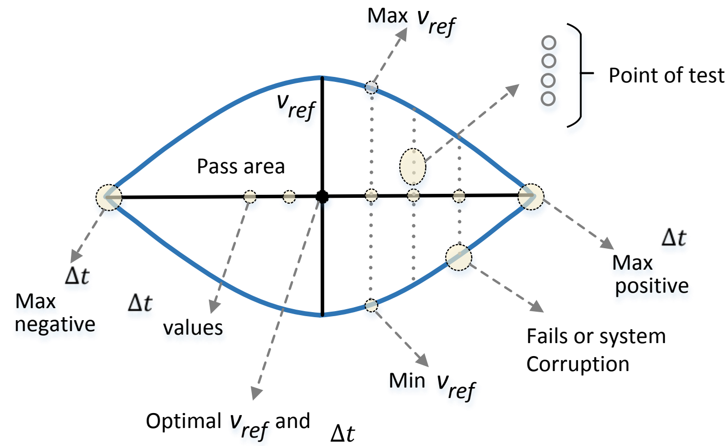


Fig. 3.5 Functional eye diagram based on multiple margin points.

resulting pass/fail matrix gives an engineer the solution space in which the system can operate without fault, as shown in Fig. 3.5. By using the SMV method, worst case patterns can be identified, and gives the engineer better insights to the amount of margin on a link, especially when different stresses are added.

The individual test point results are plotted as pass or fail. The plots for each link resemble the eye diagram seen on a traditional oscilloscope. The test time per point is far less than for BERT. The typical dwell time at a particular test point is 1 second. This is equivalent to a confidence level of much less than one percent.

Cross margin tests only check the values along the horizontal and vertical axis. The number of IBIST steps on each axis is programmable. An IBIST step is equivalent to an IBIST unit. The margin point is reached when any lane on the link finds at least one inconsistent data. This test gives the signal integrity validation engineer a rough look into the amount of margin on the link. Since minimal margin points are tested, the test takes about one tenth of the time of a full margin test. If the PG&C test passes, the next voltage increment is tested. If the test fails, the voltage and time values are noted, and the test moves to either the negative values to be tested or to the next phase interpolation to be tested. When the test is complete, the failing points can be charted, resulting in a plot that is similar to a traditional oscilloscope eye.

IBIST is used more qualitatively than quantitatively. This means that the shape, position and opening of the eye are important, not the raw values.

When a Bang-Bang phase detector is used in a phase-interpolator (PI) circuit, both in phase and quadrature phase clocks are required. These are generally referred to as *I* and *Q* clocks. The *I*

clock samples the data and the Q clock samples the edge of the data, providing phase information between the local clock and the incoming data.

The eye width (e_w) margin is measured by using jitter injection module (JIM) and delay in I-Q clocks generation to get eye-width information. The on-die jitter injection circuit is designed to inject jitter onto the receive data stream. This is accomplished by using a modification of the PI circuit to "adjust" the phases of a reference clock to generate a "jittered clock". When the phase jitter injection portion of the circuit is enabled, the jitter injection circuit employs an algorithm to define the jitter profile.

The eye height (e_h) margining is accomplished by introducing offset to V_{ref_n} and V_{ref_p} into the data sampler, as shown in Fig. 3.5. In margin mode, $V_{ref_n}$and $V_{ref_p}$are connected to a resistor ladder based bias generator.

An important capability of the SMV on-die instrumentation architecture is to measure and show the effective e_w of the equalized Rx data. This information can be used to adjust the equalization settings, a task that cannot be realized with external test equipment.

The SMV on-die instrumentation architecture provides both timing and voltage sampling, enabling complete eye-diagram reconstruction. Furthermore, SMV on-die instrumentation architecture also provides serial BER measurement capability before the deserializer to help solve most test, verification, characterization and debug challenges for high-speed transceivers through a non-intrusive interface.

3.7. Conclusions

In this chapter, the HSIO link testing methods at both chip and system levels were presented. Functional testing by using embedded instruments based on the IBIST was explained in detail.

It is concluded that SMV has emerged as a new, robust methodology for predicting the performance of a complex electronic system over its lifespan. Using on-chip embedded instrumentation within silicon, in conjunction with software that accesses this on-board logic, SMV measures the true operating margins at the devices' I/O buffers behind the pins. As such, SMV can remove the absolute dependency designers have had on legacy test and measurement technologies such as oscilloscopes, which can no longer cost-effectively validate today's very

high-speed serial I/O and memory buses.

As the speed, density and complexity of today's modern designs continue to increase, SMV plays an increasingly important role in enhancing the reliability and availability of electronic systems.

4. HSIO Receiver Equalization by Surrogate-Based Optimization

There is an increasingly higher number of mixed-signal circuits within microprocessors and SoC. A significant portion of them corresponds to HSIO links. Post-silicon validation of HSIO links can be critical for making a product release qualification decision under aggressive launch schedules. The optimization of receiver analog circuitry in modern HSIO links is a very time consuming post-silicon validation process. Current industrial practices are based on exhaustive enumeration methods to improve either the system margins or the jitter tolerance compliance test. In this chapter, these two requirements are addressed in a holistic optimization-based approach. A novel objective function based on these two metrics is proposed. The method employs Kriging to build a surrogate model based on system margining and jitter tolerance measurements. The proposed method, tested with three different realistic server HSIO links, is able to deliver optimal system margins and guarantee jitter tolerance compliance while substantially decreasing the typical post-silicon validation time.

4.1. Introduction

Complexity of new embedded systems has grown to an amazing level. Today's most advanced processors and SoC incorporate millions of transistors, and must be compatible with dozens of operating systems, hundreds of platform components and thousands of hardware devices and software applications. To ensure leading performance, reliability, and compatibility in this complex environment, companies invest over hundreds of millions of dollars annually in component and platform validation [INTEL-03].

The combined effects of increased product complexity, performance requirements, and TTM commitments have added tremendous pressure on post-silicon validation [Keshava-10], which is usually the last step prior to volume manufacturing.

Within the server segment, there are conditions that further increase system complexities. These include increased I/O density and serviceability, decreased cost and power consumption, as

well as non-flexible form factors [Lee-11]. The latter implies that channel lengths remain unchanged, thus turning the problem towards analog circuitry optimization.

One of the major challenges in HSIO EV is the PHY tuning process, where EQ techniques are used to cancel any undesired effect, such as Tx jitter, attenuation or ISI, among others [Hodgkiss-83], [Yuan-14], [Zhang-15]. PHY tuning is one of the most time-consuming processes in post-silicon validation [Cheng-11], [Wang-15]. In addition, when PVT conditions, as well as the multiple channels and devices or add-in cards are considered, the tuning complexity increases exponentially.

The current industrial practice to perform PHY tuning is based on an exhaustive or complete enumeration method; it is an empirical procedure based on the expert knowledge of the validation engineers on how the eye diagram is shaped. The method consists of maximizing either the functional eye diagram on the Rx based on the system margining response [Viveros-Wacher-14] or the JTOL measurements [Fan-09] and then doing a trade-off to arrive at a single set of EQ coefficient values that satisfy both test scenarios. Due to the large number of electrical parameters, the number of PHY tuning settings, the number of system margin measurements required, and the long JTOL test time, finding the best set of EQ coefficients for margining and meeting the JTOL mask is challenging and very time consuming [Liu-04]. In order to overcome these limitations new techniques to optimize the EQ coefficients are required.

In this chapter, a holistic optimization approach is described that merges system margining and jitter tolerance measurements to optimize the Rx analog circuitry during industrial post-silicon validation. The methodology concurrently optimizes Rx system margins and JTOL, by defining an objective function that combines both type of measurements, and by using a Kriging surrogate-based modeling approach to efficiently perform optimization. The proposed method is able to deliver optimal system margins and guarantee jitter tolerance compliance while substantially decreasing the typical post-silicon validation time.

This chapter corresponds to an extended version of [Rangel-Patiño-16]. Here it is presented a detailed description of system margining and jitter tolerance measurements and how they are used for PHY tuning. It is also provided a detailed mathematical development of the objective function and the Kriging surrogate-based modeling. In contrast to [Rangel-Patiño-16], the methodology by optimizing the Rx tuning on three different HSIO links is illustrated, including USB3, SATA3 and PCIe3, on a real industrial validation platform. In all the examples, it is

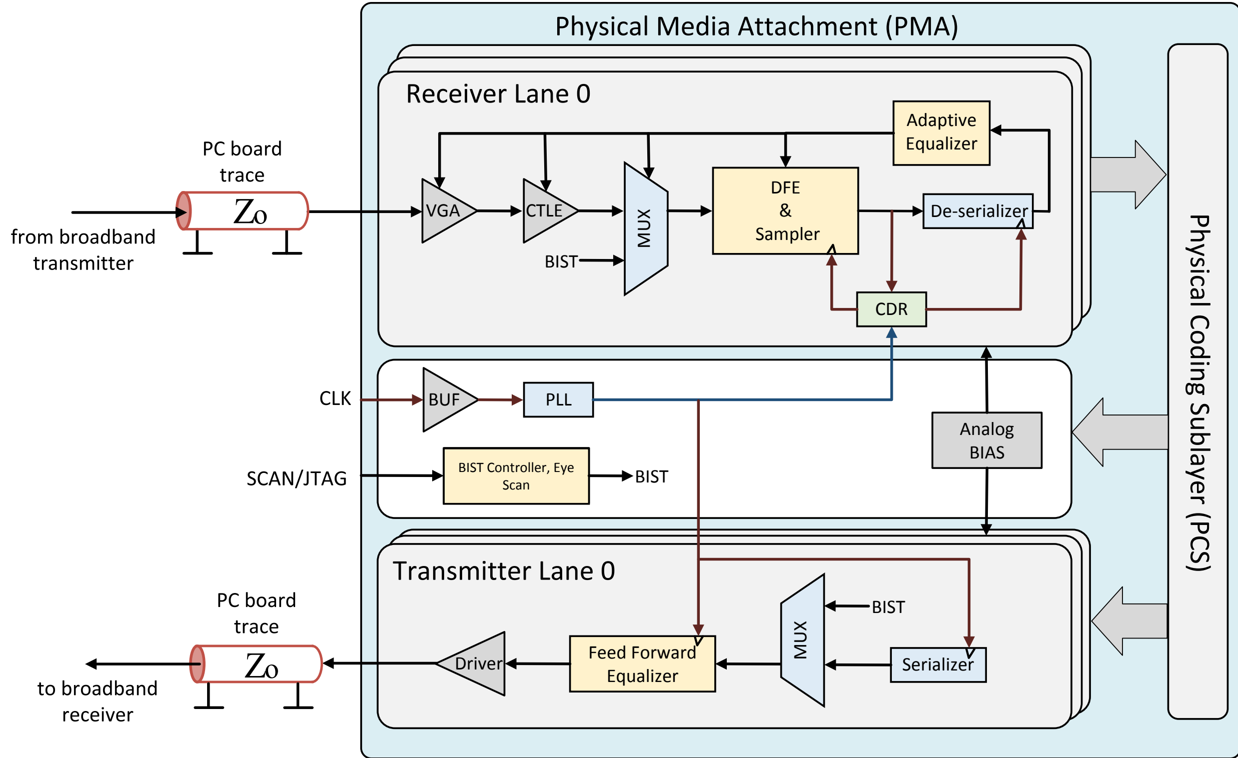


Fig. 4.1 Architecture of a typical SerDes PHY.

demonstrated the efficiency of the method to deliver optimal margins while ensuring jitter tolerance compliance. The results show a substantial improvement for both system margins and jitter tolerance as compared with the current industrial practice, as well as a dramatic reduction of the typical time required for PHY tuning.

The chapter is organized as follows. Section 4.2 presents the system measurements. The objective function formulation is presented in Section 4.3 and the surrogate model and optimization technique are described in Section 4.4. Section 4.5 shows the test cases where the holistic approach was tested, and finally Section 4.6 presents the conclusions.

4.2. System Measurements

There are two fundamental measurements that are being used during the PHY tuning process at post-Si validation: the system margins and jitter tolerance measurements.

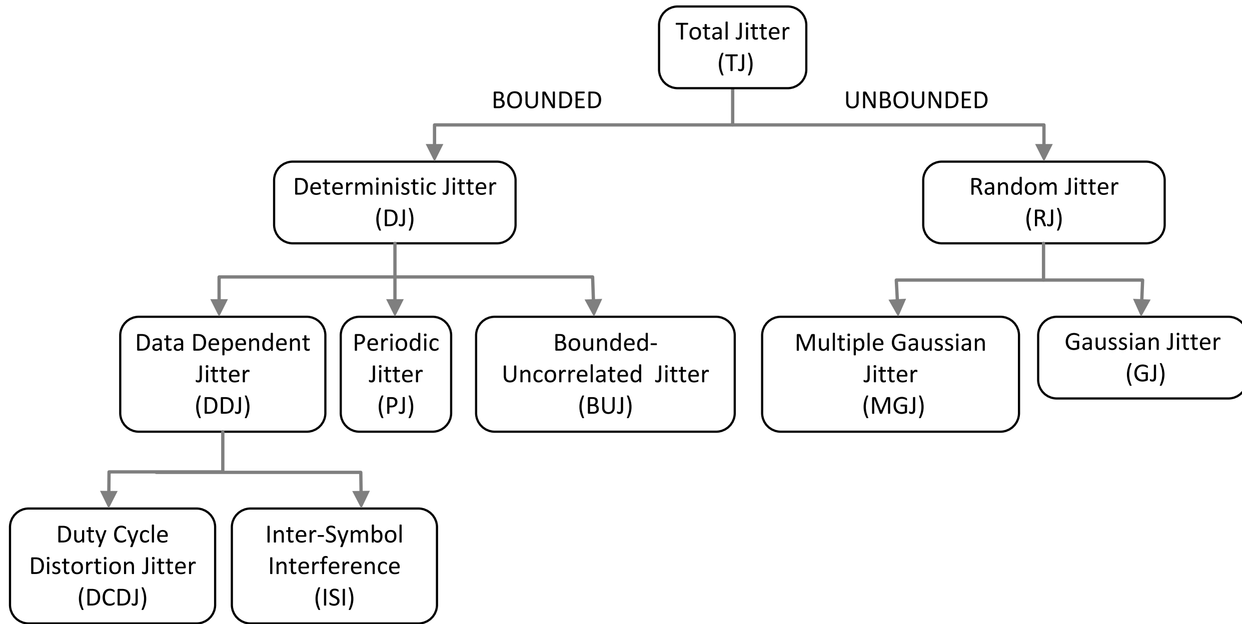


Fig. 4.2 Jitter classification and their relationships. Figure taken from [Wang-08].

4.2.1 System Margins

Measuring the system margins involves determining how the BER of a specific bus changes when several environmental and operating conditions are varied. The method consists of adjusting the validation platform operating conditions (voltage, temperature, etc.), then measure the Rx's eye opening by adjusting an specific on-die DFT instrumentation until the eye opening has been shrunk to a point the Rx detects errors or the system fails. Measuring the system margins is based in the SMV technique as described in Section 3.6.

4.2.2 Jitter Tolerance Testing

Fig. 4.1 shows the architecture of a typical serializer-deserializer (SerDes) PHY. The Tx takes parallel data to convert it into serial format, and then drives the serial data to the transmission channel. PLL circuit generates an internal high-speed serial clock for the serializer by multiplying the reference clock. The Rx receives the high speed serial data and restores it to the original parallel format. The CDR block generates from the received serial data a recovered clock to re-time the received serial data, and then the re-timed data is restored to parallel format by the de-serializer.

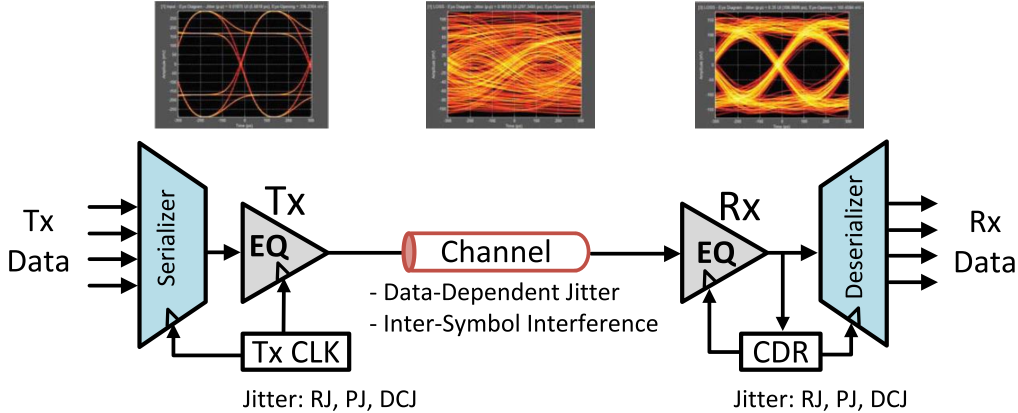


Fig. 4.3 Jitter sources in an HSIO link.

This SerDes mechanism needs the encoding and decoding logic to manipulate the transmitted data transition density to ensure the CDR can work correctly.

By encoding the clock into the data stream, the CDR guarantees that the clock and data are in phase when the jitter frequency is in the bandwidth of the CDR. However, if there is high frequency jitter in the data stream, the CDR may not track the data and the jitter may cause bit errors. Therefore, dealing with jitter to meet typical BER targets plays a crucial role when designing a robust Rx architecture [Ham-04], [Perrott-02]. Fig. 4.2 shows the jitter classification and their relationships. Each jitter can be attributed to a distinct source and has specific physical mechanisms and root causes associated with it [Wang-08].

Typical jitter sources in HSIO links that contribute to the overall accumulated jitter at the Rx are illustrated in Fig. 4.3. Some level of jitter is already induced by the non-ideal clock synthesizer inside the Tx block. Depending on the quality of the channel, ISI as well as reflections and crosstalk may degrade the signal integrity through the transmission media. At the Rx side, a non-ideal equalizer and PLL inherent phase noise of the CDR will additionally induce their own timing jitter [Agilent-03], [Casper-09], [Li-09], [M.Li-07].

One of the most common ways to measure the performance of an HSIO link is by measuring the BER through the HSIO link [Hong-08]. The fewer the errors measured, the better the performance of the link. BER measurement is typically used to characterize the Rx JTOL performance in order to determine compliance with the industry standard specifications, such as PCIe [PCISIG-16], SATA [SATAOrg-16], USB [USBOrg-16] and XAUI [10GEA-16]. Most HSIO protocols require a BER in the range from 10^{-12} to 10^{-15}. Fig. 4.4 shows the relationship between jitter and BER [Fan-09]. The time interval of interest for the left eye crossing is that one

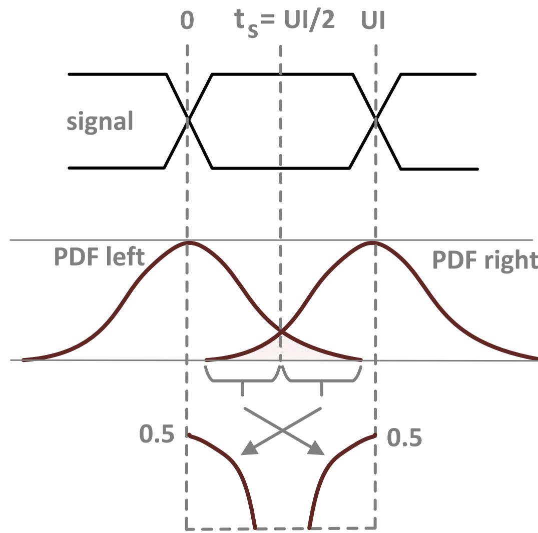


Fig. 4.4 Relationship between jitter and BER in the Rx. Figure taken from [Fan-09].

to the right of sampling instant t_s; similarly, the time interval of interest for the right eye crossing is that one to the left of t_s. Integrating the probability density functions (PDFs) of both eye crossings over their respective time intervals produces the BER function.

The goal for Rx JTOL is to verify that it can operate at a target BER when operating under worst case signaling conditions. JTOL testing consists of verifying that the measured Rx clock-recovery tolerance across frequencies is above the target threshold. If the measured JTOL curve is above the threshold curve, it indicates a passing result, thus the Rx can tolerate some more jitter. On the other hand, if the measured curve is below the threshold curve, it indicates a failing result. Both scenarios are shown in Fig. 4.5 [Wang-08].

Fig. 4.6 shows a generic JTOL testing setup which requires an instrument capable of generating a PRBS and an error detector to measure the BER. Fig. 4.7 shows the different test setups used for USB, SATA and PCIe. The amplitude of jitter is swept to the maximum that the Rx can tolerate for a range of frequencies. These measurements are compared against the test protocol's sinusoidal jitter tolerance mask.

A typical characterization of an Rx includes four jitter tests:

1) Deterministic Jitter. This is the measure of jitter tolerance for an Rx at a specific BER. This test is typically performed at different frequencies of phase modulation or periodic jitter and it is repeated at different frequencies of sinusoidal jitter (SJ) throughout the jitter tolerance spectrum.
2) Random Jitter. In this test, the random jitter (RJ) is increased while performing a closed

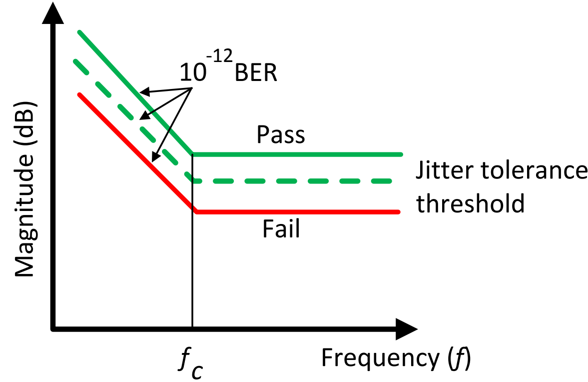


Fig. 4.5 Rx jitter tolerance threshold for testing. Figure taken from [Wang-08].

loop BER test in order to determine the RJ tolerance of an Rx.

3) Jitter Tolerance. During this test, the level of the input signal at the Rx is reduced until it reaches the BER level in order to determine if the Rx can tolerate a minimum input signal level. For a more comprehensive characterization, a composite of phase and amplitude modulation of both RJ and SJ is applied as the stress signal for the receiver characterization.
4) Clock Recovery. In order to test the CDR, jitter transfer and tolerance test are done by frequency modulating the input signal. The jitter tolerance test is a measure of BER as a function of inducing frequency modulated (FM) jitter into the Rx.

JTOL for HSIO requires validating BER against standards specifications, but direct verification of a target 10^{-12} is very time consuming, since it can take several minutes to perform a single BER test [Agilent-05], [Kossel-04]. Measurement time depends on the data rate and the required BER. HSIO protocols have data rates ranging from 5 to 16 Gb/s: SATA3 (6 Gb/s), USB3 (5 Gb/s), PCIe3 (8 Gb/s), PCIe4 (16 Gb/s). In addition, JTOL is usually measured across a range of frequencies to determine the frequency response of the device. In [Agilent-05] and [Maxim-04], the relationship between test time and BER confidence level is studied, finding that the quantity of data bits N needed to guarantee a target BER is

$$N = \frac{1}{B}\left[-\ln(1-a) + \ln\left(\sum_{k=0}^{E} \frac{(N \times B)^k}{k!}\right)\right] \tag{4-1}$$

where B is the desired BER level, a specifies the statistical probability or confidence level of BER value being less than B, and E is the number of detected errors during measurements. When no bit errors occur ($E = 0$), then the second term of (4-1) is zero and the solution is simplified. Assuming a confidence level $a = 95$, then it is necessary to transmit $N = 3\times10^{12}$ bits without errors in order

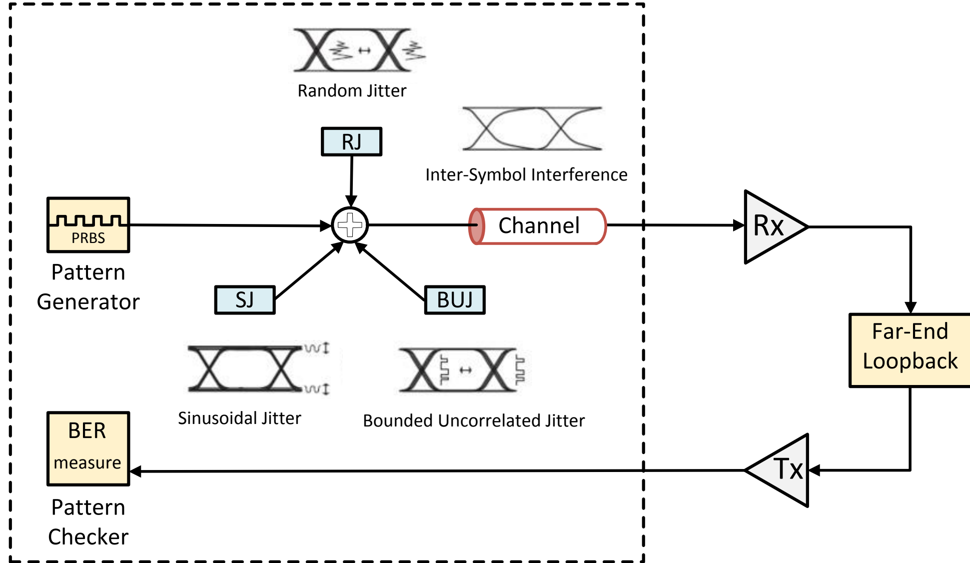


Fig. 4.6 A generic test setup for Rx jitter testing.

to meet a BER = 10^{-12}. In a SATA3 Tx this would require a time per testing point given by,

$$\text{time} = \frac{N}{\text{speed}} = \frac{3\times10^{12}}{6\times10^{9}} = 500\text{sec} = 8.3\,\text{min} \tag{4-2}$$

Therefore, the measurement time for a complete set of JTOL values can take a long time depending on the conditions. Such a large test time to perform a single BER test is not feasible for PHY tuning or for high volume production testing. The test time problem becomes much worse when taking into considerations that many design parameters and DUT settings can affect the JTOL performance.

4.3. Objective Function Formulation

In this section is developed a novel objective function considering JTOL and system margins measurements.

4.3.1 Objective Function for System Margining

Let $\boldsymbol{R}_m \in \Re^2$ denote the electrical margining system response, which consists of the eye width e_w and eye height e_h of the functional eye diagram,

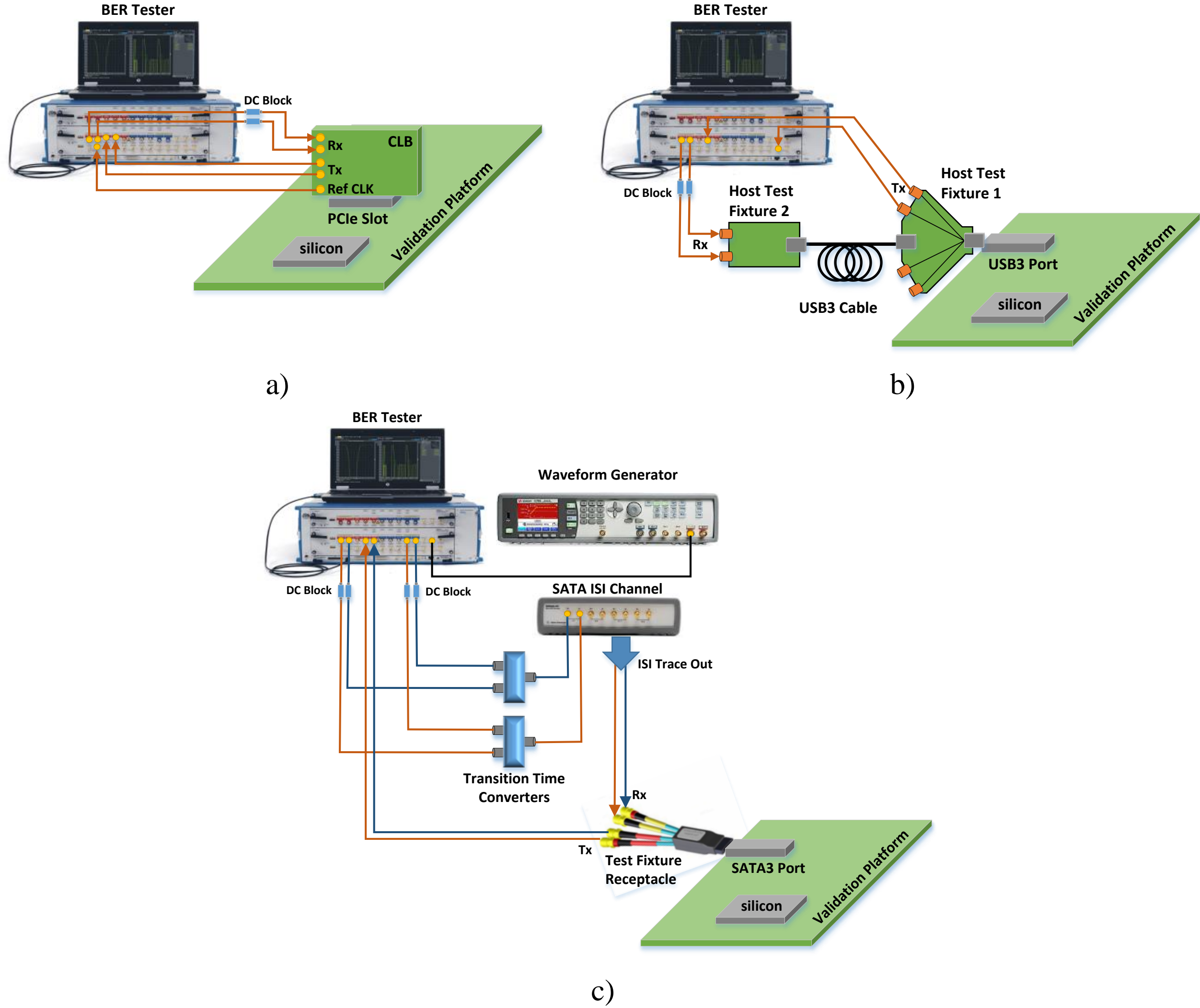


Fig. 4.7 JTOL testing setups: a) PCIe setup, b) USB setup, c) SATA setup.

$$\boldsymbol{R}_m = \boldsymbol{R}_m(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = \begin{bmatrix} e_{\mathrm{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \\ e_{\mathrm{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \end{bmatrix} \tag{4-3}$$

This electrical margining system response depends on the PHY tuning settings $\boldsymbol{x}$ (EQ coefficients), the operating conditions $\boldsymbol{\psi}$ (voltage and temperature), and the devices $\boldsymbol{\delta}$ (silicon skew and external devices).

The functional eye diagram area is defined by

$$e_a = (e_{\mathrm{w}})(e_{\mathrm{h}}) \tag{4-4}$$

where $e_a \in \Re$ is the eye area, $e_{\mathrm{w}} \in \Re$ and $e_{\mathrm{h}} \in \Re$ are the eye width and height, respectively, obtained from measured parameters,

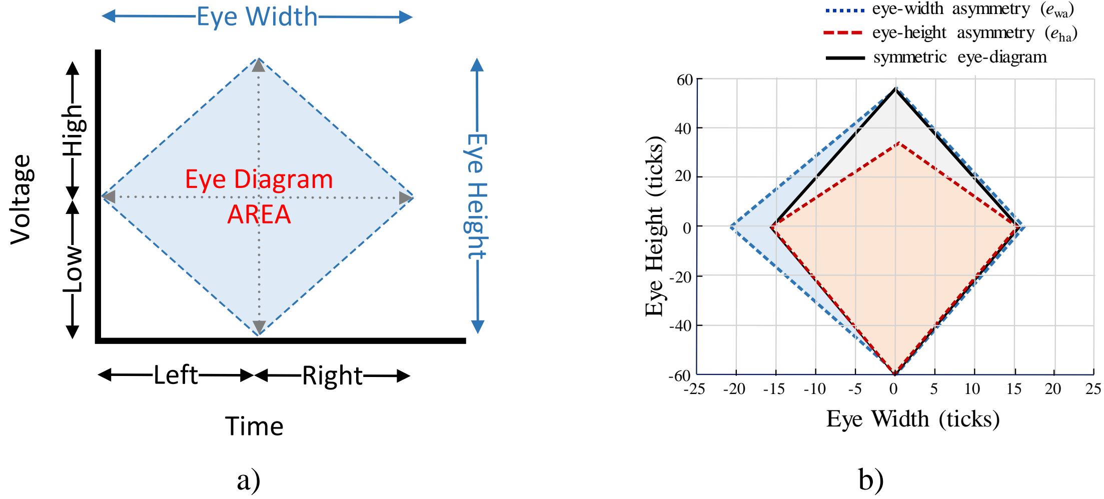


Fig. 4.8 Eye diagram: a) graphical objective function representation, b) example of asymmetries on 3 test cases of EQ.

$$e_{\mathrm{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = e_{\mathrm{wr}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) + e_{\mathrm{wl}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \tag{4-5}$$

$$e_{\mathrm{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = e_{\mathrm{hh}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) + e_{\mathrm{hl}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \tag{4-6}$$

where $e_{\mathrm{wr}} \in \Re$ and $e_{\mathrm{wl}} \in \Re$ are the eye width-right and eye width-left measured parameters, respectively, and $e_{\mathrm{hh}} \in \Re$ and $e_{\mathrm{hl}} \in \Re$ are the eye height-high and eye height-low measured parameters, respectively, as illustrated in Fig. 4.8a.

Since the objective is to maximize the area of the functional eye diagram, the initial objective function is given by

$$u(\boldsymbol{x}) = [e_{\mathrm{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})][e_{\mathrm{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] \tag{4-7}$$

Based on the operating conditions and devices, the eye diagram can be decentered with respect to the eye-width, eye-height or both. A well centered Rx eye diagram is required to have a proper sampling on the CDR. The better Rx data is aligned, the easier the phase interpolator circuitry will track for edges on the recovered data. Therefore, the objective function must consider the asymmetries of the eye diagram, as illustrated in Fig. 4.8b.

Let e_{wa} and e_{ha} be the eye-width asymmetry and eye-height asymmetry, respectively. They are defined as

$$e_{\mathrm{wa}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = \left| e_{\mathrm{wr}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) - e_{\mathrm{wl}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \right| \tag{4-8}$$

$$e_{\mathrm{ha}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = \left| e_{\mathrm{hh}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) - e_{\mathrm{hl}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \right| \tag{4-9}$$

The area of the eye diagram and the asymmetries should be scaled by weighting factors w_1, w_2, $w_3 \in \Re$ such that they become comparable. The values of these weighting factors depend on

the operating conditions and devices, and they can be selected by using initial e_{w} and e_{h} measurements.

Therefore, the objective function to be maximized is now defined as

$$u(\boldsymbol{x}) = w_1\left[e_{\mathrm{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right]\left[e_{\mathrm{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] - w_2\left[e_{\mathrm{wa}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] - w_3\left[e_{\mathrm{ha}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] \quad (4\text{-}10)$$

with w_1, w_2, and w_3 calculated from

$$w_1 = \frac{3}{\frac{1}{n}\sum_{i=1}^{n} u1_i(x)} \quad (4\text{-}11)$$

$$w_2 = \frac{1}{\frac{1}{n}\sum_{i=1}^{n} u2_i(x)} \quad (4\text{-}12)$$

$$w_3 = \frac{1}{\frac{1}{n}\sum_{i=1}^{n} u3_i(x)} \quad (4\text{-}13)$$

where $u1$, $u2$, and $u3$ are vectors containing initial e_{w} and e_{h} measurements.

From all the above, the optimization problem for system margining is

$$\boldsymbol{x}^* = \arg\max_{\boldsymbol{x}} u(\boldsymbol{x}) \quad (4\text{-}14)$$

with $u(\boldsymbol{x})$ defined by (4-10).

4.3.2 Objective Function for System Margining and Jitter Tolerance

The optimization problem is now modified such that the optimal set of EQ coefficients simultaneously maximizes the eye diagram and exceeds the JTOL mask.

The JTOL system response is denoted as vector $\boldsymbol{R}_{\mathrm{J}}$ and consists of measurements of the sinusoidal jitter amplitude $\boldsymbol{S}_{\mathrm{JA}}$ over a frequency range of interest,

$$\boldsymbol{R}_{\mathrm{J}} = \boldsymbol{R}_{\mathrm{J}}(\boldsymbol{x},\boldsymbol{\psi}) = \boldsymbol{S}_{\mathrm{JA}}(\boldsymbol{x},\boldsymbol{\psi}) \quad (4\text{-}15)$$

The new optimization problem can be defined through a constrained formulation,

$$\boldsymbol{x}^* = \arg\max_{\boldsymbol{x}} u(\boldsymbol{x}) \quad \text{subject to } \boldsymbol{g}(\boldsymbol{x}) \le \boldsymbol{0}, \quad (4\text{-}16)$$

with $u(\boldsymbol{x})$ defined by (4-10) and

$$\boldsymbol{g}(\boldsymbol{x}) = \boldsymbol{S}_{\mathrm{JAspec}} - \boldsymbol{S}_{\mathrm{JA}} \quad (4\text{-}17)$$

where $\boldsymbol{S}_{\text{JAspec}}$ is the JTOL specification mask in the frequency range of interest.

A more convenient unconstrained formulation can be defined by adding a penalty term, as

$$U(\boldsymbol{x}) = u(\boldsymbol{x}) - r_0^g \|\boldsymbol{G}(\boldsymbol{x})\|_2^2 \tag{4-18}$$

where $\boldsymbol{G}(\boldsymbol{x})$ is the JTOL penalty function defined as,

$$\boldsymbol{G} = \max\{\boldsymbol{0}, \boldsymbol{g}(\boldsymbol{x})\} \tag{4-19}$$

The optimal solution depends on the value of $r_0^g \in \Re$, which is a penalty coefficient defined as,

$$r_0^g = \frac{|u(\boldsymbol{x}_0)|}{\|\boldsymbol{g}(\boldsymbol{x}_0)\|_2^2} \tag{4-20}$$

where $\boldsymbol{x}_0$ is the starting point for optimization.

In summary, the holistic objective function to optimize system margining and meet the JTOL mask is

$$\boldsymbol{x}^* = \arg\max_{\boldsymbol{x}} U(\boldsymbol{x}) \tag{4-21}$$

with

$$U(\boldsymbol{x}) = w_1[e_{\text{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})][e_{\text{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] - w_2[e_{\text{wa}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] - w_3[e_{\text{ha}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] - r_0^g \|\boldsymbol{G}(\boldsymbol{x})\|_2^2 \tag{4-22}$$

4.4. Surrogate Model and Optimization

To solve (4-21), a surrogate-based optimization strategy is followed. Kriging [Sacks-89] is selected as the underlying modeling technique, given its adequacy for dealing with multiple optima and non-continuous responses. The implementation exploits the Matlab[1] Kriging toolbox DACE [Lophaven-02]. To enhance the efficiency of the approach, DoE for selecting fitting points is applied.

4.4.1 Design of Experiments

DoE is a set of statistical methods for allocating points in the design space with the

[1] MATLAB, R2015b, The MathWorks, Inc., 3 Apple Hill Drive, Natick MA 01760-2098, 2015.

objective to maximize the amount of useful information. In this case, measurements from the system at these points are taken to create the training data set that is subsequently used to construct the surrogate model. When sampling the points, there is a clear trade-off between the number of points used and the amount of information that can be extracted from these points. The samples are typically spread apart as much as possible in order to capture global trends in the design space [Koziel-11].

The key issues in the selection of an appropriate DoE include:

a) The dimensionality of the problem.
b) Whether noise is an important source of error.
c) The number of simulations or experiments that can be afforded.
d) The type of surrogate used to model the problem.
e) The shape of the design space.

In this case, a low discrepancy sequence algorithm is selected for DoE to cover the non-uniformity of data points sequence by using the Sobol sequence [Cheng-00], [Sobol-67]; hence, it is guaranteed to cover the space as uniformly as possible for the number of points chosen.

4.4.2 Low-discrepancy Sequences

In this section [Cheng-00] and [Weisstein-17] are followed to describe the low-discrepancy sequences. Discrepancy is a measure of non-uniformity of a sequence of points placed in a unary hypercube $[0, 1]^d$. The most widely studied distance measure is the star discrepancy.

Given a point set

$$P = \{\boldsymbol{x}_n\}_{n=0}^{N-1} \tag{4-23}$$

in the s-dimensional unit cube $I = [0,1)^s$, the star discrepancy is defined as

$$D_N^*(P) \equiv \sup_{J \in Y^*} D(J, P) \tag{4-24}$$

where Y^* is the class of all s-dimensional subintervals J of I of the form

$$J \equiv \prod_{i=1}^{s} [0, u_i) \tag{4-25}$$

with $0 \le u_i \le 1$ for $1 \le i \le s$. The local discrepancy is defined as

$$D(J,P) \equiv \left| \frac{\text{number of } x_n \in J}{N} - \text{Vol}(J) \right| \tag{4-26}$$

where Vol(J) is the content of J.

In this context, the term "star" from "star discrepancy" refers to the fact that the s-dimensional subintervals have a vertex at the origin. In other words, for every subset E of $[0, 1]^d$ of the form $[0, u_1) \times ... \times [0, u_d)$, it is divided the number of points $\boldsymbol{x}_k$ in E by N and take the absolute difference between this quotient and the volume of E. The maximum difference is the star discrepancy D^*_N.

A sequence $x_1, x_2, .., x_N$ of points in $[0, 1]^d$ is a low-discrepancy sequence if for any $N > 1$

$$D_N^*(x_1, \ldots x_N) \leq c(d) \frac{(\log N)^d}{N} \tag{4-27}$$

where the constant $c(d)$ depends only on the problem dimension d. The idea behind the low-discrepancy sequences is to let the fraction of points within any subset E of $[0, 1]^d$ of the form $[0, u_1) \times ... \times [0, u_d)$ be as close as possible to its volume. In that manner, the low-discrepancy sequences will spread over $[0, 1]^d$ as uniformly as possible, reducing gaps and clustering of points.

4.4.3 The Sobol Sequence

The Sobol sequence [Sobol-67] is generated from a set of special binary fractions of length w bits, u_i^j, $i = 1, 2,\ldots, w$, $j = 1, 2,\ldots, d$. The numbers u_i^j are called direction numbers.

In order to generate direction numbers for dimension j, it is started with a primitive (irreducible) polynomial over the field F_2 with elements $\{0, 1\}$. Suppose the primitive polynomial in dimension j is

$$p_j(x) = x^q + a_1 x^{q-1} + \ldots + a_{q-1} x + 1 \tag{4-28}$$

The direction numbers in dimension j are generated using the following q-term recurrence relation

$$u_i^j = a_1 u_{i-1}^j \oplus a_2 u_{i-2}^j \oplus \ldots \oplus a_{q-1} u_{i-q+1}^j \oplus u_{i-q}^j \oplus (u_{i-q}^j / 2^q) \tag{4-29}$$

where $i > q$. $\oplus$ denotes the bitwise XOR operation. The initial numbers $u_1^j \cdot 2^w, u_2^j \cdot 2^w, \ldots, u_q^j \cdot 2^w$ can be arbitrary odd integers smaller than $2, 2^2,\ldots,$ and 2^q, respectively. The Sobol sequence

$$x_n^j (n = \sum_{i=0}^{w} b_i 2^i, b_i \in \{0,1\}) \quad (4\text{-}30)$$

in dimension j is generated by

$$x_n^j = b_1 u_1^j \otimes b_2 u_2^j \oplus \ldots \oplus b_w u_w^j \quad (4\text{-}31)$$

It should use a different primitive polynomial to generate Sobol sequence in each dimension [Cheng-00].

4.4.4 Kriging Surrogate Model

Kriging is a surrogate modeling technique to approximate deterministic data. It has proven to be very useful for tasks such as optimization [Jones-98], design space exploration, visualization, prototyping, and sensitivity analysis [Wang-06]. A detailed mathematically description of Kriging is given in [Santner-03] and [Forrester-08]. The popularity of Kriging has generated research in many areas, including several extensions to Kriging to handle different problem settings, e.g., by adding gradient information in the prediction [Morris-93], or by approximating stochastic simulations [Staum-09].

It is named after the pioneering work of D. G. Krige (a South African mining engineer), and was formally developed in [Matheron-63]. Then [Jones-98], and [Sacks-89] made it popular in the context of the modeling and optimization of deterministic functions, respectively. The Kriging method in its basic formulation estimates the value of a function at some unsampled location as the sum of two components, the linear model (e.g., polynomial trend) and a systematic departure representing low (large scale) and high frequency (small scale) variation components, respectively.

Kriging considers both the distance and the degree of variation between known data points when estimating values in unknown areas. A Kriged estimate is a weighted linear combination of the known sample values around the point to be estimated. Applied properly, Kriging allows to derive weights that result in optimal and unbiased estimates. It attempts to minimize the error variance and set the mean of the prediction errors to zero so that there are no over- or under-estimates.

A unique feature of Kriging is that it provides an estimation of the error at each interpolated point, providing a measure of confidence in the modeled surface.

In this work, ordinary Kriging [Queipo-05] is used that estimates a deterministic function f as

$$f_p(\boldsymbol{x}) = \mu + \varepsilon(\boldsymbol{x}) \tag{4-32}$$

$$E(\varepsilon) = 0 \tag{4-33}$$

$$\operatorname{cov}(\varepsilon(\boldsymbol{x}^i), \varepsilon(\boldsymbol{x}^j)) \neq 0 \forall i, j \tag{4-34}$$

where μ is the mean of the response at base points ($\boldsymbol{x}$), and ε is the error with zero expected value, and with a correlation structure being a function of a generalized distance between the base points.

In contrast to linear regression models, the stochastic process approach assumes that the errors are dependent. In other words, the correlation between errors is related to the distance between the corresponding points. Then, the distance used is the spatial weighted distance obtained by

$$\Delta(\boldsymbol{x}^i, \boldsymbol{x}^j) = \sum_{k=1}^{N} \theta_k \left| x_k^i - x_k^j \right|^{p_k} \text{ with } \theta_k \geq 0, p_k \in [1,2] \tag{4-35}$$

where x_k^i and x_k^j are the kth components of the base points $\boldsymbol{x}^i$ and $\boldsymbol{x}^j$, and N denotes the number of dimensions in the set of design variables $\boldsymbol{x}$. The smaller the distance between $\boldsymbol{x}^i$ and $\boldsymbol{x}^j$, the higher the correlation, and hence if the distance increases the correlation drops to zero. The rate and manner at which this happens is governed by p_k and θ_k, where p_k determines the initial drop in correlation as distance increases [Lophaven-02]. θ_k are unknown correlation parameters used to fit the model.

A possible correlation structure [Sacks-89] is given by

$$\operatorname{cov}(\varepsilon(\boldsymbol{x}^i), \varepsilon(\boldsymbol{x}^j) = \sigma^2 \boldsymbol{R} \tag{4-36}$$

where σ identifies the standard deviation of the response at sampled design points, σ^2 is the variance, and $\boldsymbol{R}$ is the correlation $n \times n$ matrix between the base points.

$$\boldsymbol{R} = \begin{bmatrix} R(\boldsymbol{x}^1, \boldsymbol{x}^1) & R(\boldsymbol{x}^1, \boldsymbol{x}^2) & R(\boldsymbol{x}^1, \boldsymbol{x}^N) \\ R(\boldsymbol{x}^2, \boldsymbol{x}^1) & R(\boldsymbol{x}^2, \boldsymbol{x}^2) & R(\boldsymbol{x}^1, \boldsymbol{x}^N) \\ \vdots & \vdots & \vdots \\ R(\boldsymbol{x}^N, \boldsymbol{x}^1) & R(\boldsymbol{x}^N, \boldsymbol{x}^1) & R(\boldsymbol{x}^N, \boldsymbol{x}^N) \end{bmatrix} \tag{4-37}$$

Here it is used a Gaussian correlation function of the form

$$R(\boldsymbol{x}^i, \boldsymbol{x}^j) = \exp[-\sum_{k=1}^{N} \theta_k \left| x_k^i - x_k^j \right|^2] \tag{4-38}$$

The Kriging-based surrogate model $\boldsymbol{R}_s$ is defined as

$$\boldsymbol{R}_s(\boldsymbol{x}) = \left[R_{s.1}(\boldsymbol{x})\ldots R_{s.m}(\boldsymbol{x})\right]^T \tag{4-39}$$

The model estimates the responses at unsampled points by the Kriging predictor [Sacks-89] by

$$R_{s.j}(\boldsymbol{x}) = \bar{\mu}_j + \boldsymbol{r}^T(\boldsymbol{x})\boldsymbol{R}^{-1}(\boldsymbol{f}_j - \boldsymbol{1}\bar{\mu}_j) \tag{4-40}$$

where **1** denotes an N-vector of ones, and

$$\boldsymbol{f}_j = \left[R_{sm.j}(\boldsymbol{x}^1)\ldots R_{sm.j}(\boldsymbol{x}^N)\right]^T \tag{4-41}$$

The bar above the variables denotes estimates, $\boldsymbol{r}$ identifies the correlation vector between the set of prediction points $\boldsymbol{x}$ and the base points,

$$\boldsymbol{r}^T(\boldsymbol{x}) = \left[R(\boldsymbol{x},\boldsymbol{x}^1)\ldots R(\boldsymbol{x},\boldsymbol{x}^N)\right]^T \tag{4-42}$$

The mean $\bar{\mu}_j$ is the estimated value of μ_j and can be calculated using

$$\bar{\mu}_j = \frac{\boldsymbol{1}^T\boldsymbol{R}^{-1}\boldsymbol{f}_j}{\boldsymbol{1}^T\boldsymbol{R}^{-1}\boldsymbol{1}} \tag{4-43}$$

The unknown parameter θ_k, for the Kriging model can be estimated by maximizing the following likelihood function $g(\boldsymbol{R})$ given by [Queipo-05]

$$g(\boldsymbol{R}) = -\frac{N}{2}\ln(\bar{\sigma}^2) - \frac{1}{2}\ln|\boldsymbol{R}| \tag{4-44}$$

in which the variance

$$\bar{\sigma}_j^2 = \frac{1}{N}(\boldsymbol{f}_j - \boldsymbol{1}\bar{\mu}_j)^T\boldsymbol{R}^{-1}(\boldsymbol{f}_j - \boldsymbol{1}\bar{\mu}_j) \tag{4-45}$$

and $|\boldsymbol{R}|$ are both functions of θ_k.

4.4.5 Optimization using the Surrogate Model

Once the Kriging model is built using a set of training data, the model is evaluated at a set of testing base points. If the model does not meet an error criteria, the Kriging parameters are re-estimated by using additional training data, testing again the model. This process is iterated until reached some convergence criterion. The surrogate-based optimization (SBO) procedure solves (4-21) using objective function (4-22). For optimization, the DACE toolbox is used that employs

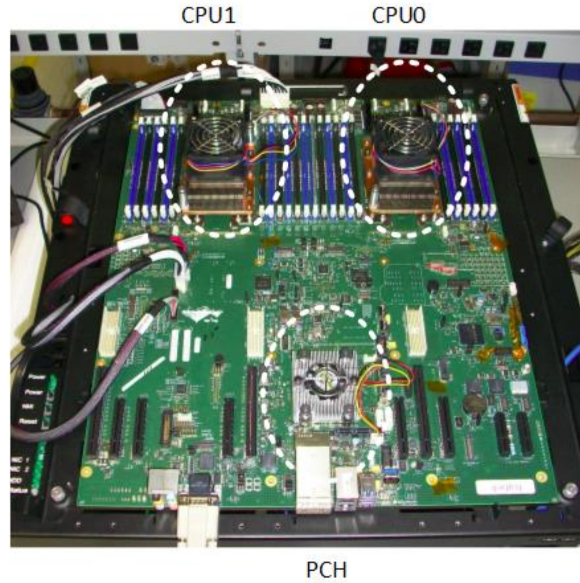


Fig. 4.9 Post-Silicon industrial validation platform.

the *fmincon* optimization routine from MATLAB optimization toolbox.

4.5. Test Cases

The proposed methodology in this chapter was tested in a post-silicon industrial environment, using an Intel server platform shown in Fig. 4.9, comprised mainly of a CPU and a platform controller hub (PCH). The PCH is a family of Intel microchips which controls data paths and support functions used in conjunction with the Intel CPU through direct media interface (DMI), as shown in Fig. 4.10. Within the PCH, the methodology was tested on three different

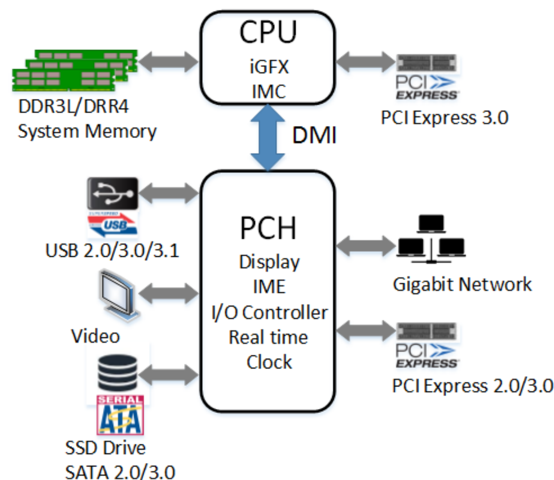


Fig. 4.10 Bock diagram of the platform controller hub.

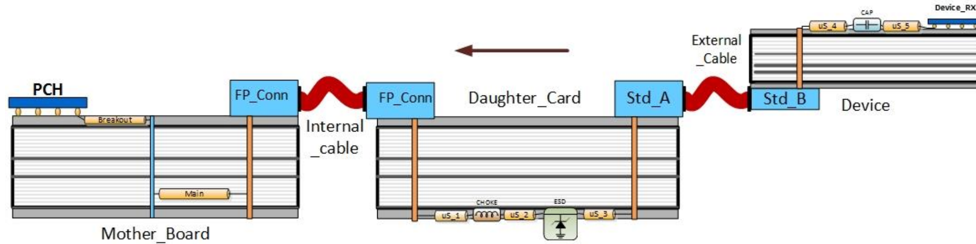


Fig. 4.11 USB3 Rx channel topology.

HSIO links: USB3 Super-speed Gen 1 [USBOrg-16], PCIe Gen3 [PCISIG-16], and SATA3 [SATAOrg-16].

As mentioned before, the complexity of HSIO buses used on Intel server platforms are exacerbated by the interaction of channel components characteristics, such as packages, PCB, input/output density, connectors, cables and devices, as well as its intrinsic elements such as insertion loss (IL), SNR, HVM variations, temperature and humidity impact on IL, etc. Several channel optimizations, including flexible routing [Lopez-Miralrio-13] hybrid PCB stack-up [Mendez-Ruiz-13], crosstalk cancellation [Xiao-12], and impedance mismatch [Ye-11], are utilized to mitigate the aforementioned complexity. Despite the use of these techniques during platform design, the Rx of each interface still needs to be tuned for optimal performance during post-silicon validation time frame.

4.5.1 Test Case 1: USB3

In the case of USB3, the channel topology is comprised of the Tx driver, the Tx based board transmission lines (TL), several via transitions, an I/O card connector, an internal cable that attaches a daughter card, followed by an external cable at which is attached at the other end another connector for the Rx I/O card, followed by another set of TL, and DC blocking capacitors at the Rx side of the device. Its simplified topology is illustrated in Fig. 4.11. The bandwidth limitations and inherent non-idealities of this system essentially result from the large amount of interconnects. Hence, the goal is to optimize the Rx equalization coefficients as a way to compensate for the channel limitations.

Fig. 4.12 illustrates the test setup specific for USB3. We stress the Rx with a BER tester, sending a compliant pattern including all jitter impairments as per specification. The host computer is capable of modifying Rx EQ coefficients and DFT circuitry of the DUT as well as sending

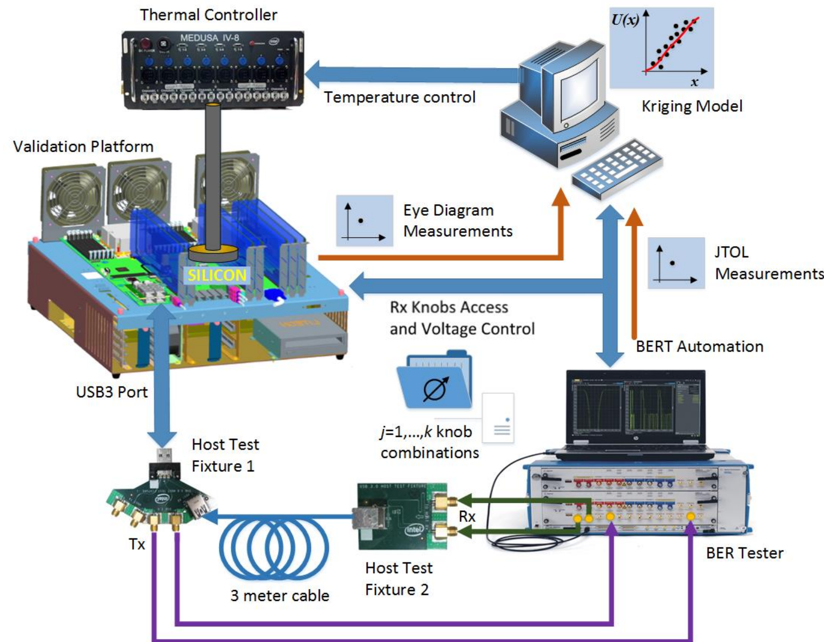


Fig. 4.12 The holistic methodology test setup for USB system margining and JTOL optimization.

commands to the BER tester to sweep the injected jitter amplitude and frequencies. Then, we measure system margins and JTOL and record results for each set of Rx EQ coefficients.

Following the SBO methodology described in Section 4.4 to solve problem (4-21) that uses the objective function (4-22) as a figure of merit, an optimal set of EQ coefficient values was found. The set of values found were verified by measuring the Rx inner eye height/width as well as JTOL using a commercial device. The EQ settings obtained through the proposal showed an improvement of 125% on eye diagram area as compared to the initial EQ settings, and a 32%

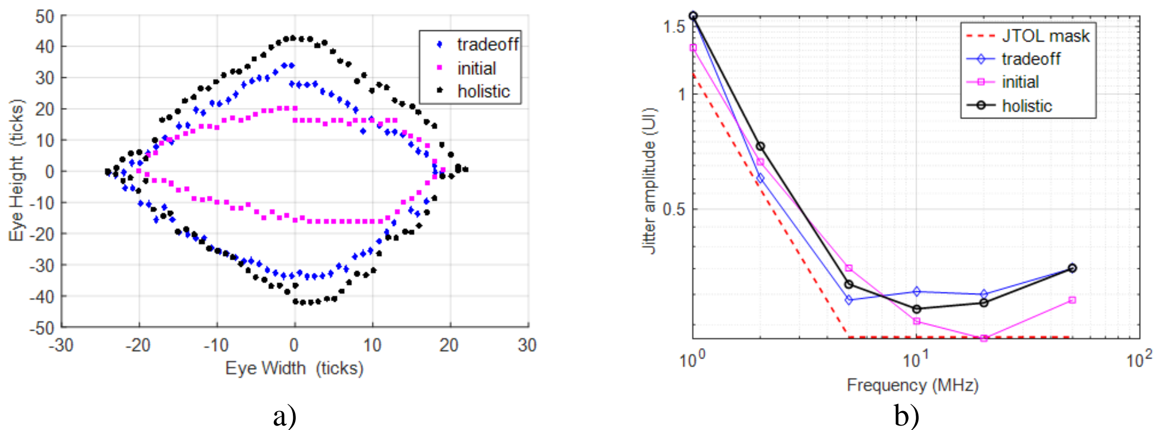


Fig. 4.13 USB3 results comparing the proposed methodology against the initial design and the trade-off approach: a) eye width versus eye height, b) JTOL testing results.

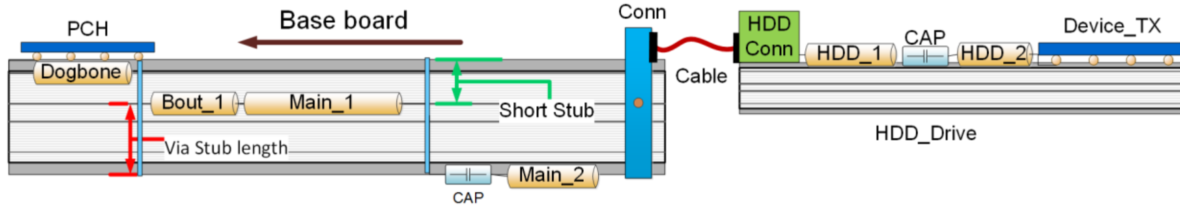


Fig. 4.14 SATA Rx channel topology.

improvement as compared with the traditional (tradeoff) approach, as shown in Fig. 4.13a. Similarly, the JTOL results show a substantial improvement with margins well above the specification limit template, as seen in Fig. 4.13b. The efficiency of this approach was also demonstrated by a significant time reduction on post-silicon validation: while the traditional process requires days for a complete optimization, the method proposed here can be completed in a few hours.

4.5.2 Test Case 2: SATA3

A similar scenario to the USB3 topology is found in the SATA3 channel, which also includes board TLs, several via transitions and I/O card connectors, however, a 1 m SATA cable is used to connect the base board to the device I/O card, as illustrated in Fig. 4.14. Fig. 4.12 also applies in general to the test setup used for SATA3, with the exception of replacing the respective test fixtures and switching the 3 m cable for a SATA3 compliance interconnect channel.

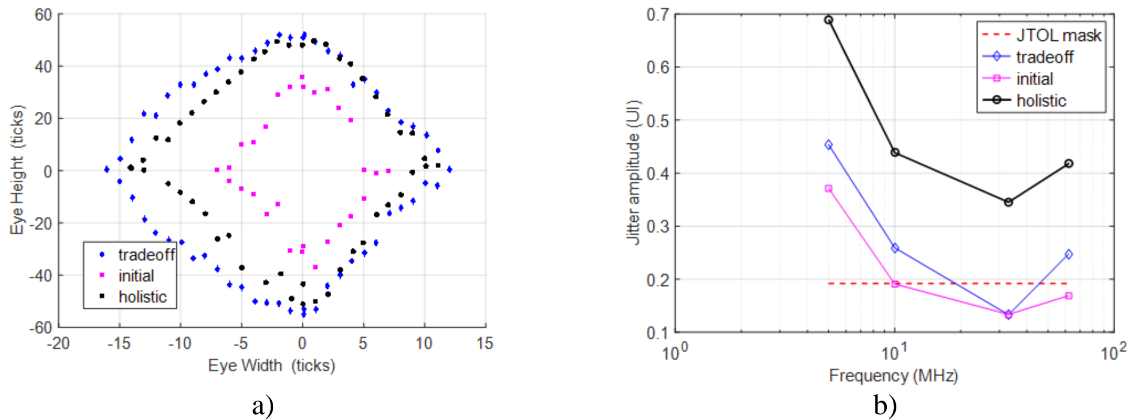


Fig. 4.15 SATA results comparing the proposed methodology against the initial design and the trade-off approach: a) eye width versus eye height, b) JTOL testing results.

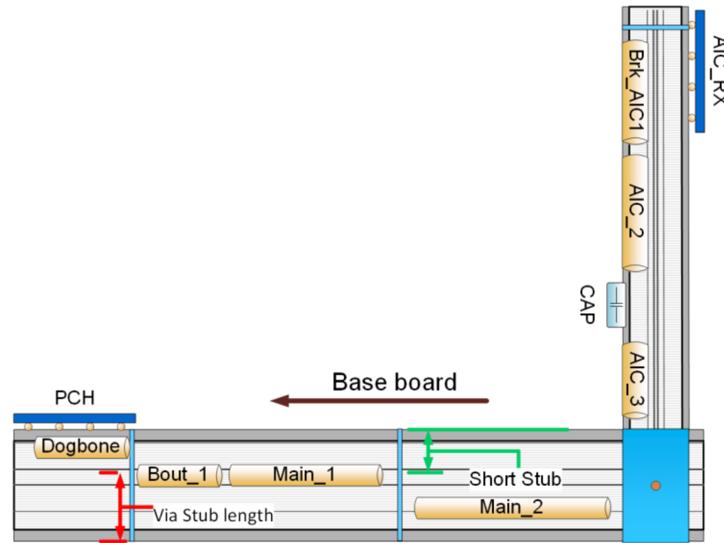


Fig. 4.16 PCIe Gen3 Rx channel topology.

The eye diagram area measured when using the EQ coefficients obtained through the holistic methodology shows a 182% improvement against the initial values, as depicted in Fig. 4.15a. The tradeoff approach derives a slightly larger eye area than the one obtained with the proposal. However, the JTOL results from the tradeoff approach fall below the spec mask at 33 MHz, as seen in Fig. 4.15b, rendering a compliance failure. Thus, it is clear in the SATA3 case that with the holistic approach both the eye diagram and the JTOL margins are optimized. Furthermore, the execution following the proposal took less than 30% of the time required for the tradeoff approach to reach a passing solution for both type of measurements.

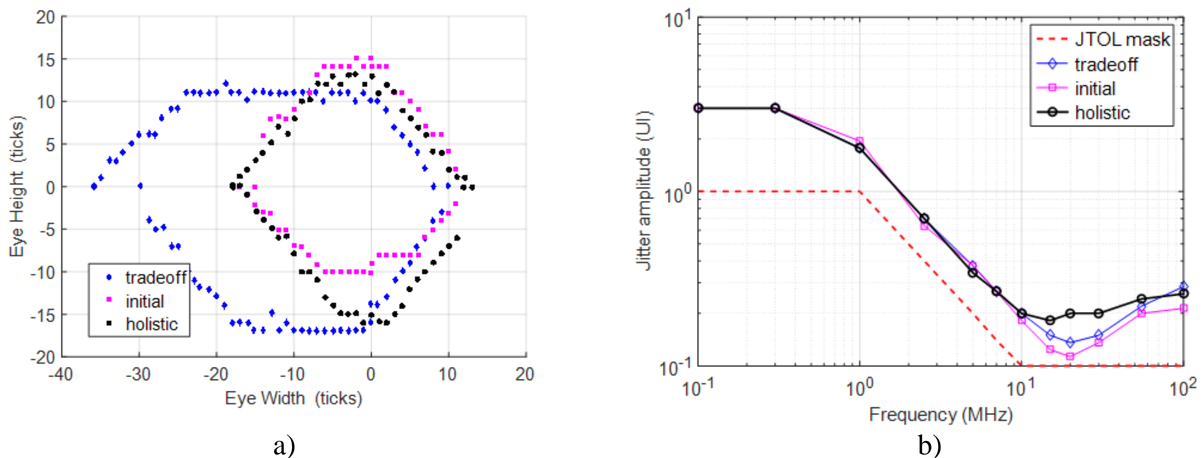


Fig. 4.17 PCIe results comparing the proposed methodology against the initial design and the trade-off approach: a) eye width versus eye height, b) JTOL testing results.

4.5.3 Test Case 3: PCIe

Fig. 4.16 shows the PCIe topology implemented. As in the previous test cases, the PCIe topology includes the Tx driver, the base board TLs and via transitions. It also includes a slot connector and an add-in card in which TLs and other internal devices are found. In the PCIe test setup, a compliance load board is used to connect the measuring instruments, as seen in Fig. 4.16, instead of the test fixtures and cables shown in Fig. 4.12 for USB3 and SATA3.

Results from the PCIe test case provide a clear example of the role of asymmetries in the objective function discussed in Sub-section 4.3.2. Fig. 4.17a shows the PCIe functional eye diagram results, where the smallest area is obtained with the initial Rx EQ coefficients. The area obtained with the holistic approach is 14% larger than the area measured with the initial Rx EQ settings. The center of both of these eyes is located near the 0-tick value in both axis, thus the width and height asymmetry values are low. The area obtained from the tradeoff approach is the largest from the three eyes, however, the large asymmetry seen on the horizontal axis could eventually lead to system failures (see Fig. 4.17a). Additionally, the JTOL results obtained with the holistic approach show the largest margins with respect to the specification limits, as shown in Fig. 4.17b. As with the other two test cases, validation time was significantly decreased using the holistic approach, in this test case by up to 70% with respect to the traditional trade-off approach.

4.6. Conclusions

In this chapter it was demonstrated a holistic optimization approach that merges system margining and jitter tolerance measurements for PHY tuning during industrial post-silicon validation. The method uses Kriging to build a surrogate model for efficient optimization, and a novel objective function based on system margining and jitter tolerance measurements. The experimental results, tested on three different HSIO links on a real industrial validation platform, demonstrated the efficiency of the method to deliver optimal margins while ensuring jitter tolerance compliance, showing a substantial improvement for both system margins and jitter tolerance as compared with the current industrial practice, and dramatically accelerating the typical time required for PHY tuning.

5. Ethernet Transmitter Equalization by Direct Optimization

Enhanced small form-factor pluggable (SFP+) is a specification for a new generation of optical modular transceivers. The devices are designed for use with small form factor (SFF) connectors, and offer high speed and physical compactness. SFP+ modules require high-quality ASIC/SerDes Tx because IEEE and fibre channel standards place strict requirements on the optical interface, and linear/limiting SFP+ module types have Tx paths that do not correct for timing jitter. This introduces a design challenge to guarantee performance over PVT conditions. Adjusting the Tx equalization across PVT and different interconnect channels can be a time-consuming task in post-silicon validation. In order to overcome this problem, this chapter proposes a direct optimization method based on a suitable objective function formulation to efficiently tune the Tx equalizer and optimize the eye diagram to successfully comply with industrial specifications.

5.1. Introduction

The development of high speed Internet has driven data-transmission technology to fully commercialize on 10 Gbps data rates. One of the key components in the PHY is the transceiver module, which enables transmit and receive operations at the end of each fiber optic link. Transceiver modules, such as some Ethernet protocols like 10- Gigabit Small Form Factor Pluggable (XFP/SFP) and Enhanced SFP (SFP+), are regulated by specifications that ensure consistency between suppliers with requirements for eye mask measurements. These eye mask definitions specify Tx output performance in terms of voltage amplitude and time to ensure far-end Rx can reliably recognize the two logic levels in the presence of timing noise and jitter [ANRITSU-10]. However, as technology moves towards higher data rates, ISI has a significant impact on signal integrity and timing, which results in poor eye diagrams [Hall-00]. As described in Section 2.2, ISI is defined as one logic symbol interfering with a subsequent symbol; it is

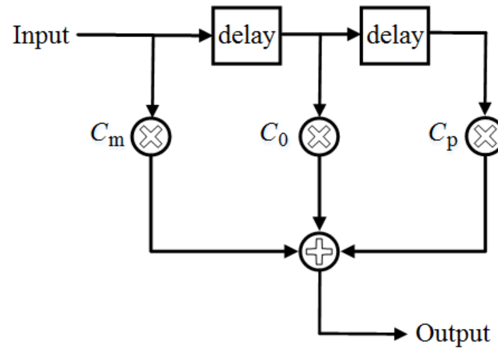


Fig. 5.1 Block diagram of a 3-tap transmit FIR filter.

typically caused by channel impairments such as frequency dependent losses [Guo-08], mode conversion, and multiple reflections due to characteristic impedance discontinuities. In order to mitigate ISI and other undesired effects, adding pre-emphasis and de-emphasis circuits at the Tx is extensively used to adjust the signal prior to the influence of the channel [Higashi-05]. Because of their inherent stable response and easily achievable linear phase property, the FIR filter is commonly used for emphasis circuits [Higashi-05]. The core operations in FIR filters involves multiplication and accumulation of filter coefficients with the input digital data, and those can be realized using as many multipliers and adders as the number of filter coefficients, respectively [Reddy-15]. Per IEEE standard for Ethernet Section 5, clause 77 [IEEE-15], the equalization for SFP+ Tx may be accomplished with a FFE 3-tap FIR filter. Fig. 5.1 shows a block diagram of a FFE 3-tap FIR filter, where C_{m}, C_0 and C_{p} represent the three filter coefficients.

The output signal of the FIR filter is represented as

$$y(t) = \sum_{i=0}^{N} c_i x(t - iT_d) \tag{5-1}$$

where c_i are the tap coefficients, N is the total tap number, and the delay per tap T_d is 1 unit interval (UI). The filter response can be adjusted by controlling the tap number and coefficients values.

Many simplifications in the FIR design implementation can be made when the coefficients are constant. However, FIR filters with reconfigurable coefficients are required in many application scenarios [Kumm-13], where the filter order can be dynamically changed depending on the amplitude of both the filter coefficients and the inputs. These filters are useful for equalization techniques in HSIO links to cancel any undesired effect, such as Tx jitter, attenuation or ISI, among others [Rangel-Patiño-17b]. SFP+ Tx FIR filter is not self-adaptive, and then tuning is required during post-silicon validation. The current post-silicon practices to perform the

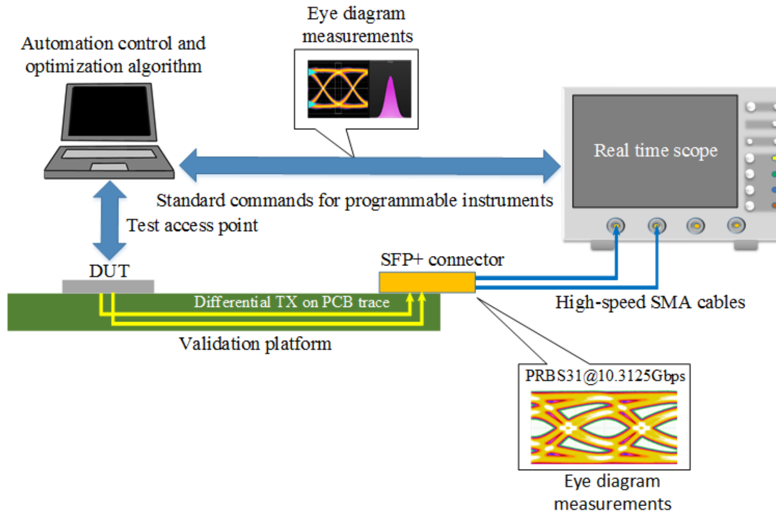


Fig. 5.2 Test setup for SFP transmitter optimization.

coefficients tuning are based on an exhaustive enumeration method that consumes a large amount of validation time and resources. A recent work [Dhanesh-17] proposed a new methodology based on an empirical algorithm that improves substantially the time for SFP coefficients tuning, but still requires days to obtain a set of optimal coefficients values. There have been several FIR filter coefficients optimization techniques reported in the literature [Y.Cheng-10], [Kumm-13], [Reddy-15]; however, all of these techniques are applied only at design simulation level.

This chapter essentially reproduces the work in [Duron-Rosales-17], where it is proposed a simple yet efficient optimization technique for a reconfigurable FIR filter used in a SFP+ Tx, by defining an effective objective function and by using direct numerical optimization in a post-silicon validation platform. The chapter is organized as follows. Sections 5.2 and 5.3 describe the system test setup and system measurements, respectively. The objective function formulation and the optimization procedure are presented in Section 5.4. Finally, Sections 5.5 and 5.6 present the results obtained and the conclusions, respectively.

5.2. System Test Setup

The test setup is shown in Fig. 5.2. The eye diagram of the DUT is measured at the end of the SFP+ connector using subminiature (SMA) cables connected to a high-speed, real time oscilloscope. The oscilloscope must have enough bandwidth capabilities to measure at least the 5th harmonic of the incoming signal and capabilities for S-parameters de-embedding to eliminate

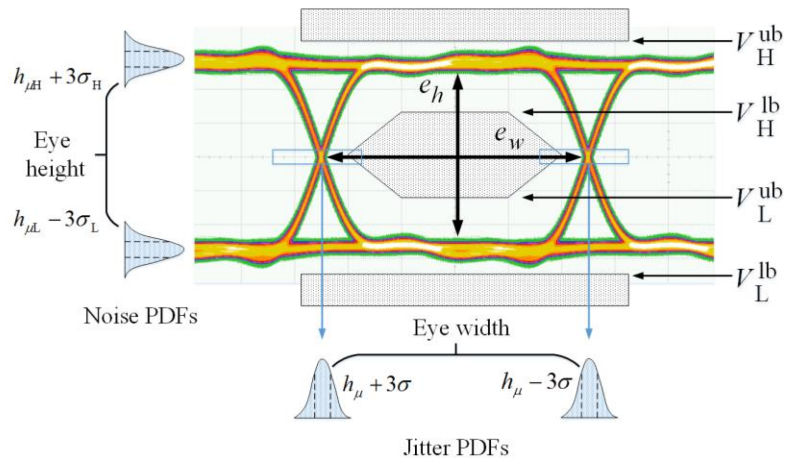


Fig. 5.3 Eye diagram and SFP+ Tx mask.

cables insertion loss. A computer executes the algorithm using a fully automated control by accessing the DUT through the TAP registers for the FFE coefficients, sending instruments commands for eye diagram, jitter and histogram measurements on the scope.

5.3. System Measurements

An eye diagram is a useful tool for understanding signal impairments in the PHY of an HSIO data systems, verifying Tx output compliance, and revealing the amplitude and time distortion elements that degrade the BER for diagnostic purposes. Histograms are used to statistically analyze time and amplitude data of eye diagrams, offering important computational information when observing impairments in HSIO signals. The definition for eye height is derived from computing the difference between the inner 3σ points on the inside of the histograms of the one and zero levels, as shown in Fig. 5.3, where σ is the standard deviation of the histograms. The eye width is essentially the effective distance between the inner two 3σ points on the time histograms. To compute jitter, the time variances of the rising and falling edges of an eye diagram at the crossing point are captured, as shown in Fig. 5.3. The time histogram, shown below the eye pattern, is analyzed to determine the amount of jitter. The peak-to-peak jitter is defined as the full width of the histogram, meaning all data points present.

5.4. Objective Function Formulation and Optimization

Let $\boldsymbol{R}_E \in \Re^3$ denote the signal integrity system response, which consists of the eye amplitude histogram mean high $h_{\mu\mathrm{H}}$, the histogram mean low $h_{\mu\mathrm{L}}$, and the total jitter J_T on the eye diagram,

$$\boldsymbol{R}_E = \boldsymbol{R}_E(\boldsymbol{x},\boldsymbol{\psi}) = \left[h_{\mu\mathrm{H}}(\boldsymbol{x},\boldsymbol{\psi}) \quad h_{\mu\mathrm{L}}(\boldsymbol{x},\boldsymbol{\psi}) \quad J_\mathrm{T}(\boldsymbol{x},\boldsymbol{\psi})\right]^\mathrm{T} \tag{5-2}$$

This signal integrity system response is a function of the PHY tuning settings $\boldsymbol{x} \in \Re^N$ (FIR tap coefficients), and the operating conditions $\boldsymbol{\psi}$ (voltage and temperature). The eye height $e_\mathrm{h} \in \Re$ is obtained from,

$$e_\mathrm{h}(\boldsymbol{x},\boldsymbol{\psi}) = h_{\mu\mathrm{H}}(\boldsymbol{x},\boldsymbol{\psi}) + 3\sigma_\mathrm{H} + h_{\mu\mathrm{L}}(\boldsymbol{x},\boldsymbol{\psi}) - 3\sigma_\mathrm{L} \tag{5-3}$$

where σ_H and σ_L are the standard deviation of the histogram mean high and the histogram mean low, respectively.

Since the goal is to maximize the eye diagram, the initial objective function consists of $-e_\mathrm{h}$, however as the eye width is a function of the total jitter J_T, it must to consider J_T in the objective function formulation.

The e_h and J_T must be scaled by weighting factors w_1, w_2, $\in \Re$ such they become comparable. The values of these weighting factors can be selected by using initial e_h, and J_T measurements. Therefore, the objective function is defined as

$$u(\boldsymbol{x}) = -w_1\left[e_\mathrm{h}(\boldsymbol{x},\boldsymbol{\psi})\right] + w_2\left[J_\mathrm{T}(\boldsymbol{x},\boldsymbol{\psi})\right] \tag{5-4}$$

with w_1, and w_2 are calculated from

$$w_1 = \frac{2}{\frac{1}{k}\sum_{i=1}^{k} e_\mathrm{h}(\boldsymbol{x}^{(i)})} \tag{5-5}$$

$$w_2 = \frac{1}{\frac{1}{k}\sum_{i=1}^{k} J_\mathrm{T}(\boldsymbol{x}^{(i)})} \tag{5-6}$$

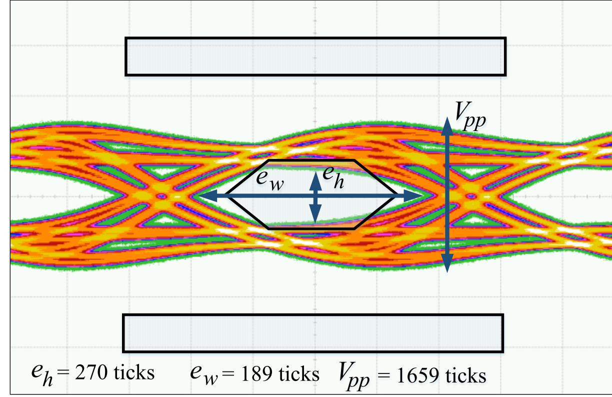


Fig. 5.4 SFP eye diagram over mask before optimization.

where $\boldsymbol{x}^{(i)}$ are k randomly distributed base points for initial measurements of eye height and total jitter.

The optimization problem for the signal integrity system is

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} u(\boldsymbol{x}) \tag{5-7}$$

with $u(\boldsymbol{x})$ defined by (5-4).

The optimization problem will be now modified such that the optimal set of coefficients maximizes the eye diagram without exceeding the mask limits. The new optimization problem can be defined through a constrained formulation,

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} u(\boldsymbol{x}) \text{ subject to } l_1(\boldsymbol{x}) \le 0,\, l_2(\boldsymbol{x}) \le 0 \tag{5-8}$$

with

$$l_1(\boldsymbol{x}) = (h_{\mu\mathrm{H}} + 3\sigma_{\mathrm{H}}) - V_{\mathrm{H}}^{\mathrm{ub}} \tag{5-9}$$

$$l_2(\boldsymbol{x}) = V_{\mathrm{L}}^{lb} - (h_{\mu\mathrm{L}} - 3\sigma_{\mathrm{L}}) \tag{5-10}$$

where $V^{\mathrm{ub}}{}_{\mathrm{H}}$ and $V^{\mathrm{lb}}{}_{\mathrm{L}}$ are the eye mask specification limits: voltage high upper bound, and voltage low lower bound, respectively.

A more convenient unconstrained formulation can be defined by adding a penalty term, as

$$U(\boldsymbol{x}) = -u(\boldsymbol{x}) + \rho_0^l \left| L(\boldsymbol{x}) \right|^2 \tag{5-11}$$

where $L(\boldsymbol{x})$ is the eye mask limit penalty function, defined as

$$L(\boldsymbol{x}) = \max\left\{0, l_1(\boldsymbol{x}), l_2(\boldsymbol{x})\right\} \tag{5-12}$$

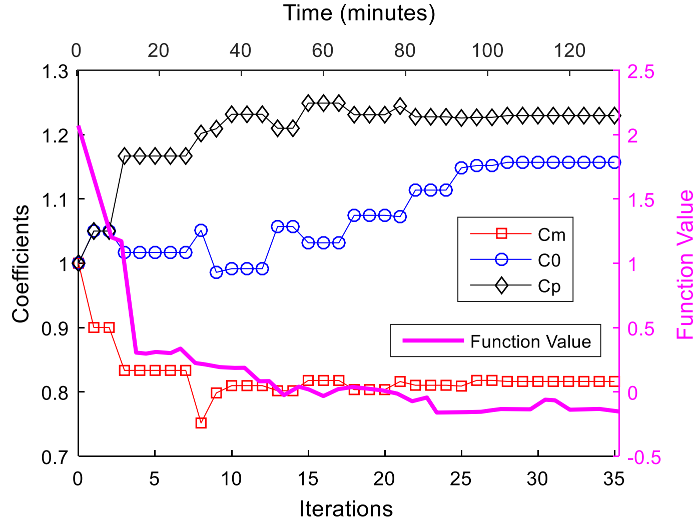


Fig. 5.5 SFP FIR normalized coefficients responses and function values across iterations.

The optimal solution depends on the value of the penalty coefficient $\rho_0^l \in \Re$,. Here ρ_0^l is defined as

$$\rho_0^l = \frac{|u(\boldsymbol{x}^{(0)})|}{\left|\max\{l_1(\boldsymbol{x}^{(0)}), l_2(\boldsymbol{x}^{(0)})\right|^2} \tag{5-13}$$

where $\boldsymbol{x}^{(0)}$ is the starting point. Then, the objective function to optimize eye diagram and meet eye mask specification is

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} U(\boldsymbol{x}) \tag{5-14}$$

with

$$U(\boldsymbol{x}) = -w_1\left[e_{\rm h}(\boldsymbol{x},\boldsymbol{\psi})\right] + w_2\left[J_{\rm T}(\boldsymbol{x},\boldsymbol{\psi})\right] + \rho_0^l\left|L(\boldsymbol{x})\right|^2 \tag{5-15}$$

The objective is to find the optimal set of FIR coefficients values $\boldsymbol{x}^*$ by solving (5-14) using the Nelder-Mead method [Lagarias-98].

5.5. Results

A PRBS of length ($2^{31}-1$) - PRBS31 - is considered the standard for stressing HSIO circuits to achieve a confidence level in the operating margins of a product. PRBS31 provides a stressful environment to detect RJ, SJ, ISI, and crosstalk. When the input signal to the FIR becomes a PRBS31 with a data rate of at 10.3125Gbps, the resultant eye diagram is shown in Fig. 5.4. Since

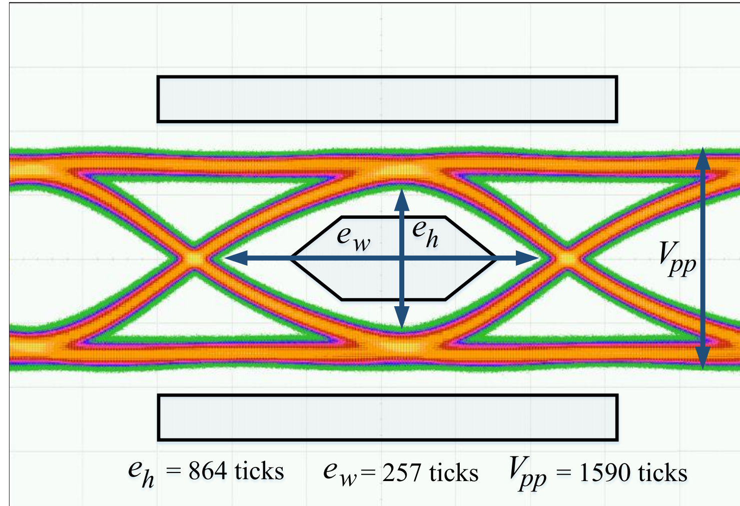


Fig. 5.6 SFP eye diagram over mask after optimization.

the FFE tap coefficients are not properly equalized, the eye diagram is significantly distorted, with an eye height and eye width of 270 ticks and 189 ticks, respectively. Such e_h and e_w levels are so low that do not meet the required eye mask. Fig. 5.4 also shows the zero crossing points on the horizontal axis are not compressed enough, leading to high jitter measurements. In terms of the vertical axis, the voltage peak-to-peak is 1,659 ticks, which translates into wider noise histograms. Hence, the goal is to optimize the Tx equalization coefficients as a way to compensate for the channel effects, achieving an specs compliant eye diagram.

Through the optimization process defined in Section 5.4, a set of Tx coefficients is found in just 35 iterations, as shown in Fig. 5.5. The optimized equalization coefficients improve substantially with an e_h and e_w, as shown in Fig. 5.6, being now 864 ticks and 257 ticks, respectively, which corresponds to an improvement of 252% on eye diagram area as compared to that one with the initial coefficients. The efficiency of this approach was also demonstrated by a significant time reduction on post-silicon validation. While the traditional process requires 4 days for a complete optimization using an exhaustive approach, the method proposed here can be completed in just 2 hours.

5.6. Conclusions

A direct optimization approach is proposed to find the best Tx FIR filter settings to counteract ISI and other undesired effects in high-speed data transmission. The optimal set of FFE

tap coefficients are determined by numerical optimization of an objective function expressed in terms of the required specifications on eye mask. Subsequently, the optimized coefficients are evaluated by measuring the real eye diagram of the physical system, showing a great mitigation of the ISI effects, and accelerating the typical required time for Tx coefficients tuning. The approach allows fulfilling in an efficient manner strict IEEE and fibre channel standards as applied to high-speed interconnects based on optical interfaces, significantly enhancing current industrial practices in this arena.

6. PCIe Transceiver Equalization by Direct Optimization

PCIe is a high-performance interconnect architecture widely adopted in the computer industry. PCIe data rates increase on every new generation. To mitigate channel effects due to the increase in transmission speeds, the PCIe specification defines requirements to perform EQ at the Tx and at the Rx. During the EQ process, one combination of Tx/Rx EQ coefficients must be selected to meet the performance requirements of the system. Testing all possible coefficient combinations is prohibitive. Current industrial practice consists of finding a subset of combinations at post-silicon validation using maps of EQ coefficients, which are obtained by measuring the eye height, eye width, and the eye asymmetries of the received signal. Given the large number of electrical parameters and the multiplicity of signal eyes that are produced by on-die probes for observation, finding this subset of coefficients is often a challenge. In order to overcome this problem, a direct optimization method based on a suitable objective function formulation to efficiently tune the Tx and Rx EQ coefficients to successfully comply with the PCIe specification is presented in this chapter. The proposed optimization approach is based on a low-cost computational procedure combining pattern search and Nelder-Mead methods to efficiently solve an objective function with many local minima, and evaluated by lab measurements on a realistic industrial post-silicon validation platform.

6.1. Introduction

PCIe [Wilen-03] is a packet based high-speed point-to-point interconnection technology that evolves with new computer industrial demands [PCISIG-17]. PCIe allows a star-topology architecture with strong similarity to the modern switched Ethernet fabric, and it is the primary interface for a host CPU to connect with I/O devices. The direct memory access (DMA) and other resources are also available to PCIe devices without having to share the data bus with other devices

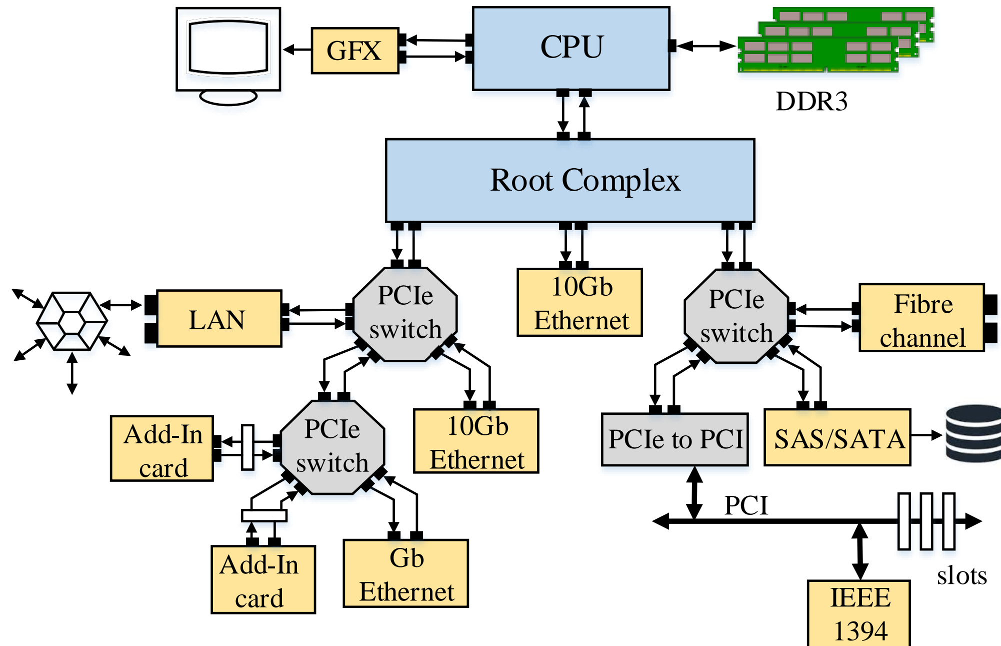


Fig. 6.1 PCIe switched architecture. Figure taken from [PCISIG-17].

in the same system. Fig. 6.1 illustrates an example of a PCIe switched architecture composed of a root complex (RC) that connects the CPU, the memory subsystem, and the graphics controller to the I/O devices, multiple endpoints (I/O devices), switch components, and a PCIe to PCI bridge, all interconnected via PCIe links. As illustrated in Fig. 6.1, an RC may support one or more PCIe ports. Each interface defines a separate hierarchy domain that may be composed of a single endpoint or a sub-hierarchy containing one or more switch components and endpoints [PCISIG-17].

The PCIe bandwidth has been scaled by means of multiple lanes (×1, ×2, ×4, ×8, ×16, and ×32) and interconnections rates have increased from 2.5 Gb/s of the first generation (PCIe1), to 5 Gb/s (PCIe2) and 8 Gb/s (PCIe3) [Gatto17]. PCIe has been continually enhancing its performance, and the next generation (PCIe4) is expected to operate at 16 Gb/s [Gonzales-15], [Ren-15], targeting 512 Gb/s capacity over 32 lanes. However, as transmission speeds increase, the transmission channel effects such as reflections, electromagnetic coupling, and attenuation are more severe, causing the signals to become more susceptible to errors [Casper-07], [M.Li-07], [Stojanovic-04]. Additionally, PCIe channels are bandwidth-limited by default and cause large signal attenuation at high frequencies. This generates distortion and spreading of the transmitted signal over multiple symbols, causing ISI, which can make the signal unreadable at the Rx, producing bit errors and too closed eye diagrams. The most practical solution to this problem is

signal conditioning to open the eye diagram [Rangel-Patiño-17a] before the Rx samples the data, being on-chip EQ the most practical way to compensate for the channel attenuation [ALTERA-13]. PCIe3 specification defines the requirements to perform EQ at the Tx and/or at the Rx to mitigate undesired effects and minimize the BER. For the Tx EQ, the signal can be reshaped before the signal is transmitted in an effort to overcome the distortion introduced by the channel. At the Rx, the signal can be reconditioned to improve the signal quality.

PCIe3 specification defines an adaptive mechanism for EQ to determine the optimum value of the Tx and Rx EQ coefficients within a fixed time limit. A typical PCIe system may have hundreds of combinations of EQ coefficients, and some of these combinations will produce better EQ results than others. Testing every coefficients combination using an exhaustive enumeration method to find the best one is impractical, as this approach usually consumes a large amount of time. In order to reduce the selection time, the current practice is to find out a subset of coefficient combinations during post-silicon validation, and then program it into the system BIOS. The current industrial method to find out the best subset of coefficients consists of using maps of EQ coefficients, which are obtained by measuring the eye height, eye width, and the eye asymmetries of the received signal. These maps show how the Rx performs at different locations of the coefficient space. These EQ maps are intuitive visual indicators that help experienced post-silicon validation engineers to find the optimal coefficient combination by inspection. The method consists of finding the set of coefficients that qualify the eye-width, eye-height, and eye diagram asymmetries as near optimal. However, data collection to generate the EQ maps consumes a very large amount of post-silicon validation schedule and resources.

In this chapter, it is proposed a simple yet efficient optimization methodology to find out the optimal subset of coefficients for the Tx and Rx in a PCIe equalization process. The procedure implies defining an effective objective function, and then applying a direct numerical optimization method using lab measurements in an industrial post-silicon validation platform. To overcome the problem of multiple local minima in the measurement-based objective function, an efficient combination of pattern search and Nelder-Mead methods is employed. The obtained eye-diagram results confirm the effectiveness of the proposed approach.

The present chapter expands the work in [Rangel-Patiño-18a]. The organization of the chapter is as follows. Section 6.2 describes the PCIe EQ process. The PCIe link equalization based on Tx EQ coefficient matrix maps is presented in Section 6.3. The objective function formulation

and the optimization procedure are presented in Section 6.4. The system test setup and system measurements are described in Section 6.5. Finally, the results are discussed in Section 6.6, and conclusions are given in Section 6.7.

6.2. PCI Express Equalization

PCIe3 provides a bit rate of 8 Gb/s while still using the same copper channel as PCIe2. PCIe channels allow up to 22 dB of attenuation at 4 GHz. The high frequency components are therefore diminished while crossing such a bandwidth-limited channel. To mitigate the effects of ISI and other channel-induced noise impairments, the PCIe3 specification defines the provision of performing equalization at the transmitter and at the Rx.

6.2.1 Tx and Rx Equalizers

Most Tx SerDes implementations comprise a FFE 3-tap FIR filter. Fig. 5.1 shows a block diagram of a FIR filter, where C_{m}, C_0, and C_{p} represent the three filter taps coefficients. The pre-cursor (C_{m}) and post-cursor (C_{p}) coefficients refer to whether the FFE filter taps work on an advanced or delayed signal with respect to time. Through the FFE filter, the serial data signal is delayed by several flip-flops which implement the filter taps. Three consecutive received pulses (v_{nm}, v_{n}, v_{np}) are multiplied with the three different filter tap coefficients, and the results are summed and driven to the serial data output [Duron-Rosales-17], [Rangel-Patiño-18a]. The filter response can be then adjusted by controlling the tap coefficients values. Therefore, the output signal (v_{out}) of the FIR filter is given by

$$v_{\mathrm{out}} = v_{\mathrm{nm}} C_{\mathrm{m}} + v_{\mathrm{n}} C_0 + v_{\mathrm{np}} C_{\mathrm{p}} \tag{6-1}$$

The pre-emphasis/de-emphasis is implemented at the Tx driver by pre-conditioning the signal before transmitting it through the channel. Through this mechanism, the high-frequency content of the transmitted signal is amplified (pre-emphasis) or the low-frequency content of the signal is decreased (de-emphasis) [Rangel-Patiño-17b].

As described in Section 2.5, the EQ topology at the Rx can be a combination of a CTLE that works independently of the clock recovery circuit, and a DFE. The CTLE is a simple one tap

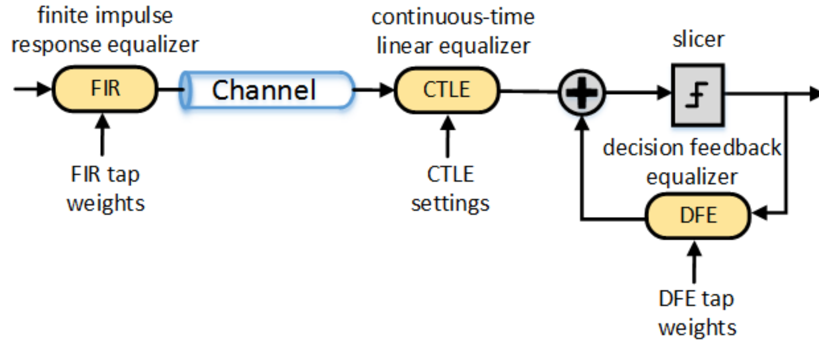


Fig. 6.2 A PCIe channel with Tx and Rx equalizers.

coefficient (C_r) continuous-time circuit with high-frequency gain boosting, whose transfer function can compensate the channel response [Rangel-Patiño-18a]. The topology is basically a simple RC network, as shown in Fig. 2.6. The differential-pair emitter resistor attenuates the low-frequency signals while the capacitor allows the high-frequency signal content, thus resulting in high frequency gain improving.

The DFE topology is the optimal option for systems in which noise limits the amount of EQ that can be done. The signal is entered to a slicer circuit which decides whether the input signal is a "0" or "1" (see Fig. 6.2). Each DFE tap is multiplied by its corresponding weight value, and the results are summed to correct the amplitude of the input signal [Rangel-Patiño-18a], [Stauffer-08]. Fig. 6.2 shows the simultaneous implementation of Tx and Rx equalizers in a PCIe channel.

6.2.2 Equalization Process

PCIe3 specification establishes some predefined set of values for the three Tx coefficients, which are referred to as presets, and then are adaptively changed during the link training and equalization procedure, in which both downstream port and upstream port devices (see Fig. 6.3) negotiate each to other the Tx EQ values to guarantee a BER less than 10^{-12}. Since the Tx does not know the channel parameters, the Tx EQ coefficients are computed at the upstream port by the coefficient adaptation algorithm in the medium access control (MAC) layer using the received signal, as shown in Fig. 6.3. Then, these coefficients are communicated to the downstream port by using the PCIe protocol. The Tx at the downstream port then applies the received coefficients setting to the Tx EQ circuitry. The Rx drives two types of quality feedback by measuring the eye opening or evaluating eye edge ISI. This process of computing the coefficients, communicating

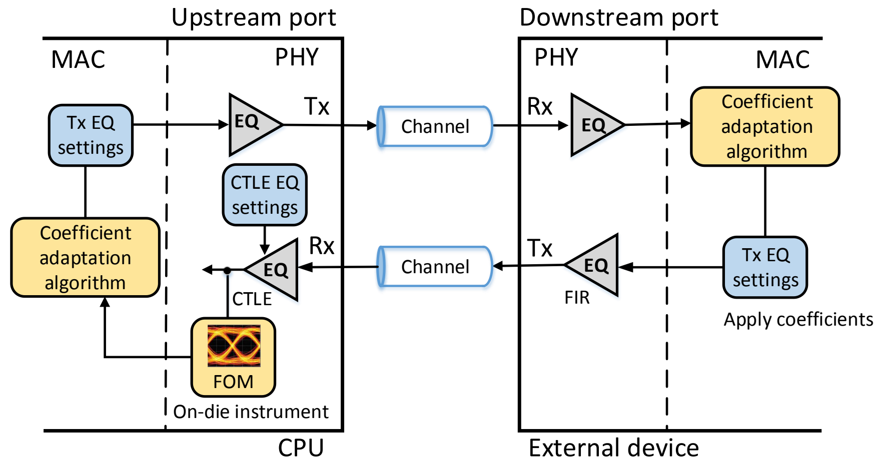


Fig. 6.3 PCIe Tx/Rx adaptive equalization.

them to the Tx, and checking the signal quality can be repeated multiple times until the required BER is achieved [Kumar], [PCISIG-12]. The equalization procedure consists of four phases [PCISIG-11]:

Phase 0: Downstream port transmits the Tx preset values to the upstream port running either at Gen1 or Gen2.

Phase 1: Downstream port and upstream port handshake and ensure a BER < 10^{-4} before the link is ready to move to the next phase.

Phase 2: Upstream port adjusts the Tx equalization settings of the downstream port together with its Rx settings independently for each of the lanes on the link. This phase must ensure that the Rx at upstream port have a BER < 10^{-12}.

Phase 3: Similar to Phase 2, but the downstream port adjusts the Tx equalization settings of the upstream port together with its Rx settings independently for each of the lanes on the link. This phase must ensure that the Rx at downstream port has a BER < 10^{-12}.

6.3. Transmitter Equalization Coefficient Matrix

The values of the Tx coefficients are subjected to the following protocol constraints:

$$\left|C_{\mathrm{m}}\right|+\left|C_{0}\right|+\left|C_{\mathrm{p}}\right|=1 \text{ subject to } C_{0}>0,\, C_{\mathrm{m}}\leq 0,\, C_{\mathrm{p}}\leq 0 \tag{6-2}$$

These constraints are implemented by determining only C_{m} and C_{p} to fully define v_{out} from (6-1), being C_0 implied by (6-2). Additionally, the coefficients range and tolerance are constrained

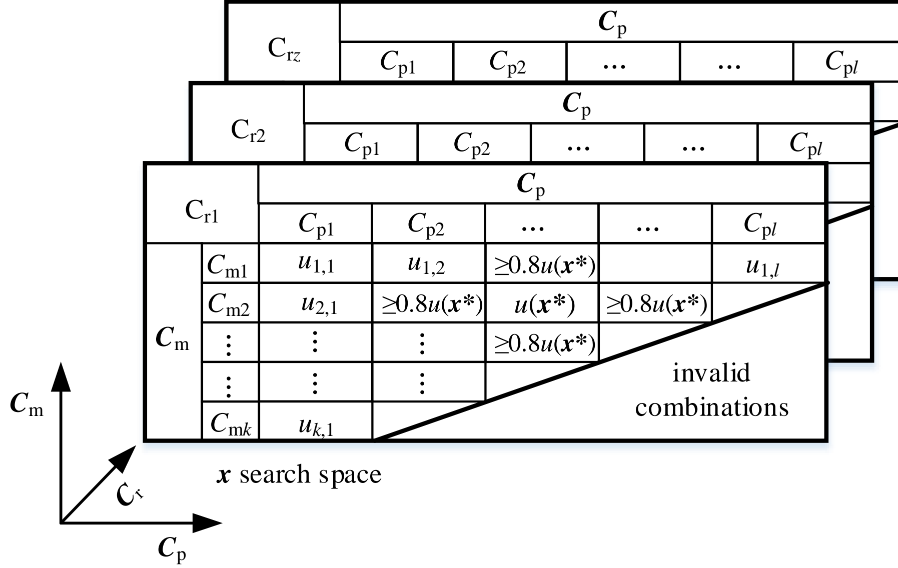


Fig. 6.4 PCIe EQ map coefficients search space for optimization.

by the some requirements, as follows:

a) The coefficients must support all eleven values for the presets, and their respective tolerances as defined by the Tx preset ratios table in the PCIe specification [PCISIG-17].

b) In order to keep the output transmitted power constant with respect to coefficients, the full swing (FS) which indicates the maximum differential voltage that can be generated by the Tx is defined as

$$FS = |C_m| + |C_0| + |C_p| \tag{6-3}$$

c) The flat level voltage should always be greater than the minimum differential voltage that can be generated by the Tx indicated as the low frequency (LF) parameter,

$$C_0 - |C_m| - |C_p| \geq LF \tag{6-4}$$

When the above constraints are applied, the resulting coefficients space may be mapped onto a triangular matrix, as shown in Fig. 6.4, where several EQ maps, one per CTLE coefficient (C_r) value are superimposed. C_m and C_p coefficients are mapped onto the y-axis and x-axis, respectively. Each matrix cell corresponds to a valid combination of C_m and C_p coefficients, and $u(\boldsymbol{x}^*)$ correspond to a combination of C_m, C_p and C_r that results in an eye diagram qualified as optimum as explained later in greater detail. This EQ maps can be used as an intuitive visual indicator of the equalization performance.

The current post-silicon practical method to find the best subset of coefficients for both Tx

and Rx, consists of using these EQ maps, which are obtained by measuring the eye height, eye width, and eye asymmetries of the received signal for each of the C_m and C_p combinations. Three EQ maps are generated for each of the CTLE coefficient (C_r) values, and each lane and device pairing may require one or more EQ maps. The current industrial method, used by experienced validation engineers, consists of visually analyzing each of the EQ maps to select the coefficients C_m and C_p for the FIR filter in the Tx, and C_r for the CTLE in the Rx, that correspond to an eye qualified as optimum (maximum eye height, maximum eye width, and minimum eye asymmetry). However, this has to be performed by ensuring at the same time that the responses around the best C_m, C_p matrix cell are at least 80% of the value of that matrix cell, as illustrated in Fig. 6.4 , to avoid selecting a combination of too-high sensitivity. Due to the large number of EQ maps, finding the optimal subset of coefficients is usually a very challenging task, considering the large number electrical parameters, and the multiplicity of signal eyes that are produced by on-die probes [Iyer-06] for observation.

6.4. Objective Function Formulation and Optimization

The objective is to find the optimal set of coefficients to maximize the functional eye diagram based on margins response. Here the work in [Rangel-Patiño-17a], and [Rangel-Patiño-17b] is followed to define the corresponding objective function. Let $\boldsymbol{R}_m \in \Re^2$ denote the electrical system margins response, which consists of the width and height of the functional eye diagram,

$$\boldsymbol{R}_m = \boldsymbol{R}_m(\boldsymbol{x}, \boldsymbol{\psi}, \boldsymbol{\delta}) = \left[e_w(\boldsymbol{x}, \boldsymbol{\psi}, \boldsymbol{\delta}) \quad e_h(\boldsymbol{x}, \boldsymbol{\psi}, \boldsymbol{\delta}) \right]^T \tag{6-5}$$

where $e_w \in \Re$ and $e_h \in \Re$ are the width and height, respectively, of the eye diagram. The eye width and height are function of the coefficient values (C_m, C_p, C_r) contained in vector $\boldsymbol{x}$, and they also depend on the operating conditions ($\boldsymbol{\psi}$) and the connected devices ($\boldsymbol{\delta}$).

Since the objective is to find the optimal set of coefficient values to maximize the functional eye diagram area, the initial objective function to be minimized is defined as

$$u(\boldsymbol{x}) = -\left[e_w(\boldsymbol{x}, \boldsymbol{\psi}, \boldsymbol{\delta}) \right] \left[e_h(\boldsymbol{x}, \boldsymbol{\psi}, \boldsymbol{\delta}) \right] \tag{6-6}$$

Based on the operating conditions and devices, the eye diagram may be decentered with respect to the eye-width (asymmetry e_{wa}), eye-height (asymmetry e_{ha}), or both. Hence, the objective function must consider these asymmetries. The area of the eye diagram and the

asymmetries are scaled by weighting factors w_1, w_2, $w_3 \in \Re$ such that they become comparable. Hence, a better objective function is defined as

$$u(\boldsymbol{x}) = -w_1[e_{\mathrm{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})][e_{\mathrm{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] + w_2[e_{\mathrm{wa}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] + w_3[e_{\mathrm{ha}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] \tag{6-7}$$

with w_1, w_2, and w_3 calculated from

$$w_1 = \frac{3}{\frac{1}{n}\sum_{i=1}^{n}[e_{\mathrm{w}}(\boldsymbol{x}^{(i)})][e_{\mathrm{h}}(\boldsymbol{x}^{(i)})]} \tag{6-8}$$

$$w_2 = \frac{1}{\frac{1}{n}\sum_{i=1}^{n} e_{\mathrm{wa}}(\boldsymbol{x}^{(i)})} \tag{6-9}$$

$$w_3 = \frac{1}{\frac{1}{n}\sum_{i=1}^{n} e_{\mathrm{ha}}(\boldsymbol{x}^{(i)})} \tag{6-10}$$

where $\boldsymbol{x}^{(i)}$ are n randomly distributed base points ($i = 1, \ldots n$) for initial measurements of eye width and eye height.

The optimization problem for system margining is then defined as,

$$\boldsymbol{x}^* = \arg \min_{\boldsymbol{x}} u(\boldsymbol{x}) \tag{6-11}$$

with $u(\boldsymbol{x})$ defined by (6-7).

As described in Section 6.3, it is required to ensure the optimal system margin response is within a suitable area in the coefficients search space of the EQ map. In order to satisfy this requirement, the four margin responses around $u(\boldsymbol{x}^*)$ must be at least 80% of the value of $u(\boldsymbol{x}^*)$, as shown in Fig. 6.4, where $u_{i,j}$ are the objective function values per (6-7) for the i-th C_{m} and j-th C_{p} values, and

$$\boldsymbol{C}_{\mathrm{m}} = [C_{\mathrm{m}1} \quad \cdots \quad C_{\mathrm{m}k}]^{\mathrm{T}} \quad \text{is the vector of Tx FIR pre-cursor values} \tag{6-12}$$

$$\boldsymbol{C}_{\mathrm{p}} = [C_{\mathrm{p}1} \quad \cdots \quad C_{\mathrm{p}l}]^{\mathrm{T}} \quad \text{is the vector of Tx FIR post-cursor values} \tag{6-13}$$

$$\boldsymbol{C}_{\mathrm{r}} = [C_{\mathrm{r}1} \quad \cdots \quad C_{\mathrm{r}z}]^{\mathrm{T}} \quad \text{is the vector of Rx CTLE coefficient values} \tag{6-14}$$

The optimization problem is now modified such that the optimal set of coefficients maximizes the system margins response without exceeding the limit of $0.8u(\boldsymbol{x}^*)$ in the vicinity. The new optimization problem can be defined through a constrained formulation,

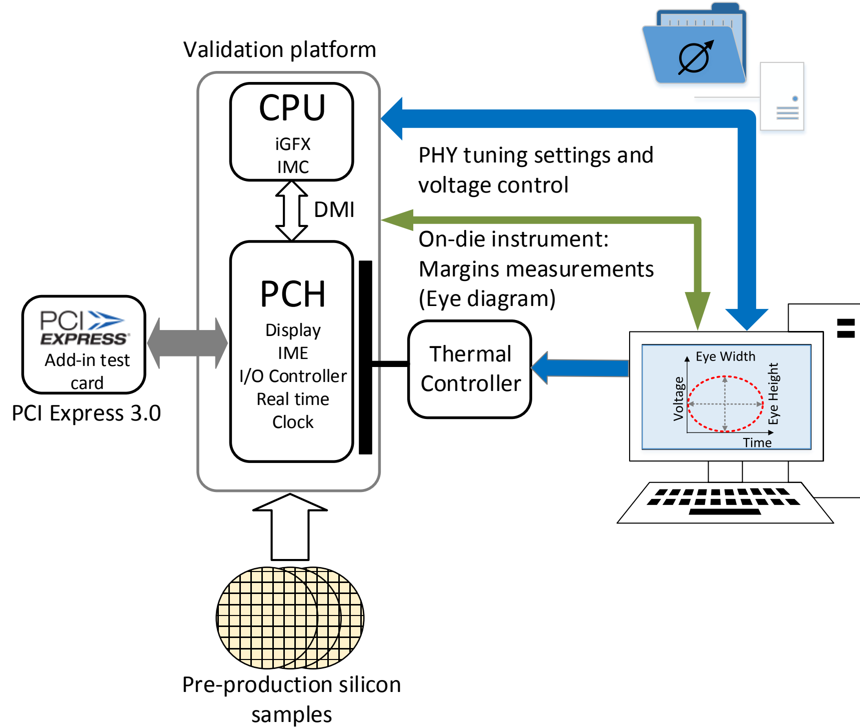


Fig. 6.5 PCI Express test setup: an Intel server post-silicon validation platform.

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} u(\boldsymbol{x}) \text{ subject to } l_1(\boldsymbol{x}) \leq 0, l_2(\boldsymbol{x}) \leq 0, l_3(\boldsymbol{x}) \leq 0, l_4(\boldsymbol{x}) \leq 0 \tag{6-15}$$

with

$$l_1(\boldsymbol{x}) = 0.8u(C_{\mathrm{m}i^*}, C_{\mathrm{r}}, C_{\mathrm{p}j^*}, \boldsymbol{\psi}, \boldsymbol{\delta}) - u(C_{\mathrm{m}i^*+1}, C_{\mathrm{p}j^*}, \boldsymbol{\psi}, \boldsymbol{\delta}) \tag{6-16}$$

$$l_2(\boldsymbol{x}) = 0.8u(C_{\mathrm{m}i^*}, C_r, C_{\mathrm{p}j^*}, \boldsymbol{\psi}, \boldsymbol{\delta}) - u(C_{\mathrm{m}i^*-1}, C_{\mathrm{p}j^*}, \boldsymbol{\psi}, \boldsymbol{\delta}) \tag{6-17}$$

$$l_3(\boldsymbol{x}) = 0.8u(C_{\mathrm{m}i^*}, C_{\mathrm{r}}, C_{\mathrm{p}j^*}, \boldsymbol{\psi}, \boldsymbol{\delta}) - u(C_{\mathrm{m}i^*}, C_{\mathrm{p}j^*+1}, \boldsymbol{\psi}, \boldsymbol{\delta}) \tag{6-18}$$

$$l_4(\boldsymbol{x}) = 0.8u(C_{\mathrm{m}i^*}, C_{\mathrm{r}}, C_{\mathrm{p}j^*}, \boldsymbol{\psi}, \boldsymbol{\delta}) - u(C_{\mathrm{m}i^*}, C_{\mathrm{p}j^*-1}, \boldsymbol{\psi}, \boldsymbol{\delta}) \tag{6-19}$$

where C_{mi^*} and C_{pi^*} are the set of coefficients that maximize the margins response for each of the C_{r} values. Notice that it is assumed in (6-15)-(6-19) that $u(\boldsymbol{x})$ is negative around $\boldsymbol{x}^*$, which can be easily ensured by weighting factors (6-8)-(6-10).

A more convenient unconstrained formulation can be defined by adding a penalty term, as

$$U(\boldsymbol{x}) = u(\boldsymbol{x}) + \gamma_0^l |L(\boldsymbol{x})|^2 \tag{6-20}$$

where $L(\boldsymbol{x})$ is a corner limits penalty function, defined as

$$L(\boldsymbol{x}) = \max\{0, l_1(\boldsymbol{x}), l_2(\boldsymbol{x}), l_3(\boldsymbol{x}), l_4(\boldsymbol{x})\} \tag{6-21}$$

The optimal solution depends on the value of the penalty coefficient $\gamma_0^l \in \Re$,. Here γ_0^l is defined as

$$\gamma_0^l = \frac{|u(\boldsymbol{x}^{(0)})|}{\left|\max\{l_1(\boldsymbol{x}^{(0)}), l_2(\boldsymbol{x}^{(0)}), l_3(\boldsymbol{x}^{(0)}), l_4(\boldsymbol{x}^{(0)})\right|^2} \tag{6-22}$$

where $\boldsymbol{x}^{(0)}$ is the starting point. Then, the objective function to optimize the system margins response is

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} U(\boldsymbol{x}) \tag{6-23}$$

with

$$U(\boldsymbol{x}) = -w_1[e_{\mathrm{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})][e_{\mathrm{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] + w_2[e_{\mathrm{wa}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] + w_3[e_{\mathrm{ha}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})] + \gamma_0^l |L(\boldsymbol{x})|^2 \tag{6-24}$$

The optimal set of coefficients values $\boldsymbol{x}^*$ is found by solving (6-23), and using a low cost computational optimization technique without the need of estimating gradients. The combination of pattern search method [Hooke-61] and the Nelder-Mead method [Lagarias-98] is a good approach to deal with the objective function which contains many local minima. The optimization starts with pattern search, which serves for exploring the design space until finding a potential region where the global minimum is located. Then, the solution found by pattern search is used as seed for the Nelder-Mead method, which further minimizes the objective function for a more precise solution.

6.5. System Test Setup

The system under test is an Intel post-silicon validation platform involving a CPU and a PCH [Rangel-Patiño-16] as described in Section 4.5. The PCIe link is exercised at the packet level with a protocol add-in test card which emulates the external device, as shown in Fig. 6.5. Measurements are based on SMV [Rangel-Patiño-17a] as described in chapter 3, which is a methodology to assess how much margin is in the design with respect to PVT, by using an internal test circuitry [Rangel-Patiño-17b]. The optimization algorithm described in Section 6.4 is implemented in Python, using the SciPy [SciPy-17] modules for Nelder-Mead and pattern search algorithms.

Fig. 6.6 PCIe objective function values across iterations.

6.6. Results

Through the optimization process defined in Section 6.4, a set of Tx and Rx coefficients is found in just 47 iterations, as shown in Fig. 6.6, which are executed in 4 hours. The initial optimization with pattern search finds a solution at iteration 25, which is used as seed for the Nelder-Mead method to finalize the problem. Fig. 6.7 shows the evolution of the three coefficients

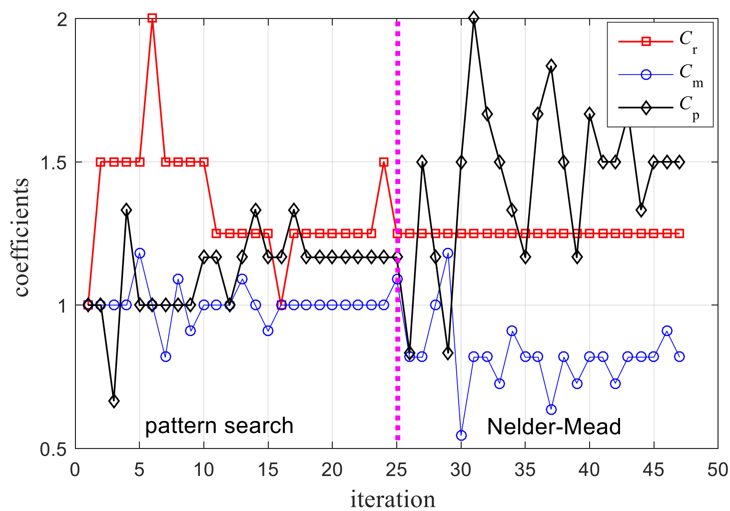


Fig. 6.7 PCIe normalized coefficients responses across iterations.

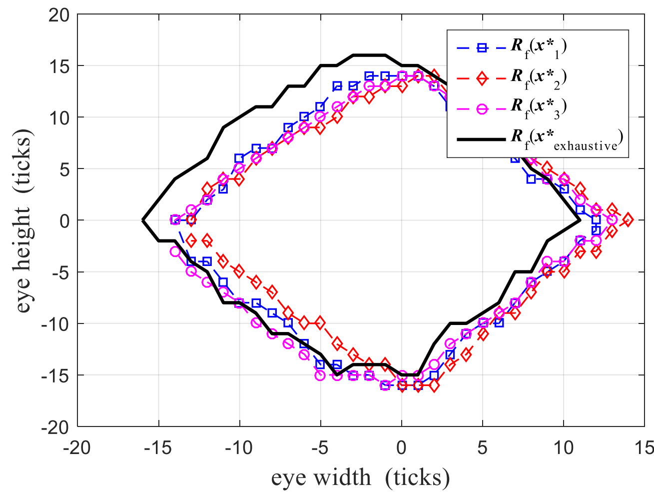


Fig. 6.8 PCIe eye diagram results: comparing the proposed methodology ($\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}^*)$) with three different seeds against the exhaustive method ($\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}^*_{\mathrm{exhaustive}})$).

during the optimization process.

In order to confirm the robustness of the technique, the procedure was ran three times using different seeds for the pattern search method. The optimized equalization coefficients were programmed into the system BIOS to measure the Rx eye diagrams, as shown in Fig. 6.8. The optimal eye diagrams found do not show significant differences between them (from a practical engineering point of view), confirming the robustness of the approach.

A comparison on eye diagrams between the proposed methodology against the initial design and the exhaustive method is shown in Fig. 6.9. The optimized equalization coefficients yield an eye diagram with an e_{h} and e_{w} being now 30 ticks and 27 ticks, respectively, which corresponds to an improvement of 35% on eye diagram area as compared to that one with the initial coefficients. Even though the optimized coefficients show an eye diagram area decrease of 6% as compared to the exhaustive method, the efficiency of this approach is demonstrated by the reduction of the eye diagram asymmetries (more centered eye diagram), and a significant time reduction in post-silicon validation. While the exhaustive method requires 24 machine-hours of data collection plus 8 man-hours for data (EQ maps) analysis for a complete optimization (prone to human errors), the method proposed here can be completed in just 4 hours.

In the initial PCIe link optimizations performed, the eye-width and eye-height asymmetries were not considered in the objective function since they caused too many local minima. However, the eye diagram with the first optimized coefficients using this initial approach yielded a maximized area but with a large eye-width asymmetry. It was concluded that for PCIe, the eye

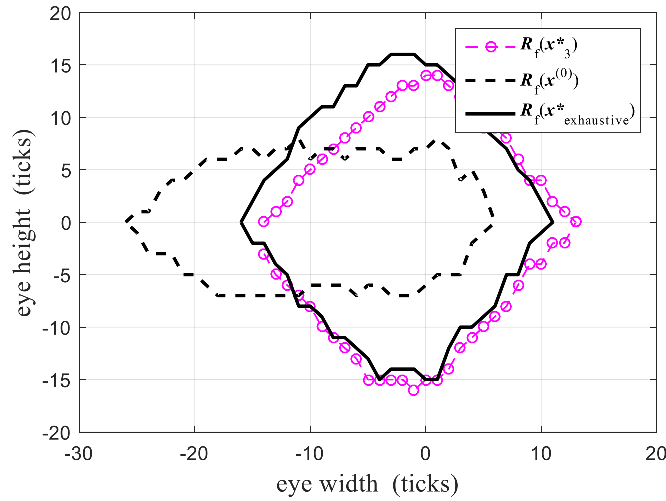


Fig. 6.9 PCIe eye diagram results: comparing the proposed methodology ($\boldsymbol{R}_f(\boldsymbol{x}^*)$) against the initial design ($\boldsymbol{R}_f^{(x0)}$) and the exhaustive method ($\boldsymbol{R}_f(\boldsymbol{x}^*_{exhaustive})$).

diagram can be easily decentered with respect to the eye-width, eye-height, or both, based on the operating conditions and devices. Henceforth, the objective function for PCIe link optimization must consider the asymmetries. It was found that the combination of pattern search and the Nelder-Mead methods is a good approach to deal with the objective function containing too many local minima.

6.7. Conclusion

A direct optimization approach for PCIe link equalization is proposed based on a suitable objective function formulation to efficiently tune the Tx FIR filter and Rx CTLE EQ coefficients to mitigate ISI and other undesired channel effects, and successfully comply with the PCIe specification. The optimized EQ coefficients were evaluated by measuring the real eye diagram of the physical system, demonstrating a great mitigation of the ISI and channel effects, and accelerating the typically required long time for Tx and Rx EQ coefficients tuning, significantly enhancing current PCIe Tx/Rx tuning industrial practices in post-silicon validation.

7. HSIO Receiver Coarse Surrogates Modeling

As microprocessor design scales to the 10-nm technology and beyond, traditional pre- and post-silicon validation techniques are unsuitable to get a full system functional coverage. Physical complexity and extreme technology process variations severely limits the effectiveness and reliability of pre-silicon validation techniques. This scenario imposes the need of sophisticated post-silicon validation approaches to consider complex electromagnetic phenomena and large manufacturing fluctuations observed in actual physical platforms. One of the major challenges in electrical validation of HSIO links in modern computer platforms lies in the PHY tuning process, where equalization techniques are used to cancel undesired effects induced by the channels. Current industrial practices for PHY tuning in HSIO links are very time consuming since they require massive lab measurements. An alternative is to use machine learning techniques to model the PHY, and then perform equalization using the resultant surrogate model. In this chapter, a metamodeling approach based on neural networks is proposed to efficiently simulate the effects of a receiver equalizer PHY tuning settings. Several DoE techniques are used to find a neural model capable of approximating the real system behavior without requiring a large amount of actual measurements. The models performance are evaluated by comparing with measured responses on a real server HSIO link.

7.1. Introduction

Technology scaling and advanced silicon packaging techniques are allowing high density integration. However, as process technologies scale down, traditional IC design methods are challenged by the problem of increased silicon process variation. Design-time optimization and post-silicon tuning are techniques currently used to maximize the parametric yield based on statistical design for high-speed computer systems. Accurate simulations for design-time optimization techniques which exhaustively explore the design space are computationally very expensive given the complexity of the system involved [Duron-Rosales-17].

On the other hand, adaptive tuning in analog design has been widely adopted to confront the silicon process variation. Tunable elements are proposed to adjust the analog circuit

performance after chip fabrication [H.Huang-01], [Miller-03]. As described in Sub-section 1.4.8, these tunable elements provide a way to reconfigure HSIO links in post-silicon servers to mitigate the effects of system channels' variability [Rangel-Patiño-17a]. The adoption of circuit tuning, however, introduces new design challenges. A tunable circuit may contain a large number of control knobs for reconfiguration, and it is extremely expensive to repeatedly run a large number of highly accurate simulations over all process variations and environmental corners to validate a given design during pre-silicon validation [Wang-16], making necessary to perform tuning at post-silicon based on physical measurements.

Post-silicon tuning requires first to measure the circuit performance and then determine the optimal knobs set based on measurement results. Current industrial practices for post-silicon tuning in HSIO links are very time consuming since they are typically based on exhaustive testing requiring massive lab measurements [Rangel-Patiño-16], resulting in an extremely high cost. Therefore, the challenge is how to make the post-silicon circuit tuning inexpensive by significantly reducing the number of lab measurements.

Several methodologies have been proposed to address the aforementioned challenge. A method to do Tx equalization based on eye diagram analysis and direct optimization is proposed in [Duron-Rosales-17]. In contrast, the problem of Rx equalization is addressed in [Rangel-Patiño-16] by doing surrogate-based optimization using Kriging modeling. An extension of [Rangel-Patiño-17a] is presented in [Rangel-Patiño-17c] by developing several surrogate models to choose the most accurate one at the expense of increasing data collection time on the real system, and then perform numerical optimization of the PHY tuning Rx equalizer settings for a SATA Gen 3 channel topology.

In this chapter, the application of machine learning techniques is explored to address the aforementioned challenge with emphasis on the modeling process. In contrast to [Rangel-Patiño-17c], here a highly accurate surrogate model is not searched, but looking for a suitable coarse neural model by employing a frugal DoE method for data collection. This is done not only for SATA Gen3, but also for USB3 Superspeed Gen 1. The ultimate goal will be to use the resultant coarse neural model in a space mapping optimization approach [Bandler-04], [Rayas-Sánchez-16]. Also in contrast to [Rangel-Patiño-17c], in this chapter an abbreviated review on machine learning techniques is provided as applied to post-silicon validation, as well as a detailed formulation on the artificial neural networks (ANN) based modeling and training technique employed, including

the regularization scheme to control ANN generalization. More specifically, it is proposed a metamodeling approach, based on ANN, to efficiently simulate the silicon equalizer circuitry of the Rx. The model is generated using a frugal set of training data exploiting several DoE approaches to reduce the number of test cases. The neural model performance is evaluated by comparing with actual measured responses on an industrial server validation platform. First, a hardware mechanism provides automated measurements over multiple test cases. Then the data collected is arranged to develop a learning procedure to predict the circuit behavior by an artificial neural network. This neural model can be later used for efficient circuit tuning at post-silicon validation. The proposed methodology is illustrated by the neural modeling of a silicon equalizer Rx circuitry of two current industrial HSIO channel topologies: USB3 Super-speed Gen 1 and SATA Gen 3.

The present chapter expands the work in [Rangel-Patiño-18b]. The rest of this chapter is organized as follows. In Section 7.2, a brief review on machine learning is provided as applied to post-silicon validation. Section 7.3 provides basic concepts on ANN. The ANN-based receiver modeling technique is presented in Section 7.4. The system for experimental evaluation is described in Section 7.5. Results from the proposed modeling approach are compared to actual measured responses in Section 7.6. The last section presents the conclusions.

7.2. Machine Learning in Post-Silicon Validation

Machine learning algorithms, a branch of artificial intelligence, build statistical models from examples, which are then used to make predictions when faced with cases not seen before. On the other hand, the goal of HSIO post-silicon validation is to understand and validate from physical examples the correct operation of the design, identify bugs, and determine the best settings to avoid any failure. Machine learning aims at a similar goal: learning from examples and identifying the structure in a system [DeOrio-13]. In addition, the large volume of data generated from typical post-silicon testing suggests the application of machine learning techniques to predict post-silicon behavior.

There has been recent research on machine learning applications to some areas of post-silicon validation. In [Rahmani-17], authors propose a trace signal simulation-based selection technique that exploits machine learning to efficiently identify a small set of key traceable signals,

reducing the simulation cost. An algorithm that applies anomaly detection techniques is proposed in [DeOrio-13] for post-silicon bug diagnosis. A Bayesian model fusion is described in [Wang-16] to efficiently reuse the data from pre-silicon and reduce the data collection for tuning during post-silicon. Machine learning is applied in [Pridhiviraj-15] to bug finding in post-silicon server power management. In [Deyati-14], several neural models are developed to learn post-silicon unknown module-level behavior and diagnose localized design bugs.

It is seen that all the previously cited machine learning approaches to post-silicon validation have been focused on developing efficient and reliable techniques for diagnosis, failure detection, or bug identification. An assessment of several surrogate modeling and DoE techniques to identify the best approach for an HSIO link model and simulation is realized in [Rangel-Patiño-17c]. From that assessment, polynomial-based surrogate modeling (PSM) combined with Sobol DoE with 150 samples was identified as the most accurate surrogate model [Rangel-Patiño-17c]. While an accurate model is desirable for direct optimization, it can be still expensive since it requires a significant amount of lab measurements to develop. Additionally, the required time to evaluate and even to train any metamodel becomes, for practical purposes, insignificant as compared to the time required to collect the measurement data. On the other hand, it has been demonstrated [Chavez-Hurtado-16], [Rayas-Sánchez-17] that both ANN and polynomial functional surrogates perform better than SVM and Kriging surrogates in cases with a very limited amount of training data, while polynomial surrogates exhibit better performance than ANN only in cases with low-dimensionality and small regions of interest, Then, a neural modeling approach is proposed to efficiently approximate the effects of an HSIO post-silicon receiver equalizer with a very reduced set of testing and training data, and possibly a large number of knobs. The resultant metamodel, obtained from the proposed inexpensive method, could later be used as a fast coarse model in a space mapping approach [Bandler-04], [Rayas-Sánchez-16] to find the optimal equalizer settings that maximize the actual HSIO performance.

Several other innovative approaches have been proposed to find out the optimal performance of the system in post-silicon validation. In [Li-13], [Plouchart-14], and [Wang-16] a statistical framework, referred to as Bayesian model fusion (BMF), is proposed for post-silicon

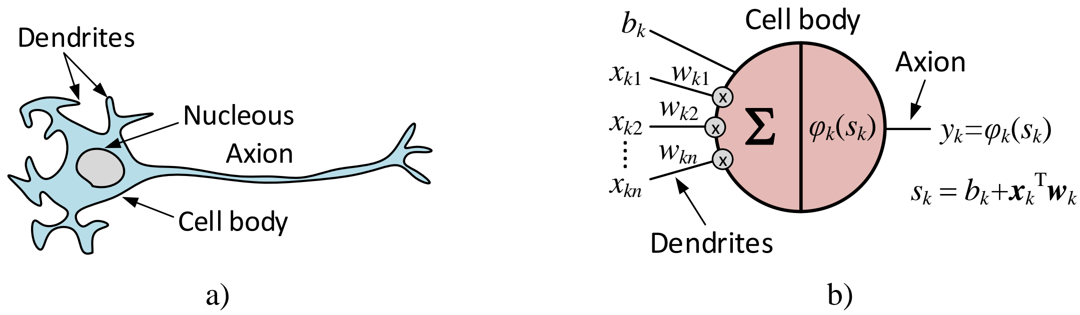


Fig. 7.1 Neural representations: a) simplified diagram of a biological neuron, b) inner-product artificial neuron (modified from [Rayas-Sánchez-15]).

tuning. That methodology is based on the assumption that an early-stage (e.g. pre-silicon) model or data is already available. Then, a relatively small number of post-silicon measurements may be required by applying Bayesian inference, allowing the post-silicon cost of tuning to be substantially reduced. However, that BMF approach is not feasible in a post-silicon environment if not enough pre-silicon model information is available, which is the case of this research. Similarly, in [Tao-14], a methodology for programming a reconfigurable RF receiver is proposed, showing a maximum efficiency of 27.5× speed-up as compared with the exhaustive search. In [X.Li-07], a post-silicon tuning methodology is proposed based on a dynamic programming algorithm [Bertsekas-05] combined with a fast Monte Carlo simulation flow for statistical analysis and discrete optimization. That method achieves 20× speed-up as compared with the exhaustive search. These methodologies allow very significant acceleration of the tuning time in post-silicon validation. However, it is unclear if they could be easily applied when dealing with a large number of circuit knobs, which is the current case.

7.3. Basic Concepts on Artificial Neural Networks

7.3.1 Artificial Neurons

The fundamental processing element of an ANN is the neuron. A comparison between biological and artificial neurons is shown in Fig. 7.1. An artificial neuron can be designed by a set of inputs weighted by synapses, a summing node, and a linear or nonlinear (usually sigmoid) activation function [Suzuki-11]. Its corresponding transfer function can represented by

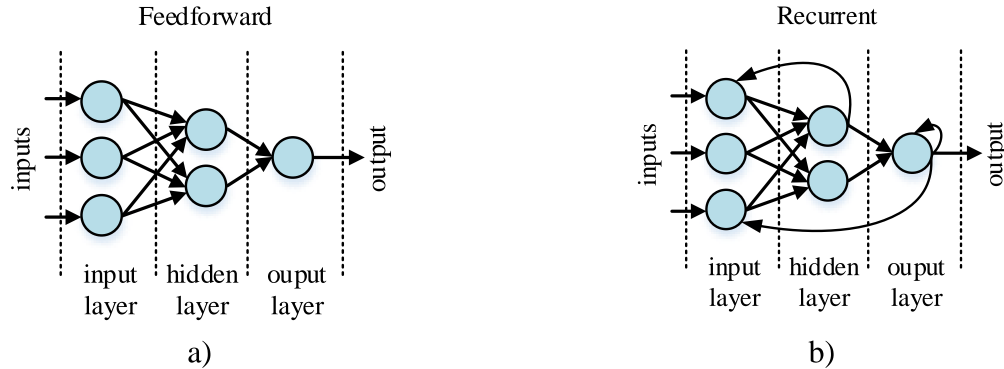


Fig. 7.2 ANN topologies: a) feedforward, b) recurrent. Figure taken from [Suzuki-11].

$$y_k = \varphi_k\left(b_k + \boldsymbol{x}_k^{\mathrm{T}} \boldsymbol{w}_k\right) \tag{7-1}$$

where $\boldsymbol{x}_k \in \Re^n$ is the vector of n input signals to the neuron, $b_k \in \Re$ is the biasing element of the neurons, $\boldsymbol{w}_k \in \Re^n$ is the vector of weighting factors that model the synapse strengths, and $y_k \in \Re$ is the output signal from the activation function $\varphi(\cdot)$ [Silva-11], [Rayas-Sánchez-15]. This particular type of neuron is named as inner-product neuron.

7.3.2 ANN Topologies

Each neuron receives inputs from the adjacent neurons, process the information, and produces an output. Typically, an ANN contains three types of layers, respectively called input layer, hidden layer, and output layer [Zhang-00], and different ANN structures or topologies can be created by using different number of neurons and by connecting them in different configurations.

Several ANN topologies have been developed for multiple applications, including signal processing, pattern recognition, control, etc., as well as for different types of analyses (static, frequency domain, time-domain, etc.) [Zhang-00]. Different ANN topologies can be built by using different processing elements (neurons) and by the specific manner in which they are linked, resulting in numerous possible topologies. Most topologies can be divided into two basic classes: feedforward topology and recurrent topology, as illustrated in Fig. 7.2. Multilayer perceptrons (MLP) are feedforward networks widely used as the preferred ANN topology [Rayas-Sánchez-04]. In general, the MLPs with one or two hidden layers are commonly used for multiple applications [Villiers-92].

7.4. ANN-Based Receiver Metamodeling

Metamodels are scalable parameterized mathematical models that emulate the component behavior over a user-defined design space. These techniques allow developing an approximation of a system response within a design region of interest, following a “black-box” approach. The problem of modeling in post-silicon validation can be mapped to a mathematical problem of function estimation in presence of noisy data points. The most popular estimators are neural networks and Kernel estimation. In [Goulermas-07], authors demonstrate the functional estimation capability of an ANN.

ANNs are particularly suitable to approximate high-dimensional and highly nonlinear relationships, in contrast to more conventional methods such as numerical curve-fitting, empirical or analytical modeling, or response surface approximations [Vicario-16]. ANNs have been used in many areas of applications, including RF and microwave circuits [Zhang-00], EM-based design optimization [Rayas-Sánchez-04], control process, telecommunications, biomedical, remote sensing, pattern recognition, and manufacturing, just to mention a few [Haykin-99]. Recently, ANNs have been used for HSIO simulations, but they were focused to model the nonlinear relationships between channel parameters and system performance to speed up system simulations, as in [Bistola-15] and [Liu-15]. In [Goay-17], authors proposed ANNs for eye diagram modeling based on simulations, and they use an adaptive sampling method for data collection process.

Once trained, ANN provides a fast way to perform a large number of I/O links and channel simulations that take into account the die-to-die process variations, board impedances, channel losses, add-in cards, end-point devices, and operating conditions [Beyene-07]. ANN modeling involves two inter-related process: a) neural network model development - that includes selection of representative training data, network topology, and training algorithms; and b) neural model validation - the neural network model is tested and validated according to its generalization performance in a given region of interest. A large amount of training data is usually needed to ensure model accuracy, and this could be very expensive in the post-silicon validation environment. An alternative to reduce the dimension of the learning set is to properly select the learning points by using DoE, to ensure adequate design space parameter coverage [Mack-07].

In the conventional modeling approach, an ANN, denoted also as a surrogate model, is trained such that its response $\boldsymbol{R}_{\mathrm{s}}$ approximates the target or fine model response $\boldsymbol{R}_{\mathrm{f}}$ in a region of

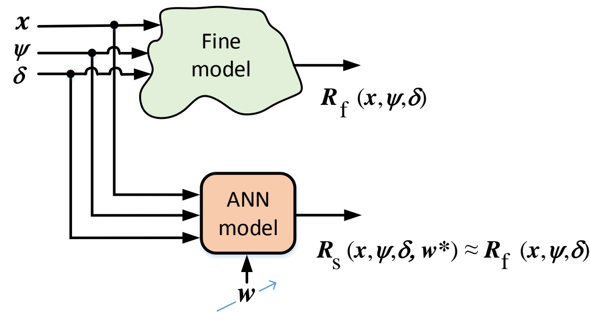


Fig. 7.3 ANN modeling concept. Figure modified from [Rayas-Sánchez-04].

interest for the design parameters $\boldsymbol{x}$ (Rx knobs settings), and the independent variables according to the kind of simulation/measurements $\boldsymbol{\psi}$ (operating conditions), and type of devices $\boldsymbol{\delta}$, as illustrated in Fig. 7.3 [Rayas-Sánchez-01], where $\boldsymbol{w}$ contains the internal parameters of the ANN (weighting factors, bias elements, etc. of all the neurons). Once the ANN is trained with sufficient learning samples, that is, once the optimal $\boldsymbol{w}$ is found, denoted as $\boldsymbol{w}^*$, the ANN can be used as a fast and reliable model.

The complexity of the ANN must be properly selected, i. e., the number of the internal free parameters has to be sufficiently large to achieve a small learning error, and sufficiently small to avoid a poor generalization performance. This training can be seen as an optimization problem where the internal parameters of the ANN are adjusted such that the ANN model best fit the training and testing data.

7.4.1 ANN Topology

Multilayer perceptrons are feedforward networks widely used as the preferred ANN topology. Since a 3-layer perceptron (3LP) is in principle sufficient for universal approximation [Hornik-89], a 3LP is used to implement the neuromodel, with n inputs (equal to the number of Rx knobs), h hidden neurons, and m outputs (number of system responses of interest), as shown in Fig. 7.4 [Rayas-Sánchez-01]. The hyperbolic tangents is used as the selected activation function $\varphi(\cdot)$ for the hidden neurons.

The number of hidden neurons depends on the nonlinearity level of the I/O relationship and the size of the training data set. Literature reports usage of either experience or a trial-and-error processes to judge the number of hidden neurons [Zhang-03]. The appropriate number of

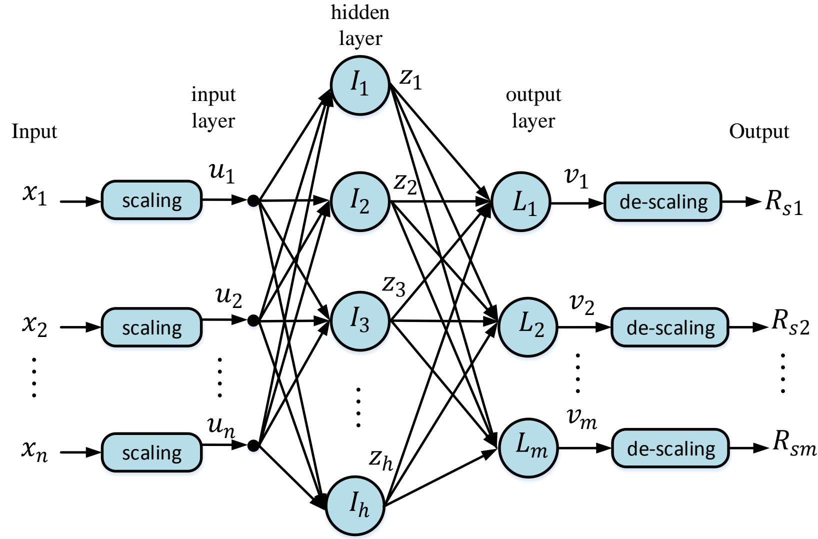


Fig. 7.4 A 3-layer perceptron including the scaling process. Figure modified from [Rayas-Sánchez-04].

neurons can also be determined through an adaptive processes, which means adding or deleting neurons during training [Devabhaktuni-01], [Kwok-97]. In this chapter, the required complexity of the ANN, determined by h, depends on the required generalization performance for a given set of training and testing data [Rayas-Sánchez-01], as explained in Section 7.4.3, and is defined algorithmically.

7.4.2 Decomposed Modeling

There can be problems where the complete set of responses contained in $\boldsymbol{R}_\text{f}$ is difficult to approximate using a surrogate model with a single ANN. Additionally, when a model has many input and output variables, a massive amount of data are usually required for ANN model training to achieve good accuracy. This massive data generation and model training might become too expensive and impractical. To overcome this limitation, a decomposition approach to simplify the high-dimensional problem into a set of small sub-problems can be used. In this way, the cost of data generation and model development is reduced [Rayas-Sánchez-04]. Then the learning process can be distributed among several ANNs, which results in dividing the output space into a set of subspaces. The corresponding ANNs can then be trained individually, to match each response contained in $\boldsymbol{R}_\text{f}$, as illustrated in Fig. 7.5 [Rayas-Sánchez-01]. This implies the solution of several independent optimization problems instead a single one, which can be implemented in parallel.

7.4.3 ANN Modeling and Training

Let $\boldsymbol{R}_\mathrm{f} \in \Re^m$ represent the actual electrical margining system response, denoted as a fine model response, which consists of the eye width $e_\mathrm{w} \in \Re$ and eye height $e_\mathrm{h} \in \Re$ of the measured eye diagram,

$$\boldsymbol{R}_\mathrm{f}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = [e_\mathrm{w}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \quad e_\mathrm{h}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})]^\mathrm{T} \tag{7-2}$$

The electrical margining system response depends on the Rx knobs settings $\boldsymbol{x} \in \Re^n$, the operating conditions $\boldsymbol{\psi}$ (voltage and temperature), and the devices $\boldsymbol{\delta}$ connected to the system. The ANN is trained to find an optimal vector of weighting factors $\boldsymbol{w}$, such that the ANN response, denoted as $\boldsymbol{R}_s$, is as close as possible to the fine model response for all $\boldsymbol{x}$, $\boldsymbol{\psi}$, $\boldsymbol{\delta}$ in the region of interest,

$$\boldsymbol{R}_\mathrm{s}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta},\boldsymbol{w}) \approx \boldsymbol{R}_\mathrm{f}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \tag{7-3}$$

The ANN main input-output relationship is denoted as

$$\boldsymbol{R}_s = \boldsymbol{f}(\boldsymbol{x}) \tag{7-4}$$

The objective is to develop a fast and accurate ANN model for $\boldsymbol{f}$ by training the ANN with a set of measured learning data.

There are three main learning techniques: a) supervised learning, b) unsupervised learning, and c) reinforcement learning. These learning techniques can be employed in principle by any given type of ANN architecture [Zhang-00]. In this work, the supervised learning is used, which is a technique that sets the internal parameters of the ANN from training data that include desired or target responses.

Initializing the weight parameters $\boldsymbol{w}$ is the first step in training. It is intended to provide a good starting point for the optimization. The random-weight is the more common method for MLP weight initialization, where the weights are initialized with small random values [Thimm-97]. A good starting point for knowledge-based neural network can be provided by using physical/electrical knowledge and experience of the problem [Zhang-00]. In this work, a decoupling network process is used with initial set of inputs and outputs to compute initial weighting factors $\boldsymbol{w}_0$ and then initial errors.

Once the ANN is trained, its performance has to be evaluated. A common way to measure the learning performance of the resultant ANN is by calculating the mean squared error (MSE) at

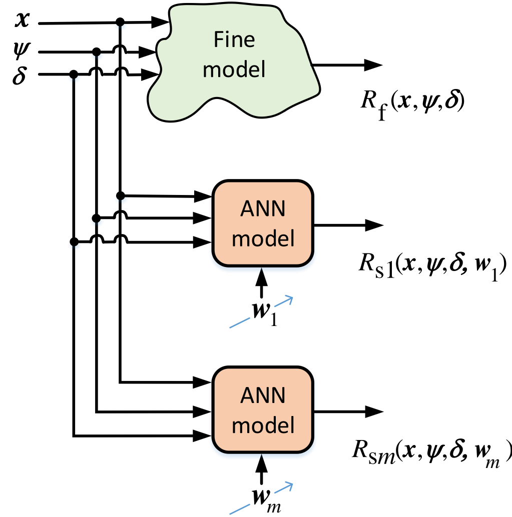


Fig. 7.5 ANN decomposed modeling. Figure modified from [Rayas-Sánchez-04].

all the learning base points. A simple strategy would be to select the ANN that corresponds to the minimum MSE in the learning data set. However, a drawback of this strategy is that the "best" performing ANN model, in terms of the smallest MSE in the learning set, is not necessarily the actual best ANN model, since ANNs with a large number of weighting factors yield small learning errors but introduce too much nonlinearity, which produces large errors at basepoints not seen during training (an effect known as over-fitting or over-learning) [Haykin-99], [Suzuki-11]. In this chapter, a different ANN modeling approach is proposed based on [Rayas-Sánchez-06].

The goal is to develop a fast and accurate ANN model by training the ANN with a set of measured learning data. The learning data are pairs of ($\boldsymbol{x}_L$, $\boldsymbol{t}_L$), with $L = 1, 2\ldots, l$, where $\boldsymbol{t}_L$ contains the desired fine model outputs or targets (obtained from measurements) for the ANN model at the $\boldsymbol{x}_L$ inputs, and l is the total number of learning samples. During training, the voltage/temperature (VT) of the system is kept fixed at nominal conditions and without changing the external device. Under these conditions, $\boldsymbol{\psi}$ and $\boldsymbol{\delta}$ remain constant. Therefore, the ANN model during training is treated as

$$\boldsymbol{R}_{\mathrm{s}L} = \boldsymbol{R}_{\mathrm{s}}(\boldsymbol{x}_L, \boldsymbol{w}) \tag{7-5}$$

The ANN performance during training is evaluated by computing the difference between ANN outputs and the targets for all the learning samples,

$$\boldsymbol{E}_L(\boldsymbol{w}) = \boldsymbol{R}_{\mathrm{s}L}(\boldsymbol{x}_L, \boldsymbol{w}) - \boldsymbol{t}_L \tag{7-6}$$

where $\boldsymbol{E}_L$ is the learning error matrix.

Following [Rayas-Sánchez-06], the problem of training the ANN is formulated as solving the following optimization problem:

$$\boldsymbol{w}^* = \arg\min_{\boldsymbol{w}} \left\| \boldsymbol{E}_L(\boldsymbol{w}) \right\|_F \tag{7-7}$$

To control the generalization performance while solving (7-7), T testing base points ($\boldsymbol{x}_T$) are used not being used during the training. The scalar learning and testing errors are given by

$$\varepsilon_L = \left\| \boldsymbol{R}_{sL}(\boldsymbol{x}_L, \boldsymbol{w}) - \boldsymbol{R}_{fL} \right\|_F \tag{7-8}$$

$$\varepsilon_T = \left\| \boldsymbol{R}_{sT}(\boldsymbol{x}_T, \boldsymbol{w}) - \boldsymbol{R}_{fT} \right\|_F \tag{7-9}$$

where $\boldsymbol{R}_{fT}$ and $\boldsymbol{R}_{sT}$ are the output matrices of the fine model and ANN model, respectively, at the T testing base points, and $\boldsymbol{R}_{fL}$ is the fine model response at the L learning base points.

The 3LP is trained by using the Bayesian regularization [MacKay-92] method available in MATLAB Neural Network Toolbox. The algorithm for training the ANN is shown in Fig. 7.6. The learning ratio is first defined to split the pairs of inputs and targets into the learning and testing datasets. As mentioned before, the learning process often begins by initializing the ANN weights with arbitrary values using a random number generator [Thimm-97], however, in this case we use a decoupling network process with initial set of inputs and outputs to compute initial weighting factors $\boldsymbol{w}_0$ and corresponding initial error $\varepsilon_T^{\text{old}}$. Then, training the 3LP is started with just one hidden neuron ($h = 1$), and calculate the corresponding learning and testing errors. The complexity of the ANN (h) is kept increasing until the current testing error is larger than the previous one, and the current learning error is smaller than the current testing error, as in [Rayas-Sánchez-06] (see Fig. 7.6).

7.5. Experimental System Configuration and DoE Approaches

The system under test is a server post-silicon validation platform, comprised mainly of a CPU and a PCH. The PCH is a family of Intel microchips which integrates a range of common I/O blocks required in many market segments, and these include USB [USBOrg-16], PCI Express [PCISIG-16], SATA [SATAOrg-16], SD/SDIO/MMC, and Gigabit Ethernet MAC, as well as general embedded interfaces such as SPI, I2C, UART, and GPIO. The PCH also provides control data paths with the Intel CPU through DMI interface, as shown in Fig. 7.7. This figure also shows

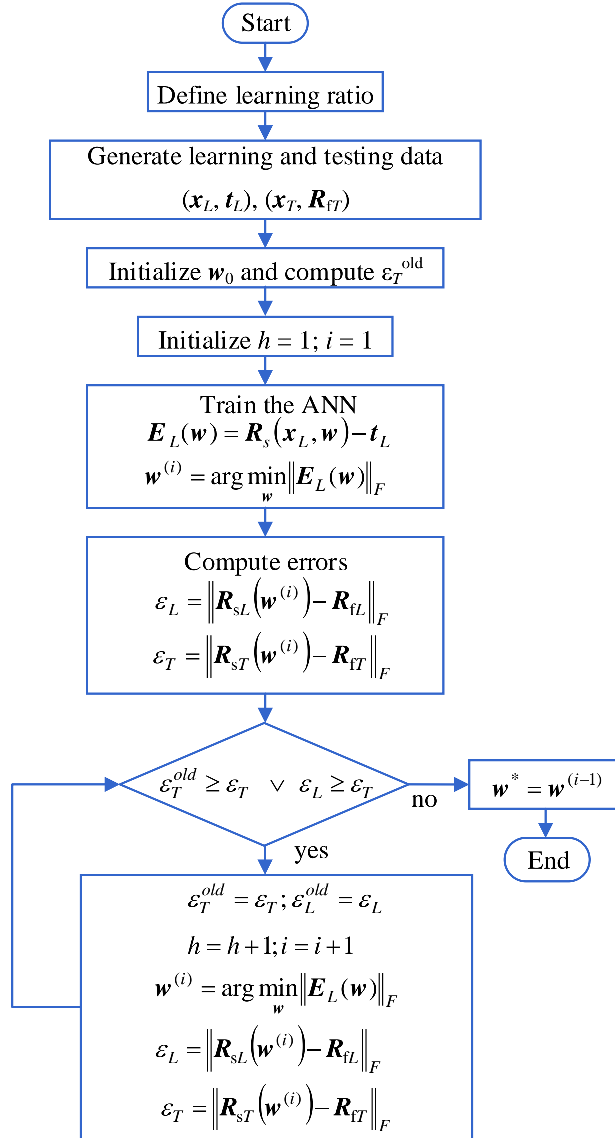


Fig. 7.6 Algorithm for training the ANN with controlled generalization performance.

the automation mechanism to read the Rx eye diagram parameters (eye width and eye height). Within the PCH, the methodology was tested on two different HSIO links: USB3 Super-speed Gen 1 and SATA Gen 3.

The measurement system is based in the SMV process [Rangel-Patiño-16], [Viveros-Wacher-14], which is a methodology to verify the signal integrity of a circuit board and assess how much margin is in the design relative to silicon characteristics and processes as described in chapter 3.

Three different DoE techniques are employed to explore the desired solution space with a reduced number of test cases. For each test case, seven input variables are used that represent Rx

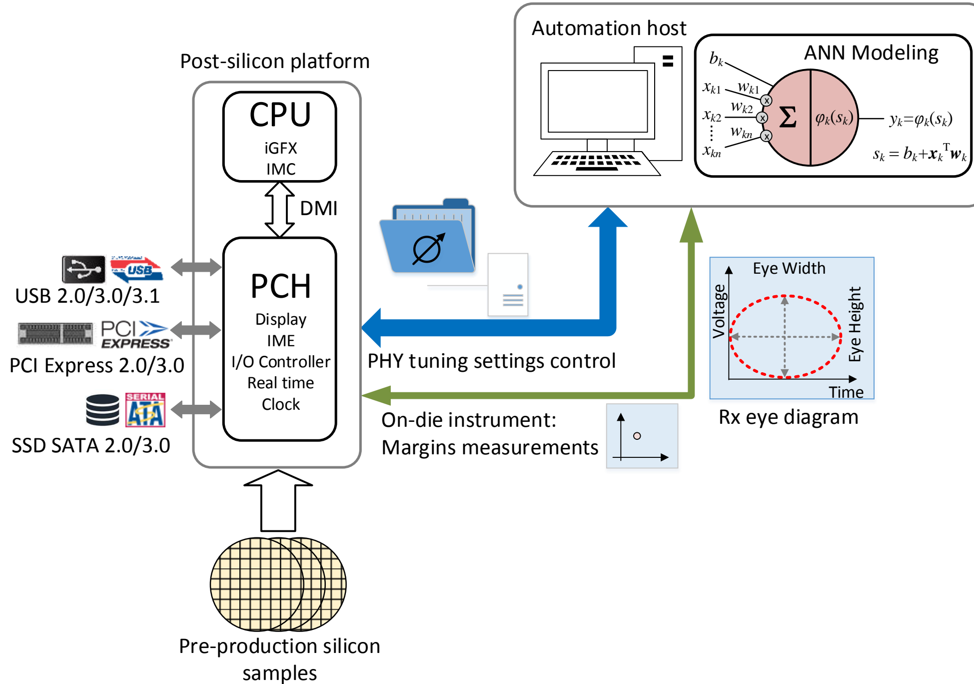


Fig. 7.7 HSIO server post-silicon hardware configuration for Rx metamodeling.

knobs ($n = 7$), which are settings used in three main Rx circuitry blocks (CTLE, VGA, and CDR), and then the eye measurements from the system under test is retrieved. The employed DoE techniques are: 1) Box Behnken (BB), which is a type of second order response surface methodology (RSM) that combines factorial designs with balanced incomplete blocks designs [Wu-00], using 62 experiments; 2) orthogonal arrays (OA) [Chang-05], using an $L_{27}(3^9)$ array in order to capture non-linear effects in the objective function by only running 27 experiments; and 3) Sobol [Sobol-67] low-discrepancy sequence to sample the solution space. Given the quasi-Monte Carlo sampling approach of Sobol, the solution space is better explored as the number of samples increases, at the expense of increasing test time on the real system. Therefore, three different Sobol DoE are used, denoted as Sobol50, Sobol100 and Sobol150, with 50, 100, and 150 samples, respectively.

System margining testing is very time consuming when running many test cases for PHY tuning. A single test case with 3 repetitions can take up 20 minutes, and then running a Sobol150 can take up 50 hours of testing for a single VT corner. The objective of comparing several DoEs is to find a suitable sampling strategy that provides adequate ANN model performance with the least amount of testing time.

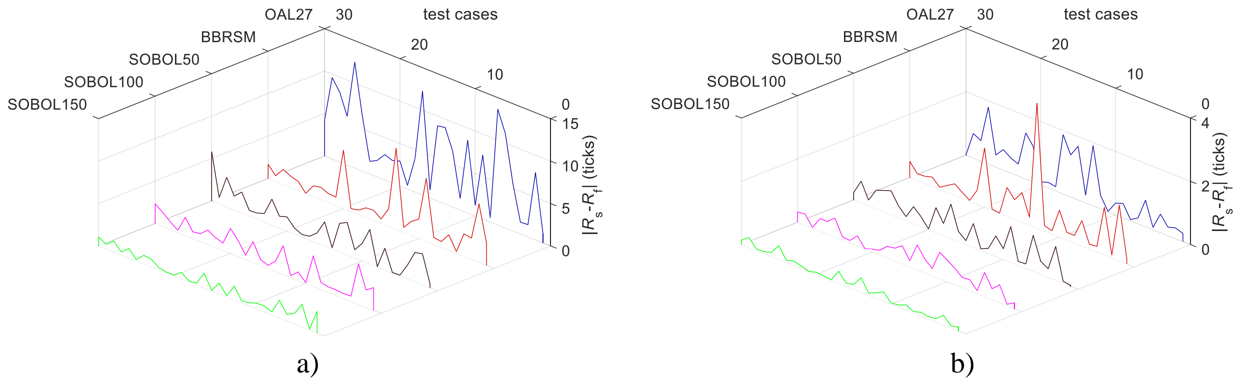


Fig. 7.8 Comparison of SATA neural model generalization performance for different DoE techniques: a) eye height error; b) eye width error.

7.6. Neural Modeling Results

Fig. 7.8 shows the generalization error of the already trained neural model (at $\boldsymbol{w}^*$), comparing the different DoEs for SATA. It is seen that the best performance is achieved with Sobol150. The three Sobol cases provide the best generalization performance, as confirmed in Fig. 7.8. However, Sobol50 is able to achieve acceptable accuracy with only 50 samples.

Fig. 7.9 shows the learning performance of the neural training algorithm for SATA. The best performance is achieved with h = 3 for the eye width ANN, achieving a maximum relative learning error of 3.65%, and 7.63% for the relative testing error. For the eye height ANN, best performance is achieved with h = 4, yielding 7.98% of learning error and 6.75% of testing error. Thus, the metamodels are able to reach above 90% of accuracy for these initial sampling points.

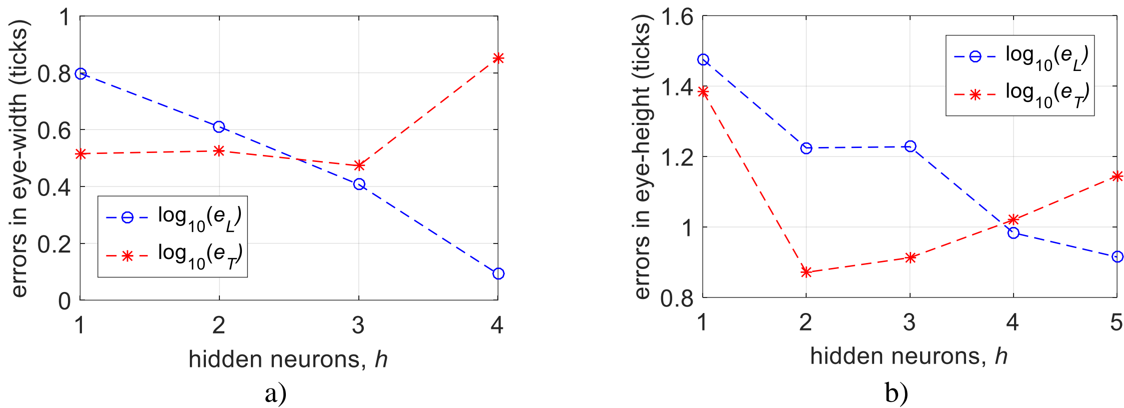


Fig. 7.9 Learning and testing errors during SATA neural training using Sobol50, for a) eye width and b) eye height.

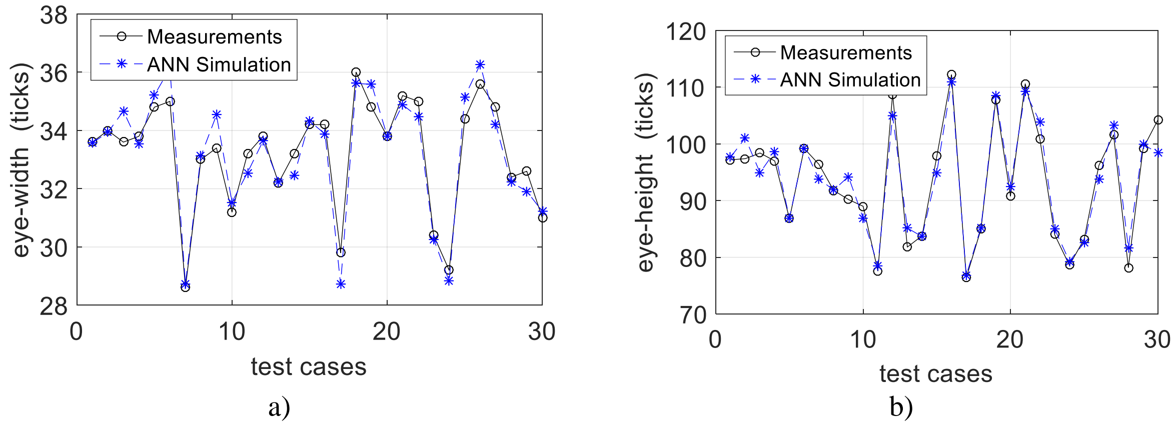


Fig. 7.10 Neural model generalization performance using Sobol50 for a) SATA eye width; b) SATA eye height.

The neural model response at $\boldsymbol{w}^*$ and $h = 3$ for e_w and $h = 4$ for e_h from Sobol50 is compared in Fig. 7.10a and Fig. 7.10b, respectively, with the fine model (real measurements), by using 30 testing base points not used during training, in order to test the generalization performance. It is observed that the neural model effectively simulates the actual physical measurements with a total relative error of 1.7% for the e_w response and 2.5% for the e_h response. In other words, the ANN metamodel is able to predict margins with up to 95% of accuracy when using equalization values not used during the ANN training.

Similar results for the case of USB3 Super-speed Gen 1 were obtained, where ten input variables (n = 10) were used that represent the corresponding Rx knobs, which again are settings used in the three main Rx circuitry blocks. The results are presented in Fig. 7.11. It is seen that for USB, the resultant neural model also effectively simulates the fine model (physical platform), finding a total relative error of 6.7% for the e_w response, as shown in Fig. 7.11a, and a 5.7% relative

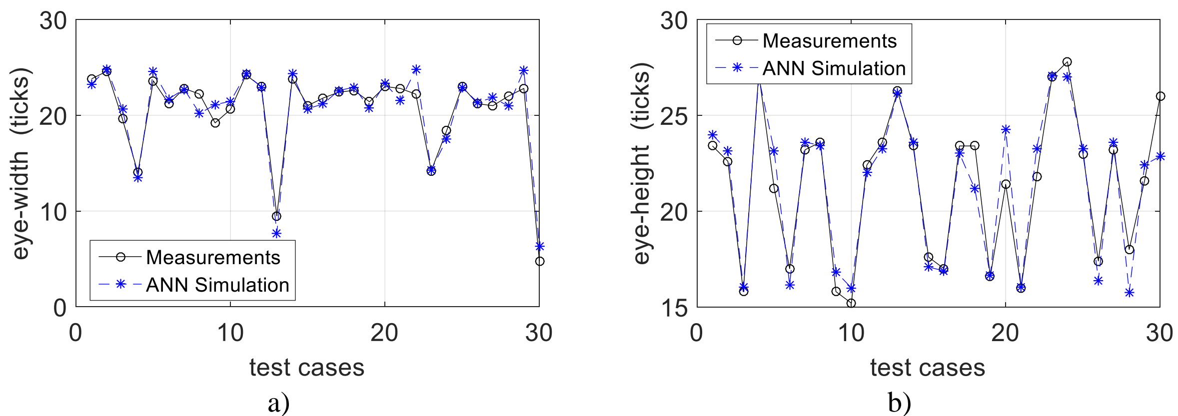


Fig. 7.11 Neural model generalization performance using Sobol50 for a) USB width; and b) USB eye height.

error for the e_h response, as shown in Fig. 7.11b. This metamodel performance was achieved using also a Sobol50 DoE.

7.7. Conclusion

A metamodeling technique based on artificial neural networks was presented to efficiently simulate the effects of the receiver equalization circuitry in industrial HSIO links. The neural model is trained using different DoE approaches to identify the best system response sampling strategy that yields an acceptable neural model with a very reduced set of learning and testing samples. The resultant neural model approximates with sufficiently accuracy the eye diagram of a real post-silicon HSIO validation platform. The proposed machine learning approach can be exploited to develop extremely efficient vehicles to drive fast PHY tuning in HSIO links. Through this procedure, an efficient surrogate model was found that approximates the system with a reduced set of testing and training data, suitable for a future co-Kriging or space mapping optimization for PHY tuning.

8. HSIO Receiver Equalization by Space Mapping Optimization

One of the major challenges in HSIO links electrical validation is the PHY tuning process. Equalization techniques are employed to cancel any undesired effect. Typical industrial practices require massive lab measurements, making the equalization process very time consuming. In this chapter, the Broyden-based input SM algorithm is exploited to efficiently optimize the PHY tuning Rx equalizer settings for a SATA Gen 3 channel topology. A good-enough surrogate model is used as the coarse model, and an industrial post-silicon validation physical platform as the fine model. A map between the coarse and the fine model Rx equalizer settings is implicitly built, yielding an accelerated SM-based optimization of the PHY tuning process.

8.1. Introduction

Adaptive tuning circuits have been broadly adopted to confront the silicon process variation, and to cancel undesired effects such as jitter, attenuation, crosstalk, and inter-symbol interference. These tunable elements provide a way to reconfigure HSIO links in post-silicon computer servers [Rangel-Patiño-16], as illustrated in Fig. 8.1. Typical industrial practices for PHY tuning involve exhaustive testing of these tunable parameters, requiring massive lab measurements, making it one of the most time-consuming processes in post-silicon validation [Cheng-11], [Rangel-Patiño-17b], [Wang-15].

Several methods have been proposed to address this challenge. A statistical framework, referred to as Bayesian model fusion (BMF), is proposed in [Li-13], [Plouchart-14], and [Wang-16]. This methodology is based on the assumption that pre-silicon models are already available. However, that BMF approach is not feasible in a post-silicon environment where not enough pre-silicon data is available. In order to overcome this limitation, other methods [Rangel-Patiño-16], [Rangel-Patiño-17a], [Rangel-Patiño-17b] have been proposed by using surrogate models

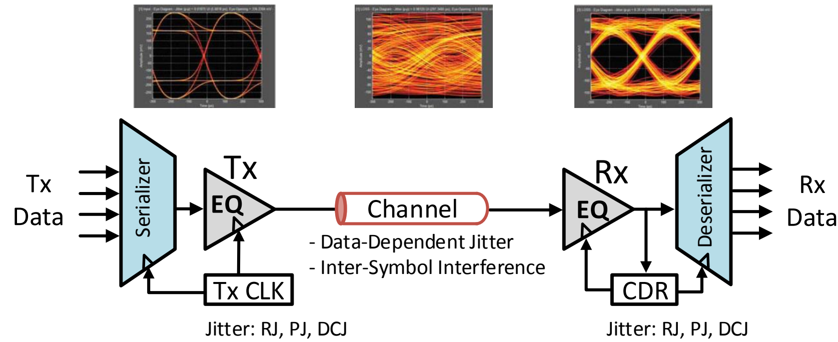


Fig. 8.1 HSIO link reconfiguration in post-silicon server validation to cancel out the effects of system channels' variability.

developed from a set of learning base points generated from DoE [Koziel-11]. These metamodels treat the system as a black box, aiming to approximate the input-output relationship for the system under study [Fu-14]. Once a very-accurate surrogate model is developed, direct optimization can be applied to find the optimal PHY tuning parameters.

While an accurate surrogate model is desirable for direct SBO, it can be computationally expensive to develop. By combining an adequate modeling technique with a suitable DoE approach, a coarse surrogate model can be efficiently developed with a very reduced set of data, as in [Rangel-Patiño-17a], [Rangel-Patiño-18c]. Once this coarse model is available, SM techniques can be exploited.

In the present chapter, the Broyden-based input SM optimization algorithm, better known as aggressive SM (ASM) [Bandler-95], [Rayas-Sánchez-16], is used for the first time in HSIO PHY tuning optimization. The SM approach takes advantage of a coarse surrogate model developed following [Rangel-Patiño-17c]. In this case, the fine model is a measurement-based post-silicon validation industrial platform. The approach is illustrated by optimizing the PHY tuning Rx equalizer settings for a SATA Gen 3 channel topology, accelerating tuning from several days to a few hours.

The present chapter expands the work in [Rangel-Patiño-18c]. The organization of the chapter is as follows. Section 8.2 describes the fine model and coarse model development, and presents the objective function. Section 8.3 describes the ASM algorithm, and Section 8.4 presents the optimization results. Finally, Section 8.5 concludes the work.

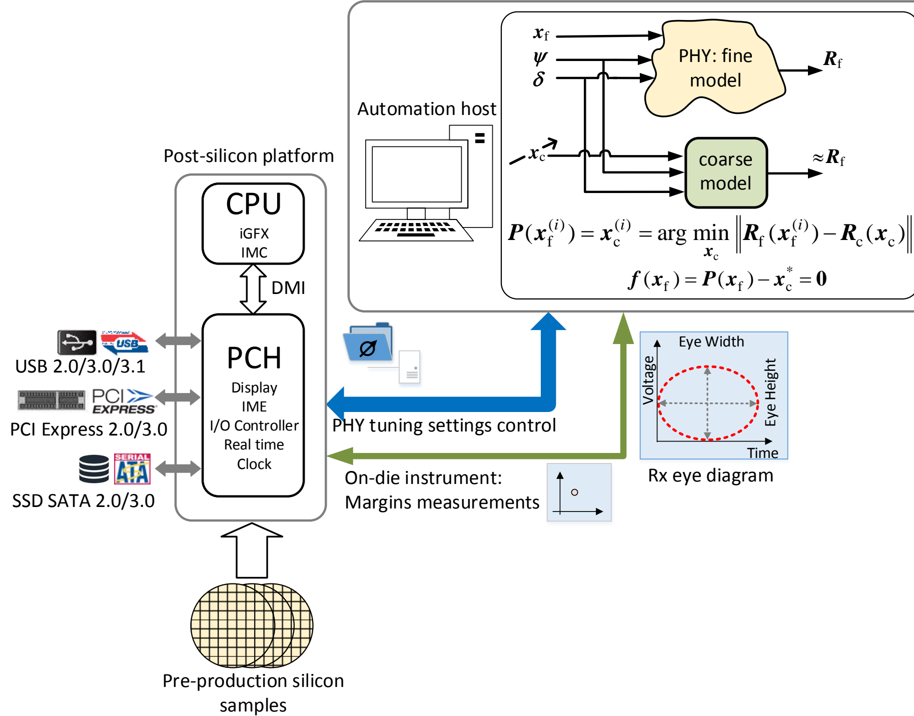


Fig. 8.2 Test setup for SM optimization: an Intel server post-silicon validation platform.

8.2. Broyden-Based Input Space Mapping

SM optimization methods belong to the general class of surrogate-based optimization algorithms [Booker-99]. They are specialized on the efficient optimization of computationally expensive models. The most widely used SM approach to efficient design optimization is the ASM or Broyden-based input space mapping algorithm [Rayas-Sánchez-16]. ASM efficiently finds an approximation of the optimal design of a computationally expensive model (fine model) by exploiting a fast but inaccurate surrogate representation (coarse model) [Rayas-Sánchez-16]. ASM aims at finding a solution that makes the fine-model response close enough to the desired response.

8.2.1 Fine Model

The fine model is an Intel server post-silicon validation platform in an industrial environment, as shown in Fig. 8.2. The platform is comprised mainly of a CPU and a PCH [Rangel-Patiño-16]. The PCH is a family of Intel microchips that controls data paths and support functions

used in conjunction with the Intel CPU through DMI [Rangel-Patiño-17b] as described in Section 4.5. Within the PCH, the methodology is applied to an HSIO link SATA Gen3 [SATAOrg-16]. The SATA channel topology is comprised of the Tx driver, the Tx base board transmission lines, several via transitions, an I/O card connector, and 1 m SATA cable used to connect the base board to the device I/O card, as illustrated in Fig. 4.14. The measurement system is based on the SMV Intel process [Rangel-Patiño-17b], [Viveros-Wacher-14] as described in chapter 3.

Let $\boldsymbol{R}_\text{f} \in \Re^m$ represent the actual (measured) electrical margining system response, denoted as a fine model response, which consists of the eye width $e_\text{w} \in \Re$ and eye height $e_\text{h} \in \Re$ of the measured eye diagram,

$$\boldsymbol{R}_\text{f}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = \left[e_\text{w}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \quad e_\text{h}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right]^\text{T} \tag{8-1}$$

This electrical margining system response depends on the PHY tuning settings $\boldsymbol{x}$ (EQ coefficients), the operating conditions $\boldsymbol{\psi}$ (voltage and temperature), and the devices $\boldsymbol{\delta}$ (silicon skew and external devices). Five input variables that represent the SATA Rx PHY tuning coefficients are used, which are settings used in three main Rx circuitry blocks (CTLE, VGA, and CDR). $e_\text{w} \in \Re$ and $e_\text{h} \in \Re$ are obtained from measured parameters,

$$e_\text{w}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = e_\text{wr}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) + e_\text{wl}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \tag{8-2}$$

$$e_\text{h}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = e_\text{hh}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) + e_\text{hl}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \tag{8-3}$$

where $e_\text{wr} \in \Re$ and $e_\text{wl} \in \Re$ are the eye width-right and eye width-left measured parameters, respectively, and $e_\text{hh} \in \Re$ and $e_\text{hl} \in \Re$ are the eye height-high and eye height-low parameters, respectively.

8.2.2 Coarse Model

Surrogate models can be constructed using data from high-reliability models or from measurements, and provide fast approximations of the original system or component at new design points [Queipo-05]. In [Rangel-Patiño-17a], several surrogate models are analyzed trained with different DoE techniques to find a good coarse model able to approximate a USB3.1 Gen1 HSIO link with a very reduced amount of measurements, selecting the best combination of surrogate modeling technique and DoE in terms of accuracy and development time. Here, [Rangel-Patiño-17c] is followed to develop a coarse surrogate model for an HSIO link SATA Gen3. By using the

PHY tuning setting coefficients as inputs $\boldsymbol{x}$ and the corresponding eye height and width as outputs $\boldsymbol{R}_{\mathrm{c}}$, the Kriging surrogate modeling technique [Rangel-Patiño-17b] is selected with a Sobol [Rangel-Patiño-17c] DoE approach with only 50 samples.

8.2.3 Objective Function

Since the objective is to find out the optimal set of PHY tuning settings $\boldsymbol{x}$ that maximize the functional eye diagram area, the objective function is given by

$$u(\boldsymbol{x}) = -\left[e_{\mathrm{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right]\left[e_{\mathrm{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] \tag{8-4}$$

During optimization, both $\boldsymbol{\psi}$ and $\boldsymbol{\delta}$ are kept fixed.

8.3. ASM Optimization

ASM starts by finding the optimal coarse model design $\boldsymbol{x}_{\mathrm{c}}^{*}$ from direct numerical optimization, that yields the optimal coarse model response, $\boldsymbol{R}_{\mathrm{c}}(\boldsymbol{x}_{\mathrm{c}}^{*}) = \boldsymbol{R}_{\mathrm{c}}^{*}$. ASM takes $\boldsymbol{R}_{\mathrm{c}}^{*}$ as the target response for the fine model, aiming to find a fine model design, $\boldsymbol{x}_{\mathrm{f}}^{\mathrm{SM}}$ (also known as the space-mapped solution) that makes the fine model response $\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}_{\mathrm{f}}^{\mathrm{SM}})$ as close as possible to the target response $\boldsymbol{R}_{\mathrm{c}}^{*}$.

The central part of the ASM algorithm is the parameter extraction process [Rayas-Sánchez-16], which can be considered as a vector function $\boldsymbol{P}$ representing the mapping between both design parameter spaces, $\boldsymbol{x}_{\mathrm{c}}^{(i)} = \boldsymbol{P}(\boldsymbol{x}_{\mathrm{f}}^{(i)})$. If the current extracted parameters $\boldsymbol{x}_{\mathrm{c}}^{(i)}$ correspond approximately to $\boldsymbol{x}_{\mathrm{c}}^{*}$, then the current fine model response approximates the desired response, $\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}_{\mathrm{f}}^{(i)}) \approx \boldsymbol{R}_{\mathrm{c}}^{*}$. To find $\boldsymbol{x}_{\mathrm{f}}^{\mathrm{SM}}$, the ASM algorithm solves a system of nonlinear equations defined as,

$$\boldsymbol{f}(\boldsymbol{x}_{\mathrm{f}}) = \boldsymbol{P}(\boldsymbol{x}_{\mathrm{f}}) - \boldsymbol{x}_{\mathrm{c}}^{*} \tag{8-5}$$

The parameter extraction process consists of finding, for the i-th fine model design $\boldsymbol{x}_{\mathrm{f}}^{(i)}$, the coarse model design $\boldsymbol{x}_{\mathrm{c}}^{(i)}$ whose corresponding response $\boldsymbol{R}_{\mathrm{c}}(\boldsymbol{x}_{\mathrm{c}}^{(i)})$ is as close as possible to $\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}_{\mathrm{f}}^{(i)})$. This can be realized by solving

$$\boldsymbol{P}(\boldsymbol{x}_{\mathrm{f}}^{(i)}) = \boldsymbol{x}_{\mathrm{c}}^{(i)} = \arg\min_{\boldsymbol{x}_{\mathrm{c}}} \left\| \boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}_{\mathrm{f}}^{(i)}) - \boldsymbol{R}_{\mathrm{c}}(\boldsymbol{x}_{\mathrm{c}}) \right\|_2^2 \tag{8-6}$$

Begin

$\boldsymbol{x}_{\mathrm{c}}^{*} = \arg\min_{\boldsymbol{x}_{\mathrm{c}}} U(\boldsymbol{R}_{\mathrm{c}}(\boldsymbol{x}_{\mathrm{c}}, \psi))$

$i = 0, \boldsymbol{x}_{\mathrm{f}}^{(i)} = \boldsymbol{x}_{\mathrm{c}}^{*}, \boldsymbol{B}^{(i)} = \boldsymbol{I}, \ \delta = 0.3$

$\boldsymbol{f}^{(i)} = \boldsymbol{P}(\boldsymbol{x}_{\mathrm{f}}^{(i)}) - \boldsymbol{x}_{\mathrm{c}}^{*}$ using (8-6)

repeat until *StoppingCriteria*

solve $\boldsymbol{B}^{(i)}\boldsymbol{h}^{(i)} = -\boldsymbol{f}^{(i)}$ for $\boldsymbol{h}^{(i)}$

$\boldsymbol{x}_{\mathrm{f}}^{(\mathrm{test})} = \boldsymbol{x}_{\mathrm{f}}^{(i)} + \boldsymbol{h}^{(i)}$

while $\boldsymbol{x}_{\mathrm{f}}^{(\mathrm{test})} \prec \boldsymbol{x}_{\mathrm{f}}^{\min} \vee \boldsymbol{x}_{\mathrm{f}}^{(\mathrm{test})} \succ \boldsymbol{x}_{\mathrm{f}}^{\max}$

$\boldsymbol{h}^{(i)} = \delta \boldsymbol{h}^{(i)}$

$\boldsymbol{x}_{\mathrm{f}}^{(\mathrm{test})} = \boldsymbol{x}_{\mathrm{f}}^{(i)} + \boldsymbol{h}^{(i)}$

end

$\boldsymbol{x}_{\mathrm{f}}^{(i+1)} = \boldsymbol{x}_{\mathrm{f}}^{(\mathrm{test})}$

$\boldsymbol{f}^{(i+1)} = \boldsymbol{P}(\boldsymbol{x}_{\mathrm{f}}^{(i+1)}) - \boldsymbol{x}_{\mathrm{c}}^{*}$ using (8-6)

$\boldsymbol{B}^{(i+1)} = \boldsymbol{B}^{(i)} + \dfrac{\boldsymbol{f}^{(i)}\boldsymbol{h}^{(i)\mathrm{T}}}{\boldsymbol{h}^{(i)\mathrm{T}}\boldsymbol{h}^{(i)}}, \ i = i+1$

end

Fig. 8.3 Pseudo-code for the Broyden-based input space mapping optimization. Figure taken from [Rayas-Sánchez-11].

The system of equations $\boldsymbol{f}(\boldsymbol{x}_{\mathrm{f}})$ is directly solved by using Broyden's updating formula [Broyden-65]. Notice that solving $\boldsymbol{f}(\boldsymbol{x}_{\mathrm{f}})$ is equivalent to solving the mapping equation $\boldsymbol{P}(\boldsymbol{x}_{\mathrm{f}}) = \boldsymbol{x}_{\mathrm{c}}^{*}$, which denotes that a solution to the system is found when the extracted parameters are equal to the optimal coarse model design, implying also that the fine model response is sufficiently close to the target response.

The next iterate in the algorithm is predicted by

$$\boldsymbol{x}_{\mathrm{f}}^{(i+1)} = \boldsymbol{x}_{\mathrm{f}}^{(i)} + \boldsymbol{h}^{(i)} \tag{8-7}$$

where $\boldsymbol{h}^{(i)}$ solves the linear system defined as,

$$\boldsymbol{B}^{(i)}\boldsymbol{h}^{(i)} = -\boldsymbol{f}(\boldsymbol{x}_{\mathrm{f}}^{(i)}) = -\boldsymbol{f}^{(i)} \tag{8-8}$$

where Broyden matrix $\boldsymbol{B}$ is an approximation of the Jacobian of $\boldsymbol{f}$ with respect to $\boldsymbol{x}_{\mathrm{f}}$ at the current iterate i. The matrix $\boldsymbol{B}$ is first initialized by the identity matrix and updated by using Broyden's formula,

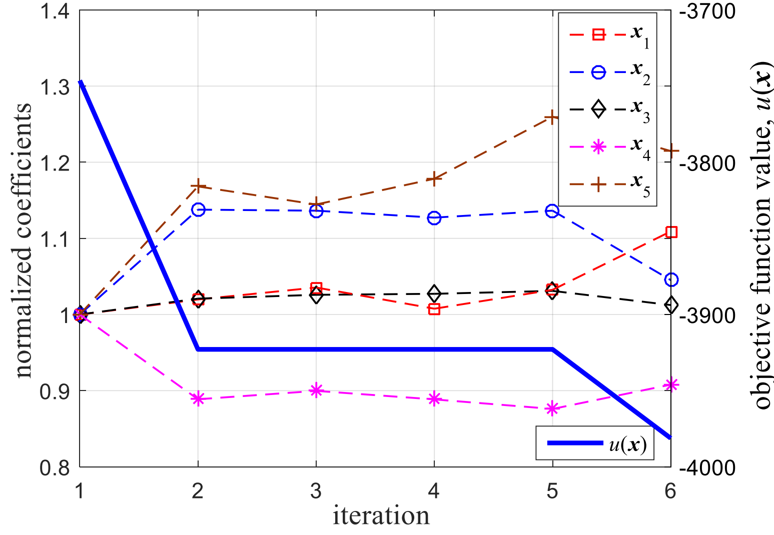


Fig. 8.4 Normalized SATA coefficients and objective function values across SM optimization iterations.

$$\boldsymbol{B}^{(i+1)} = \boldsymbol{B}^{(i)} + \frac{\boldsymbol{f}^{(i)}\boldsymbol{h}^{(i)\mathrm{T}}}{\boldsymbol{h}^{(i)\mathrm{T}}\boldsymbol{h}^{(i)}} \tag{8-9}$$

The pseudo-code used to implement this algorithm is based on [Rayas-Sánchez-11] as shown in Fig. 8.3.

The stopping criteria considered in this work include four possibilities: when a root of the nonlinear system is found; when the relative change in the fine-model design parameters is small enough; when the maximum relative error in the fine-model response with respect to the target response is small enough; or when a maximum number of iterations is reached; as follows

$$\left\|\boldsymbol{f}(\boldsymbol{x}_\mathrm{f}^{(i)})\right\|_\infty < \varepsilon_1 \vee \tag{8-10}$$

$$\left\|\boldsymbol{x}_\mathrm{f}^{(i+1)} - \boldsymbol{x}_\mathrm{f}^{(i)}\right\|_2 \le \varepsilon_2(\varepsilon_2 + \left\|\boldsymbol{x}_\mathrm{f}^{(i)}\right\|_2) \vee \tag{8-11}$$

$$\left\|\boldsymbol{R}_\mathrm{f}(\boldsymbol{x}_\mathrm{f}^{(i)}) - \boldsymbol{R}_\mathrm{c}(\boldsymbol{x}_\mathrm{c}^{*})\right\|_\infty \le \varepsilon_3(\varepsilon_3 + \left\|\boldsymbol{R}_\mathrm{c}(\boldsymbol{x}_\mathrm{c}^{*})\right\|_\infty) \vee \tag{8-12}$$

$$i > i_{\max} \tag{8-13}$$

where ε_1, ε_2, and ε_3 are arbitrary small positive scalars.

8.4. Optimization Results

After applying the Broyden-based input SM algorithm [Rayas-Sánchez-16], a space-

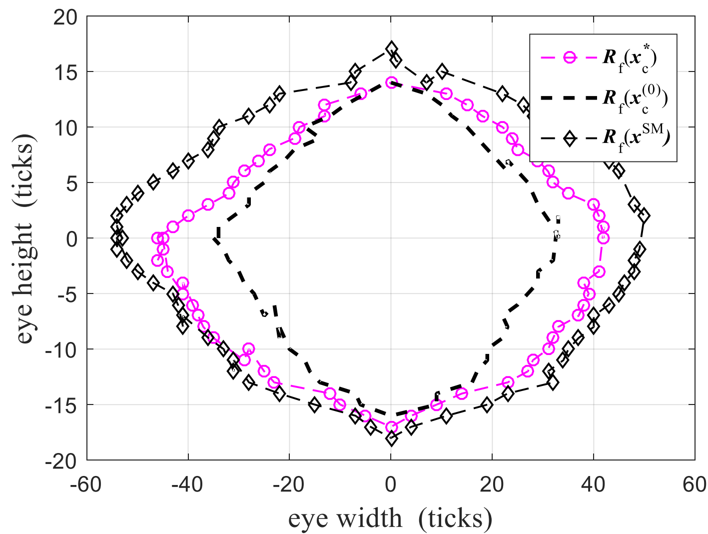


Fig. 8.5 Comparison between the system fine model responses at the initial Rx EQ coefficients, $\boldsymbol{x}_c^{(0)}$, at the optimal coarse model solution, $\boldsymbol{x}_c^*$, and at the space-mapped solution found, $\boldsymbol{x}^{SM}$.

mapped solution, $\boldsymbol{x}^{SM}$, is found in just 6 iterations (or fine model evaluations), as shown in Fig. 8.4. The set of Rx EQ coefficients contained in $\boldsymbol{x}^{SM}$ makes the measured SATA Rx inner eye height and width of the PCH as open as that one predicted by the optimized coarse surrogate model. The SM solution ($\boldsymbol{x}^{SM}$) found makes an improvement of 85% on the fine model eye diagram area as compared to that one with the initial settings ($\boldsymbol{x}_c^{(0)}$), and a 33% improvement as compared to that one with the optimal coarse model solution ($\boldsymbol{x}_c^*$), as shown in Fig. 8.5.

The efficiency of this approach is also demonstrated by a very significant time reduction in post-Si validation and PHY tuning Rx equalization. While the traditional industrial process requires days for a complete empirical optimization (based on engineering expertise), the method proposed here can be completed in a few hours. The technique can easily be applied to other interfaces such as USB and PCI express.

8.5. Conclusion

In this chapter, it was demonstrated how the Broyden-based input SM optimization algorithm, better known as ASM, can efficiently optimize the PHY tuning receiver equalizer settings by using a low-cost low-precision surrogate as the coarse model, and a measurement-based post-silicon validation platform as the fine model. The experimental results, based on a real

industrial validation platform, demonstrated the efficiency of the method to deliver an optimal eye diagram, showing a substantial performance improvement while significantly reducing the typical time required for the PHY tuning process.

.

General Conclusions

As microprocessor design scales to the 10-nm technology and beyond, traditional pre- and post-silicon validation techniques are unsuitable to get a full system functional coverage. Technology scaling and advanced silicon packaging techniques are allowing continuously higher density of integration. Physical complexity and extreme technology process variations severely limits the effectiveness and reliability of pre-silicon validation techniques. To ensure leading performance, reliability, and compatibility in this complex environment, companies invest over hundreds of millions of dollars annually in component and platform validation.

This scenario imposes the need of sophisticated post-silicon validation approaches to consider complex electromagnetic phenomena and large manufacturing fluctuations observed in actual physical platforms. However, product complexity, performance requirements, and time-to-market (TTM) commitments are adding tremendous pressure on post-silicon validation. In this situation, validation teams are continuously looking for opportunities to make validation faster and cheaper. The idea of connecting simulation and optimization with post-silicon validation has been discussed and demonstrated trough this doctoral dissertation as a viable solution to overcome the current post-silicon challenges to improve efficiency and quality of HSIO links validation.

In Chapter 1, a detailed description of post-silicon validation was presented. The key challenges in post-silicon validation of HSIO links were listed. The idea of connecting simulation with validation has been discussed as a potential solution to overcome the current post-silicon challenges. It is concluded that bringing CAD methodologies into post-silicon can improve validation efficiency

At higher data rates, several EQ techniques can be used to compensate for jitter and noise and then maximizing the eye diagram before the Rx sampling fails to satisfy the required BER. In Chapter 2, an overview of the most popular existing EQ topologies to mitigate the effects of jitter and noise in HSIO links was presented. Design trade-offs are required between Tx and Rx implementations or a combination of both. It is concluded that equalization techniques, such as the continuous-time adaptive equalizer to adaptively determine equalizer settings, are required.

The design complexity has made it almost impossible for engineers armed with legacy measurement technologies, such as oscilloscopes, to accurately measure the overall signal integrity

on HSIO. Using on-chip embedded instrumentation within silicon, in conjunction with software that accesses this on-board logic is a solution to this challenge. In Chapter 3, the HSIO testing methods at both chip and system levels were presented. Functional testing by using embedded instruments based on the IBIST was explained in detail, and a new approach to design validation, known as SMV was discussed.

The empirical optimization of receiver analog circuitry in modern HSIO links is a very time consuming post-silicon validation process. Current industrial practices are based on exhaustive enumeration methods to improve either the system margins or the jitter tolerance compliance test. In Chapter 4, a holistic optimization approach that merges system margining and jitter tolerance measurements for PHY tuning was demonstrated. The method uses Kriging to build a surrogate model for efficient optimization, and a novel objective function based on system margining and jitter tolerance measurements. The experimental results demonstrated the efficiency of the method to deliver optimal margins while ensuring jitter tolerance compliance, showing a substantial improvement for both system margins and jitter tolerance as compared with the current industrial practice, and dramatically accelerating the typical time required for PHY tuning.

Some interface specifications define requirements to perform EQ at the Tx. Adjusting the Tx equalization across PVT and different interconnect channels can be also a very time-consuming task in post-silicon validation. Therefore, to overcome this challenge, Chapter 5 proposed a direct optimization approach based on suitable objective functions formulation to efficiently tune the Tx FIR filter for the Ethernet SFP+ interface. The optimized coefficients are evaluated by measuring the real eye diagram of the physical system, showing a great mitigation of the ISI effects, and accelerating the typical required time for Tx coefficients tuning. The approach allows fulfilling in an efficient manner strict IEEE and fibre optics channel standards as applied to high-speed interconnects based on optical interfaces, significantly enhancing current industrial practices.

In order to mitigate channel effects due to the increase in transmission speeds, the PCIe specification defines requirements to perform EQ at the Tx and at the Rx. During the EQ process, one combination of Tx/Rx EQ coefficients must be selected to meet the performance requirements of the system. Testing all possible coefficient combinations is prohibitive. In Chapter 6, it is proposed a direct optimization approach for PCIe link equalization based on a suitable objective function formulation to efficiently tune the Tx FIR filter and Rx CTLE EQ coefficients to mitigate ISI and other undesired channel effects, and successfully comply with the PCIe specification. The

optimized EQ coefficients were evaluated by measuring the real eye diagram of the physical system, demonstrating a great mitigation of the ISI and channel effects, and accelerating the typically required long time for Tx and Rx EQ coefficients tuning; significantly enhancing current PCIe Tx/Rx tuning industrial practices in post-silicon validation.

While an accurate surrogate model is desirable for direct surrogate-based optimization, it can be very computationally expensive. However, by combining a good modeling technique with a suitable DoE approach, an efficient surrogate model can be developed. In Chapter 7, several surrogate models trained with different DoE techniques are studied to find a good coarse model able to approximate a real server HSIO link with a very reduced amount of measurements. Then, a metamodeling technique based on artificial neural networks is presented to efficiently simulate the effects of the receiver equalization circuitry in industrial HSIO links. The neural model is trained using different DoE approaches to identify the best system response sampling strategy that yields an acceptable neural model with a very reduced set of learning and testing samples. Through this procedure, an efficient surrogate model is found that approximates the system with a reduced set of testing and training data, suitable for a future co-Kriging or space mapping optimization for PHY tuning.

In Chapter 8, it was demonstrated how the Broyden-based input SM algorithm can efficiently optimize the PHY tuning Rx equalizer settings by using a low-cost low-precision surrogate model, and a measurement-based post-silicon validation platform as the fine model. The experimental results, based on a real industrial validation platform, demonstrated the efficiency of the method to deliver an optimal eye diagram, showing a substantial performance improvement and accelerating the typical required time for PHY tuning.

In essence, this doctoral dissertation proposes direct and surrogate-based optimization methods, including space mapping, based on suitable objective functions to efficiently tune the Tx and Rx equalizers coefficients. The experimental results, based on real industrial validation platforms, demonstrated the efficiency of the proposed methods, showing a substantial improvement as compared with the current industrial practice, and accelerating the typical required time for equalizers tuning.

The proposed optimization techniques along with the objective functions are not limited to server validation platforms. The same procedures could be applied to other computer platforms for post-silicon validation, such as the client market segment to include laptops and desktops, and

devices segment to include cell phones and tablets.

This thesis dissertation offers the possibility of a number of future research opportunities. One possible future work consists of using the proposed optimization techniques for PHY tuning but including in the objective functions power consumption parameters. Capabilities of servers and their power consumption have increased over time. Servers in data centers waste a substantial amount of energy. The reason is that servers are deployed and configured for peak capacity and performance. Also, when servers are in operation, the entire chassis and rack will heat up; cooling is then required to keep the components at a safe operating temperature, but cooling takes additional power. Therefore, power consumption emerges as a significant expense for many companies. There is currently a high research effort to reduce the servers power consumption. Therefore, through the optimization process the performance of the different HSIO interfaces could be optimized considering as constraints power consumption parameters, then the SoC power consumption could be optimized as well.

A computer SoC is mainly comprised of a CPU and a PCH in the same package. Communication between both chips is through DMI and uplinks interfaces. The optimization techniques along with the objective functions for PCIe proposed in this thesis dissertation, could also be applied in a future work for the DMI and uplinks PHY tuning.

The ultimate goal of post-silicon electrical validation is to statistically predict the HSIO electrical behavior in a real system environment across different process corners and operating conditions. Such a prediction leads to a reasonable PRQ decision. One of the process corners is aging. Once post-silicon validation testing is completed, some silicon samples are exposed to an aging process which can take few weeks. Then, margin data is collected from these aging parts and use for the statistically prediction. The surrogate modeling techniques discussed in this thesis dissertation could also be used in a future work for silicon aging modeling. By having HSIO aging models, the aging process time could be avoided, further accelerating the post-silicon electrical validation.

Conclusiones Generales

A medida que el diseño de los microprocesadores se escala a la tecnología de los 10 nm y más allá, las técnicas tradicionales de validación pre- y post-silicio son inadecuadas para conseguir una cobertura funcional completa del sistema. Los avances tecnológicos en manufactura de silicio y las nuevas técnicas de empaque han permitido una alta integración de circuitos. Complejidades físicas del diseño, y variaciones extremas en los procesos tecnológicos limitan severamente la efectividad y confiabilidad de las técnicas de validación pre-silicio. Para asegurar un alto rendimiento, confiabilidad y compatibilidad en este ambiente tan complejo, las compañías de semiconductores invierten cientos de millones de dólares anualmente en plataformas y componentes para validación.

Este escenario impone la necesidad de técnicas sofisticadas de validación post-silicio que consideren el complejo fenómeno electromagnético, y las variaciones del sistema resultado de los procesos de manufactura que se observan en las plataformas de validación. Sin embargo, la complejidad del producto, los requerimientos de desempeño, y los tiempos de lanzamiento a producción ocasionan una gran presión en la validación post-silicio. En esta situación, los equipos de validación constantemente están en búsqueda de oportunidades para hacer la validación más rápida y económica. La idea de conectar técnicas de simulación y optimización con la validación post-silicio se ha planteado a través de esta tesis doctoral como una solución viable para superar los actuales retos en post-silicio y mejorar la eficiencia y calidad en la validación de los enlaces HSIO.

En el Capítulo 1, una descripción detallada de los que es la validación post-silicio fue presentada. Los retos más importantes en la validación post-silicio de los enlaces HSIO fueron listados. La idea de conectar simulación con validación ha sido discutida como solución potencial para superar los actuales retos post-silicio. Se concluye que conectar metodologías CAD con post-silicio puede mejorar la eficiencia de la validación.

En altas velocidades de transmisión de datos, varias técnicas EQ pueden ser utilizadas para compensar el efecto del ruido y entonces maximizar el diagrama de ojo antes de que el Rx muestre fallas y poder satisfacer el BER requerido. En el Capítulo 2, una revisión de las topologías EQ existentes más populares para mitigar los efectos del ruido en los enlaces HSIO fue presentada.

Compromisos de diseño son requeridos entre las implementaciones de Tx y Rx. Se concluye que las técnicas de ecualización, tales como el ecualizador adaptivo de tiempo continuo, son requeridas para determinar los parámetros del ecualizador de manera adaptiva.

La complejidad del diseño ha hecho casi imposible para los ingenieros armados con tecnologías de medición tradicionales, tales como osciloscopios, poder medir con precisión la integridad de señal en los enlaces HSIO. Empleando instrumentos embebidos en el silicio, en combinación con programación que permita el acceso a la lógica, constituyen una solución a este problema. En el Capítulo 3, métodos de prueba de HSIO, tanto a nivel componente como a nivel sistema, fueron presentados. Pruebas funcionales empleando instrumentos embebidos basados en IBIST fueron presentadas en detalle, y un nuevo enfoque para validación de diseño conocido como SMV fue presentado.

La optimización de los circuitos analógicos del receptor en los modernos enlaces HSIO es un proceso que lleva tiempo en la validación post-silicio. Las actuales prácticas industriales están basadas en métodos de enumeración exhaustiva para mejorar ya sea los márgenes del sistema o bien las pruebas por especificación de tolerancia al ruido. En el Capítulo 4 se demostró un enfoque de optimización holístico para sintonizar el PHY, que fusiona los márgenes del sistema con las mediciones de tolerancia al ruido. El método emplea Kriging para construir un modelo sustituto para optimización eficiente, y una novedosa función objetivo basada en los márgenes del sistema y las mediciones de tolerancia al ruido. Los resultados experimentales demostraron la eficacia del método para lograr márgenes óptimos, asegurando al mismo tiempo el cumplimiento a las especificaciones de tolerancia al ruido, los resultados también demostraron una mejora sustancial en márgenes y tolerancia al ruido de fase comparada con la práctica industrial actual, pero además acelerando en forma dramática el tiempo típico requerido para la sintonización del PHY.

Algunas especificaciones de interface definen requerimientos para efectuar EQ en el Tx. Lograr ajustar la ecualización Tx considerando PVT y diferentes canales de interconexión puede consumir demasiado tiempo en la validación post-silicio. Para superar este reto, en el Capítulo 5 se propuso un enfoque de optimización directa basado en la formulación de una función objetivo adecuada para eficientemente sintonizar el filtro FIR en el TX para la interface Ethernet SFP+. Los coeficientes optimizados son evaluados por medio de mediciones de diagrama de ojo en un sistema implementado en un laboratorio industrial, mostrando una mitigación sustancial de los efectos ISI, y acelerando el tiempo típico requerido para sintonizar los coeficientes en el Tx. El método permite

cumplir eficientemente los estrictos estándares IEEE de fibra óptica para interconexiones de alta velocidad basados en interfaces ópticas, y además mejorar significativamente las actuales prácticas industriales.

Para poder mitigar los efectos de canal debido al incremento en las velocidades de transmisión, la especificación industrial de PCIe define requerimientos para efectuar EQ tanto en el Tx como en el Rx. Durante el proceso de EQ, una combinación de coeficientes EQ Tx/Rx debe ser seleccionada para cumplir los requerimientos de desempeño del sistema. Evaluar todas las posibles combinaciones es prohibitivo. En el Capítulo 6 se propuso un enfoque de optimización directa para la ecualización del enlace PCIe basado en una formulación de función objetivo adecuada para sintonizar eficientemente el filtro FIR en el Tx, y los coeficientes EQ del CTLE en el Rx y así poder mitigar ISI y otros efectos no deseados del canal, y exitosamente cumplir con la especificación PCIe. Los coeficientes EQ optimizados fueron evaluados por medio de mediciones de diagramas de ojo, demostrando una significativa mitigación del efecto ISI y los efectos del canal, además de acelerar el tiempo típico requerido para sintonizar los coeficientes EQ del Tx y Rx; mejorando significativamente las actuales practicas industriales para sintonización de PCIe Tx/Rx en la validación post-silicio.

En general, un modelo sustituto preciso siempre es deseable para optimización, sin embargo, puede resultar muy costoso computacionalmente obtenerlo. Combinando una buena técnica de modelado con un DoE adecuado, un modelo sustituto eficiente puede ser desarrollado. En el Capítulo 7, varios modelos sustitutos entrenados con diferentes técnicas de DoE son estudiados para encontrar un modelo burdo suficientemente bueno, capaz de aproximarse a un verdadero enlace de HSIO empleando una muy reducida cantidad de mediciones. Adicionalmente, una técnica de modelado basada en redes neuronales artificiales es presentada para eficientemente simular la circuitería de ecualización de un enlace HSIO en un ambiente industrial. El modelo neuronal es entrenado empleando diferentes DoE para identificar la mejor estrategia de muestreo del sistema, que permita un modelo neuronal aceptable con un reducido conjunto de muestras de prueba y aprendizaje. A través de este procedimiento, un modelo sustituto eficiente es encontrado, el cual se aproxima al sistema con un reducido conjunto de datos de entrenamiento, siendo adecuado para optimización basado en mapeo espacial o co-Kriging en la sintonización del PHY.

En el Capítulo 7 fue demostrado como el algoritmo de mapeo espacial basado en Broyden puede eficientemente optimizar el PHY para la sintonización de los parámetros del ecualizador del

Rx utilizando un modelo sustituto de bajo costo computacional y baja presión, y una plataforma de validación post-silicio como el modelo fino. Los resultados experimentales demostraron la eficiencia del método propuesto, permitiendo logra un diagrama de ojo optimizado, mostrando una mejora sustancial en el desempeño del sistema, y acelerando el tiempo típico para sintonización de PHY.

En esta tesis doctoral, métodos de optimización directa, de modelo sustituto, e incluyendo mapeo espacial, fueron propuestos basados en novedosas funciones objetivos para eficientemente sintonizar los coeficientes de los ecualizadores en el Tx y Rx. Los resultados experimentales, basados en una plataforma de validación post-silicio en un ambiente industrial demostraron la eficiencia de los métodos propuestos, mostrando una mejora sustancial comparada con las prácticas industriales actuales, y acelerando el tiempo típico requerido para sintonizar los ecualizadores.

Las técnicas de optimización propuestas, junto con las funciones objetivo desarrolladas, no están limitas a plataformas de validación de servidores. Los mismos procedimientos pueden ser aplicados a otras plataformas computacionales para validación post-silicio, tales como los segmentos de mercado dedicados a laptops, y desktops, así como a teléfonos celulares y a tabletas.

Esta tesis ofrece la posibilidad de un número de oportunidades de investigación futura. Un posible trabajo futuro consiste en usar las técnicas de optimización propuestas para la sintonización del PHY pero incluyendo en las funciones objetivo parámetros de consumo de energía. Las capacidades de los servidores se han incrementado significativamente, pero también su consumo de energía. Los servidores en los centros de datos consumen una gran cantidad de energía. Esto se debe a que los servidores son configurados y utilizados a su máxima capacidad de operación. Además, cuando los servidores están en operación, todo el chasis se calienta; así que se requiere refrigeración para mantener los sistemas a una temperatura de operación segura, pero la refrigeración requiere energía adicional. Así que el consumo de energía se ha convertido en un gasto significativo para las compañías con grandes centros de datos. Actualmente existe un gran esfuerzo en investigación para reducir el consumo de energía de los servidores. Por lo tanto, a través de un abordaje de optimización similar al propuesto en esta tesis, se podría optimizar el rendimiento de las diferentes interfaces de HSIO considerando como restricciones parámetros de consumo de energía, minimizando así el consumo de la misma.

Un SoC para computadoras está constituido principalmente por un CPU y un PCH en el

mismo empaquetado. La comunicación entre ambos circuitos integrados es a través de las interfaces DMI y *uplinks*. Las técnicas de optimización y la función objetivo para PCIe propuestas en esta tesis doctoral, podrían también ser adaptadas a la sintonización del PHY de DMI y *uplinks*, optimizando de esta manera la comunicación entre el CPU y el PCH.

La meta final de la validación eléctrica en post-silicio es poder predecir estadísticamente el desempeño eléctrico de las interfaces HSIO en un sistema empleado en su aplicación comercial, en las diferentes condiciones de operación y considerando las variaciones de procesos. Esta predicción permite una decisión PRQ razonable. Una de las variaciones de procesos es el envejecimiento. Una vez que las pruebas de validación post-silicio se han completado, algunas muestras son expuestas a un proceso de envejecimiento, el cual puede tomar algunas semanas. Posteriormente, datos de márgenes son colectados de estas partes envejecidas y los datos son utilizados para la predicción estadística. Las técnicas de modelado sustituto discutidas en esta tesis doctoral podrían ser empleadas para modelar el envejecimiento. Teniendo modelos HSIO de envejecimiento, el tiempo dedicado al mismo podría evitarse, y entonces se podría acelerar aún más la validación eléctrica post-silicio.

Appendix

A. LIST OF INTERNAL RESEARCH REPORTS

1) F. E. Rangel-Patiño, J. E. Rayas-Sánchez, A. Viveros-Wacher, E. A. Vega-Ochoa, and N. Hakim, "High-speed links receiver optimization in post-silicon validation exploiting Broyden-based input space mapping," Internal Report *PhDEngScITESO-18-04-R (CAECAS-18-02-R)*, ITESO, Tlaquepaque, Mexico, April 2018.

2) F. E. Rangel-Patiño, J. E. Rayas-Sánchez, E. A. Vega-Ochoa, and N. Hakim, "Direct optimization of a PCI Express link equalization in industrial post-silicon validation," Internal Report *PhDEngScITESO-17-32-R (CAECAS-17-15-R)*, ITESO, Tlaquepaque, Mexico, Nov. 2017.

3) F. E. Rangel-Patiño, J. E. Rayas-Sánchez, A. Viveros-Wacher, J. L. Chávez-Hurtado, E. A. Vega-Ochoa, and N. Hakim, "Post-silicon receiver equalization metamodeling by using artificial neural networks," Internal Report *PhDEngScITESO-17-29-R (CAECAS-17-13-R)*, ITESO, Tlaquepaque, Mexico, Aug. 2017.

4) F. E. Rangel-Patiño and J. E. Rayas-Sánchez, "Circuit modeling with artificial neural networks," Internal Report *PhDEngScITESO-17-25-R (CAECAS-17-12-R)*, ITESO, Tlaquepaque, Mexico, Jul. 2017.

5) F. E. Rangel-Patiño, J. L. Chávez-Hurtado, A. Viveros-Wacher, J. E. Rayas-Sánchez, and N. Hakim, "Coarse surrogates for eye diagram system margining optimization in a server post-silicon validation platform," Internal Report *PhDEngScITESO-17-08-R (CAECAS-17-06-R)*, ITESO, Tlaquepaque, Mexico, May 2017.

6) F. E. Rangel-Patiño, I. Duron-Rosales, J. E. Rayas-Sánchez, J. L. Chávez-Hurtado, and N. Hakim, "Reconfigurable FIR filter coefficient optimization in post-silicon validation to improve eye diagram for optical interconnects," Internal Report *PhDEngScITESO-17-05-R (CAECAS-17-03-R)*, ITESO, Tlaquepaque, Mexico, May 2017.

7) F. E. Rangel-Patiño, J. E. Rayas-Sánchez, and N. Hakim, “A holistic formulation for system margining and jitter tolerance optimization in industrial post-silicon validation,” Internal Report *PhDEngScITESO-16-25-R (CAECAS-16-14-R)*, ITESO, Tlaquepaque, Mexico, Dec. 2016.

8) F. E. Rangel-Patiño and J. E. Rayas-Sánchez, “An overview on channel equalization for high-speed serial links,” Internal Report *PhDEngScITESO-16-01-R (CAECAS-16-01-R)*, ITESO, Tlaquepaque, Mexico, Jan. 2016.

9) F. E. Rangel-Patiño and J. E. Rayas-Sánchez, “System marginality validation: an on-die silicon test methodology,” Internal Report *PhDEngScITESO-15-17-R (CAECAS-15-16-R)*, ITESO, Tlaquepaque, Mexico, Dec. 2015.

10) F. E. Rangel-Patiño and J. E. Rayas-Sánchez, “Towards a suitable objective function formulation for equalizer optimization for post-silicon electrical validation,” Internal Report *PhDEngScITESO-15-06-R (CAECAS-15-09-R)*, ITESO, Tlaquepaque, Mexico, Jun. 2015.

11) F. E. Rangel-Patiño and J. E. Rayas-Sánchez, “Eye-diagram approaches and their correlation for high speed interconnects analysis,” Internal Report *PhDEngScITESO-15-01-R (CAECAS-15-01-R)*, ITESO, Tlaquepaque, Mexico, Feb. 2015.

12) F. E. Rangel-Patiño, J. E. Rayas-Sánchez, and N. Hakim, “Challenges and opportunities in post-silicon electrical validation of high speed I/O’s,” Internal Report *PhDEngScITESO-14-08-R (CAECAS-14-08-R)*, ITESO, Tlaquepaque, Mexico, Oct. 2014.

13) F. E. Rangel-Patiño and J. E. Rayas-Sánchez, “Computer-aided design: historical review, state of the art, and future trends,” Internal Report *PhDEngScITESO-14-01-R (CAECAS-14-03-R)*, ITESO, Tlaquepaque, Mexico, Jul. 2014.

B. LIST OF PUBLICATIONS

B.1. Journal Papers

1) **F. E. Rangel-Patiño**, J. L. Chávez-Hurtado, A. Viveros-Wacher, J. E. Rayas-Sánchez, and N. Hakim, “System margining surrogate-based optimization in post-silicon validation,” *IEEE Trans. Microwave Theory Techn.*, vol. 65, no. 9, pp. 3109-3115, Sep. 2017. (p-ISSN: 0018-9480; e-ISSN: 1557-9670; published online: 29 May 2017; DOI: 10.1109/TMTT.2017.2701368)

2) **F. E. Rangel-Patiño**, A. Viveros-Wacher, J. E. Rayas-Sánchez, I. Durón-Rosales, E. A. Vega-Ochoa, N. Hakim and E. López-Miralrio, “A holistic formulation for system margining and jitter tolerance optimization in industrial post-silicon validation,” *IEEE Trans. Emerging Topics Computing*, vol. 6, no. **, pp. **-**, ** 2018. (p-ISSN: **; e-ISSN: 2168-6750; published online: 29 Sep. 2017; DOI: 10.1109/TETC.2017.2757937; regular publication pending)

3) **F. E. Rangel-Patiño**, J. E. Rayas-Sánchez, A. Viveros-Wacher, J. L. Chávez-Hurtado, E. A. Vega-Ochoa, and N. Hakim, “Post-silicon receiver equalization metamodeling by artificial neural networks,” *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. **, pp. **, *** 2018. (p-ISSN: 0278-0070; e-ISSN: 1937-4151; published online: 8 May 2018; DOI: 10.1109/TCAD.2018.2834403; regular publication pending)

B.2. Conference Papers

1) **F. Rangel-Patino**, A. Viveros-Wacher, J. E. Rayas-Sánchez, E. A. Vega-Ochoa, I. Duron-Rosales, and N. Hakim, “A holistic methodology for system margining and jitter tolerance optimization in post-silicon validation,” in *IEEE MTT-S Latin America Microwave Conf. (LAMC-2016)*, Puerto Vallarta, Mexico, Dec. 2016, pp. 1-4. (ISBN: 978-1-5090-4288-3;

e-ISBN: 978-1-5090-4287-6; INSPEC: 16670749; DOI: 10.1109/LAMC.2016.7851268).

2) I. Duron-Rosales, **F. Rangel-Patino**, J. E. Rayas-Sánchez, J. L. Chávez-Hurtado, and N. Hakim, “Reconfigurable FIR filter coefficient optimization in post-silicon validation to improve eye diagram for optical interconnects,” in *Int. Caribbean Conf. Devices, Circuits, and Systems (ICCDCS-2017)*, Cozumel, Mexico, Jun. 2017, pp. 85-88. (e-ISSN: 2165-3550; p-ISBN: 978-1-5386-1963-6; e-ISBN: 978-1-5386-1962-9; INSPEC: 16996086; DOI: 10.1109/ICCDCS.2017.7959697).

3) **F. Rangel-Patino**, J. L. Chávez-Hurtado, A. Viveros-Wacher, J. E. Rayas-Sánchez, and N. Hakim, “Eye diagram system margining surrogate-based optimization in a server silicon validation platform,” in *European Microwave Conf. (EuMC-2017)*, Nuremberg, Germany, Oct. 2017, pp. 540-543. (ISBN: 978-1-5386-3964-1; e-ISBN: 978-2-87487-047-7; https://www.researchgate.net/publication/323571676).

4) **F. E. Rangel-Patiño**, J. E. Rayas-Sánchez, E. A. Vega-Ochoa, and N. Hakim, “Direct optimization of a PCI Express link equalization in industrial post-silicon validation,” in *IEEE Latin American Test Symp. (LATS 2018)*, Sao Paulo, Brazil, Mar. 2018, pp. 1-6. (ISBN: 978-1-5386-1473-0; e-ISBN: 978-1-5386-1472-3; INSPEC: 17749128; DOI: 10.1109/LATW.2018.8347238).

5) A. Viveros-Wacher, R. Baca-Baylón, **F. E. Rangel-Patiño**, M. A. Dávalos-Santana, E. A. Vega-Ochoa, and J. E. Rayas-Sánchez, “Jitter tolerance acceleration using the golden section optimization technique,” in *IEEE Latin American Symp. Circuits and Systems Dig. (LASCAS 2018)*, Puerto Vallarta, Mexico, Feb. 2018, pp. 1-4. (e-ISSN: 2473-4667; p-ISBN: 978-1-5386-2312-1; e-ISBN: 978-1-5386-2311-4; DOI: 10.1109 /LASCAS.2018.8399908).

6) **F. E. Rangel-Patiño**, J. E. Rayas-Sánchez, A. Viveros-Wacher, E. A. Vega-Ochoa, and N. Hakim, “High-speed links receiver optimization in post-silicon validation exploiting Broyden-based input space mapping,” in *IEEE MTT-S Int. Conf. Num. EM Mutiphysics*

Modeling Opt. RF, Microw., Terahertz App. (NEMO-2018), Reykjavik, Iceland, Aug. 2018, pp. 1-3.

7) J. E. Rayas-Sánchez, **F. E. Rangel-Patiño**, A. Viveros-Wacher, J. L. Chávez-Hurtado, J. R. del-Rey, F. Leal-Romo, and Z. Brito-Brito, “Industry-oriented research projects on computer-aided design of high-frequency circuits and systems at ITESO Mexico,” in *European Microwave Conf. (EuMC-2018)*, Madrid, Spain, Oct. 2018, pp. *-*. (work accepted, to be published)

B.3. INTEL Conference Papers

1) A. Viveros-Wacher, **F. E. Rangel-Patiño**, and M. Davalos, “Artificial Neural Network Meta-Models for Receiver Equalization”, in *Intel Design & Test Technology Conference (DTTC)*, Oct. 2017

2) I. Duron-Rosales, **F. E. Rangel-Patiño**, and Dhanesh M.A., N. Hakim, “Accelerated Tuning based on Direct Eye Diagram Optimization for SFI Transmitter”, in *Intel Design & Test Technology Conference (DTTC)*, Oct. 2017

3) E. A. Vega-Ochoa, A. Viveros-Wacher, D. C. Olea-Gutierrez, V. M. Castillo, **F. E. Rangel-Patiño**, "PCI Express Link Equalization by Eye Diagram Direct Optimization", in *Intel 12th Joint Seminar on Signal and Power Integrity (JSSPI)*, Jan. 2018.

4) Viveros-Wacher, R. Baca-Baylon, E. A. Vega-Ochoa, M. A. Davalos-Santana, **F. E. Rangel-Patiño**, "Jitter Tolerance Acceleration Using the Golden Section Optimization Technique", in *Intel 12th Joint Seminar on Signal and Power Integrity (JSSPI)*, Jan. 2018.

5) Dhanesh M.A., F. E. **Rangel-Patiño**, "Ethernet FIR Filter Coefficient Optimization to Improve Eye Diagram", in *Intel 12th Joint Seminar on Signal and Power Integrity (JSSPI)*, Jan. 2018.

Bibliography

[Aaron-56] M. R. Aaron, "The use of least squares in system design," *IRE Trans. Circuit Theory*, vol. CT:3, pp. 224-231, 1956.

[Abeysekera-05] S. S. Abeysekera and Y. Ye, "Zero based blind equalizer implementation using zero forcing, MMSE and decision feedback concepts," in *Proceedings of Fifth International Conference on Information, Communications and Signal Processing*, Bangkok, Feb. 2005, pp. 96-100.

[Abramovici-06] M. Abramovici, P. Bradley, K. Dwarakanath, P. Levin, G. Memmi, and D. Miller, "A reconfigurable design-for-debug infrastructure for socs," *Proceedings of the 43rd Design Automation Conference*, July 2006, pp. 7–12.

[Adir-11] A. Adir, S. Copty, S. Landa, A. Nahir, G. Shurek, A. Ziv, C. Meissner, and J. Schumann, "A unified methodology for pre-silicon verification and post-silicon validation" *Design, Automation & Test in Europe Conference & Exhibition*, 2011, pp. 1-6.

[Agilent-03] Agilent Tech. (2003), *Jitter Analysis Techniques for High Data Rates* [Online]. Available: www.agilent.com

[Agilent-05] Agilent Tech (2005), *Total Jitter Measurement at Low Probability Levels, Using Optimized BERT Scan Methods* [Online]. Available: www.agilent.com

[Alessandri-93] F. Alessandri, M. Mongiardo, and R. Sorrentino, "New efficient full wave optimization of microwave circuits by the adjoint network method," *IEEE Microwave Guided Wave Lett*., vol. 3, pp. 414–416, Nov. 1993.

[ALTERA-13] ALTERA. (2013). *FPGAs at 40 nm and >10 Gbps: Jitter, Signal Integrity, Power, and Process-Optimized Transceivers* [Online]. Available:

https://www.altera.com/en_US/pdfs/literature/wp/wp-01092-stratix-iv-gt-10gbps-transceivers.pdf.

[Anis-08] E. Anis, and N. Nicolici, "On by-passing blocking bugs during post-silicon validation," *Proc. European Test Symp*., pp. 69-74, 2008.

[ANRITSU-10] ANRITSU (2010). *Understanding Eye Pattern Measurements*, application note no. 11410-00533 (revision A) [Online]. Available: https://www.anritsu.com

[Atef-13] M. Atef and H. Zimmermann, *Optical Communication over Plastic Optical Fibers,* Berlin: Springer, 2013.

[Bala-04] V. Balan, J. Caroselli, J. Chem, C. Desai and C. Liu, "A 4.8-6.4 Gbps serial link for backplane applications using decision feedback equalization," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Oct. 2004, pp. 31-34

[Balamurugan-09] G. Balamurugan, B. Casper, J. Jaussi, M. Mansuri, F. O'Mahony, and J. Kennedy, "Modeling and analysis of high-speed I/O Links," *IEEE Transactions on Advanced Packaging*, vol. 32, no. 2, pp. 237 –247, May 2009.

[Bandler-94] J. W. Bandler, R. Biernacki, S. H. Chen, P. A. Grobelny, R. H. Hemmers, “Space mapping technique for electromagnetic optimization” *IEEE Transactions on Microwave Theory and Techniques*, vol: 42, Issue: 12, 1994, pp. 2536-2544.

[Bandler-95] J. W. Bandler, R. M. Biernacki, S. H. Chen, R. H. Hemmers, and K. Madsen, “Electromagnetic optimization exploiting aggressive space mapping,” *IEEE Trans. Microw. Theory Techn.*, vol. 41, no. 12, pp. 2874-2882, Dec. 1995.

[Bandler-04] J. W. Bandler, Q. Cheng, S. A. Dakroury, A. S. Mohamed, M. H. Bakr, K. Madsen and J. Søndergaard, “Space mapping: the state of the art,” *IEEE Trans. Microwave Theory Tech.*, vol. 52, no. 1, pp. 337-361, Jan. 2004.

[Bentley-01] B. Bentley and R. Gray, “Validating the Pentium®4 processor”, *Proceedings of the 38th annual Design Automation Conference*, Las Vegas, Nevada, United States: ACM, 2001, pp. 244-248.

[Bertsekas-05] D. Bertsekas, *Dynamic Programming and Optimal Control*, Belmont, MA: Athena Scientific, 2005.

[Beyene-07] W. T. Beyene, “Application of artificial neural networks to statistical analysis and nonlinear modeling of high-speed interconnect systems,” *IEEE Trans. Computer-Aided Design of Integrated Circuits Systems*, vol. 26, no. 1, pp. 166-176, Jan. 2007.

[Bishop-06] C. Bishop, “Pattern recognition and machine learning”, Springer, New York, 2006, vol. 4.

[Bistola-15] S. Bistola, “High-speed interconnect simulation using artificial neural networks”, in *Intel Design & Test Technology Conference (DTTC)*, Oregon, CA, Oct. 2015.

[Bojan-07] T. Bojan, A. Aguilar, M., Shlomo, E., and T. Shachar, “Functional coverage measurements and results in post-Silicon validation of Core™ 2 Duo family”, *Proceedings of the 2007 IEEE international High Level Design Validation and Test Workshop* (November 07 - 09, 2007). HLDVT. IEEE Computer Society, Washington, DC, 145-150.

[Booker-99] A. J. Booker, J. E. Dennis Jr., P. D. Frank, D. B. Serafini, V. Torczon, and M. W. Trosset, “A rigorous framework for optimization of expensive functions by surrogates,” *Struct. Optim.*, vol. 17, pp. 1–13, Feb. 1999.

[Broyden-65] C. G. Broyden, "A class of methods for solving non-linear simultaneous equations", *Math. Comp*., vol. 19, pp. 577-593, 1965.

[Caffee-12] T. Caffee, E. Johnson, “Bandwidth Tests Reveal Shrinking Eye Diagrams and Signal Integrity Problems, White Paper,” 2012 ASSET InterTech, Inc.

[Cai-02] Y. Cai, B. Laquai, and K. Luehman, “Jitter testing for gigabit serial communication transceivers,” *IEEE Des. Test Comput*., 19(1), pp. 66–74, January/February 2002.

[Cai-05] Y. Cai, A. Bhattacharyya, J. Martone, A. Verma, and W. Burchanowski, “Comprehensive production test solution for 1.5 Gbps and 3.0 Gbps serial ATA based on AWG and undersampling techniques,” in *Proc. Int. Test Conf.*, Austin, TX, November 2005, Paper 27.1.

[Casper-07] B. Casper, P. Pupalaikis, and J. Zerbe, “Serial data equalization,” in *12th Conference and Technology Exhibition DesignCon 2007,* Santa Clara, CA, Jan. 2007.

[Casper-09] B. Casper and F. O'Mahony, "Clocking analysis, implementation and measurement techniques for high-speed data links - a tutorial," *IEEE Transactions on Circuits and Systems I*, vol. 56, pp. 17–39, Jan. 2009.

[Chang-05] Y. P. Chang et al, "Design of discrete-value passive harmonic filters using sequential neural-network approximation and orthogonal array", in *IEEE PES Transmission and Distribution Conference & Exposition: Asia and Pacific*, Dalian, China, Aug. 2005, pp. 1-6.

[Chang-07] K. H. Chang, I. L. Markov, and V. Bertacco, "Automating post-silicon debugging and repair," *Proceedings of the 2007 international conference on Computer-aided design*, November 2007, pp. 91–98.

[Chavez-Hurtado-16] J. L. Chavez-Hurtado and J. E. Rayas-Sánchez, "Polynomial-based surrogate modeling of RF and microwave circuits in frequency domain exploiting the multinomial theorem," *IEEE Trans. Microwave Theory Techn*., vol. 64, no. 12, pp. 4371-4381, Dec. 2016.

[Chen-08] K. Chen, S. Malik, and P. Patra, "Runtime validation of memory ordering using constraint graph checking," *HPCA*, 2008, pp. 415–426.

[Cheng-00] J. Cheng and M. J. Druzdzel, "Computational investigation of low-discrepancy sequences in simulation algorithms for bayesian networks," in *Proc. of the Sixteenth Conf. on Uncertainty in Artificial Intelligence*, San Francisco, CA, 2000, pp. 72-81.

[Cheng-08] Q. S. Cheng, J. W. Bandler, S. Koziel, "Combining coarse and fine models for optimal design" *IEEE Microwave Magazine*, February 2008, pp 79-88.

[K.Cheng-10] K. Cheng and H. Chang, "Recent advances in analog, mixed-signal, and RF testing," Information and Media Technologies, vol. 5, no. 2, pp. 338–365, 2010.

[Y.Cheng-10] Y. S. Cheng, Y. C. Lai, and R. B. Wu, "Optimization of FIR filter to improve eye diagram for general transmission line systems," in *Design, Automation & Test in Europe Conference & Exhibition*, Dresden, Germany, April 2010, pp. 1321-1324.

[Cheng-11] Y. S. Cheng and R. B. Wu, "Direct eye diagram optimization for arbitrary transmission lines using FIR filter," *IEEE Trans. Components, Packaging and Manufacturing Technology*, vol. 1, no. 8, pp. 1250-1258, Aug. 2011.

[Chung-00] Y. S. Chung, C. Cheon, I. Park, and S. Hahn, "Optimal shape design of microwave device using FDTD and design sensitivity analysis," *IEEE Trans. Microwave Theory Tech*., vol. 48, pp. 2289–2296, Dec. 2000.

[Dally-97] W. J. Dally and J. Poulton, "Transmitter equalization for 4-Gbps signaling," *IEEE Micro*, vol. 17, pp. 48-56, Feb. 1997.

[DeOrio-13] A. DeOrio, Q. Li, M. Burgess, and V. Bertacco, "Machine learning-based anomaly detection for post-silicon bug diagnosis," in *Europe Conf. & Exhibition (DATE) in Design, Automation & Test, Grenoble*, France, March 2013.

[De Paula-08] F. M. De Paula, M. Gort, A. J. Hu, S. J. E. Wilton, and J. Yang, "Backspace: formal analysis for post-silicon debug," *Proceedings of the 2008 International Conference on Formal Methods in Computer-Aided Design*, November 2008, pp. 1–10.

[Devabhaktuni-01] V. K. Devabhaktuni, M. Yagoub, and Q. J. Zhang, "A robust algorithm for automatic development of neural-network models for microwave applications," *IEEE Trans. Microwave Theory Tech.*, vol. 49, no. 12, pp. 2282-2291, Dec. 2001.

[Deyati-14] S. Deyati, B. Muldrey, A. Banerjee, and A. Chatterjee, “Atomic model learning: A machine learning paradigm for post silicon debug of RF/analog circuits,” in *IEEE 32nd VLSI Test Symp. (VTS),* Napa, CA, April 2014.

[Dhanesh-17] M. A. Dhanesh and J. Mendoza-Bonilla, “Ethernet SFI Transmitter Optimization,” in *Intel 11th Joint Seminar on Signal and Power Integrity*, Santa Clara, CA, Jan. 30, 2017.

[Duron-Rosales-17] I. Duron-Rosales, F. Rangel-Patiño, J. E. Rayas-Sánchez, J. L. Chávez-Hurtado, and N. Hakim, “Reconfigurable FIR filter coefficient optimization in post-silicon validation to improve eye diagram for optical interconnects,” in *Int. Caribbean Conf. Devices, Circuits, and Systems (ICCDCS-2017)*, Cozumel, Mexico, Jun. 2017, pp. 1-4.

[Fan-09] Y. Fan and Z. Zilic, “Accelerating jitter tolerance qualification for high speed serial interfaces,” in *IEEE Int. Symp. Quality Electronic Design*, San Jose, CA, Mar. 2009, pp. 360-365.

[Farjad-Rad-99] R. Farjad-Rad, CK. K. Yang, M. Horowitz and T. H. Lee, “A 0.3 µm CMOS 8-Gb/s 4-PAM serial link transceiver,” in *VLSI Circuits Symposium*, Kyoto, Japan, Jun 1999, pp. 41-44.

[Fiedler-97] A. Fiedler, R. Mactaggart, J. Welch and S. Krishnan, “A 1.0625 Gbps transceiver with 2x-oversampling and transmit signal pre-emphasis,” in *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA., Feb 1997, pp. 238-239.

[Foley-01] D. J. Foley and M.P. Flynn, “A low-power 8-PAM serial transceiver in 0.5-µm digital CMOS,” in *IEEE Conference on Custom Integrated Circuits*, San Diego, CA, May 2001, pp. 123-126.

[Forrester-08] A. Forrester, A. Sobester and A. Keane, *Engineering Design Via Surrogate Modelling: A Practical Guide*. Hoboken, NJ: Wiley, 2008.

[Friedman-01] J. Friedman, T. Hastie, and R. Tibshirani, “The elements of statistical learning”, Springer Series in Statistics, 2001, vol. 1.

[Fu-14] M. C. Fu, *Handbook of Simulation Optimization.* vol. 216. New York, NY: Springer, 2014.

[Gambill-08] K. Gambill, “System margin validation,” December 2008. [Online].Available: http://download.intel.com/design/intarch/papers/321078.pdf

[Gatto17] A. Gatto, P. Parolari, M. Brunero, F. Corapi, V. Costa, C. Meani, and P. Boffi, “Intra-datacenter links exploiting PCI express generation 4 interconnections,” in *Optical Fiber Communications Conference and Exhibition (OFC)*, Los Angeles, CA, March 2017, pp. 1-3.

[Gillis-98] P. Gillis, F. Woytowich, K. McCauley, and U. Baur, “Delay test of chip I/Os using LSSD boundary scan,” in *Proc. Int. Test Conf.*, Washington, DC, October 1998, pp. 83–90.

[Gizopoulos-06] D. Gizopoulos, *Advances in Electronics Testing – Challenges and Methodologies*. Netherlands: Springer, 2006.

[Gonzales-15] D. Gonzales, “PCI express 4.0 electrical previews,” *PCI-SIG Developers Conference*, Tel Aviv, Israel, March 2015.

[Goodenough-10] J. Goodenough, R. Aitken, “Post-silicon is too late avoiding the $50 million paperweight atarts with validated Designs”, *Design Automation Conference (DAC)*, 2010 47th ACM/IEEE, pp. 8–11.

[Goulermas-07] J. Y. Goulermas, P. Liatsis, Z. Xiao-Jun, and P. Cook, "Density-driven generalized regression neural networks (DD-GRNN) for function approximation," *IEEE Trans. Neural Netw.*, vol. 18, no. 6, pp. 1683-1696, Nov. 2007.

[Goupil-10] A. Goupil and J. Palicot, “An efficient blind decision feedback equalizer,” *IEEE Commun. Lett*, vol. 14, pp. 462-464, May 2010.

[Goay-17] C. H. Goay and P. Goh, “Neural networks for eye height and eye width prediction with an improved adaptive sampling algorithm,” in *Asian Simulation Conf. (AsiaSim),* Melaka, Malaysia, Aug. 2017.

[Gray-08] R. Gray, “Post-silicon validation experience: history, trends, and challenges”, *GSRC Workshop on Post-Si Validation*, Anaheim, June 9, 2008.

[Graham-53] R. S. Graham, “Relay computer for network analysis,” *Bell Labs. Rec.*, vol. 31. pp. 152-157. Apr. 1953.

[Gu-12] C. Gu, “Challenges in post-Silicon validation of high-speed I/O links,” in *Proc. Intl. Conf. on Computer-Aided Design (ICCAD), IEEE/ACM*, San Jose, CA, Nov. 2012, pp. 547-550.

[Guo-08] W.-D. Guo, F.-N. Tsai, G.-H. Shiue, and R.-B. Wu, “Reflection enhanced compensation of lossy traces for best eye-diagram improvement using high-impedance mismatch,” *IEEE Trans. Adv. Packag.*, vol. 31, no. 3, pp. 619-626, Aug. 2008.

[Hall-00] S. H. Hall, G. Hall, and J. A. McCall, *High-Speed Digital System Design:A Handbook of Interconnect Theory and Design Practice*, Hoboken NJ: Wiley 2000.

[Ham-04] B. Ham, “Methodologies for Jitter and Signal Quality Specification,” *Tech. Report T11.2 / Project 1316-DT/ Rev 12.2*, INCITS, Washington, DC, Jan. 2004.

[Haykin-99] S. Haykin, *Neural Networks: A Comprehensive Foundation*. New Jersey, MA: Prentice Hall, 1999.

[Heath-04] M. W. Heath, W. P. Burleson and I.G. Harris, “Synchro-tokens: eliminating nondeterminism to enable chip-level test of globally-asynchronous locally-synchronous SoC’s,” *Proc. Design, Automation and Test in Europe*, pp. 1532-1546, 2004.

[Hermans-06] C. Hermans and M. S. J. Steyaert, “A high-speed 850-nm optical receiver front-end in 0.18-/spl mu/m CMOS,” *IEEE J. Solid-State Circuits*, vol. 41, pp. 1606-1614, Jul. 2006.

[Higashi-05] H. Higashi, S. Masaki, M. Kibune, S. Matsubara, T. Chiba, Y. Doi, H. Yamaguchi, H. Takauchi, H. Ishida, K. Gotoh, and H. Tamura, “A 5-6.4-Gb/s 12-channel transceiver with pre-emphasis and equalization,” *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 978-985, Apr. 2005.

[Hodgkiss-83] W. Hodgkiss and L. F. Turner. “Practical equalization and synchronization strategies for use in serial data transmission over H.F. channels,” *Radio and Electronic Engineer*, vol. 53, no. 4, pp. 141-145, Apr. 1983.

[Hong-08] D. Hong, K.T. Cheng, “Bit-error rate estimation for bang-bang clock and data recovery circuit,” in *26th IEEE VLSI Test Symp.*, San Diego, CA, April, 2008, pp. 17 – 22.

[Hooke-61] R. Hooke, and T. A. Jeeves, “Direct search solution of numerical and statistical problems,” *Journal of the Association for Computing Machinery*, vol. 8, no. 2, pp. 212-229, April 1961.

[Hornik-89] K. Hornik, M. Stinchcombe, and H. White, "Multilayer feedforward networks are universal approximators," *Neural Networks*, vol. 2, no. 5, pp. 359-366, May 1989.

[J.Huang-01] J.-L. Huang and K.-T. Cheng, "An on-chip short-time interval measurement technique for testing high-speed communication links," in *Proc. VLSI Test Symp*., Marina Del Rey, CA, April 2001, pp. 380–385.

[H.Huang-01] H. Huang and E. K. F. Lee, "Design of low-voltage CMOS continuous time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1168-1177, Aug. 2001.

[IEEE-03] *IEEE Std. 1149.6-2003, IEEE Standard for Boundary Scan Testing of Advanced Digital Networks*, IEEE Press, New York, 2003.

[IEEE-15] *IEEE Standard for Ethernet*. IEEE Standard 802.3-2015.

[INTEL-03] Intel Corp., "Intel platform and component validation - a commitment to quality, reliability and compatibility", White Paper, Intel Corporation, 2003.

[Iyer-06] P. Iyer, S. Jain, B. Casper, and J. Howard, "Testing high-speed IO links using on-die circuitry," in 19th *International Conference on VLSI Design,* Hyderabad, India, Jan. 2006.

[Jones-98] D. R. Jones, M. Schonlau, and W. J. Welch, "Efficient global optimization of expensive black-box functions," *Journal of Global Optimization*, vol. 13, pp. 455–492, June 1998.

[Josephson-01] D. Josephson, S. Poehlman and V. Govan, "Debug methodology for the McKinley processor," *Proc. Intl. Test Conf*., pp. 451-460, 2001.

[Josephson-06] D. Josephson, "The good, the bad, and the ugly of silicon debug," *Proc. Design Automation Conf*., pp. 3-6, 2006.

[Keshava-09] J. Keshava, "Post-silicon validation challenges", *International Test Conference 2009*, ITC'09, Nov. 1, 2009.

[Keshava-10] J. Keshava, N. Hakim, C. Prudvi, "Post-silicon validation challenges: How EDA and academia can help," *Design Automation Conference (DAC), 47th ACM/IEEE*, June 2010, pp. 3 –7.

[Kossel-04] M. Kossel and M. Schmatz, "Jitter Measurements of High-Speed Serial Links," *IEEE Design & Test of Computers*, vol. 21, no. 6, pp. 536–543, Nov.-Dec. 2004.

[Koziel-08] S. Koziel, Q. S. Cheng, J. W. Bandler, "Space Mapping", *IEEE Microwave Magazine*, December 2008, pp 105-122.

[Koziel-11] S. Koziel, and X. S. Yang, *Computational Optimization, Methods and Algorithms.* Heidelberg, Germany: Springer, 2011.

[Krall-08] C. Krall, K. Witrisal, G. Leus and H. Koeppl, "Minimum mean square error equalization for second order Volterra systems," *IEEE Trans. Signal Process*, vol. 56, pp. 4729-4737, Jul. 2008.

[Kumar] LOGIC FRUIT. S. Kumar, and P. Agarwal, *PCI Express 3.0 Equalization: The Mystery Unsolved*, [Online]. White Paper, Logic Fruit Technologies. Available: http://www.logic-fruit.com.

[Kumm-13] M. Kumm, K. Möller, P. Zipf, "Reconfigurable FIR Filter Using Distributed Arithmetic on FPGAs," in *IEEE Int. Symp. Circuits and Systems (ISCAS)*, Kuala Lumpur, Malaysia, May 2013.

[Kwok-97] T. Y. Kwok and D. Y. Yeung, "Constructive algorithms for structure learning in feedforward neural networks for regression problems," *IEEE Trans. Neural Networks*, vol. 8, no. 3, pp. 630-645, May 1997.

[Lagarias-98] J. C. Lagarias, J. A. Reeds, M. H. Wright, and P. E. Wright, "Convergence properties of the Nelder-Mead simplex method in low dimensions," *Society for Industrial and Applied Mathematics J. Optim.,* vol. 9, no. 1, pp. 112–147, 1998.

[Laquai-01] B. Laquai and Y. Cai, "Testing gigabit multilane SerDes interfaces with passive jitter injection filters," in *Proc. Int. Test Conf.*, Baltimore, MD, October 2001, pp. 297–304.

[Le-02] M. Q. Le, P. J. Hurst and J. P. Keane, "An adaptive analog noise-predictive decision-feedback equalizer," *IEEE J. Solid-State Circuits*, vol. 37, pp. 105-113, Feb 2002.

[Lee-98] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits,* Cambridge, UK: Cambridge University Press, 1998.

[Lee-11] B. T. Lee, M. Mazumder, and R. Mellitz, "High speed differential I/O overview and design challenges on Intel enterprise server platforms," in *IEEE Int. Symp. on Electromagnetic Compatibility*, Long Beach, CA, Aug. 2011, pp. 779-784.

[M.Li-07] M. Li, *Jitter, Noise, and Signal Integrity at High-Speed*, Boston, MA: Prentice Hall, 2007.

[X.Li-07] X. Li, B. Taylor, Y. Chien, et al., "Adaptive post-silicon tuning for analog circuits: concept, analysis and optimization," in *IEEE/ACM Int. Conf. Computer-Aided Design (ICCAD)*, San Jose, CA, Dec. 2007.

[Li-09] M. Li, "Jitter Challenges and Reduction Techniques at 10 Gb/s and Beyond," *IEEE Trans. on Advanced Packaging*, vol. 32, no. 2, pp. 290–297, May 2009.

[Li-13] X. Li, F. Wang, S. Su, et al. "Bayesian model fusion: a statistical framework for efficient pre-silicon validation and post-silicon tuning of complex analog and mixed-signal circuits," in *IEEE/ACM Int. Conf. Computer-Aided Design (ICCAD)*, San Jose, CA, Dec. 2013.

[Lin-05] M. Lin, K.-T. Cheng, J. Su, M. C. Sun, J. Chen, and S. Lu, "Production-oriented interface testing for PCI express by enhanced loopback technique," in *Proc. Int. Test Conf.*, Austin, TX, November 2005, Paper 27.3.

[Liu-04] J. Liu and X. Lin, "Equalization in high-speed communication systems," *IEEE Circuits and Systems Magazine*, vol. 4, no. 2, pp. 4-17, Sep. 2004.

[Liu-15] M. Liu and J. H. Tsai, "USB3.1 silicon and channel design optimization using artificial neural network modeling", in *IEEE Electromagnetic Compatibility and Signal Integrity Symp.*, Santa Clara, CA, May. 2015.

[Lopez-Miralrio-13] E. Lopez Miralrio, C. Mendez Ruiz, T. Lin, J. Sytwu, J. Hsu, T. Su, C. Ye, and X. Ye, "Signal integrity design of via with extra routing stub for device routing flexibility," in *Proc. IEEE Electrical Design of Advanced Packaging & Systems Symposium*, Nara, Japan, Dec. 2013, pp. 189-192.

[Lophaven-02] S. N. Lophaven, H. B. Nielsen, J. Søndergaard, "Aspects of the Matlab toolbox DACE," Internal Report *IMM-TR-2002-13*, Technical University of Denmark, Lyngby, 2002.

[Mack-07] Y. Mack, T. Goel, W. Shyy, R. Haftka, "Surrogate model-based optimization framework: a case study in aerospace design," in *Evolutionary Computation in Dynamic and Uncertain Environments. Studies in Computational Intelligence*, S. Yang, YS. Ong, Y. Jin, Ed., Berlin: Springer, 2007, vol. 51, pp. 323-342.

[MacKay-92] D. J. C. MacKay, "Bayesian interpolation," *Neural Computation*, vol. 4, no. 3, pp. 415-447, May 1992

[Makand-05] T. M. Makand, M. J. Tripp, "Device testing," U.S. Patent No. 6,885,209, April 26, 2005.

[Matheron-63] G. Matheron, "Principles of geostatistics," *Economic Geology*, vol. 58, no. 8, pp. 1246-1266, Dec. 1963.

[Maxim-04] Maxim (2004), *Physical Layer Performance: Testing the Bit Error Ratio (BER)* [Online]. Available: www.maximintegrated.com

[Mendez-Ruiz-13] C. Mendez Ruiz, C. Ye, X. Ye, E. Lopez Miralrio, M. Yin, J. Hsu, and T. Su "Improve signal integrity performance by using hybrid PCB stackup," in *Proc. IEEE International Symposium on Electromagnetic Compability*, Denver, CO, Aug. 2013, pp. 317-321.

[Miller-03] G. Miller, M. Timko, H.-S.Lee, E. Nestler, M. Mueck, and P. Ferguson, "Design and modeling of a 16-bit 1.5msps successive approximation adc with non-binary capacitor array," in *Proc. Int. Great Lakes Symp. on VLSI*, Washington, D. C, April 2003, pp. 161 - 164

[Mitra-10] S. Mitra, S. A. Seshia, N. Nicolici, "Post-silicon validation opportunities, challenges and recent advances" *Design Automation Conference (DAC)*, 2010 47th ACM/IEEE, pp. 12–17.

[Moore-65] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, April 19, 1965.

[Morris-93] M. D. Morris, T. J. Mitchell and D. Ylvisaker, "Bayesian design and analysis of computer experiments: use of derivatives in surface prediction," *Technometrics*, vol. 35, no. 3, pp. 243–255, Aug. 1993.

[Nejedlo-03] J. J. Nejedlo, "IBIST (interconnect built-in-self-test) architecture and methodology for PCI express," in *Proc. Int. Test Conf.*, pp. 114–122, October 2003.

[Panganiban-02] J. Panganiban, "A ring oscillator based variation test chip," Ph.D. dissertation, Massachusetts Institute of Technology, 2002.

[Patra-07] P. Patra, "On the cusp of a validation wall," *IEEE Design and. Test of Computers*, Vol.24, No.2, pp.193-196, March-April 2007.

[Perrott-02] M. Perrott, M. Trott, and C. Sodini, "A modeling approach for Σ-Δ fractional-N frequency synthesizers allowing straightforward noise analysis," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1028–1038, Aug. 2002.

[PCISIG-11] PCI SIG Org. (2011), *PCIE Express 3.0 Electrical* [Online]. Available: https://pcisig.com/events/training-events-resources

[PCISIG-12] PCI SIG Org. (2012), *Designing to the New PCI Express 3.0 Equalization Requirements* [Online]. Available: https://pcisig.com/specifications.

[PCISIG-16] PCI SIG Org. (2016), *Peripheral Component Interconnect Express 3.1 Specification* [Online]. Available: https://pcisig.com/specifications.

[PCISIG-17] PCI SIG Org. (2017), *PCI Express® Base Specification Revision 4.0 Version 1.0* [Online]. Available: https://pcisig.com/specifications.

[Plouchart-14] J. Plouchart, F. Wang, X. Li, et al., "Adaptive circuit design methodology and test applied to millimeter-wave circuits," *IEEE Design & Test*, vol. 31, no. 6, pp. 8-18, July 2014.

[Pridhiviraj-15] P. Pridhiviraj, T. Dheerendra, and P. Muralidhar, "Adaptive post-silicon server validation using machine learning," *Int. J. Applied Information Systems (IJAIS),* vol. 9, no. 1, pp. 24-32, June 2015.

[Queipo-05] N. V. Queipo, R. T. Haftka, W. Shyy, T. Goel, R. Vaidynathan and P. K. Tucker, "Surrogate-based analysis and optimization," *Progress in Aerospace Sciences*, vol. 41, no. 1, pp. 1-28, Jan. 2005.

[Rahmani-17] K. Rahmani, S. Ray, and P. Mishra, "Postsilicon trace signal selection using machine learning techniques," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 2, pp. 570-580, Aug. 2017.

[Rangel-Patiño-16] F. Rangel-Patino, A. Viveros-Wacher, J. E. Rayas-Sánchez, E. A. Vega-Ochoa, I. Duron-Rosales, and N. Hakim, "A holistic methodology for system margining and jitter tolerance optimization in post-silicon validation," in *IEEE MTT-S Latin America Microwave Conf. (LAMC-2016)*, Puerto Vallarta, Mexico, Dec. 2016, pp. 1-4.

[Rangel-Patiño-17a] F. E. Rangel-Patiño, J. L. Chávez-Hurtado, A. Viveros-Wacher, J. E. Rayas-Sánchez, and N. Hakim, "System margining surrogate-based optimization in post-silicon validation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 9, pp. 3109-3115, May 2017.

[Rangel-Patiño-17b] F. E. Rangel-Patiño, A. Viveros-Wacher, J. E. Rayas-Sánchez, I. Durón-Rosales, E. A. Vega-Ochoa, N. Hakim and E. López-Miralrio, "A holistic formulation for system margining and jitter tolerance optimization in industrial post-silicon validation," *IEEE Trans. Emerging Topics Computing*, vol. **, no. **, pp. **, *** 2017. (published online: 29 Sep. 2017; DOI: 10.1109/TETC.2017.2757937).

[Rangel-Patiño-17c] F. Rangel-Patino, J. L. Chávez-Hurtado, A. Viveros-Wacher, J. E. Rayas-Sánchez, and N. Hakim, "Eye diagram system margining surrogate-based optimization in a server silicon validation platform," in *European Microw. Conf. (EuMC-2017)*, Nuremberg, Germany, Oct. 2017, pp. 540-543.

[Rangel-Patiño-18a] F. E. Rangel-Patiño, J. E. Rayas-Sánchez, E. A. Vega-Ochoa A, and N. Hakim, "Direct optimization of a PCI express link equalization in industrial post-silicon validation," in *IEEE LATS-S Latin American Test Symposium. (LATS-2018)*, Sao Paulo, Brasil, March. 2018.

[Rangel-Patiño-18b] F. E. Rangel-Patiño, J. E. Rayas-Sánchez, A. Viveros-Wacher, J. L. Chávez-Hurtado, E. A. Vega-Ochoa, and N. Hakim, "Post-silicon receiver equalization metamodeling by artificial neural networks," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. **, pp. **, *** 2018. (published online: 8 May 2018; DOI: 10.1109/TCAD.2018.2834403; regular publication pending).

[Rangel-Patiño-18c] F. E. Rangel-Patiño, J. E. Rayas-Sánchez, A. Viveros-Wacher, E. A. Vega-Ochoa, and N. Hakim, "High-speed links receiver optimization in post-silicon validation exploiting Broyden-based input space mapping," in *IEEE MTT-S Int. Conf. Num. EM Mutiphysics*

Modeling Opt. RF, Microw., Terahertz App. (NEMO-2018), Reykjavik, Iceland, Aug. 2018, pp. 1-3. (work accepted, to be published).

[Rayas-Sánchez-01] J. E. Rayas-Sánchez, *Neural Space Mapping Methods for Modeling and Design of Microwave Circuits*, Ph.D. Thesis, Dept. of Electrical and Comp. Eng., McMaster University, Hamilton, Canada, 2001.

[Rayas-Sánchez-04] J. E. Rayas-Sánchez, "EM-based optimization of microwave circuits using artificial neural networks: the state of the art," *IEEE Trans. Microwave Theory Techn.,* vol. 52, no. 1, pp. 420-435, Jan. 2004.

[Rayas-Sánchez-06] J. E. Rayas-Sánchez and V. Gutiérrez-Ayala, "EM-based Monte Carlo analysis and yield prediction of microwave circuits using linear-input neural-output space mapping," *IEEE Trans. Microwave Theory Tech.*, vol. 54, no. 12, pp. 4528-4537, Dec. 2006.

[Rayas-Sánchez-11] J. E. Rayas-Sánchez. (2011). *An Introduction to Space Mapping*. Lecture of the graduate course "Optimization-Based Modeling and Design of Electronic Circuits". Dept. of Electronics, Systems and Informatics, ITESO – The Jesuit U. of Guadalajara, Tlaquepaque, Mexico, 2011. Available:

https://desi.iteso.mx/erayas/documents/CirOpt_course/Lectures/Space_Mapping/SM_intro.pdf.

[Rayas-Sánchez-15] J. E. Rayas-Sánchez. (2015). *A Brief Introduction to Artificial Neural Networks*. Circuit Optimization Lecture. Dept. of Electronics, Systems and Informatics, ITESO, Tlaquepaque, Mexico, 2015. Available: https://desi.iteso.mx/erayas/cir_opt.htm.

[Rayas-Sánchez-16] J. E. Rayas-Sánchez, "Power in simplicity with ASM: tracing the aggressive space mapping algorithm over two decades of development and engineering applications," *IEEE Microwave Magazine*, vol. 17, no. 4, pp. 64-76, Apr. 2016.

[Rayas-Sánchez-17] J. E. Rayas-Sánchez, J. L. Chavez-Hurtado, and Z. Brito-Brito, "Design optimization of full-wave EM models by low-order low-dimension polynomial surrogate functionals," *Int. J. Numerical Modelling: Electron. Networks, Dev. Fields*., vol. 30, no. 3-4, e2094, May-Aug. 2017.

[Reddy-15] K. S. Reddy, S. K. Sahoo, "An approach for FIR filter coefficient optimization using differential evolution," in *Int. J. Electron. Commun. (AEÜ)*, 2015, vol. 65, no. 1, pp. 101–108.

[Ren-15] Y. Ren, Y. W. Kim, anH. Y. Kim, "Implementation of system interconnection devices using PCI express," in *IEEE International Conference on Consumer Electronics (ICCE),* Las Vegas, NV, Jan. 2015, pp. 281-282.

[Robertson-05] I. Robertson, G. Hetherington, T. Leslie, I. Parulkar, and R. Lesnikoski, "Testing high-speed, large scale implementation of SerDes I/Os on chips used in throughput computing systems," in *Proc. Int. Test Conf.*, Austin, TX, November 2005, Paper 38.1.

[Rotithor-00] H. Rotithor, "Postsilicon validation methodology for microprocessors", *IEEE Design & Test of Computers*, vol. 17 , Issue 4, 2000, pp. 77–88.

[Sacks-89] J. Sacks, W. J. Welch, T. J. Mitchell, and H. P. Wynn, "Design and analysis of computer experiments," *Statistical Science*, vol. 4, pp. 409-435, Nov. 1989.

[Santner-03] T. J. Santner, B. J. Williams and W. I. Notz, *The design and analysis of computer experiments*. New York, NY: Springer, 2003.

[Sarangi-06] S. Sarangi, B. Greskamp and J. Torrellas, "CADRE: Cycle-accurate deterministic replay for hardware debugging," *Proc. Dependable Systems and Networks*, pp. 301-312, 2006.

[SATAOrg-16] SATA Org. (2016), *Serial Advanced Technology Attachment 3.2 Specification* [Online]. Available: http://www.sata-io.org/

[SciPy-17] SciPy.org, PCI SIG Org. (2017), *Open-source Software for Mathematics, Science, and Engineering* [Online]. Available: https://docs.scipy.org/doc/scipy/reference/index.html.

[Shkolnitsky-10] L. Shkolnitsky and E. Einy, "Electrical system-validation methodology for embedded display port," White Paper, Intel Corporation, June 2010.

[Silas-03] I. Silas, I. Frumkin, E. Hazan, E. Mor and G. Zobin, "System-level validation of the Intel Pentium M processor," *Intel Technology Journal*, Vol. 7, No.2., pp. 37-43, May 2003.

[Silva-11] P. H. F. Silva, R. M. S Cruz, and A G. D'Assunção, "Neuromodeling and natural optimization of nonlinear devices and circuits," in *System and Circuit Design for Biologically-Inspired Intelligent Learning*, T. Temel, Ed. Hershey PA: IGI Global, 2011, ch. 15, pp. 326-348.

[Snel-01] J. Snel, "Space mapping models for RF components," *IEEE MTT-S Statistical Design Modeling Tech. for Microwave CAD Workshop*, 2001.

[Sobol-67] I. M. Sobol, "On the distribution of points in a cube and the approximate evaluation of integrals," *U.S.S.R. Computational Mathematics and Mathematical Physics*, vol. 7, no. 4, pp. 86-112, 1967.

[Sohn-03] Y. Sohn, S. Bae, H. Park, C. Kim and S. Cho, "A 2.2 Gbps CMOS look-ahead DFE receiver for multidrop channel with pin-to-pin time skew compensation," in *Proceedings of IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2003, pp. 473-476.

[Stauffer-08] D. R. Stauffer, J. T. Mechler, M. Sorna, K. Dramstad, C. R. Ogilvie, A. Mohammad, and J. Rockrohr, *High Speed SERDES Devices and Applications*, New York, NY: Springer, 2008.

[Staum-09] J. Staum, "Better simulation metamodeling: The why, what, and how of stochastic kriging," in *Proc. of the Winter Simulation Conf.*, Austin, TX, Dec. 2009, pp. 119-133.

[Stojanovic-04] V. Stojanovic and M. Horowitz, Stanford University Lecture, *Modeling and Analysis of High-Speed Links* [Online]. Available:

http://www.rle.mit.edu/isg/documents/Stojanovic_CICC03.pdf

[Suzuki-11] K. Suzuki, *Artificial Networks-Methodological Advances and Biomedical Applications.* Croatia, InTech, 2011.

[Tao-14] J. Tao, Y. Wang, M. Jun, et al., "Toward efficient programming of reconfigurable radio frequency (RF) receivers," in *19th Asia and South Pacific Design Automation Conf. (ASP-DAC)*, Singapore, Singapore, Feb. 2014.

[Tasiran-01] S. Tasiran and K. Keutzer, "Coverage metrics for functional validation of hardware designs", *IEEE Design & Test of Computers*, 18(7):36--45, Jul/Aug 2001.

[TEKTRONIX-14] TEKTRONIX. (2014). *Equalization and Serial Data Link Analysis Methods (SDLA) with 80SJNB Advanced* [Online]. Available: http://www.tek.com/document/application-note/equalization-and-serial-data-link-analysis-methods-sdla-80sjnb-advanced--0.

[Thimm-97] G. Thimm, and E. Fiesler, "High-order and multilayer perceptron initialization," *IEEE Trans. Neural Networks*, vol. 8, no. 2, pp. 349-359, Aug. 1997.

[Tiruvallur-09] K. Tiruvallur, "Beyond design challenges of IA platform productization", *International Conference on Computer-Aided Design*, Nov. 2009.

[Tripp-04] M. Tripp, T. M. Mak, and A. Meixner, "Elimination of traditional functional testing of interface timings at Intel", in *Proc. Int. Test Conf.*, pp. 1448–1454, October 2004.

[Ureel-96] J. Ureel and D. De Zutter, "A new method for obtaining the shape sensitivities of planar microstrip structures by a full-wave analysis," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 249–260, Feb. 1996.

[USBOrg-16] USB Org. (2016). *Universal Serial Bus Revision 3.1 Specification* [Online]. Available: http://www.usb.org/developers/doc

[Vicario-16] G. Vicario, G. Craparotta, and G. Pistone, "Meta-models in computer experiments: Kriging versus artificial neural network," *Qual. Reliab. Engng. Int.*, vol. 32, no. 6, pp. 2055-2065, June 2016.

[Villiers-92] J. de Villiers, and E. Barnard, "Backpropagation neural nets with one and two hidden layers," *IEEE Trans. Neural Networks*, vol. 4, no. 1, pp. 136-141, Jan. 1992.

[Viveros-Wacher-14] A. Viveros-Wacher, R. Alejos, L. Alvarez, I. Diaz-Castro, B. Marcial, G. Motola-Acuna, and E. A. Vega-Ochoa, "SMV methodology enhancements for high speed IO links of SoCs," in *IEEE VLSI Test Symp. (VTS-2014)*, Napa, CA, May. 2014, pp. 1-5.

[Wagner-08] I. Wagner and V. Bertacco, "Reversi: Post-silicon validation system for modern microprocessors," *ICCD*, 2008, pp. 307–314.

[Wang-03] Z. Wang, J. Zhu, "Transistor-Level Static Timing Analysis by Piecewise Quadratic Waveform Matching," in *Design, Automation and Test in Europe Conference and Exhibition*, Washington, DC, March 2003, pp 1026–1031.

[Wang-06] G. Wang and S. Shan, "Review of metamodeling techniques in support of engineering design optimization," *Journal of Mechanical Design*, vol. 129, no. 4, pp. 370–380, May 2006.

[Wang-08] L. T. Wang, C. E. Stroud, and N. A. Touba, *System-on-Chip Test Architectures: Nanometer Design for Testability*. Burlington, MA: Elsevier, 2008.

[Wang-15] X. Wang and Q. Hu, "Analysis and optimization of combined equalizer for high speed serial link," in *IEEE 9th Int. Conf. Anti-counterfeiting, Security, and Identification (ASID)*, Xiamen, China, Sept. 2015, pp. 43-46.

[Wang-16] F. Wang, P. Cachecho, W. Zhang, S. Sun, X. Li, R. Kanj, and C. Gu, "Bayesian model fusion: large-scale performance modeling of analog and mixed-signal circuits by reusing early-stage data," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 35, no. 8, pp. 1255-1268, Aug. 2016.

[Weisstein-17] E. W. Weisstein (MathWorld 2017), *Star Discrepancy* [Online]. Available: http://mathworld.wolfram.com/StarDiscrepancy.html

[Wile-05] B. Wile, J. C. Goss, and W. Roesner, *Comprehensive functional verification - The complete industry cycle*. San Francisco, CA: Morgan Kaufmann, 2005.

[Wilen-03] A. Wilen, J. Shade, and R. Thornburg, *Introduction to PCI Express: A Hardware and Software Developer's Guide*. Hillsboro, OR: Intel Press, 2003.

[Wu-00] C. F. J. Wu and M. Hamada, *Experiments: Planning, Analysis, and Parameter Design Optimization*, New York, NY: Wiley, 2000.

[Xiao-12] X. Ye, K. Xiao, and R. Enriquez "Differential far-end crosstalk cancellation – implementations and challenges," in *Proc. IEEE International Symposium on Electromagnetic Compability*, Pittsburgh, PA, Aug. 2012, pp. 193-198.

[Yao-09] W. Yao, Y. Shi, L. He, S. Pamarti, "Joint Design-Time and Post-Silicon Optimization for Digitally Tuned Analog Circuits," in *2009 IEEE/ACM Int. Conf. on Computer-Aided Design*, San Jose, CA, Nov. 2009, pp. 725-730.

[Ye-11] C. Ye, X. Ye, E. Vargas, and O. Argueta "Full link impedance optimization for serial IOs," in *Proc. IEEE International Symposium on Electromagnetic Compability*, Long Beach, CA, Aug. 2011, pp. 803-808.

[Yerramilli-06] S. Yerramilli, "Addressing post-silicon validation challenge: Leverage validation and test synergy," Keynote, Intl. Test Conf., 2006.

[Yuan-14] F. Yuan, A. R. Al-Taee, A. Ye, A., and S. Sadr, "Design techniques for decision feedback equalization of multi-giga-bit-per-second serial data links: a state-of-the-art review," *IET Circuits, Devices & Systems*, vol. 8, no. 2, pp. 118-130, Mar. 2014.

[Zhang-00] Q. J. Zhang and K. C. Gupta, *Neural Networks for RF and Microwave Design*. Norwood, MA: Artech House, 2000.

[Zhang-03] Q. J. Zhang, K. C. Gupta, and V. K. Devabhaktuni, "Artificial neural networks for RF and microwave design - from theory to practice," *IEEE Trans. Microw. Theory Tech*., vol. 51, no. 4, pp. 1339-1350, Apr. 2003.

[Zhang-15] H. Zhang, S. Krooswyk and J. Ou, *High Speed Digital Design: Design of High Speed Interconnects and Signaling*. Waltham, MA: Elsevier, 2015.

[Zerbe-01] J. Zerbe, P. Chau, C. Werner, W. Stonecypher, H. Liaw, G. Yeh, T. Thrush, S. Best and K. Donnelly, "A 2 Gb/s/pin 4-PAM parallel bus interface with transmit crosstalk cancellation, equalization, and integrating receivers," in *IEEE International Solid-State Circuits Conference (ISSCC)*, San Diego, CA., Feb 2001, pp. 66-67.

[Zerbe-03] J. Zerbe, C. Werner, V. Stojanovic, F. Chen, J. Wei, G. Tsang, D. Kim, W. Stonecypher, A. Ho, T. Thrush, R. Kollipara, M. Horowitz and K. Donnelly, "Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplane transceiver cell," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2121-2130, Dec. 2003.

[10GEA-16] 10GEA Org. (2016), *XAUI interface* [Online]. Available: http://www.10gea.org/whitepapers/xaui-interface/

Author Index

10GEA 55, 157
Aaron 1, 145
Abeysekera 32, 145
Abramovici 10, 145
Adir 9, 145
Agilent 55, 57, 145
Alessandri 1, 145
ALTERA 23, 87, 145
ANRITSU 75, 145
Atef 32, 145
Bala 31, 145
Balamurugan 20, 145
Bandler 1, 21, 100, 102, 118, 146, 147, 150
Bentley 11, 15, 146
Bertsekas 103, 146
Beyene 105, 146
Bishop 20, 21, 146
Bistola 105, 146
Bojan 15, 146
Caffee 36, 146
Cai 40, 146, 151
Casper 55, 86, 145, 146, 147, 150
Chang 10, 112, 147
Chavez-Hurtado 102, 147, 154
Chen 10, 146, 147, 151, 157
Cheng 21, 52, 63, 65, 77, 117, 146, 147, 149, 150, 151
Chung 1, 147
Dally 26, 147
De Paula 10, 147

DeOrio 101, 102, 147
Devabhaktuni 107, 147, 157
Deyati 102, 148
Dhanesh 77, 148
Duron-Rosales 77, 88, 99, 100, 148, 153
Fan 52, 55, 148
Farjad-Rad 26, 148
Fiedler 26, 148
Foley 26, 148
Forrester 65, 148
Friedman 20, 148
Gambill 12, 148
Gatto17 .... 86, 148
Gillis 39, 148
Goay 105, 149
Gonzales 86, 148
Goodenough 14, 148
Goulermas 105, 149
Goupil 31, 149
Graham 1, 149
Gray 12, 15, 146, 149
Gu 4, 9, 13, 16, 18, 20, 149, 156
Guo 76, 149
H.Huang 18, 100, 150
Hall 75, 149, 151
Ham 55, 149
Haykin 105, 109, 149
Heath 17, 149
Hermans 31, 149
Higashi 76, 149
Hodgkiss 52, 149
Hong 55, 149
Hooke 95, 149

Iyer 92, 150
J.Huang 40, 150
Jones 65, 150
Josephson 11, 18, 150
K.Cheng 20, 147
Keshava 4, 8, 11, 12, 19, 51, 150
Kossel 57, 150
Koziel 1, 21, 63, 118, 147, 150
Krall 32, 150
Kumar 90, 150
Kumm 76, 77, 151
Kwok 107, 151
Lagarias 81, 95, 151
Laquai 40, 146, 151
Le 31, 151
Lee 30, 52, 148, 150, 151, 152
Li 55, 102, 117, 147, 151, 153, 156
Lin 40, 151
Liu 52, 105, 145, 151
Lopez-Miralrio 69, 151
Lophaven 62, 66, 152
M.Li 23, 55, 86, 151
Mack 105, 152
MacKay 110, 152
Makand 40, 152
Matheron 65, 152
Maxim 57, 152
Mendez-Ruiz 69
Miller 18, 100, 145, 152
Mitra 10, 152
Moore 2, 35, 152
Morris 65, 152
Panganiban 20, 152

Patra 8, 10, 15, 147, 152
PCISIG 55, 69, 85, 86, 90, 91, 110, 152, 153
Perrott 55, 152
Plouchart 102, 117, 153
Pridhiviraj 102, 153
Queipo 66, 67, 120, 153
Rahmani 101, 153
Rangel-Patiño ... 4, 18, 23, 24, 26, 36, 37, 42, 44, 52, 54, 76, 86, 87, 88, 89, 92, 95, 100, 102, 111, 117, 118, 119, 120, 121, 139, 140, 141, 143, 153
Rayas-Sánchez ...... xi, 100, 102, 104, 105, 106, 107, 109, 110, 118, 119, 121, 123, 139, 140, 141, 147, 148, 153, 154
Reddy 76, 77, 154
Ren 86, 154
Robertson 40, 41, 154
Rotithor 9, 154
Sacks 62, 65, 66, 67, 154
Santner 65, 155
Sarangi 17, 155
SATAOrg 55, 69, 110, 120, 155
SciPy 95, 155
Shkolnitsky 8, 12, 45, 155
Silas 11, 17, 18, 155
Silva 104, 155
Snel 1, 155
Sohn 31, 155
Stauffer 89, 155
Staum 65, 155
Stojanovic 86, 155, 157
Suzuki 103, 109, 155
Tao 103, 155
Tasiran 15, 155
TEKTRONIX 23, 156
Thimm 108, 110, 156

Tiruvallur 8, 156
Tripp 39, 152, 156
Ureel 1, 156
USBOrg 55, 69, 110, 156
Vicario 105, 156
Villiers 104, 156
Viveros-Wacher 52, 111, 120, 153, 156
Wagner 10, 156
Wang 18, 39, 41, 52, 55, 56, 65, 100, 102, 117, 151, 153, 155, 156
Weisstein 63, 156
Wile 9, 157
Wilen 85, 157
Wu 112, 147, 149, 157
X.Li 103
Xiao 69, 149, 157
Yao 18, 157
Ye69, 145, 151, 152, 157
Yerramilli 10, 157
Yuan 52, 157
Zerbe 28, 146, 157
Zhang 52, 104, 105, 106, 108, 147, 156, 157

Subject Index

3

3LP, 106, 110

A

ANN, 1, 5, 100, 102, 103, 104, 105, 106, 107, 108, 109, 110, 112, 113, 114
ASM, 118, 119, 121, 124, 154
ATE, 38, 39
attenuation, 23, 28, 31, 52, 76, 86, 88, 117

B

backplane, 23, 145, 157
bandwidth, 23, 28, 31, 33, 38, 55, 69, 77, 86, 88
Bang-Bang, 47
BB, 112
BER, 12, 18, 20, 31, 32, 44, 48, 54, 55, 56, 57, 58, 69, 78, 87, 89, 90, 152
BERT, 47, 145
BIOS, 87, 97
BMF, 102, 117
boundary-scan, 38, 41
Box Behnken, 112
Broyden, 122, 124, 146, 153
bugs, 9, 10, 11, 15, 17, 18, 19, 101, 102, 145

C

CAD, 1, 2, 4, 19, 21, 22, 155
CDR, 40, 54, 55, 57, 60, 112, 120

Ch

channel, ix, 3, 4, 23, 24, 25, 26, 27, 29, 30, 31, 32, 33, 36, 52, 54, 55, 69, 71, 75, 76, 82, 83, 85, 86, 88, 89, 98, 100, 101, 105, 117, 118, 120, 149, 151, 155

C

CMOS, 18, 148, 149, 150, 151, 155
coarse model, 5, 102, 117, 118, 119, 120, 121, 122, 124
Coarse Model, 120
CPU, 1, 68, 85, 95, 110, 119
crosstalk, 3, 28, 30, 31, 35, 55, 69, 81, 117, 157
CTAE, 32
CTLE, 27, 29, 30, 31, 88, 91, 92, 93, 98, 112, 120
CV, 8, 11

D

data-transmission, 75
de-emphasis, 26, 27, 76, 88
deserializer, 48, 54, 88
DFE, 23, 27, 30, 31, 88, 89, 155
DFT, 4, 13, 35, 36, 38, 39, 40, 45, 54, 69, 111
DFx, 8
Direct Optimization, 75, 85
discontinuities, 23, 26, 76
DMI, 68, 110, 120
DoE, 5, 14, 45, 62, 63, 100, 102, 105, 110, 111, 115, 118, 121
DUT, 12, 13, 17, 38, 45, 58, 69, 77

E

EH, 48
electromagnetic coupling, 86
EM, 1, 105, 153, 154
Embedded, 37, 44
emphasis, 15, 21, 26, 27, 28, 30, 32, 76, 88, 100, 148, 149
EQ, 3, 4, 5, 23, 24, 25, 26, 29, 30, 31, 32, 52, 59, 61, 69, 70, 72, 73, 85, 87, 88, 89, 91, 92, 93, 97, 98, 120, 124
EQ coefficients, 52, 59, 61, 69, 72, 73, 85, 87, 89, 98, 120, 124
EQ maps, 87, 91, 92, 97
equalization, ix, 3, 4, 16, 18, 20, 23, 24, 26, 35, 46, 48, 69, 75, 76, 82, 87, 88, 89, 90, 91, 97, 98, 99, 100, 114, 115, 117, 124, 145, 146, 147, 149, 150, 153, 156, 157
equalizer, 4, 5, 18, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 55, 75, 76, 99, 100, 101, 102, 117, 118, 124, 145, 149, 151, 156
Ethernet, 3, 5, 8, 36, 75, 85, 110, 148, 150
EV, 8, 11, 12, 17, 52
EW, 48

exhaustive enumeration, ix, 4, 51, 77, 87
eye asymmetries, 85, 87, 92
eye diagram, 3, 17, 23, 25, 32, 47, 52, 58, 59, 60, 61, 70, 72, 73, 75, 77, 78, 79, 80, 81, 82, 83, 87, 91, 92, 97, 98, 100, 105, 108, 111, 115, 120, 121, 124, 125, 147, 148
eye height, 48, 58, 60, 70, 78, 79, 80, 82, 85, 87, 92, 93, 108, 111, 113, 120, 121, 124, 149
eye mask, 75, 80, 81, 82, 83
eye width, 48, 58, 59, 60, 78, 79, 82, 85, 87, 92, 93, 108, 111, 113, 120, 149

F

factorial designs, 112
feed-forward equalizer, 76
FFE, 18, 76, 78, 82, 88
filter taps, 88
fine model, 5, 105, 108, 109, 110, 114, 117, 118, 119, 120, 121, 122, 124
FIR, 5, 23, 27, 28, 29, 76, 77, 79, 81, 82, 88, 92, 93, 98, 147, 148, 151, 154
FPGA, 2, 19
functional eye, 13, 45, 52, 58, 59, 60, 73, 92, 111, 121
Functional Eye, 13, 45

H

histogram, 78, 79
HSIO, ix, 3, 4, 5, 7, 8, 9, 12, 16, 19, 20, 21, 23, 24, 26, 30, 32, 51, 52, 55, 57, 69, 73, 76, 78, 81, 99, 100, 101, 102, 105, 111, 115, 117, 118, 120
HVM, 10, 13, 14, 45, 69

I

IBIST, 42, 43, 46, 47, 48, 152
IL, 69
ISI, 3, 4, 23, 24, 25, 27, 28, 29, 30, 31, 32, 35, 42, 44, 52, 55, 75, 76, 81, 82, 86, 88, 89, 98

J

JIM, 48
jitter, 3, 4, 16, 17, 32, 35, 39, 40, 44, 48, 51, 52, 53, 55, 56, 57, 61, 69, 73, 75, 76, 78, 79, 80, 81, 117, 148, 151, 153
JTAG, 36, 38
JTOL, 5, 52, 55, 56, 57, 58, 61, 62, 70, 72, 73

K

Kriging, 5, 51, 52, 62, 65, 66, 67, 73, 100, 102, 115, 121, 156

L

loopback, 39, 40, 43, 44, 46, 151
low-discrepancy sequences, 63, 64, 147

M

machine learning, 99, 100, 101, 102, 115, 146, 148, 153
Matlab, 62
metamodel, 102, 114, 115
microprocessors, ix, 7, 8, 9, 10, 51, 154, 156
mixed-signal, ix, 1, 3, 7, 8, 15, 51, 147, 151, 156
MLP, 104, 108
Moore's law, 2, 35
MSE, 32, 108

N

Nelder-Mead method, 81, 95, 96
neural model, 99, 100, 105, 113, 114, 115
noise, ix, 8, 11, 17, 21, 24, 28, 30, 31, 32, 39, 40, 44, 55, 63, 75, 82, 88, 89, 151, 152

O

OA, 112
objective function, 5, 51, 52, 53, 58, 60, 61, 62, 67, 70, 73, 75, 77, 79, 81, 83, 85, 87, 92, 93, 95, 97, 98, 112, 121
on-die instrumentation, 44, 46, 48
optimization, ix, 1, 4, 5, 8, 18, 21, 22, 51, 52, 53, 61, 62, 65, 67, 70, 73, 75, 77, 80, 82, 85, 87, 93, 95, 96, 97, 98, 99, 100, 102, 103, 105, 106, 107, 108, 110, 115, 117, 118, 119, 121, 124, 145, 146, 147, 148, 150, 151, 152, 153, 154, 155, 156, 157
orthogonal arrays, 112

P

pattern search method, 95, 97
PCH, 68, 95, 110, 119, 124
PCIe, 5, 44, 55, 56, 69, 73, 85, 86, 87, 88, 89, 91, 95, 97, 98
PCIE, 3, 8, 152
PCIe3, 52, 57, 86, 87, 88, 89
PDFs, 56

penalty coefficient, 62, 81, 95
PG&C, 44, 47
PHY, ix, 3, 4, 5, 8, 12, 18, 21, 52, 53, 54, 58, 59, 73, 75, 78, 79, 99, 100, 112, 115, 117, 118, 120, 121, 124
PHY tuning, ix, 3, 4, 5, 8, 18, 52, 53, 58, 59, 73, 79, 99, 100, 112, 115, 117, 118, 120, 121, 124
PI, 47, 48
platform, 4, 5, 7, 9, 11, 12, 15, 19, 21, 22, 51, 52, 54, 68, 69, 73, 77, 85, 87, 95, 101, 110, 114, 115, 117, 118, 119, 124, 150, 153, 156
PLL, 54, 55
post-cursor, 25, 30, 88, 93
post-silicon, ix, 2, 4, 5, 7, 8, 9, 10, 11, 12, 15, 16, 17, 18, 19, 20, 21, 36, 51, 52, 68, 69, 71, 75, 76, 77, 82, 85, 87, 91, 95, 97, 98, 99, 100, 101, 102, 105, 110, 115, 117, 118, 119, 124, 145, 147, 148, 151, 153, 157
Post-silicon, 8, 9, 10, 51, 100, 148, 149, 150, 152, 153, 156
PRBS, 44, 56, 81
pre-cursor, 30, 31, 88, 93
pre-emphasis, 26, 27, 88
pre-silicon, 2, 4, 7, 9, 10, 11, 16, 19, 21, 99, 100, 102, 103, 117, 145, 151
Pre-silicon, 9
processor, 7, 146, 150, 155
PRQ, 8, 12, 13, 14
pseudo-random, 44, 81
PVT, ix, 31, 33, 52, 75

Q

Qualification, 8, 14

R

RC, 29, 30, 86, 89
response surface methodology, 112
RJ, 56, 57, 61, 81
RSM, 112
Rx, ix, 3, 4, 5, 12, 13, 18, 23, 24, 26, 28, 29, 30, 31, 32, 43, 45, 46, 48, 52, 54, 55, 56, 57, 60, 69, 70, 73, 75, 85, 86, 87, 88, 89, 90, 92, 93, 96, 97, 98, 100, 101, 106, 108, 111, 114, 117, 118, 120, 124

S

SATA, 3, 8, 55, 56, 71, 100, 110, 113, 117, 118, 120, 124, 155
SATA3, 52, 57, 58, 69, 71, 72, 73
SBO, 67, 118
semiconductor, 21, 35, 36
serializer, 54, 88
SFP, 75, 76, 77
signal integrity, ix, 3, 11, 35, 36, 37, 47, 55, 75, 79, 80, 111, 152
simulation, 2, 9, 10, 11, 16, 17, 19, 20, 21, 44, 77, 101, 102, 103, 106, 146, 147, 155
SJ, 56, 57, 81
SM, 1, 2, 5, 117, 118, 119, 124, 154
SMV, 4, 12, 13, 14, 16, 35, 36, 44, 45, 46, 47, 48, 49, 54, 95, 111, 156
SNR, 28, 30, 69
Sobol, 63, 64, 112, 155
SoC, 7, 8, 51, 149
space mapping, ix, 5, 100, 102, 115, 117, 118, 119, 124, 146, 153, 154
surrogate, ix, 1, 2, 5, 51, 52, 53, 62, 63, 65, 67, 73, 99, 100, 102, 105, 107, 115, 117, 118, 119, 120, 124, 147, 153, 154
surrogate-based modeling, 5, 52
SV, 8, 11
System Marginality, 12

T

T&M, 37
TAP, 38, 41, 42, 78
TL, 69
transceivers, 46, 48, 75, 145, 146
TTM, 8, 10, 14, 51
tunable elements, 18, 100, 117
Tuning knobs, 16
Tx, ix, 3, 4, 5, 12, 16, 18, 23, 24, 26, 27, 28, 30, 31, 32, 43, 46, 52, 54, 55, 58, 69, 73, 75, 76, 77, 78, 82, 85, 87, 88, 89, 90, 91, 93, 96, 98, 100, 120

U

USB, 3, 8, 36, 55, 56, 110, 114, 124, 156
USB3, 52, 57, 69, 71, 73, 100, 111, 114, 120, 151

V

VGA, 112, 120
VT, 109, 112

W

weighting factors, 60, 79, 93, 94, 104, 106, 108, 109, 110

X

XFP, 75

Z

ZF, 32