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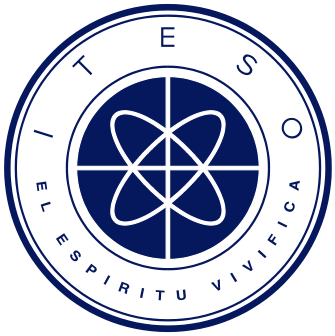
Departamento de Electrónica, Sistemas e Informática

ESPECIALIDAD EN DISEÑO DE SISTEMAS EN CHIP



DESIGN OF BIAS CIRCUIT FOR CHARGE PUMP IN 130NM BICMOS TECHNOLOGY

Tesina para obtener el grado de:

ESPECIALISTA EN DISEÑO DE SISTEMAS EN CHIP

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Dedication

I would like to thank God, for allowing me the opportunity to live not only an academic challenge but also a life experience.

To my wife Alejandra, who has been a valuable support to carry on, and help to understand that life is not always as we want it to be.

To my parents and sisters, I appreciate your patience because of my absence during this process.

I also thank my academic advisor, Dr. Esteban Martinez for his support and technical guidance throughout the specialization degree.

Finally, I would like to thank CONACYT, for its support in allowing me to take this postgraduate degree.

Abstract

The present work shows the design of a Bias circuit in 130 nm of BiCMOS process using Cadence tools. The Bias circuit is part of a Charge Pump (CP) circuit, which in turn is one block of a PLL (Phased Locked Loop) that will be used in a mixed-signal implementation of a Clock and Data Recovery (CDR) circuit. This PLL-based CDR is the project of the generation 2018 of the Specialty in System on a Chip at ITESO. A general description of the analog and digital modules that make up this project is shown at the beginning of this work. As it is described in detail in this work, the proposed design topology reveals the enormous dependence of the polarization circuit to the CP circuit. The replica method used in the Bias circuit allows to "follow" the current variations of CP charge/discharge process to compensate through an OTA (Operational Transconductance Amplifier) the level of voltage required by the tail transistors of CP circuit. The design procedure, the generation of schematics and test benches are shown during the first chapters of this work. The verification of the pre-layout design through the corners process, as well as the use of the post-layout design rules verification tools, are shown during the final chapters of this work

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Resumen

El presente trabajo muestra el diseño de un circuito de polarización en la tecnología de 130nm BiCMOS usando las herramientas de Diseño de Cadence. El circuito de polarización es parte de un circuito Charge Pump (CP), el cual a su vez es parte de un circuito PLL (Phased Locked Loop) que se utilizara en una implementación de señal mixta de un Recuperador de Datos (CDR). Este CDR basado en PLL, forma parte del proyecto de la generación 2018 de la Especialidad de Diseño de Sistemas en Chip de ITESO. Una descripción general acerca de los módulos analógicos y digitales que conforman el proyecto es mostrada al inicio de este trabajo. Como se describe en este trabajo, la topología de diseño propuesta refleja la enorme dependencia del circuito de polarización con el circuito CP. Un circuito replica permite "seguir" las variaciones de carga y descarga de corriente del circuito CP para compensar mediante un OTA (Operational Transconductance Amplifier) el nivel de voltaje requerido en los transistores del circuito diferencial del CP. El proceso de diseño, la generación de esquemáticos y bancos de pruebas son mostrados durante los primeros capítulos de este trabajo. La verificación del diseño pre-layout a través del proceso de esquinas, así como el uso el uso de las herramientas de verificación de reglas de diseño post-layout son mostradas durante los capítulos finales.

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List of Acronyms and Abbreviations

AC	Alternating Current
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDR	Clock Data Recovery
CP	Charge Pump
DC	Direct Current
DRC	Design Rule Checking
ESD	Electro Static Discharge
GBW	Gain Band Width product
I_B	Bias Current
IC	Integrated Circuit
LPF	Low Pass Filter
LVS	Layout Versus Schematic
OTA	Operational Transconductance Amplifier
PFD	Phase Frequency Detector
PLL	Phased Locked Loop
PVT	Process-Voltage-Temperature
QRC	Quantus Resistive Capacitive
SerDes	Serializer/Deserializer
SoC	System on Chip
Vbias	Bias Voltage
VCO	Voltage Controlled Oscillator
VDD	Voltage Drain Drain
V_{Dsat}	Voltage of Saturation
VH	Voltage High
VICM	Voltage Input Common Mode
VL	Voltage Low
VOCM	Voltage Output Common Mode
VSS	Voltage Source Source

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Introduction

During the recent decades, the fast growth of electronics in communication systems has allowed an extraordinary flow of information through the use of cell phones, radios, and personal computers. The invention and continuous development of ICs (Integrated Circuits) have enabled the possibility to reach great advantages in communication systems, advantages which are traduced in small size, low power, and high-speed electronic circuits. Nowadays, all the parts of a modern communication system can be found inside an IC, therefore the integration of each element has become more complex. [1]

The analysis of a communication system is extensive in terms of electronic circuits, so it can start out from the fact that to transmit or receive a signal a transceiver is required. The transceiver (transmitter/receiver in one package) is capable of generating multiple signal frequencies (either for the transmitter or the receiver) in order to pick up "channels" at different frequencies. The process to generate a variable frequency signal from a single reference frequency is known as "frequency synthesis" and it is composed of circuits called synthesizers. An example of the application of synthesizers is the broadcast channel selection.

Depending on the application, synthesizers must meet several specifications for the required performance. [1] Even though there are several types of synthesizers, the ones used in mobile communication systems are based on Phased Locked Loop (PLL). The PLL is one of the most common synthesizer architecture and its wide use is only explained by the parallel advances of integrated circuit design techniques. Today, all parts that define a PLL can be found as blocks in a single IC.

PLL is considered the heart of many communication systems. First commercial PLL used pure analog components, however, advances in integrated circuit design allowed to consider a PLL as a mixed signal circuit; in other words, its architecture involves both digital and analog signal processing units. [2] In general a PLL is defined by five main blocks: Phase Frequency

Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF), Voltage Controlled Oscillator (VCO), and Frequency Divider.

Since my graduation project is related to the CP module, from now on, I will focus the description on this module. A fundamental step in the design of the CP circuit is the definition of an appropriate operating point known as biasing. A Bias circuit plays a fundamental role in the performance of analog circuits since it is responsible for maintaining the proper DC voltage level on transistors. The use of the correct DC level guarantees the correct operation for all expected signals. [3]. In this work, we present the design of the Bias Circuit required for the Charge Pump module in 130nm BiCMOS technology using Cadence tools.

This document is organized as follow: Chapter 1 shows a background study regarding the existing data of the project; Chapter 2 presents the fundamentals of PLL and the CDR (Clock Data Recovery) application; Chapter 3 shows the design of the Bias Circuit at the transistor level, Chapter 4 deals with the pre-layout verification including the virtual integration to the CP circuit; at Chapter 5, the whole layout design is presented, and finally Chapter 6 perform rule design check, layout versus schematic and the post-layout verification.

Modules defined for the PLL will also be developed by other members of the Specialty in Design of System on Chip (SoC) in 130nm BiCMOS technology. The goal of this project is to achieve the integration of all designed modules and obtain an adequate performance of the PLL as a whole.

1. Background

1.1. Historical Review

In 1837, Samuel Morse developed one of the inventions of major relevance to communications, the electric telegraph. Morse devised a variable length binary code in which the alphabet was represented through sequences of dots and dashes. The remarkable impact of Morse's development is the fact of this is the earliest way of a binary digital communication system, in other words, Morse code is the precursor to the variable-length source coding methods used in digital data transmission. [4]

Later years the invention of the telephone by Alexander Graham Bell in 1870 introduces the possibility to establish the voice to voice communication. Although initially, first telephones were very simple and provide service for a short distance, during following decades they were improved in terms of quality of carbon microphones and coils.

Wireless communication was also developed during the last century. In 1895 Gugliermo Marconi transmitted a radio signal at a distance of 2 km approximately and two years later he patented a radio telegraph system. The invention of the vacuum diode by Fleming in 1904 was especially important for radio broadcast: Edwin Armstrong developed the *superheterodyne AM (Amplitude Modulation) radio receiver* during World War I and consequently, the first AM radio broadcast was possible in 1920. Another significant input from Armstrong was the development of the first FM (Frequency Modulation) system in 1933; however, it became popular and commercial after the end of World War II. [4]

The second part of twenty century founded the most important advances in the communications. The invention of the transistor in 1947 by Walter Brattain, John Bardeen, and William Shockley, as well as the invention of the integrated circuit by Jack Kilby and Robert Noyce in 1958, made possible the development of small size, low power, and high-speed

electronic circuits. Today, satellite communication systems, wideband microwave systems, and lightwave communication systems make possible the transmission of different information sources as voice, data and video.

1.2. CDR based on PLL

In digital communications, a Clock Data Recovery (CDR) circuit is a very important component to develop serial communications. A CDR uses clock information included in digital coded data to recover the transmitted information. [5] Most of the CDR circuits are based on PLL (Phase Locked Loop), frequency phases required by CDR are generated by PLL architecture based in VCO (Voltage Control Oscillator).

This is the first time that a CDR based on PLL system is selected by the academic members of the System on Chip Specialist at ITESO to be developed by students as graduating work. Previous generations were focused on the development and improvement of a SerDes system, so know challenges to develop a CDR based on PLL system at the moment are the interaction of the digital and analog design (integration) and the use of the new 130nm BiCMOS technology.

Relevant features for this project are the generation of eight phases by the PLL enabled by a clock selector, and the implementation of a Pseudo-Random Data Generator based on a Linear Feedback Shift Register to provide Data signals to CDR. The PLL will be designed to generate clock signals up to 800 MHz (Max 1GHz) in terms of the capability of the 130nm BiCMOS technology available at ITESO.

2. Theoretical Framework

2.1. PLL

PLL is basically a closed loop feedback frequency control system; its function is based on the phase-frequency detection or phase frequency difference detected between a reference signal, an input signal, and a feedback signal. There are three essential blocks that a PLL contains: a phase-frequency detector (PFD), a loop filter (LF), and a voltage-controlled oscillator (VCO) (**Figure 2-1**).

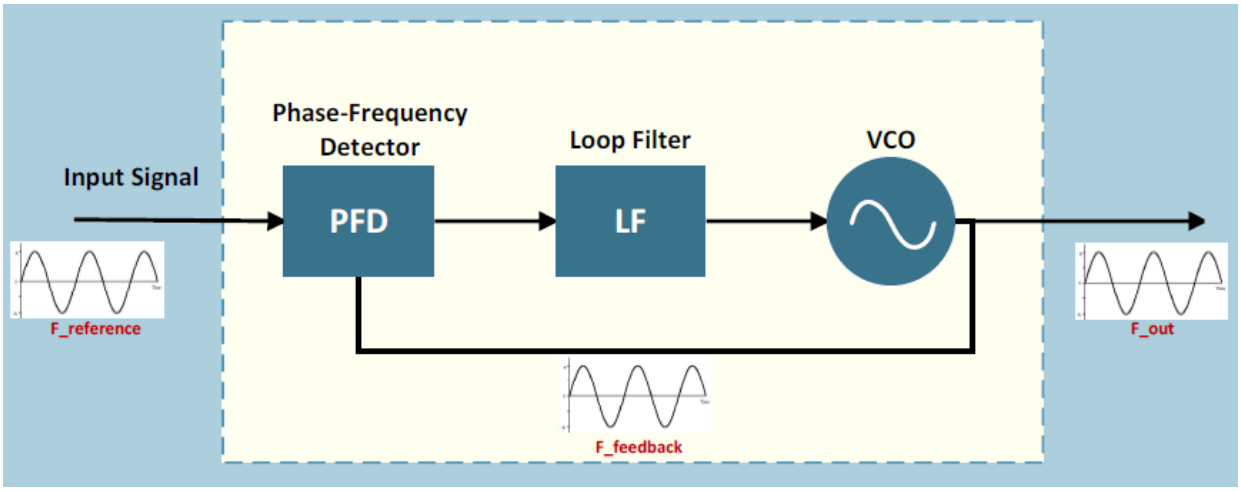


Figure 2-1 Basic phase lock loop.

The PFD compares the phase-frequency of a periodic input signal (F_reference) against of the VCO output signal (F_feedback), the result of this comparison (the PFD output) is the error between the two inputs, which is filtered by the loop filter. The loop filter supplies a controlled voltage to the VCO, which changes its frequency to reduce the phase error between the input signal and the VCO signal. Once the controlled voltage (given by the loop filter) sets the average frequency of the VCO equals the input frequency it is common to say that the PLL is *locked*. The excess of phase error eventually will cause the loss of lock.[6] The range of

frequency over the PLL can be maintained in the loop is called *lock range* which is an important parameter that indicates the capability of the PLL.

2.2. CDR

In serial communications, the receiver needs to recover the clock to sample the data on serial lines. To generate the recovered clock, the receiver requires aligning the phase of a reference clock to the transitions on the incoming data. This is known as Clock Recovery. The sampling of the incoming data signal with the recovered clock to generate a bit stream is known as Data Recovery. Both circuits together are known as Clock and Data Recovery.

The circuit shown in **Figure 2-2** is a basic implementation of a CDR circuit. The clock recovery circuit sense de data (Data In) and produces a periodic clock, the flip-flop driven by the clock retimes the data (the flipflop is sometimes called the decision circuit). The clock generated by the circuit of **Figure 2-2** must satisfy 3 conditions [7]:

- It must have the same frequency to the data rate.
- It must have a relationship with respect to the data.
- It must have a small jitter.

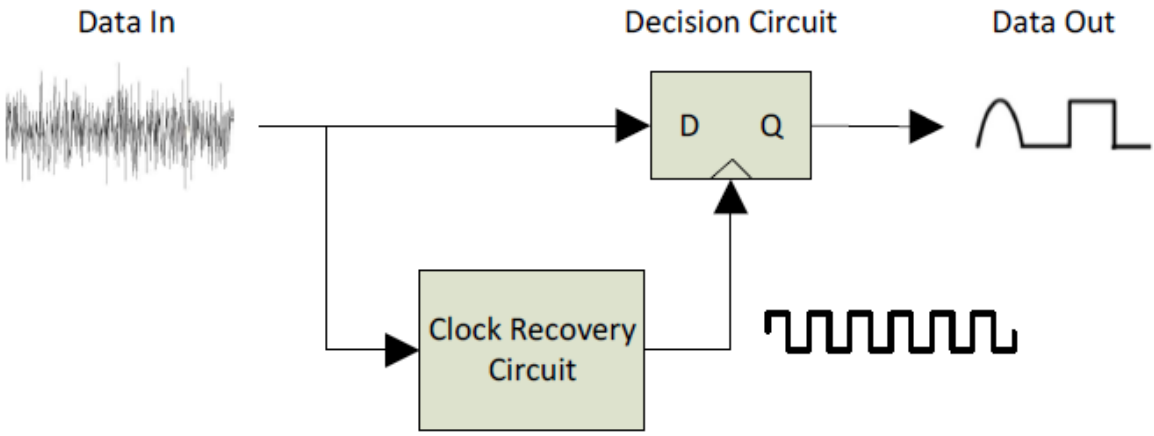


Figure 2-2 Basic CDR block diagram.

2.3. Project 2018 PLL and Clock & Data Recovery

The project developed by the members of the System on Chip Specialist at ITESO is a mixed-signal implementation which includes a high-performance analog PLL and adaptive CDR. The main building blocks of this project can be observed in **Figure 2-3**, this includes:

- Analog PLL
- High-Speed Feedback dividers and Frequency multipliers
- Pseudo-Random Data Generator
- Adaptive Clock and Data Recovery

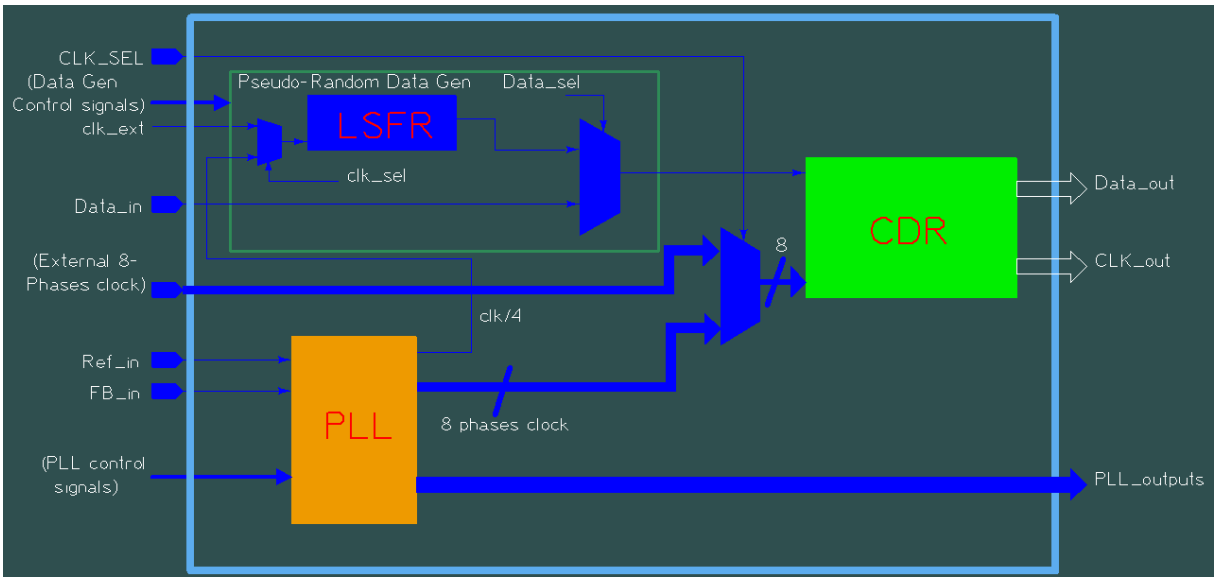


Figure 2-3 PLL and CDR general chip block architecture.

The general design requirements for the PLL block are shown in the Appendix E section. This work contributes to the development of one of the parts that make up the Analog PLL block, specifically, the development of the Bias circuit to the charge pump.

Figure 2-4 roughly represents the PLL topology developed in this project, the charge pump is used to sink and source current into a loop-filter based on the output of a PFD. The Bias circuit main purpose is to assure the correct voltage on the gate of tail transistors into the CP

circuit, even though current variations are expecting due to the performance of CP. A complete explanation about the topology of Bias circuit and CP will be presented in chapter 3.

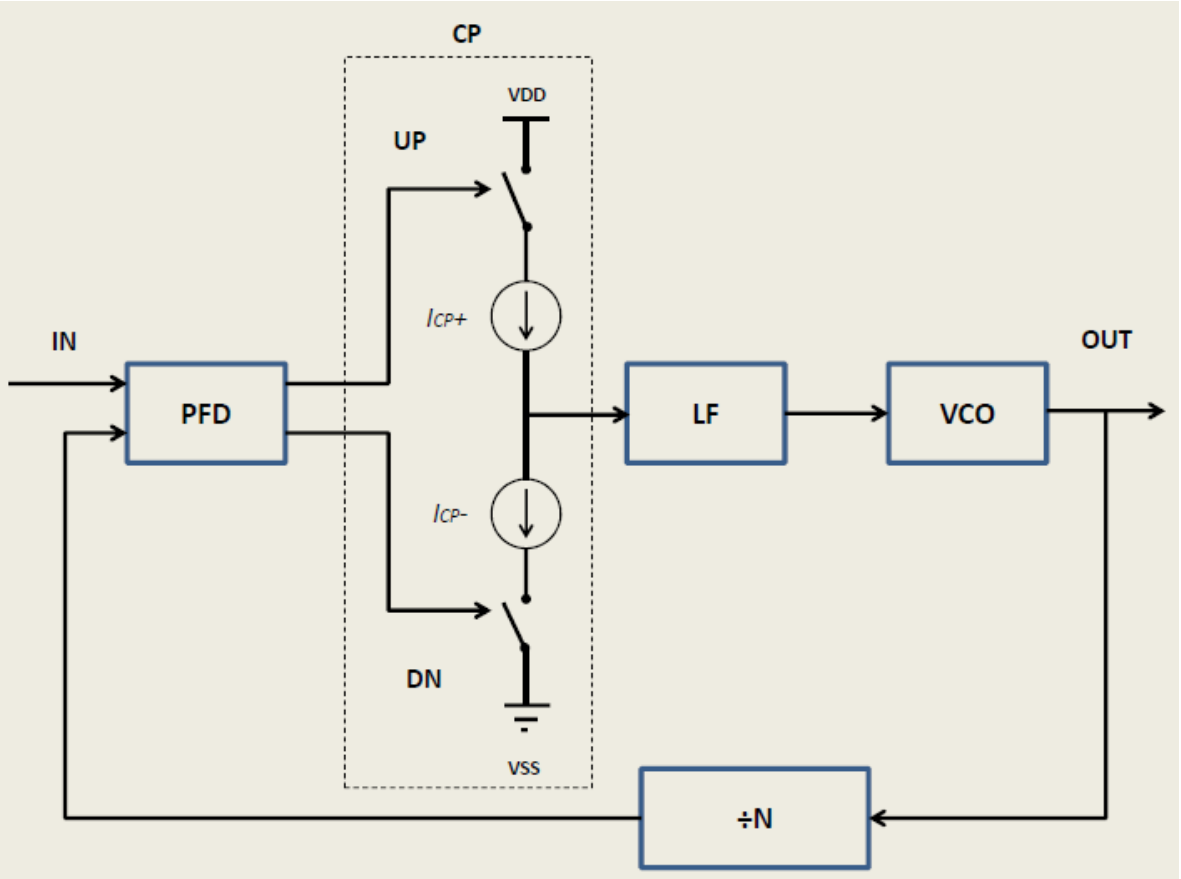


Figure 2-4 Charge pump representation inside PLL.

3. Bias Circuit Design

3.1. Architecture Description

The topology used by the charge pump circuit in the PLL project is a symmetric structure composed of two pump branches [8]. This means, designed Bias circuit will be duplicated to be used in the two charge pump branches (**Figure 3-1**).

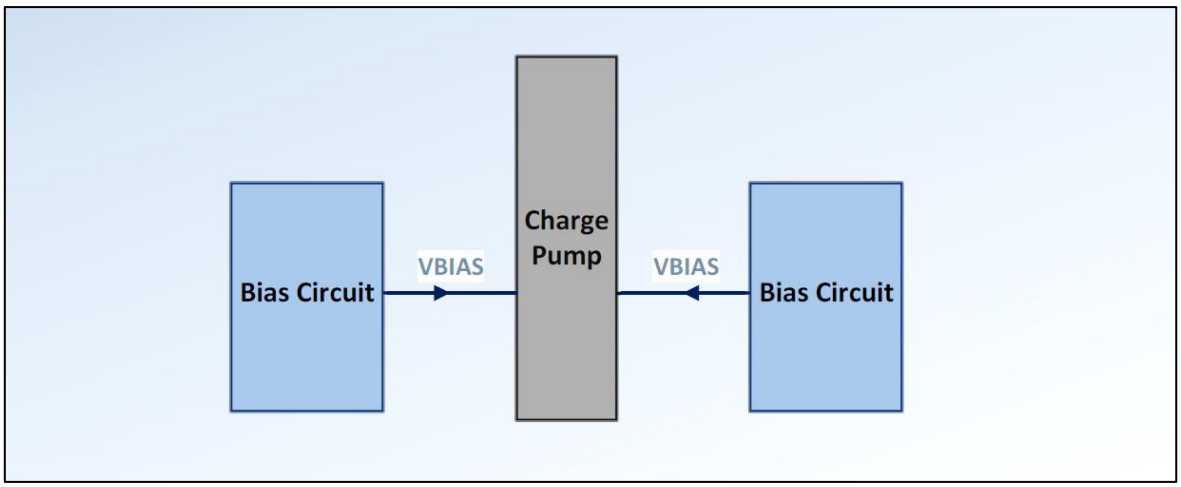


Figure 3-1 Charge pump and Bias circuit blocks.

The structure of the Bias circuit is formed by three main blocks (**Figure 3-2**): an Operational Transconductance Amplifier (OTA), a Voltage Reference and a Replica branch of the Charge Pump Circuit. A bias voltage is determinate through a control closed-loop feedback using an OTA. A Voltage Reference is required for the non-inverter OTA input to set the voltage value required to mirror it on the inverted input which senses the current on the replica circuit value.

The Replica Circuit must be capable to drive the same portion of the current of charge pump branches in order to compensate the voltage variations during the charge pump operation.

The chosen architecture for this project is based on a previous work developed by one of the System on Chip Specialty member for the SerDes project in 2016 [9], even though the application in the current project is totally different, the main principle of closed-loop feedback was the intended purpose in this work.

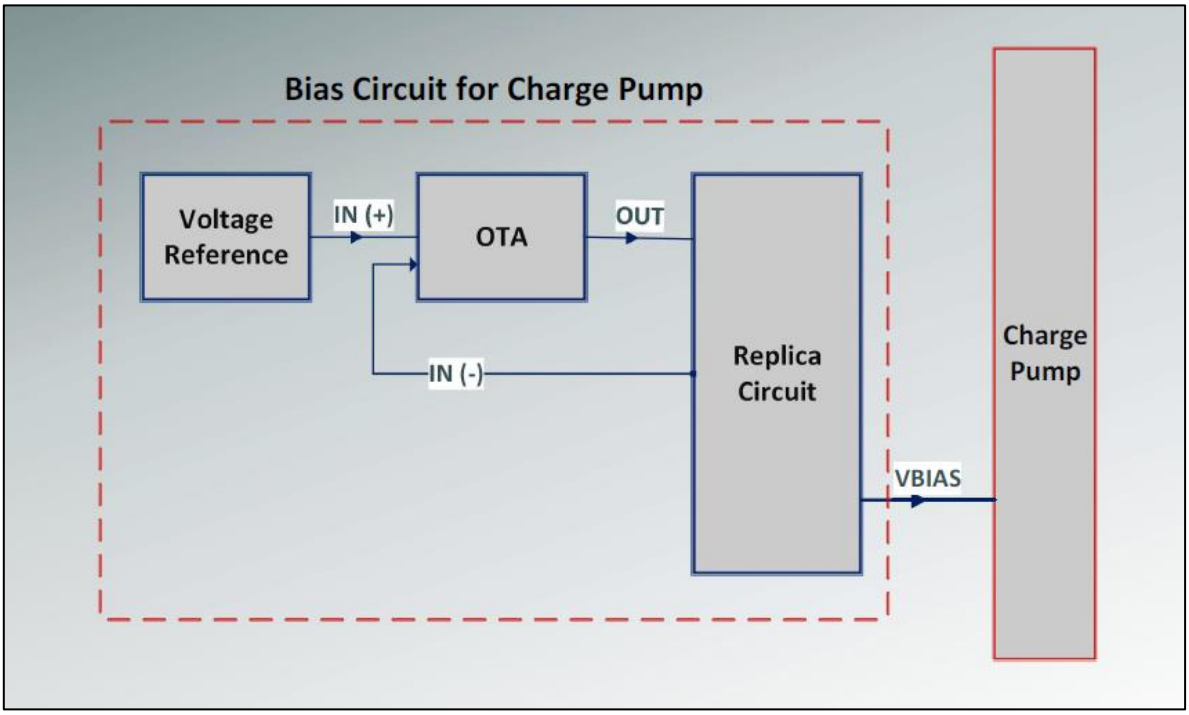


Figure 3-2 Bias circuit block diagram.

3.2. Design of OTA

The OTA design is based in two-stage N-channel OTA architecture. As previously was indicated, this topology was chosen due its high-gain (stage 1) and high-swing (stage 2) performance. The first stage (**Figure 3-3**), is composed of transistors M_1-M_4 and M_{B2}; the second stage is composed of transistors M_5 and M_{B3}. Transistor M_{B1} is connected as a diode sharing the gate terminal with M_{B2} (current mirror array) in order to provide a Vbias to M_{B2}.

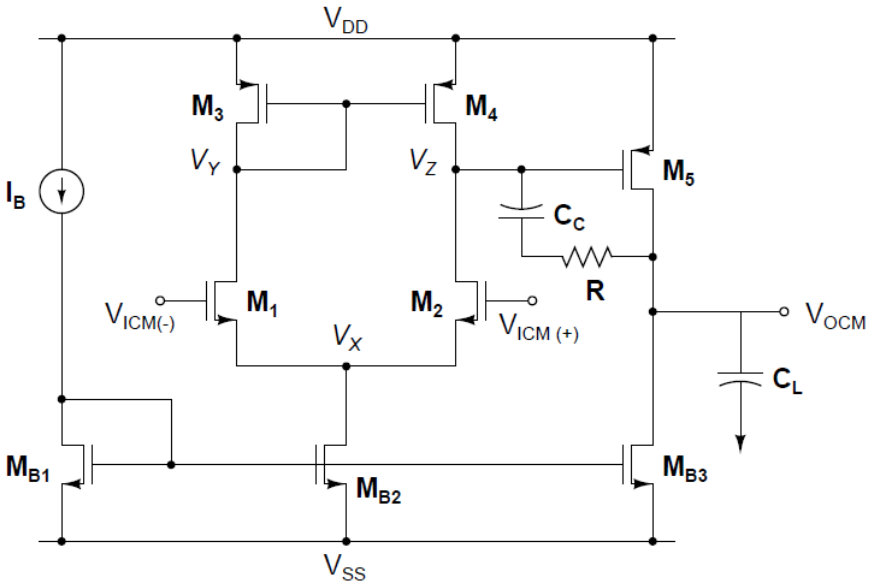


Figure 3-3 Compensated two-stage OTA topology

3.2.1 OTA Design Requirements

In accordance with required charge pump performance, the OTA requirements are showed in **TABLE I**. A gain of 40 dB was set in order to reduce the DC offset. Voltage Input Common Mode (VICM) of 985 mV is the result of the voltage level adjusted in the replica circuit due to the dynamic current is driven through the branches of the charge pump. Voltage Output Common Mode (VOCM) was set considering 0.6*VDD. The origin of VICM and VOCM values will be detailed later in the Design of Replica Circuit section. A Gain Band Width (GBW) of 40 MHz was proposed considering the unnecessary frequency domain performance due to DC application of this OTA. The capacitor load (C_L) of 1 pF was selected starting from the trade-off between a higher Cgs capacitance value of N-channel charge pump tail transistor and the compensation capacitor Cc, the relation between all these capacitances will be defined in OTA design methodology section. The parameter "α" is the factor which relates the two stages in terms of the transistor sizes and consequently relates the current values for each stage. This parameter is obtained by the following relation: [10]

$$\left(W/L\right)_{MB3} = \left(W/L\right)_{MB2}\left(\frac{I_5}{I_{MB2}}\right) \tag{3-1}$$

$$\alpha = \left(\frac{I_5}{I_{MB2}}\right) = \left(\frac{I_5}{I_B}\right) \tag{3-2}$$

TABLE I
OTA DESIGN REQUIREMENTS

Parameter	Design Requirement
Gain	40 dB
GBW	40 MHz
VDD	1.2 V
VSS	0 V
VICM	985 mV
VOCM	720 mV
C_L	1 pF
α	2
P_{diss}	≤ 1 mW

In order to simplify the OTA design, "α" parameter is proposed as an entire value, the only restriction for this does not exceed the Power dissipation (Pdiss) specified as 1 mW. Finally, VDD of 1.2V is the specified voltage for 130nm BiCMOS technology (BICMOS8HP manual technology).

3.2.2 Design of OTA

Given the design topology and requirements, there are some additional parameters required for the OTA design (**TABLE II**); these parameters are inherent to 130nm BiCMOS technology and they are obtained by a process characterization. The channel Length (L) is one of the key aspects to consider in the design flow; in this case, the criteria to select L size was choose a value greater than 2Lmin to reduce length modulation channel effect on the circuit performance, so the selected value was L=320nm (see Appendix A section). [11]

TABLE II
130NM BICMOS DESIGN PARAMETERS

Parameter	NMOS	PMOS
$K\ (uA/V^2)$	451.107	63.903
$V_{TH}\ (mV)$	280.169	-269.051

Once established the technology parameters, the next value to consider is the compensation capacitor C_C. In order to guaranty a "good stability" (60° of phase margin) in a two-stage OTA, the output pole must be 2.2 higher than the GBW (assuming that the RHP zero is placed at ten times GBW) [10], therefore the relation for C_C is:

$$C_C > (2.2/10)C_L \tag{3-3}$$

$$C_C > (2.2/10)(1\ \text{pF})$$

$$C_C > 0.22\ \text{pF}$$

The selected value for C_C according to **(3-3)** is **0.5 pF** (considering also C_C must be lower than C_L). Also, an important parameter to take into account is the static power dissipation (P_{diss}), the way to guarantee the P_{diss} will be lower than the specified value is do not exceed the Bias Current (I_B) and consequently its multiple derived from the α factor.

$$P_{diss} \leq (I_B + I_5)(V_{DD} + |V_{SS}|) \tag{3-4}$$

$$(I_B + I_5) \leq \frac{P_{diss}}{(V_{DD} + |V_{SS}|)} \leq \frac{1\ \text{mW}}{(1.2\ \text{V} + |0\ \text{V}|)} \leq \mathbf{833\ uA}$$

Then, the maximum current for the combination of I_B and I_5 is 833 μA. Now, the design equations to get the size of the transistor will be described below using the declared specifications.

$$\text{GBW} = gm_1/C_C \tag{3-5}$$

$$gm_1 = GBW * C_C$$

$$gm_1 = (40\ \text{MHz})(2\pi)(0.5\ \text{pF}) = \mathbf{125.66\ uS}$$

$$gm_1 = I_B/V_{dsat} \tag{3-6}$$

Assuming a V_{dsat} = 200 mV (a detailed explanation about the use of V_{dsat} = 200 mV can be found in Appendix Section):

$$I_B = gm_1 V_{dsat} = (125.66\ \text{uS})(200\ \text{mV}) = \mathbf{25.132\ uA}$$

$$I_5 = I_B\alpha = (25.132\ \mu\text{A})(2) = \mathbf{50.264\ uA}$$

From the equation **(3-4)**, we can note that the P_{diss} requirement is accomplished with calculated branch currents I_B and I_5:

$$(I_B + I_5) \leq (\mathbf{25.132\ uA} + \mathbf{50.264\ uA}) \leq \mathbf{833\ uA}$$

From the relationship between gm_1 and I_D, we can obtain the size (W/L) of transistor $M_{1,2}$:

$$gm_1 = \sqrt{2I_D K_N \left(W/L\right)_1} \tag{3-7}$$

$$I_D = I_B/2 \tag{3-8}$$

$$\left(W/L\right)_1 = \frac{(gm_1)^2}{I_B K_N} = \frac{(125.66\ \mu\text{S})^2}{(25.132\ \mu\text{A})(451.107\ \mu\text{A/V}^2)} = \mathbf{1.34}$$

Now, we can calculate the DC voltage at node X, which is given by (**3-9**):

$$V_X = \mathrm{V_{ICM}} - \mathrm{V_{GS1}} = \mathrm{V_{ICM}} - \mathrm{V_{TN1}} - \sqrt{\frac{\mathrm{I_B}}{\mathrm{K_N}\left(\mathrm{W}/\mathrm{L}\right)_1}} \tag{3-9}$$

$$\mathrm{V_X} = 985\ \mathrm{mV} - 280.169\ \mathrm{mV} - \sqrt{\frac{25.132\ \mu\mathrm{A}}{(451.107\ \mu\mathrm{A/V^2})(1.34)}} = \mathbf{500.92\ mV}$$

The (W/L) of transistor $M_{3,4}$ can be obtained from the DC voltage at node Out, which is given by (**3-10**):

$$\mathrm{V_{OCM}} = \mathrm{V_Z} = \mathrm{V_Y} \tag{3-10}$$

Where:

$$\mathrm{V_Y} = \mathrm{V_{DD}} - |\mathrm{V_{GS3}}| = \mathrm{V_{DD}} - |\mathrm{V_{TP3}}| - \sqrt{\frac{\mathrm{I_B}}{\mathrm{K_P}\left(\mathrm{W}/\mathrm{L}\right)_3}}$$

Therefore:

$$\left(\mathrm{W}/\mathrm{L}\right)_3 = \frac{\mathrm{I_B}}{\mathrm{K_P}(\mathrm{V_{DD}} - |\mathrm{V_{TP3}}| - \mathrm{V_Y})^2} = \frac{25.132\ \mu\mathrm{A}}{63.903\ \mu\mathrm{A/V^2}(1.2\ \mathrm{V} - |-269.051\ \mathrm{mV}| - 720\ \mathrm{mV})^2} = \mathbf{8.71}$$

The (W/L) of transistor M_5 can be obtained from factor α:

$$\mathrm{M_5} = 2\alpha\mathrm{M_4} \tag{3-11}$$

Then:

$$M_5 = \left(W/L\right)_5 = 2(2)(8.71) = \mathbf{34.86}$$

The (W/L) of transistor MB1, B2, B3 of the current mirror can be obtained from the quadratic equation of the transistor in saturation:

$$\left(W/L\right)_{MB2} = \frac{2I_B}{(V_{dsat})^2 K_N} \tag{3-12}$$

Here again, we assume V_{dsat} = 200 mV:

$$\left(W/L\right)_{MB2} = \frac{(2)(25.132\ \mu A)}{(200\ mV)^2(451.107\ \mu A/V^2)} = \mathbf{2.78}$$

$$M_{B3} = \alpha M_{B2} \tag{3-13}$$

$$M_{B3} = \left(W/L\right)_{MB3} = (2)2.78 = \mathbf{5.57}$$

Finally, to get the transistor sizes, the obtained ratio values for each transistor are evaluated taking into account the initial established value for L=320 nm.

$$\left(W/L\right)_1 = \left(W/L\right)_2 = 1.34$$

$$W_{1,2} = 1.34\ (320\ nm) = 428.8\ nm\ \approx \mathbf{430\ nm}$$

$$\left(W/L\right)_3 = \left(W/L\right)_4 = 8.71$$

$$W_{3,4} = 8.71\ (320\ nm) = 2.787\ um\ \approx \mathbf{2.8\ um}$$

$$\left(W/L\right)_5 = 34.86$$

$$W_5 = 34.86\ (320\ nm) = 11.155\ um\ \approx \mathbf{11.2\ um}$$

$$\left(W/L\right)_{MB1} = \left(W/L\right)_{MB2} = 2.78$$

$$W_{MB1,MB2} = 2.78\ (320\ \text{nm}) = 0.889\ \text{um}\ \approx \mathbf{0.880\ nm}$$

$$\left(W/L\right)_{MB3} = 5.57$$

$$W_{MB3} = 5.57\ (320\ \text{nm}) = 1.782\ \text{um}\ \approx \mathbf{1.78\ um}$$

One must remark that it may likely that undesired RHP zero may not be despicable; this occurs if the GBW is too large or the output transconductance of stage 2 was not large. In this case, it becomes necessary to employ a nulling compensation method. To accomplish this, a resistor is placed in series with the compensation capacitor. [10] The calculation of R-value is performed with (**3-14**):

$$R = \frac{1}{gm_5}\left(\frac{C_L + C_C}{C_C}\right) \tag{3-14}$$

Using results obtained related to M5 size and I_5 current, the transconductance may be obtained using the equation **(3-15**:

$$gm_5 = \sqrt{2\left(W/L\right)_5 K_P I_5} \tag{3-15}$$

$$gm_5 = \sqrt{2(34.86)(63.903\ \text{uA/V}^2)(50.264\ \text{uA})} = 473.22\ \text{uS}$$

$$R = \frac{1}{473.22\ \text{uS}}\left(\frac{1\ \text{pF} + 0.5\ \text{pF}}{0.5\ \text{pF}}\right) = \mathbf{6.669\ K\Omega}$$

3.3. Design of the Resistive Voltage Reference

The Voltage Reference circuit for the OTA's positive input (+IN) is based on a simple voltage divider concept, which takes the 985 mV from VICM requirement design (**TABLE II**) as the voltage reference to be supplied to the OTA. The Voltage Reference concept uses a

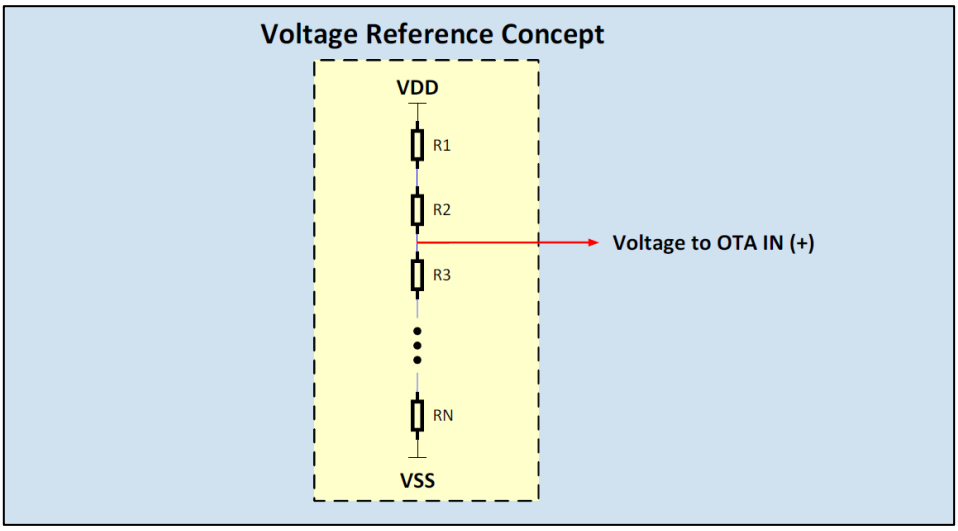


Figure 3-4 Voltage reference concept.

determined number of serial resistors between VDD and VSS, such that an approximation of VICM value can be selected from the nodes created between these two points.

A condition considered for N value (**Figure 3-4**) to distribute an eventual variation of V_{DD} is to select at least N > 10. If more resistors are placed between V_{DD} and V_{SS}, more nodes are created; therefore the voltage variation between nodes is reduced.

$$N = \frac{V_{DD}}{V_X} \tag{3-16}$$

$$M \approx \frac{V_{REF}}{V_X} \tag{3-17}$$

N: Number of resistors (entire value).

V_X: the voltage variation (increment/decrement) between nodes.

V_{REF}: Voltage Reference (VICM)

M: Number of nodes whose value measured respecting V_{SS} has the VICM (entire value).

From the above equations, an additional condition of N > M can be deducted from the fact of V_{DD} is greater than V_{REF}. To find V_X, the value of N is increased progressively (11, 12, 13…) in the equation (3-16), paralleling, the value of M is also increased in the expression (**3-17**) considering the condition N > M, combining (**3-16**) and (**3-17**) the following expression is obtained:

$$\frac{V_{DD}}{N} \approx \frac{V_{REF}}{M} \tag{3-18}$$

A progressive evaluation up till N = 30 can be found in appendix section, the coming values were determined as result of such analysis:

N = **28** M = **23**

$$\frac{V_{DD}}{N} \approx \frac{V_{REF}}{M} \rightarrow \frac{1.2\ V}{28} \approx \frac{985\ mV}{23} \rightarrow \mathbf{42.857\ mV \approx 42.826\ mV}$$

In this way:

$$V_{REF} \approx MV_X = (23)(42.857\ mV) = \mathbf{985.711\ mV}$$

According to results, 28 serial resistors (N) would be placed between V_{DD} and V_{SS} for the Voltage Regulator, this will create 27 voltage nodes between resistors and each node would have a difference of 42.857 mV (V_X) from V_{SS} till up V_{DD}. After 23 resistors (M), the consequent node would have a voltage of 985.711 mV (V_{REG}), which will be taken as the Voltage Reference.

Finally, it is not necessary to define a specific size for resistors; due to the simply serial voltage divider between V_{DD} and V_{SS}, any value of resistor would have the same effect on all nodes created. The criteria to determine the resistor size was simply to choose the lowest value available for the resistor cell OPRRPRES (RR Poli OP Resistor) of the 130nm BiCMOS technology, the lowest dimension for this cell is **W=740 nm**, **L=1.1 um** which represent a resistance value of **R=995.25 Ω.**

3.4. Design of the Replica Circuit

The Replica Circuit is the last sub-block inside the Bias circuit. The reason for its name "Replica" is because it is a mirror of a branch of the biasing circuit (the CP circuit in this case). The purpose of creating a replica of the CP design is to follow the current variations through the CP branch; this means, the same variation of current observed through the CP will be also observed in the replica branch of Bias circuit. Then the current variation through replica circuit is traduced into a node voltage variation taken by the OTA inverter input; this last process closes the relation between the elements of Bias circuit and consequently turns it to a closed loop control system.

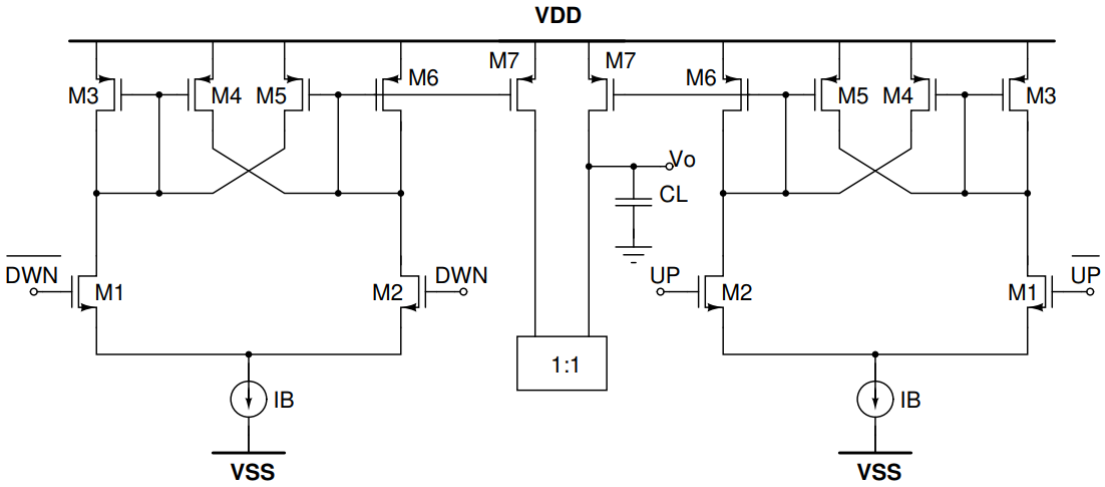


Figure 3-5 Charge pump topology used in PLL project ITESO 2018.[8]

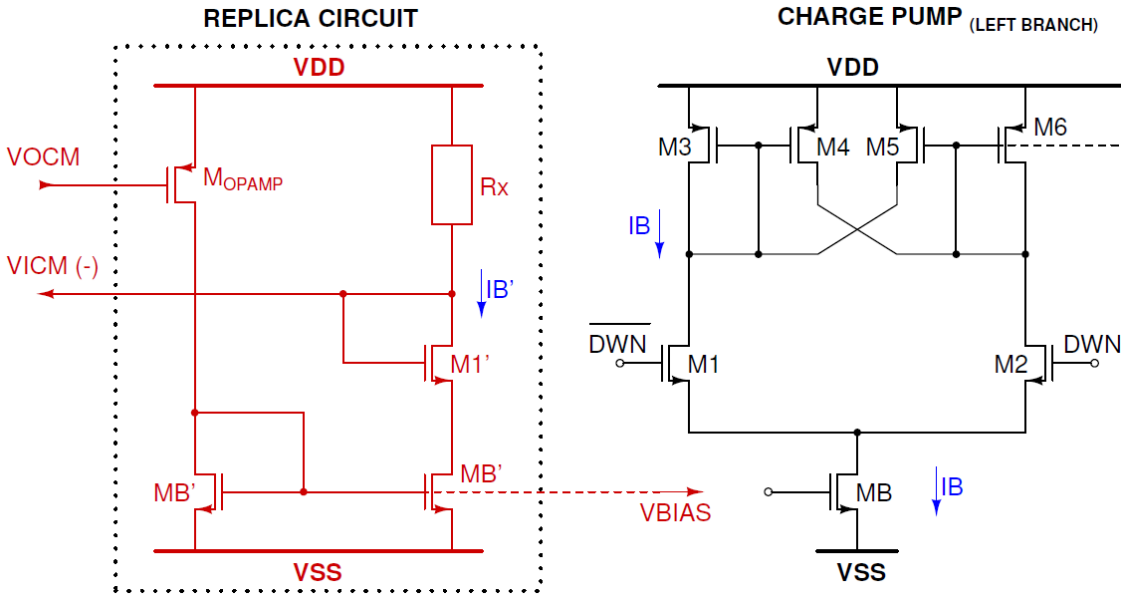


Figure 3-6 Replica circuit for a left branch of the charge pump.

The replica circuit designed is based on the topology showed in **Figure 3-5**. Keeping the current value as the main parameter in both designs requires the use of the same size of transistors, nevertheless some adaptations are required: the concept of replica is most respected, the output of this circuit is the bias voltage (Vbias) which is also the output of all blocks described in section 3.1. **Figure 3-6** shows the structure of the replica circuit, the size of MB' transistors (current mirror) are the same as the tail transistor MB of the CP, as well as the M1' transistor follows the M1.

The bias current (I_B), the bias voltage (Vbias) and sizes of transistors used in CP design are:

$$I_B = \mathbf{100\ uA} = \mathbf{IB'}$$

$$\text{Vbias} = \mathbf{335\ mV}$$

$$M1 = \mathbf{36} = \left(W/L\right)_{M1} = \left(25.2\ um/0.7\ um\right) = \mathbf{M1'}$$

$$MB = \mathbf{5} = \left(W/L\right)_{MB,} = \left(1.5\ um/0.3\ um\right) = \mathbf{MB'}$$

The rest of the elements of the replica circuit are determined using the OTA requirements and the I_B value, which is:

$$R_X = \frac{V_{DD} - VICM}{I_B{}'} \tag{3-19}$$

$$R_X = \frac{1.2V - 0.985V}{100uA} = \mathbf{2.15K\Omega}$$

$$VOCM = V_{DD} - \left|V_{GS_{MOPAMP}}\right| = V_{DD} - \left|V_{TPMOPAMP}\right| - \sqrt{\frac{I_{B,}}{K_P\left(W/L\right)_{MOPAMP}}} \tag{3-20}$$

$$\left(W/L\right)_{MOPAMP} = \frac{I_{B,}}{K_P(V_{DD} - \left|V_{TPMOPAMP}\right| - VOCM)^2}$$

$$\left(W/L\right)_{MOPAMP} = \frac{100\ \mu A}{63.903\ \mu A/V^2(1.2\ V - \left|-269.051\ mV\right| - 0.72\ V)^2} = \mathbf{35.16}$$

The function of transistor MOPAMP is fundamental to perform the main function of this circuit, a size adjustment may be required (Chapter 4) in terms of ensuring the proper bias voltage to the CP circuit.

4. Bias Circuit: Pre-Layout Verification

4.1. OTA Pre-Layout Verification

Using the schematic editor Virtuoso of Cadence, the two-stage OTA circuit is created for pre-layout verification. First, to achieve the desired OTA performance indicated in chapter 3, transistors have been re-sized through an iterative method using typical process parameters of BiCMOS technology and nominal temperature; the final values of transistor's sizes are summarized in **TABLE III**. **Figure 4-1** shows the schematic of two-stage OTA with calculated sizes of transistors.

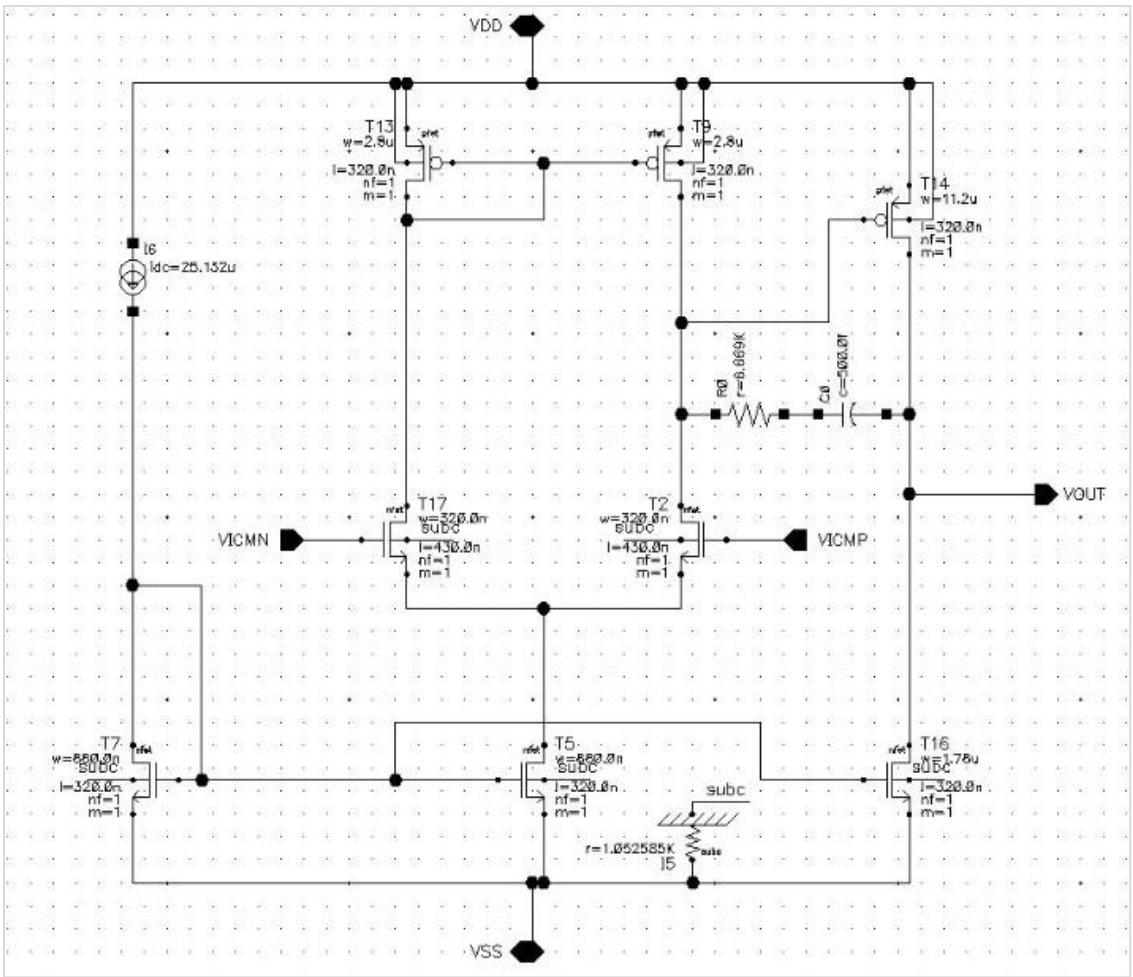


Figure 4-1 Two stage OTA schematic

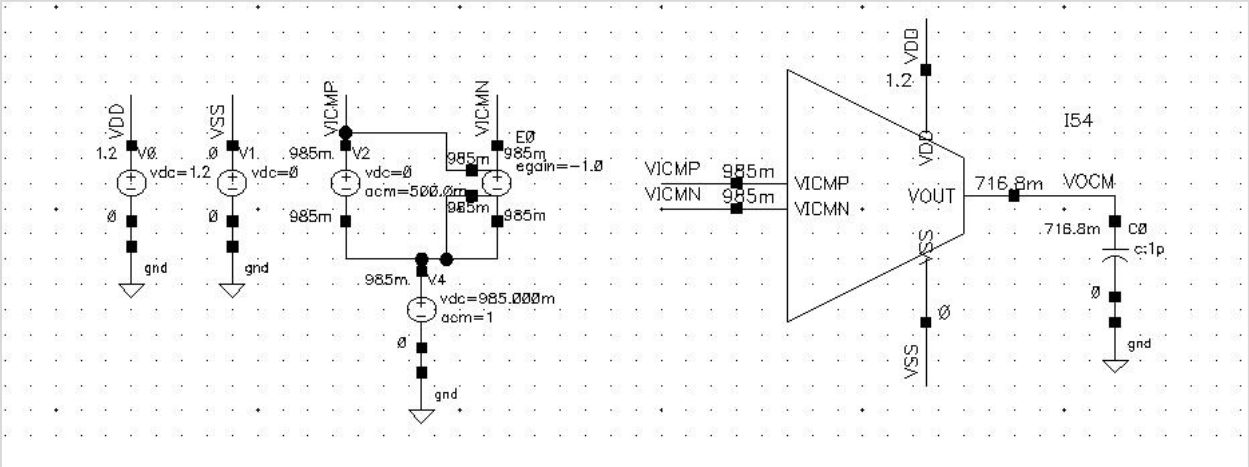


Figure 4-2 Two stage OTA test bench

Figure 4-2 shows the test bench created for simulation purposes, in this circuit differential sinusoidal inputs (0V DC, 0.5V AC) are used to perform the AC analysis, inputs are mounted on a common DC voltage (VICMP = VICMN = **985 mV**). **Figure 4-3** shows the achievement of the output (VOCM = **716.8 mV**). The resulted signal which confirms the achievement of the gain of **39.88 dB** and GBW of **35.66 MHz** is observed in **Figure 4-3**.

TABLE III
130nm FINAL OTA DESIGN PARAMETERS

Parameter	Calculated Value (um)	Final Value (um)
$L_{(All\ Transistors)}$	0.320	0.320
$W_{1,2}$	0.430	1.3
$W_{3,4}$	2.8	2.4
W_5	11.2	9.12
$W_{MB1,MB2}$	0.880	0.720
W_{MB3}	1.78	1.35

Due to a trade-off between the gain and GBW for an amplifier design, the gain has been prioritized over the GBW, the reason is the DC application of this OTA in the Bias circuit. The

requirement of 40 MHz in chapter 3 had only the purpose to avoid a very small gm value, consequently, this also avoids to deal with large transistors according to expression (**3-7**).

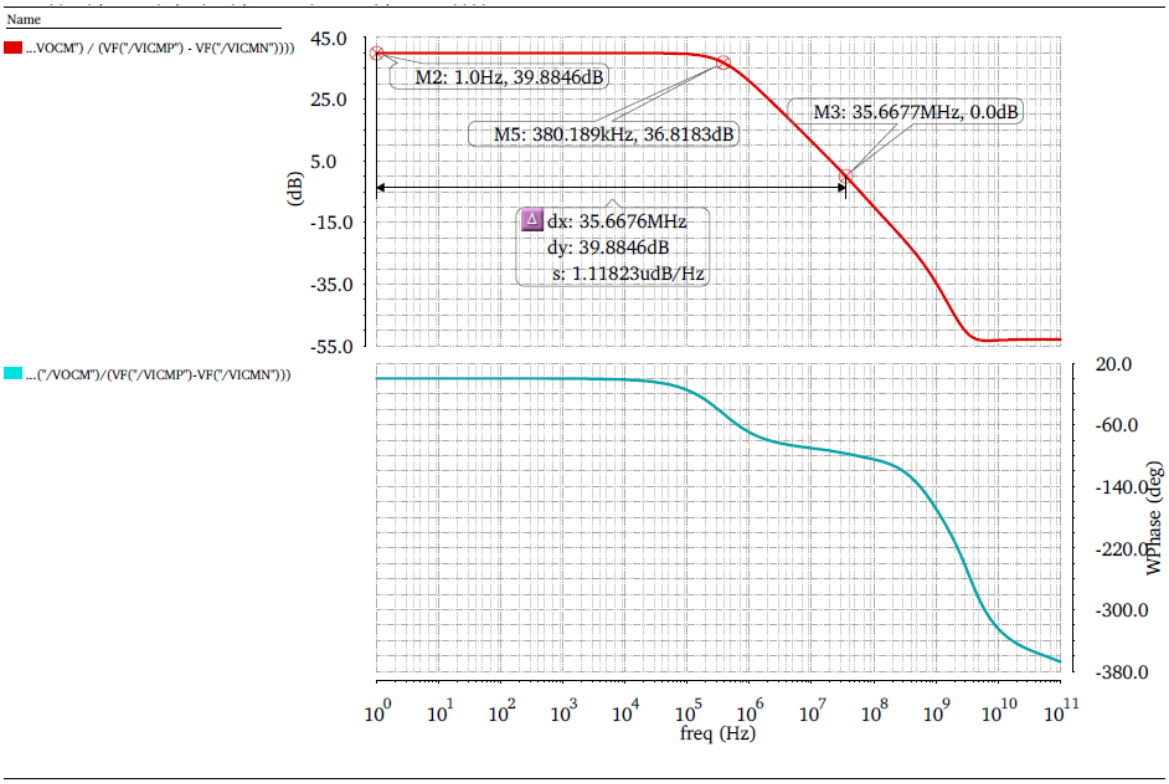


Figure 4-3 Two stage OTA AC response

4.2. Resistive Voltage Reference Pre-Layout Verification

The implementation of the voltage reference is observed in **Figure 4-4**. As described in chapter 3, this series connection of 28 resistors enable a voltage divider into each node; in this case, the required voltage is taken between resistors 24 and 23. A close view of **Vref** is shown in **Figure 4-5**, in which we observe the generated voltage of **985.7 mV**. Dimension for each resistor cell is **W=740 nm**, **L=1.1 um** which represents a resistance value of **R=995.25 Ω**. For pre-layout validation purposes, the voltage divider is connected to a VDD = 1.2V and the Vref and the output is measured. In **Figure 4-6** we present the block whose contains the voltage reference

circuit (V_ref Prelayout). **Figure 4-7** presents the transient response of circuit showing that no changes in Vref and VDD occur during the interval of 1 us.

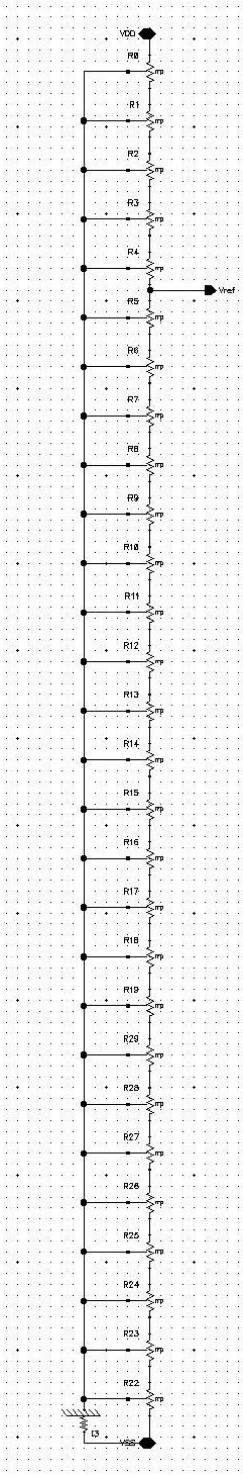


Figure 4-4 Voltage reference circuit

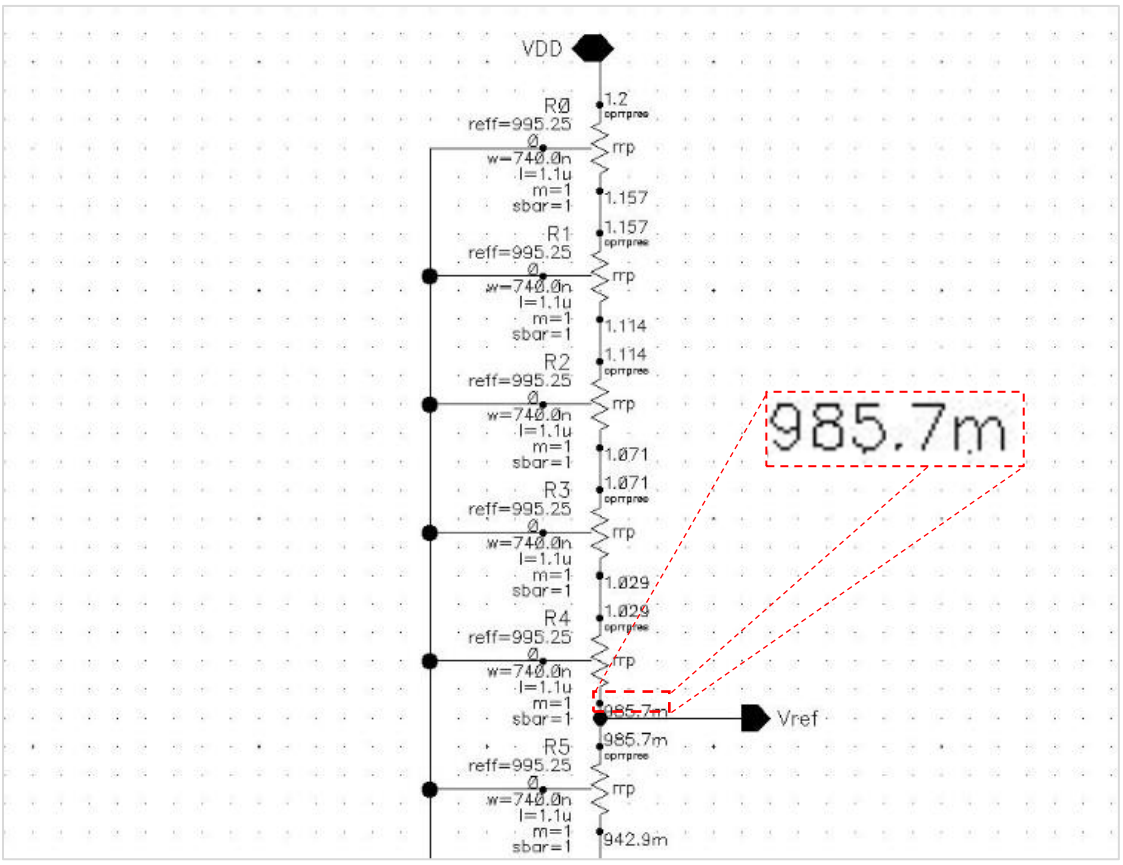


Figure 4-5 Voltage Reference Circuit (closed view at Vref)

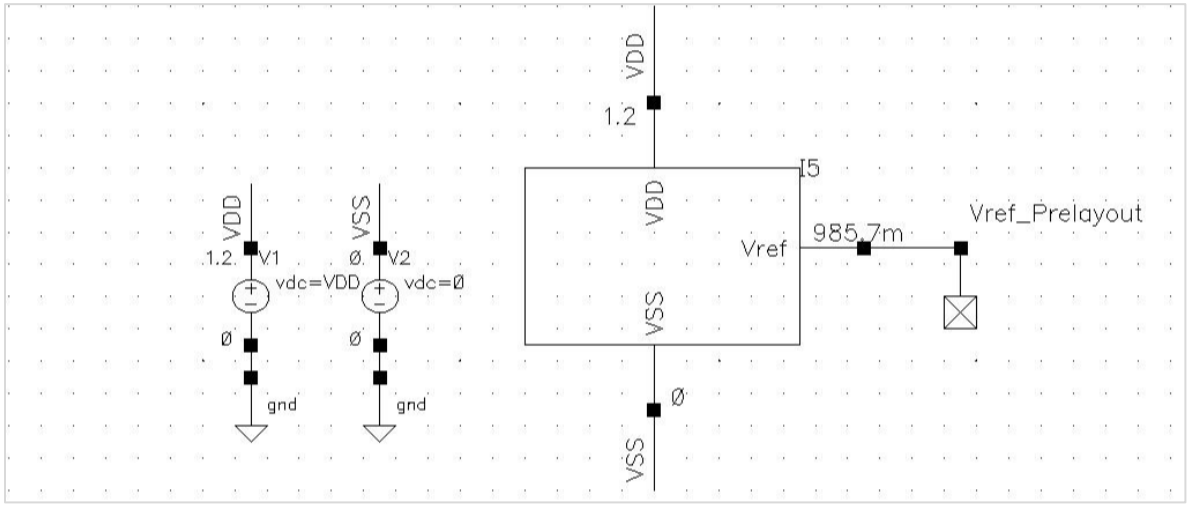


Figure 4-6 Voltage reference test bench

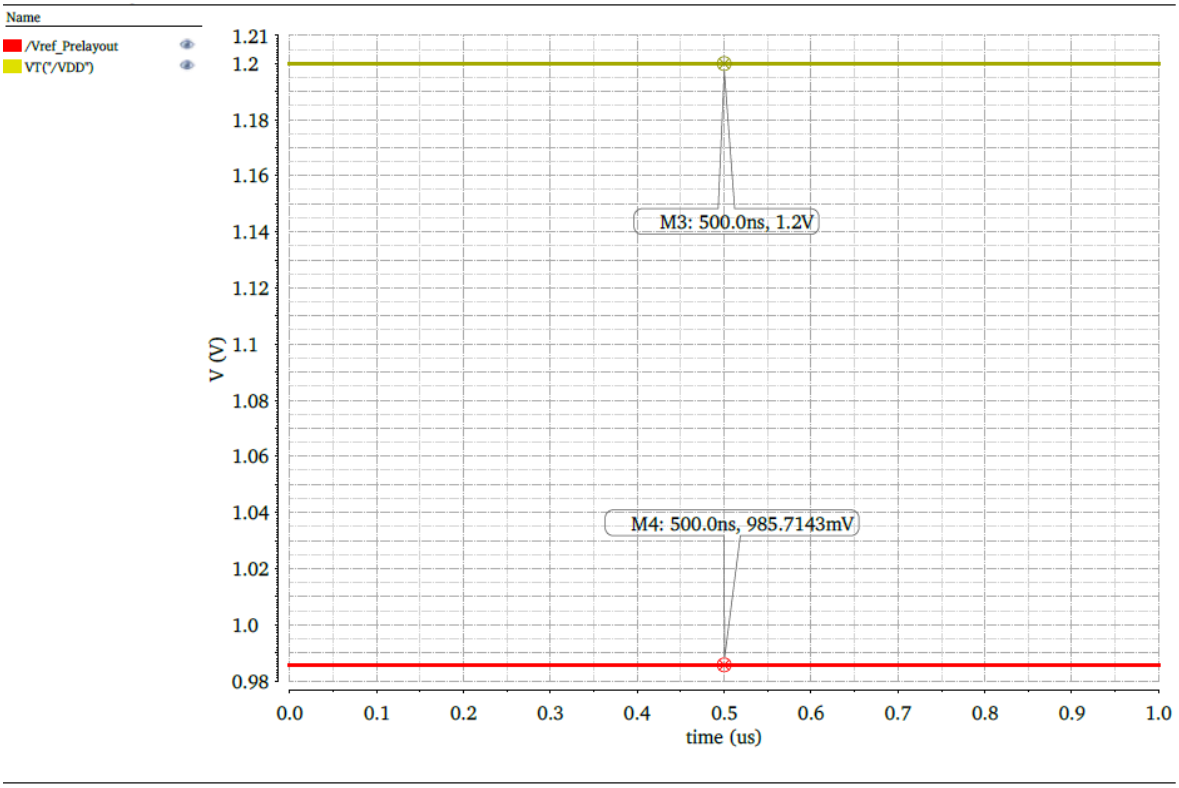


Figure 4-7 Transient response analysis for voltage reference

4.3. Replica Circuit Pre-Layout Verification

As well as the OTA design, the replica circuit was required a re-size of transistors through an iterative method, although this process was only applied to the MOPAMP transistor to satisfy the replica concept of the CP circuit. **TABLE IV** shows the final transistor sizes for the replica circuit; additionally, the multiplicity factor is used for layout flexibility purposes.

TABLE IV
130NM FINAL REPLICA CIRCUIT DESIGN PARAMETERS

Parameter	Calculated Size Transistor	Calculate Value (um)	Final Size Transistor	Multiplicity	Final Value (um)
$W/L_{(M1)}$	36	25.2 / 0.7	36	6	4.2 / 0.7
$W/L_{(MB')}$	5	1.5 / 0.3	5	1	1.5 / 0.3
$W/L_{(MOPAMP)}$	35.16	-	57.6	8	3.6 / 0.5

Figure 4-8 shows the replica circuit implemented in Virtuoso Cadence, the simulation of this sub-circuit and then its optimization (re-size of transistors) was made using the rest of the elements of Bias circuit (OTA and resistive voltage reference).

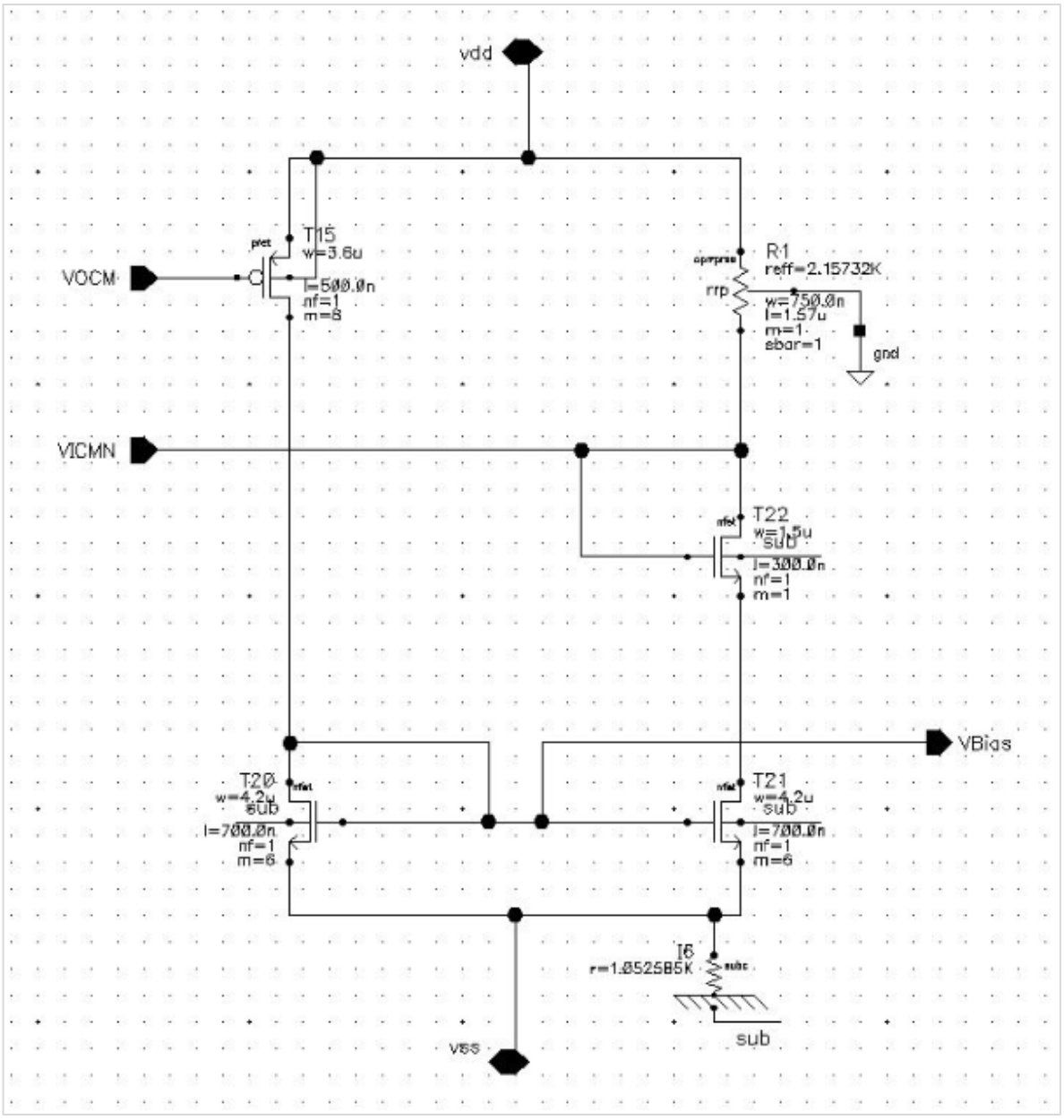


Figure 4-8 Replica circuit implementation.

4.4. Pre-Layout Verification of Assembled Bias circuit

Once two of the three elements of the Bias Circuit have been verified as separated circuits, it will proceed to validate the third one (Replica circuit), and consequently the whole functionality of the circuit, **Figure 4-9** shows the test bench which represents the join of the three blocks (Resistive Voltage Reference + OTA + Replica Circuit). In this circuit, the only stimulus

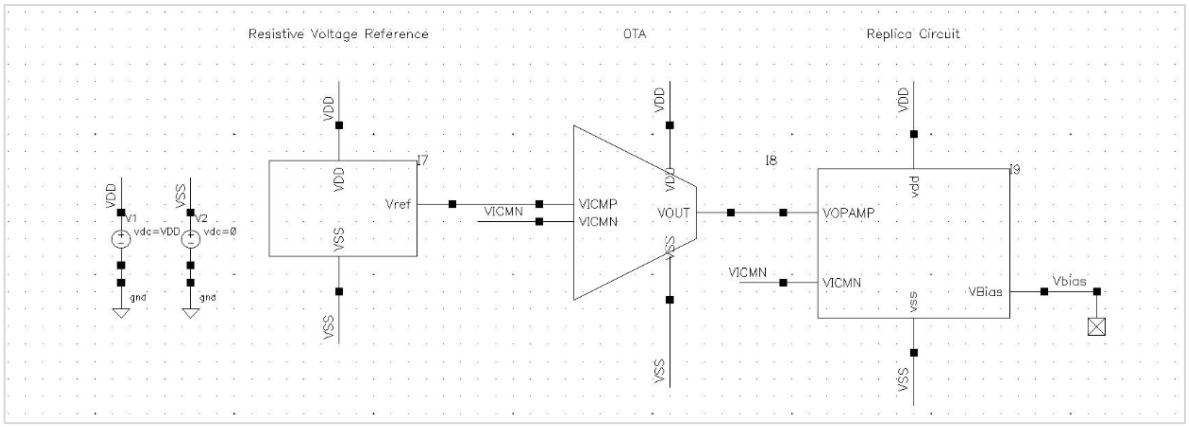


Figure 4-9 Bias circuit test bench.

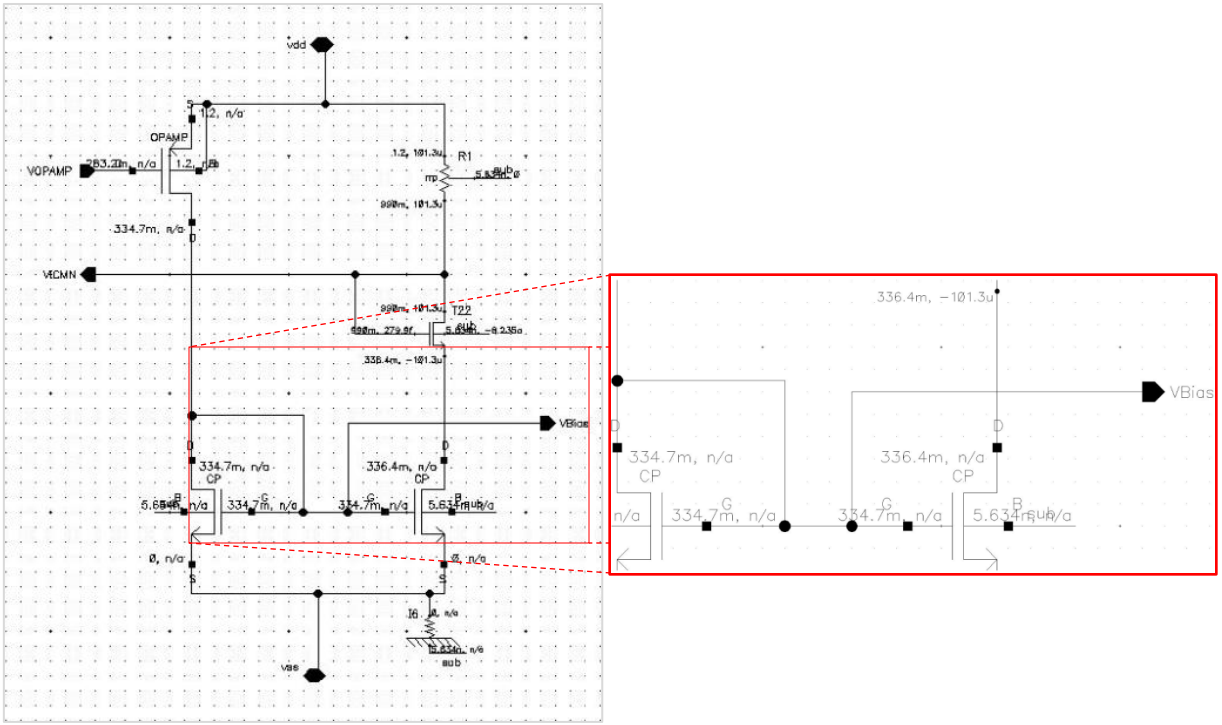


Figure 4-10 Replica circuit values after perform a transient analysis.

applied was VDD/VSS performing a DC analysis during 1us.

A non-connection pin has been placed at the output of the Replica Circuit (Vbias), this pin is the output of the submodule which provides the bias voltage to charge pump submodule. **Figure 4-10** shows the DC operating point values at Vbias node in the replica circuit after a transient analysis (steady state); as can be noted, by the current mirror effect, the two branches keep the same current value and the Vbias value. **Figure 4-11** and **Figure 4-12** show the transient response for Vbias voltage and current bias respectively, a short spike is observed in both cases during the initial activation, but after approximately 0.05µs the signals become stable. Values are shown below summarize the achievement of the assembled Bias circuit:

$$Required: \mathrm{I_B} = \mathbf{100\ \mu A} = \mathbf{I_B}' \qquad Verified: \mathrm{I_B} = \mathbf{I_B}' = \mathbf{101.28\ \mu A}$$

$$Required: \mathrm{Vbias} = \mathbf{335\ mV} \qquad Verified: \mathrm{Vbias} = \mathbf{334.66\ mV}$$

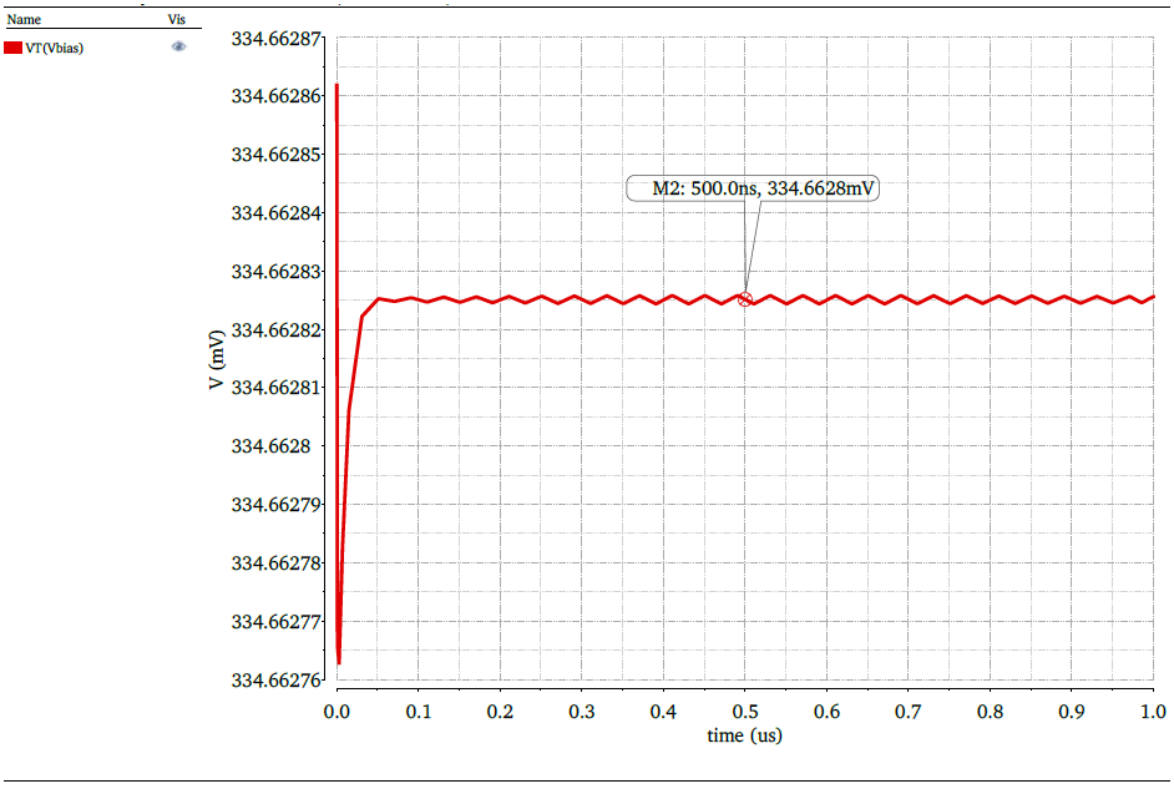


Figure 4-11 Bias voltage transient response.

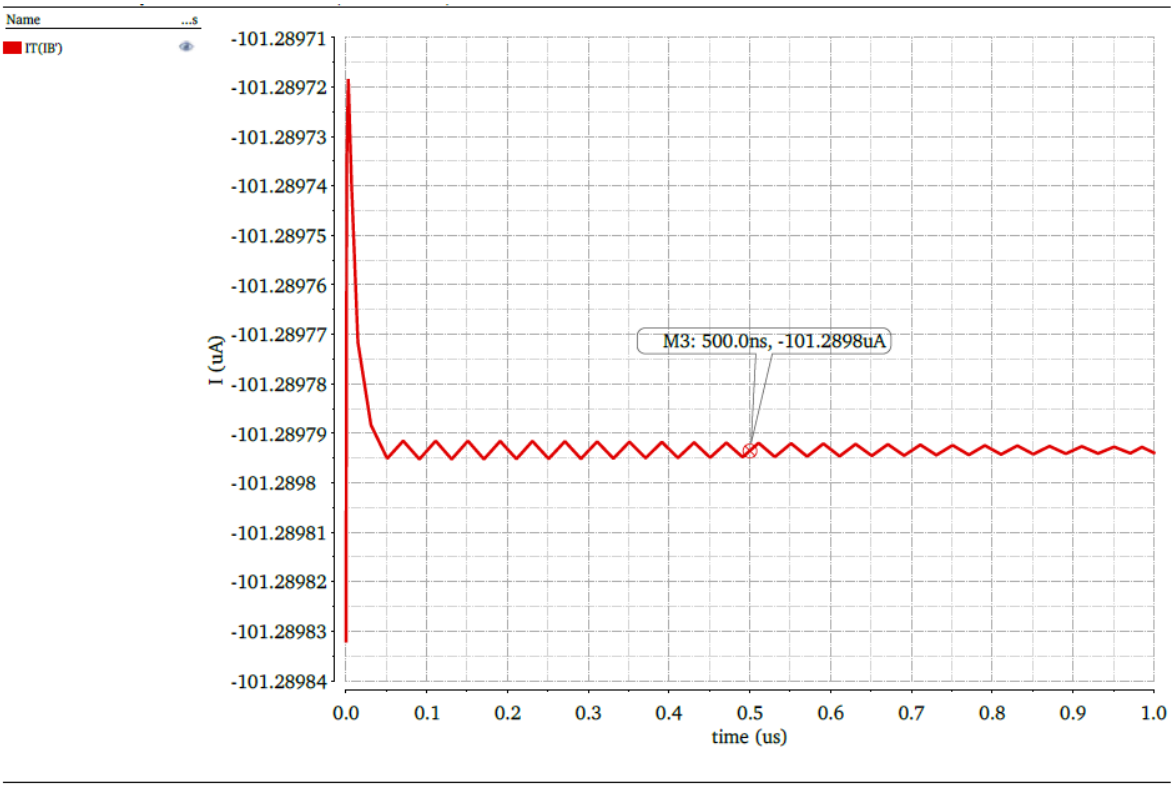


Figure 4-12 Bias current (I_B') transient response.

4.5. Pre-Layout Verification of Bias Circuit Integrated to CP Circuit

The last verification performed is the integration of the Bias circuit with the CP submodule. The way to obtain this verification is comparing the transient response of the CP (charge and discharge) using ideal current sources in contrast to the CP transient response using the Bias circuit at the transistor level. The CP circuit and test bench [12] observed in **Figure 4-13** were required for simulation purposes.

Simulation parameters in test bench are showed on **TABLE V**. **Figure 4-13** shows the dual-test bench. In this test bench, the CP Charge portion receives a differential clock signal on UP and UPN pins (this sources basically emulate the PFD performance circuit). Likewise, the CP Discharge portion receives the same differential clock signal but on DW and DWN pins. To perform a charge cycle is mandatory to enable an initial condition of 0V at the output of the

circuit (CL capacitor), to perform a discharge cycle the initial condition at the output now would be 1.2 V.

TABLE V
CP TEST BENCH SIMULATION PARAMETERS

Parameter	Value
CL	10 pF
VDD	1.2 V
VSS	0 V
VH	1.2 V
VL	0 V
Frequency	50 MHz
Rise Time	100 ps
Fall Time	100 ps

Inside the blocks showed in **Figure 4-13** are the CP circuit based on the topology showed in chapter 3, the **Figure 4-14** and **Figure 4-15** shows the CP circuit, the first one uses an ideal current source (100 µA) to produce a 336 mV (reference circuit) and, the second one uses the bias voltage circuit, the bias voltage circuit was instantiated in one block, the content of this block is observed in **Figure 4-16**.

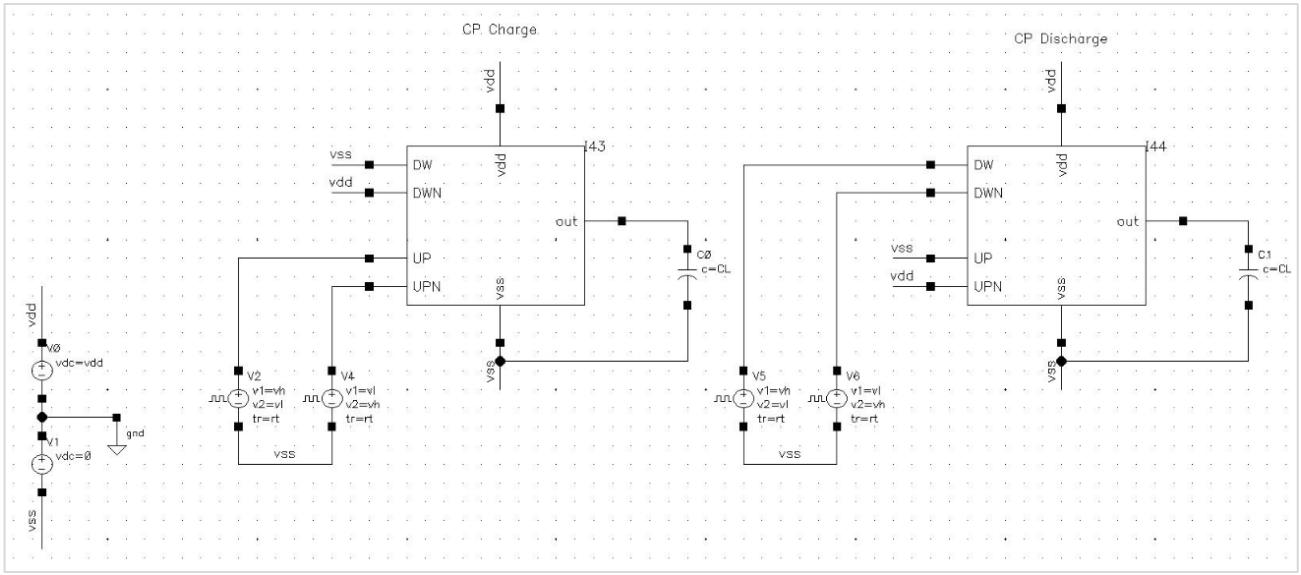


Figure 4-13 CP test bench.

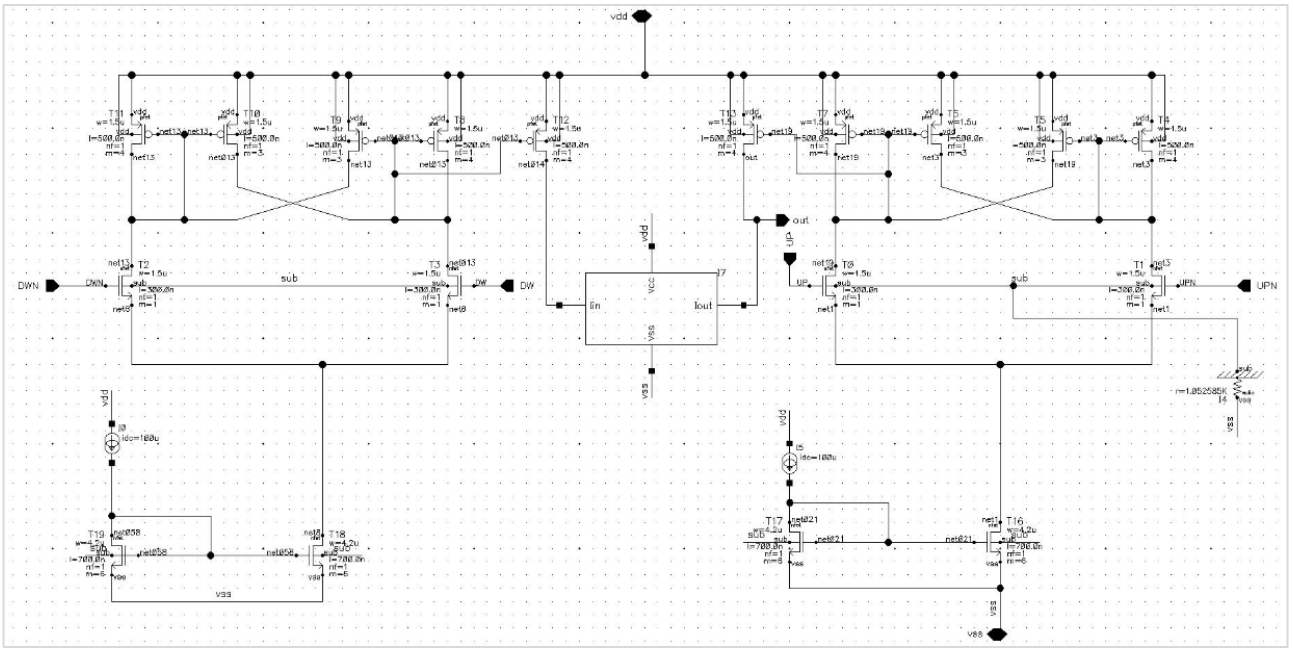


Figure 4-14 CP circuit (ideal source).

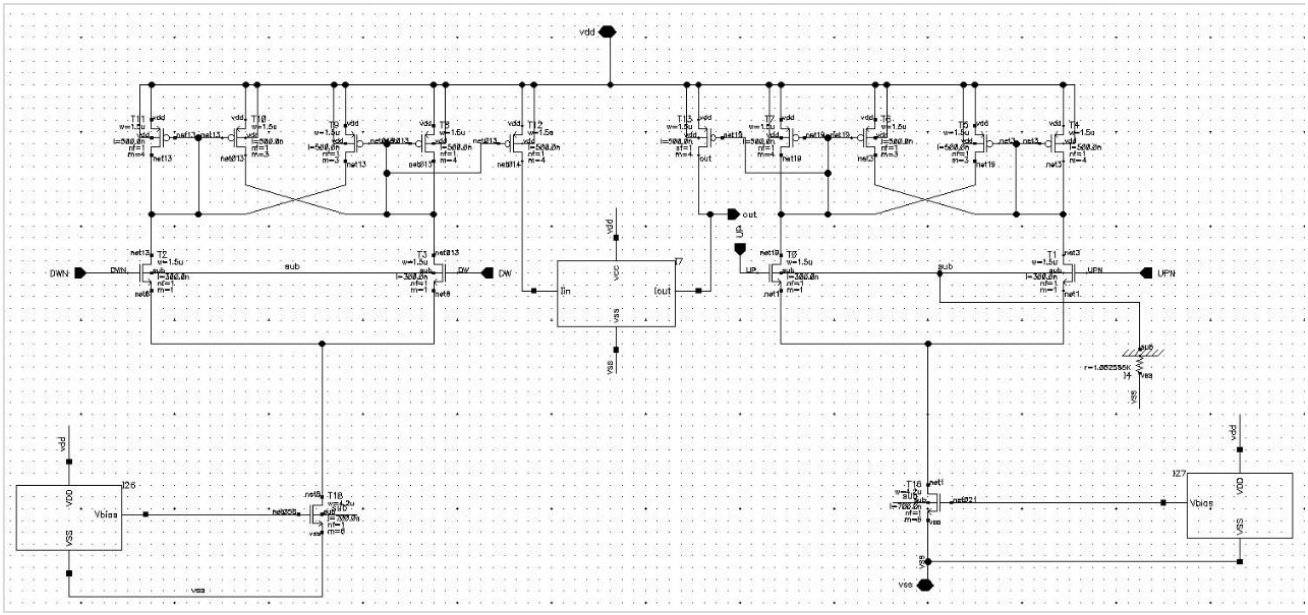


Figure 4-15 CP circuit (bias circuit).

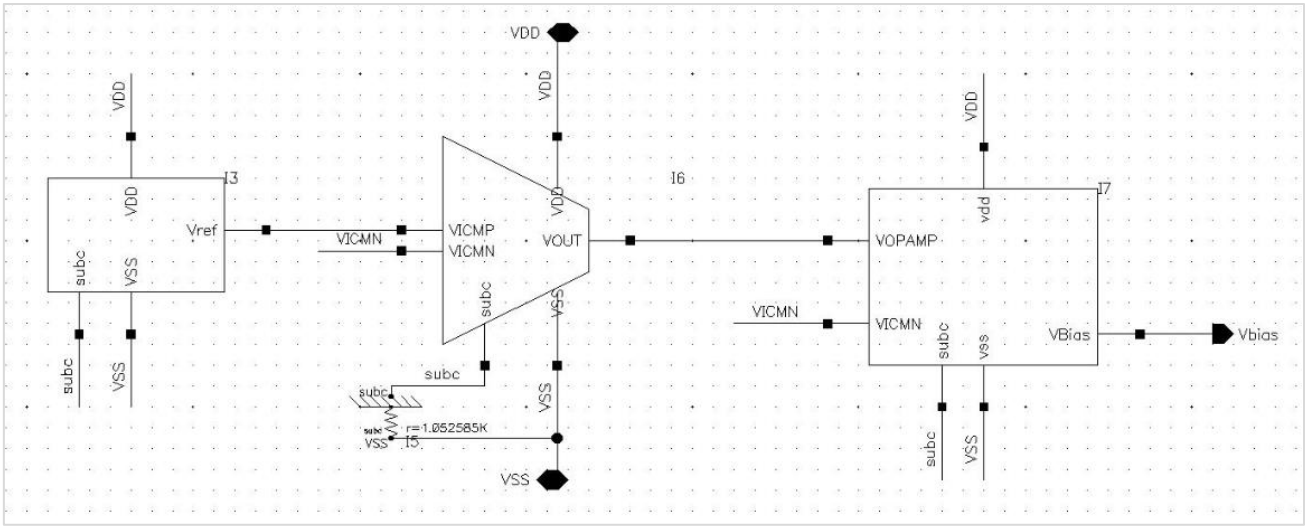


Figure 4-16 Bias circuit (portion instantiated).

The charging stage of CP circuit is observed in **Figure 4-17**, the red signal is the result of CP simulation using the ideal 100 μA source, while the yellow one is the curve generated with the Bias circuit. Notice that the difference observed between two curves is approximate of 6 mV which can be considered as acceptable since the reference signal which produces the bias voltage is an ideal source. A close view of charging steps can be observed in **Figure 4-18**. A similar behavior is observed during discharge stage of CP circuit (**Figure 4-26** and **Figure 4-20**), a minimum difference between the two compared signals (~6mV) confirms the expected performance of the Bias circuit for charge and discharge stage.

Finally, another important aspect to verify is the dynamic current drawn through the CP branches during switching interval; the current signal observed in **Figure 4-21** and **Figure Figure 4-22** is obtained from the drain current of **T0** transistor (refer to **Figure 4-15**) driven by the **UP** signal (**Figure 4-14**). Because of symmetry of circuit, its behavior is representative of the other three CP branches. The difference measured between the two circuits (~1 μA) confirms the expected performance during the CP switching current.

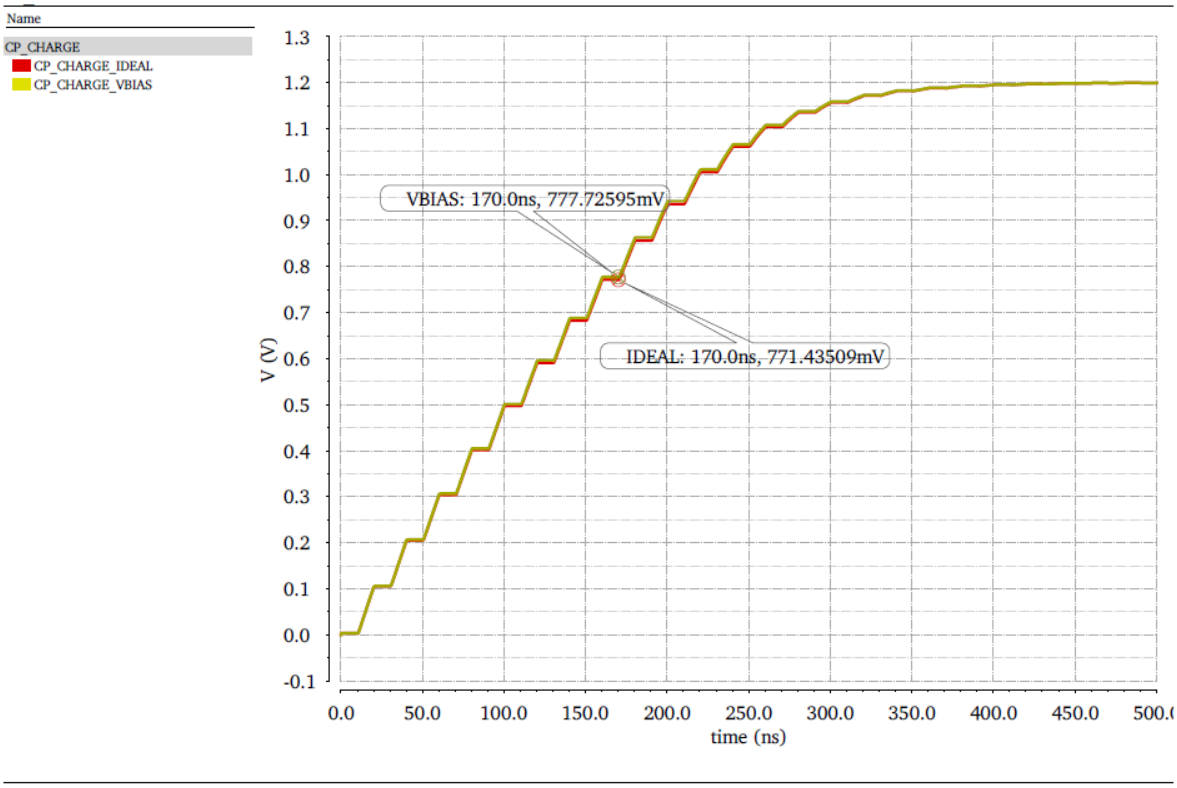


Figure 4-17 CP charge stage.

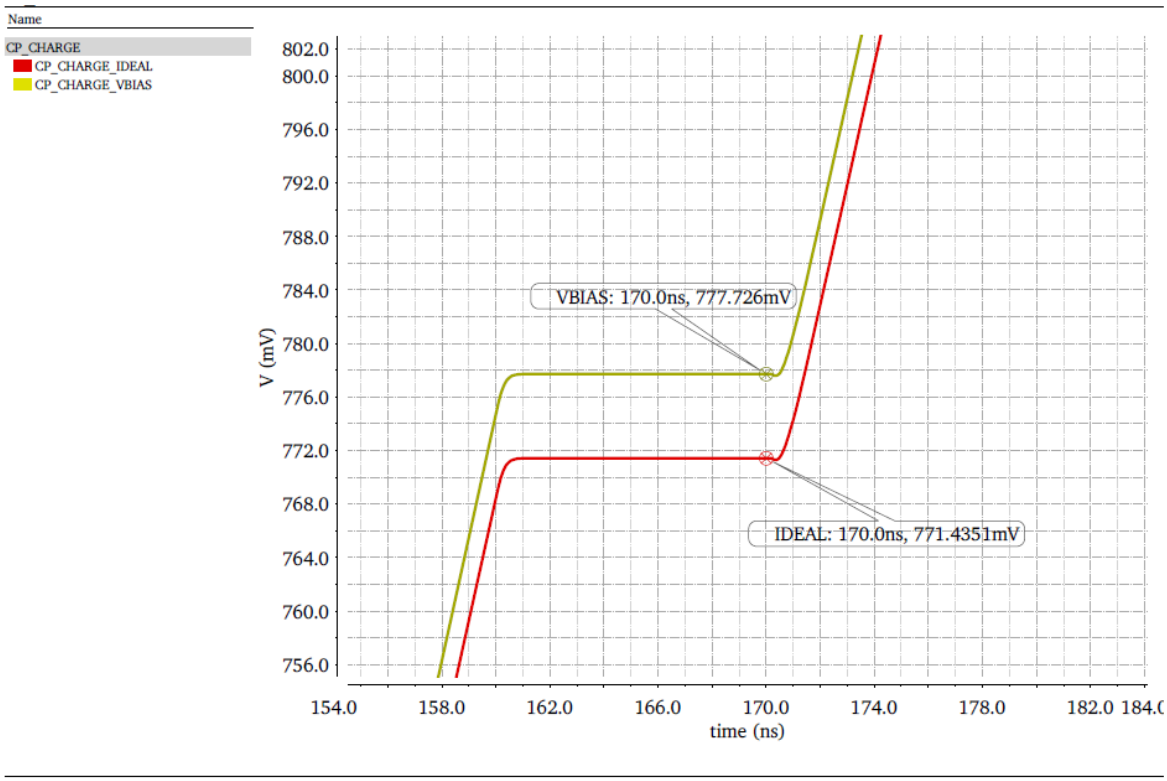


Figure 4-18 CP charge stage close view.

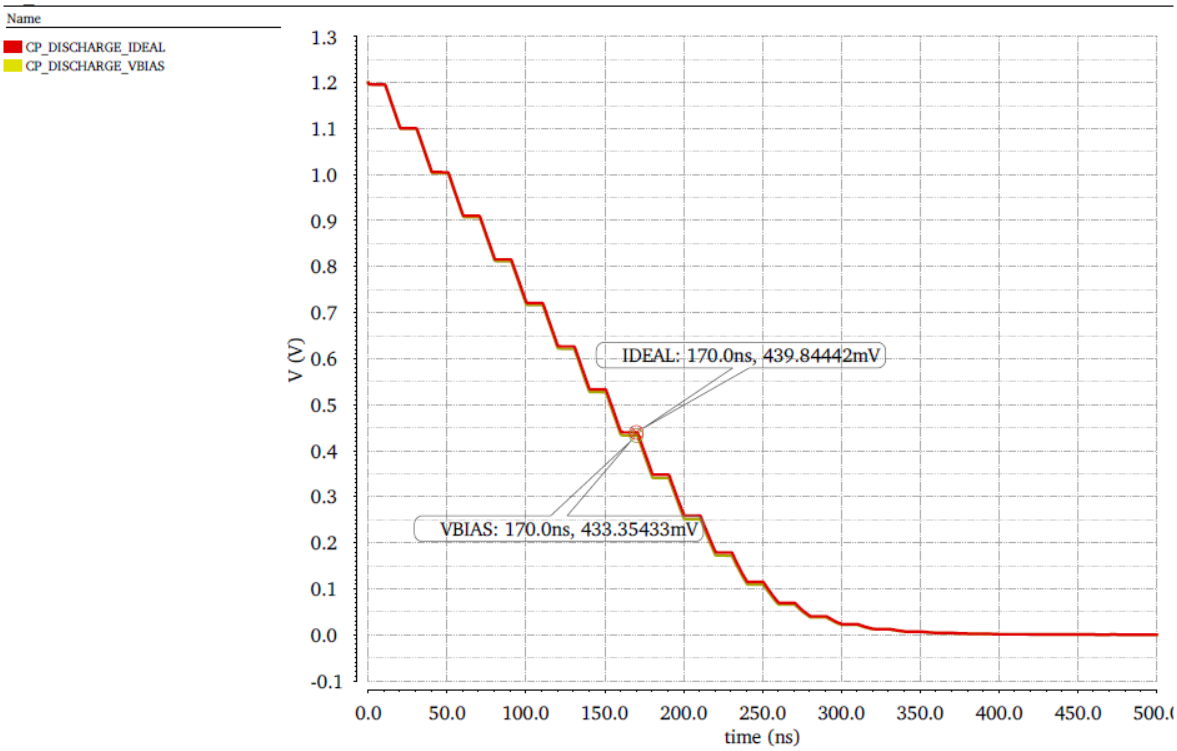


Figure 4-19 CP discharge stage.

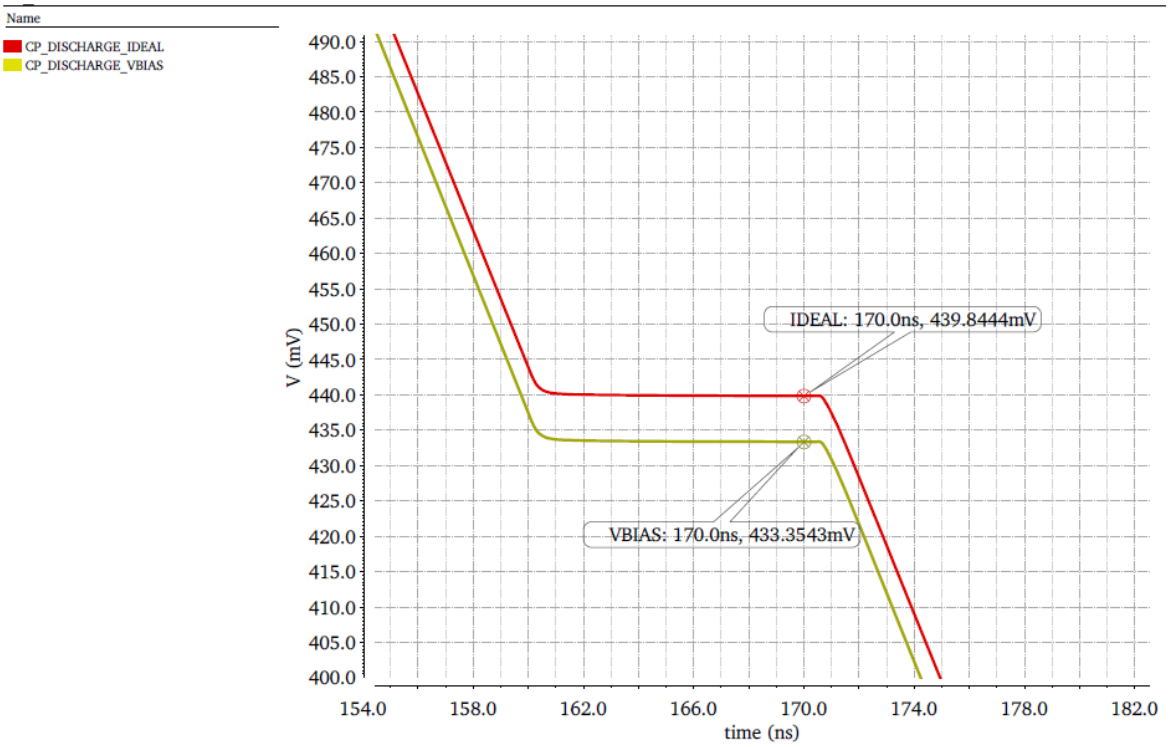


Figure 4-20 CP discharge stage (close view).

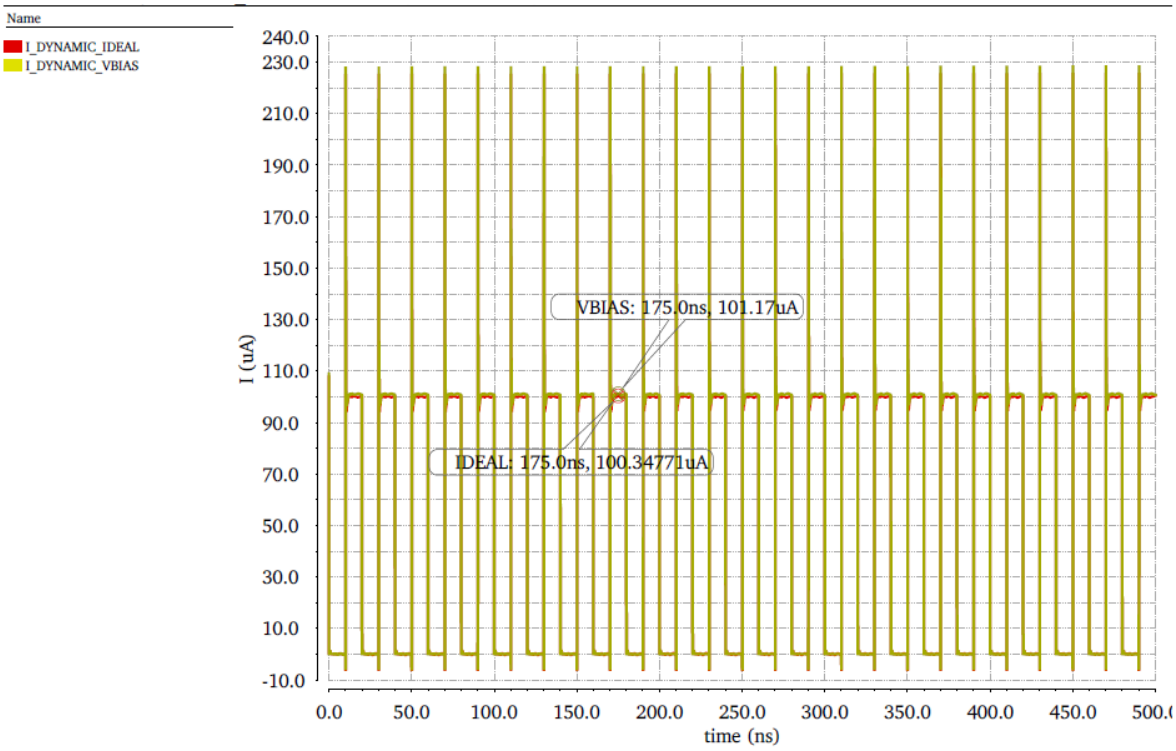


Figure 4-21 CP branch dynamic current.

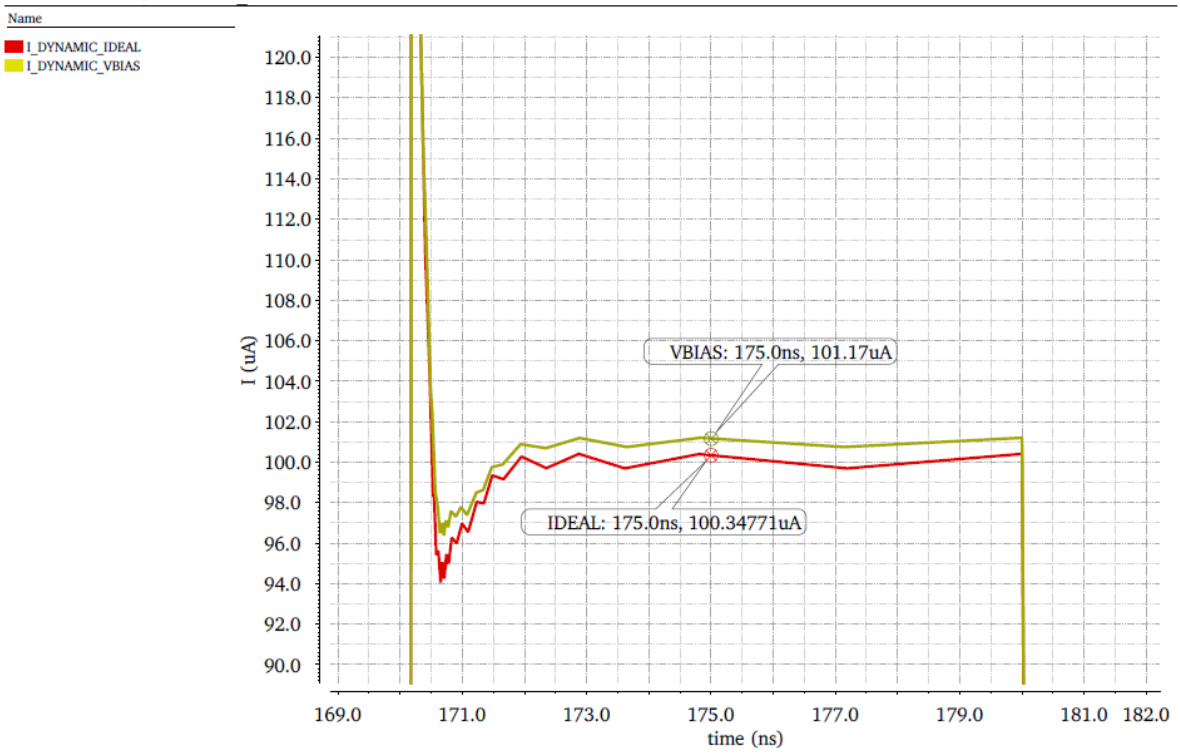


Figure 4-22 CP branch dynamic current (close view).

4.6. Bias Circuit Pre-Layout Verification (PVT)

After verification of the Bias circuit with typical values of BiCMOS process parameters and room temperature was completed then, it is mandatory to perform a process corner to verify the robustness of the design. By this, the combination of PVT (Process, Voltage, and Temperature) corners showed at **TABLE VI** was performed to OTA circuit and to the assembled Bias circuit.

TABLE VI
REPLICA CIRCUIT DESIGN PARAMETERS

Process	Temperature	Voltage
Typical (nom)	27 °C	1.2 V
Fast-Fast (ff)	120 °C	1.26 V
Slow-Slow (ss)	120 °C	1.26 V
Fast-Fast (ff)	-40 °C	1.14 V
Slow-Slow (ss)	-40 °C	1.14 V

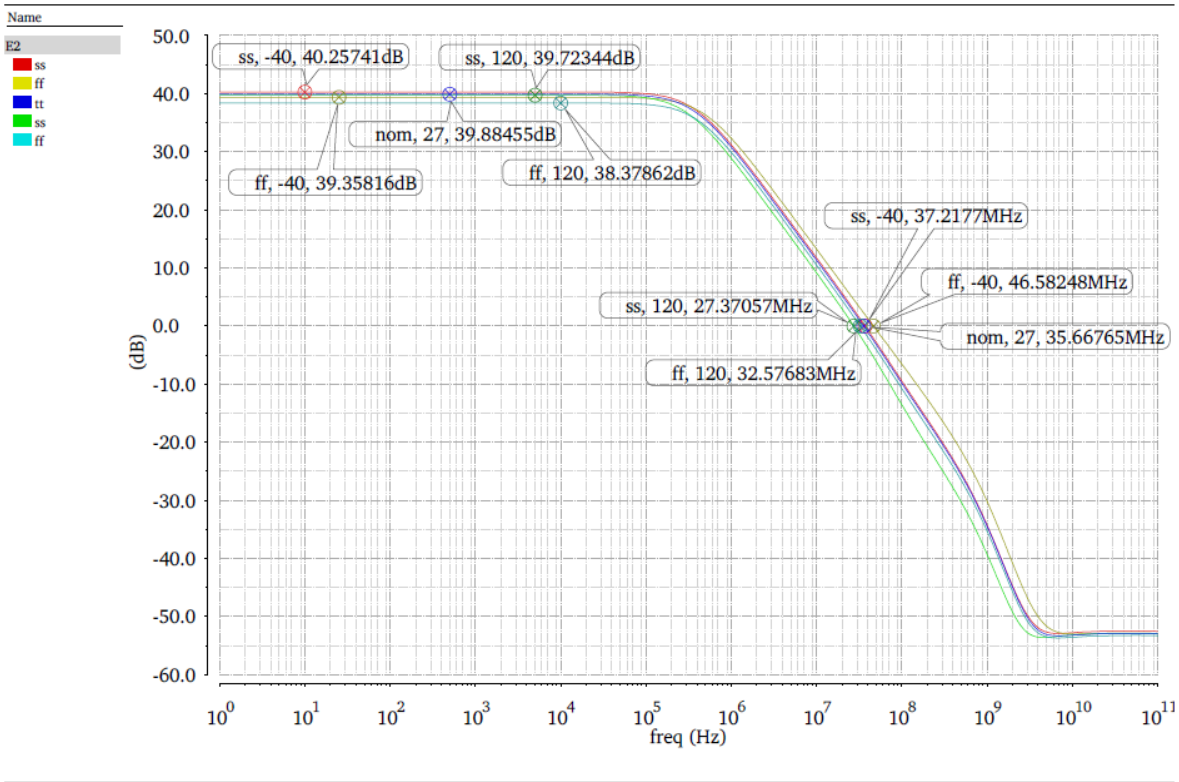


Figure 4-23 OTA PVT AC response.

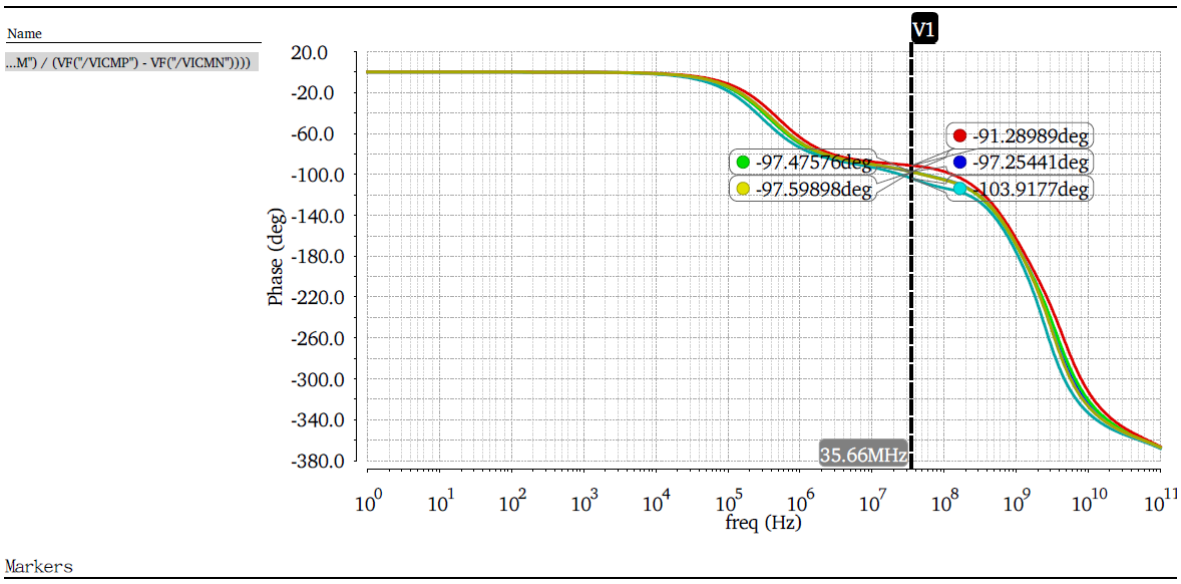


Figure 4-24 OTA phase PVT AC response.

Here we show some representative results. On **Figure 4-23** and **Figure 4-24** we present the AC response of OTA under various PVT corners. Worst case for voltage gain was observed on ff process at 120 °C and also a worst case for GBW is observed on ss process at -40°C, Regarding the transient response of OTA (**Figure 4-25**), the worst case was observed on ff corner at 120°C/1.26V (see green curve on **Figure 4-25**). The rest of PVT corners can be consulted in the Appendix D section.

The PVT corners resulting from the Bias circuit during transient response are shown in **Figure 4-26**, this plot shows the worst case on ff corner at 120°C/1.14V. The variation observed in Vbias value transient response is lightly above than expected value (> 10%), therefore a new PVT corners simulation was performed using the assembled sub-modules (CP-Bias circuit) and no degradation effect was detected on CP performance. **Figure 4-28** shows the PVT corners of the integrated submodules during CP charge stage, here a worst case is observed on ff at 120°C/1.26V, the indicated variation between nominal and corner values reaches barely 10%, this result is taken as acceptable. **Figure 4-27** shows a similar behavior during CP discharge stage. A sensitivity analysis would provide a certain evaluation about the contribution of sources observed at the circuit output, this analysis is not presented in this work, and the integrated interaction of CP-Bias circuit was taken as valid due to the final application.

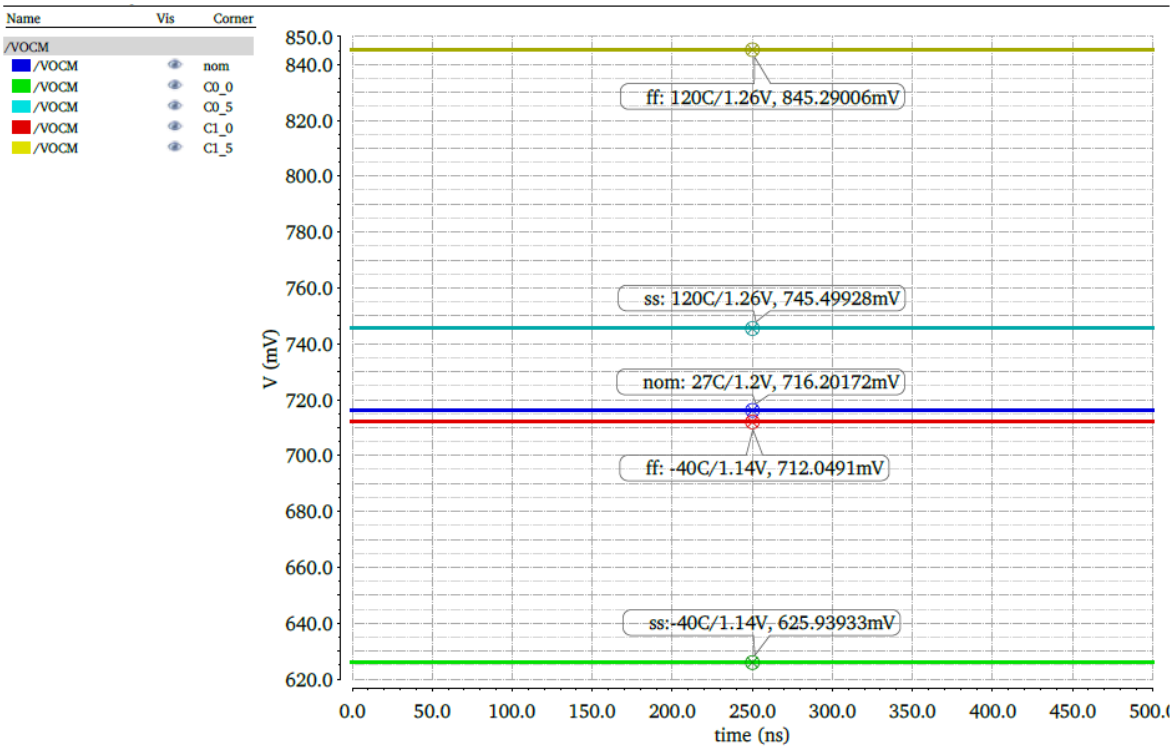


Figure 4-25 OTA PVT transient response.

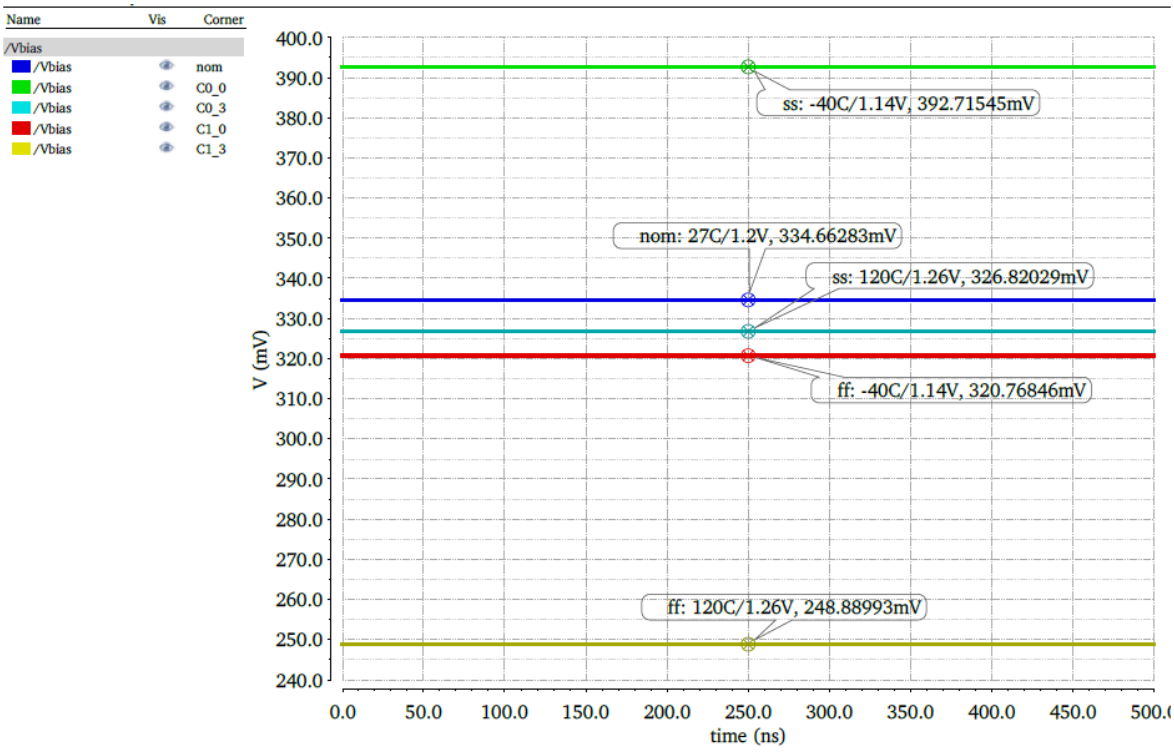


Figure 4-26 Bias circuit PVT transient response.

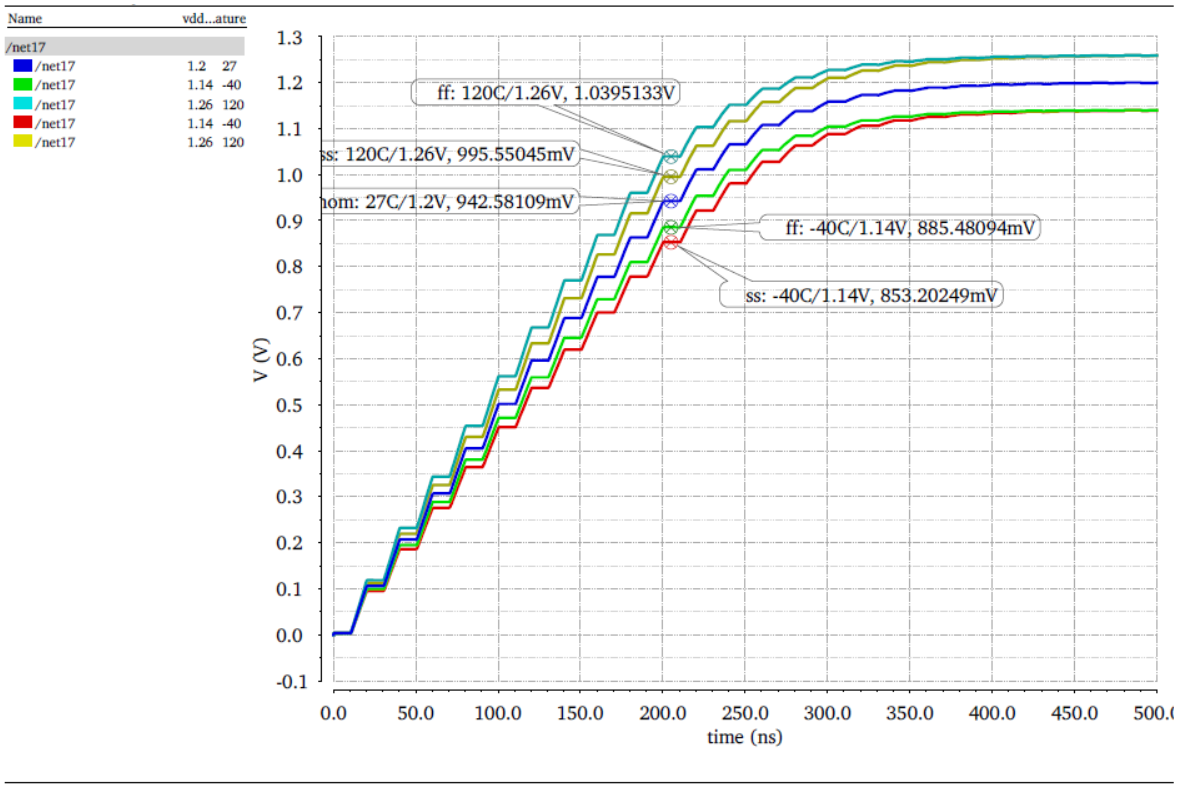


Figure 4-28 CP circuit charge stage PVT.

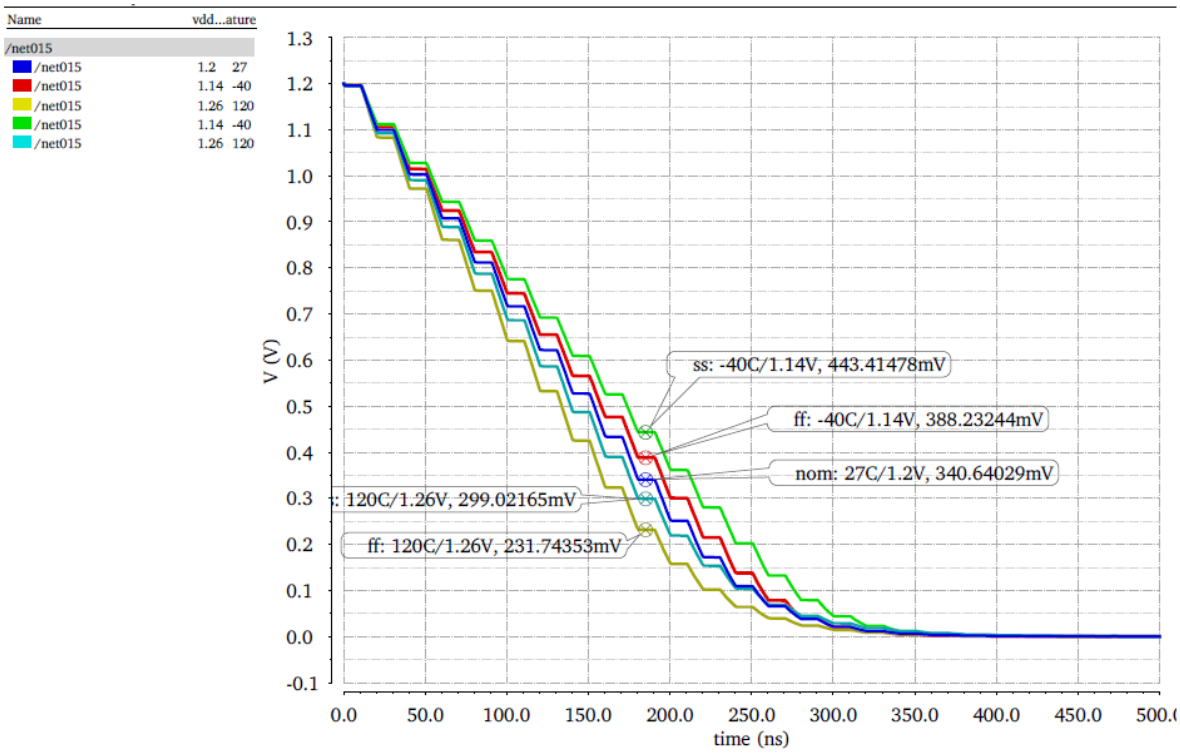


Figure 4-27 CP circuit discharge stage PVT.

5. Bias Circuit Layout Design

To reduce mismatch effects in the circuit, in the Bias circuit layout design, the inter-digitization layout technique was used since this technique in addition to reducing the S/D junction area (and consequently parasitic capacitances and gate resistance) it averages the electrical properties of the material. **Figure 5-1** shows the concept of inter-digitization layout technique, where two wide transistors (A and B) are split into an equal part of fingers, and then placed in an alternated arrange.

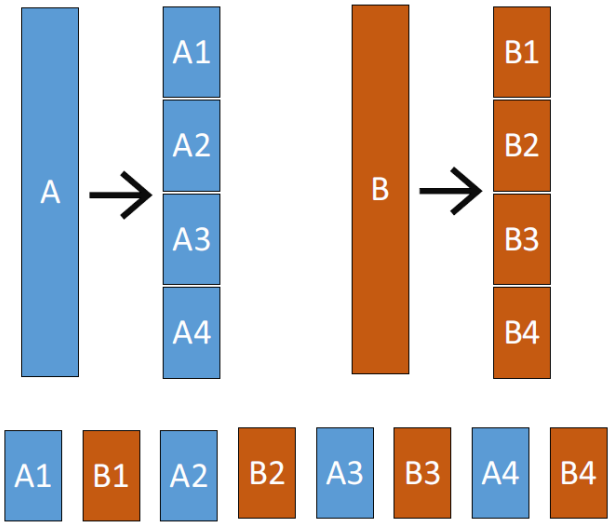


Figure 5-1 Inter-digitization layout technique.

5.1. OTA Layout Design

In consideration of inter-digitization layout technique, first transistors of the OTA circuit were split to interdigitate them, **TABLE VII** shows the final adjusted sizes for OTA layout design. Notice that the multiplicity factor is indicated to keep the size relation between W and L. Then, the ideal devices such as current source resistor', and miller capacitor were replaced by OPRRPRES cell resistor and DUALMIM cell capacitor from BiCMOS technology. To replace the current source, the voltage drop at current mirror node was considered taking the I_B value as follows in Ec. **(5-1)**:

$$R_B = \frac{V_B}{I_B} = \frac{689\ mV}{25.132\ \mu A} = 27.452\ K\Omega \tag{5-1}$$

TABLE VII
130nm FINAL OTA LAYOUT PARAMETERS

Parameter	Final Value (µm)	Adjusted Layout Value (µm)	Multiplicity
$L_{(All\ Transistors)}$	0.320	0.32	N/A
$W_{1,2}$	1.3	0.65	2
$W_{3,4}$	2.4	0.60	4
W_5	9.12	0.65	14
$W_{MB1,MB2}$	0.720	0.74	1
W_{MB3}	1.35	0.59	2

Figure 5-2 and **Figure 5-3** shows the final OTA circuit implementation and Layout respectively; as can be noticed in **Figure 5-3**, in this layout, more than a half area is utilized by dual mim capacitor device.

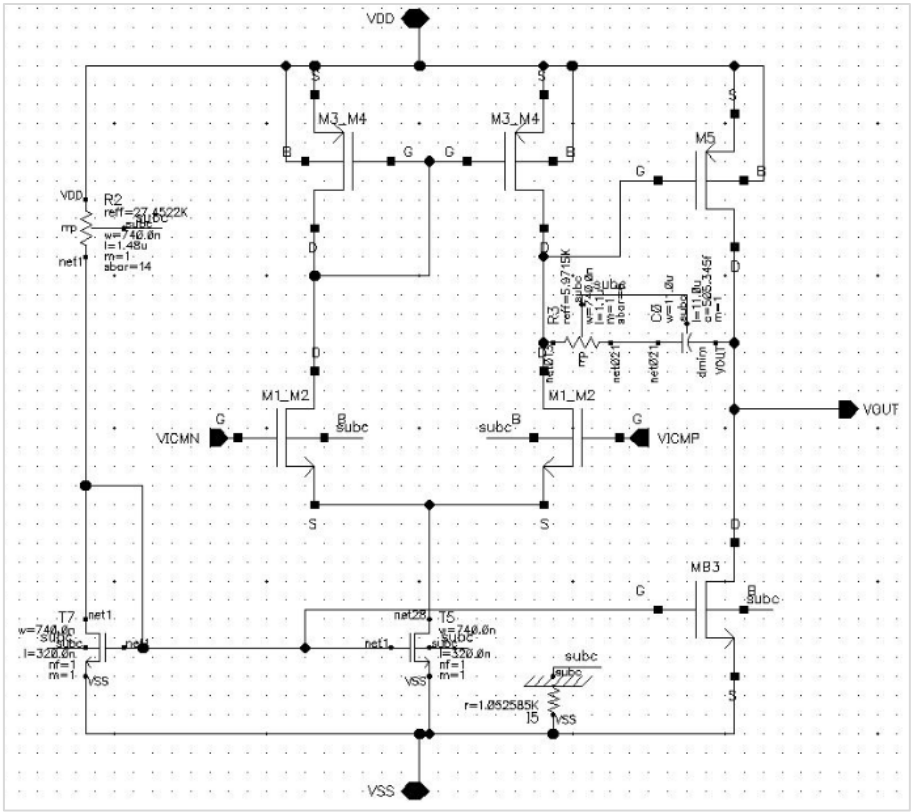


Figure 5-2 Final OTA circuit adapted for Layout.

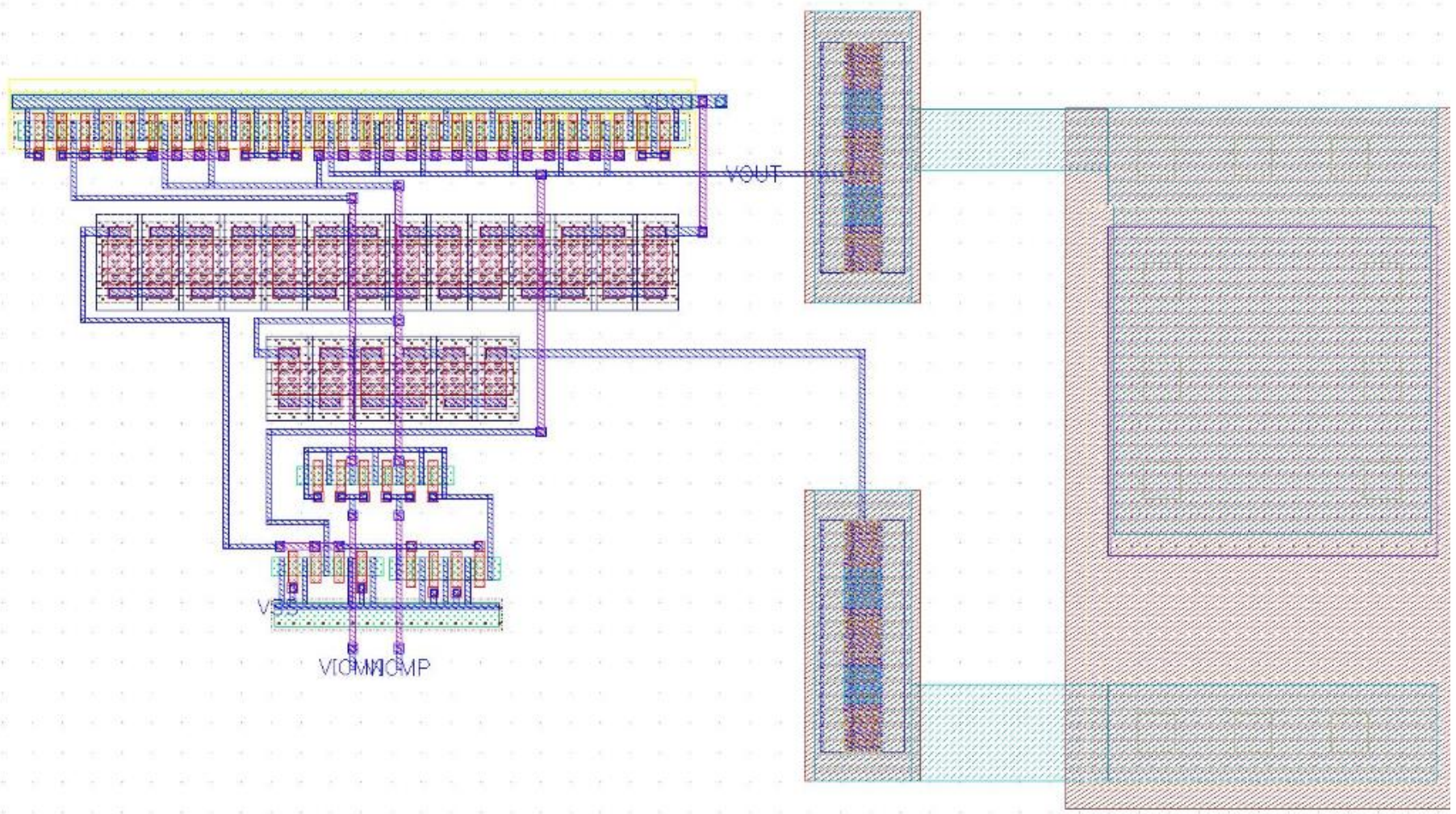


Figure 5-3 OTA layout design

5.1. Resistive Voltage Reference Layout Design

The resistive voltage reference layout is shown in **Figure 5-4**. The 28 serial resistors were placed taking care of creating a square figure, input/outputs pins are on the same side for flexibility purposes.

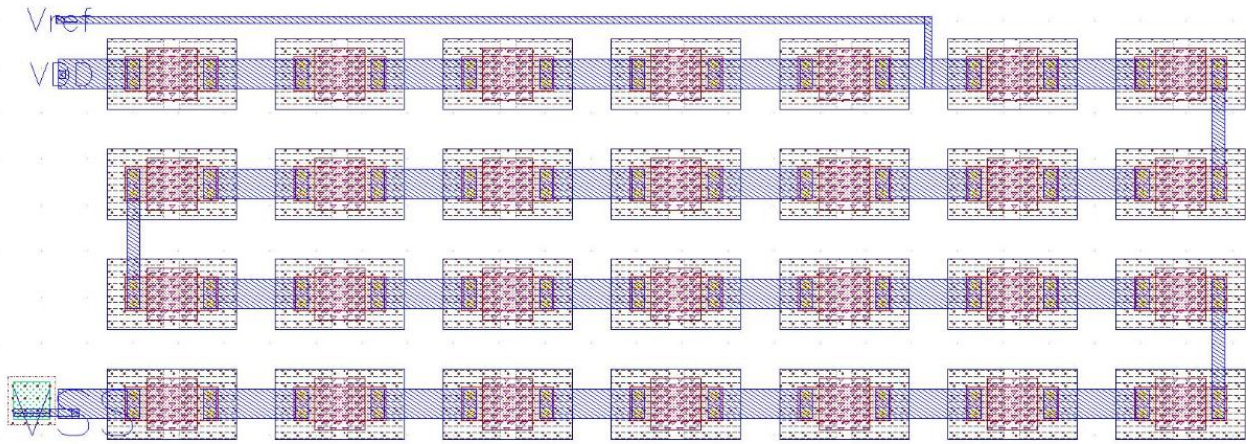


Figure 5-4 Resistive voltage reference layout

5.2. Replica Circuit Layout Design

Figure 5-5 shows the replica circuit layout, inter-digitization layout technique was also applied on this design, particularly at the current mirror transistors in order to reduce the mismatch effect. The location of input/output pins was previously considered for the integration of each part of the Bias circuit.

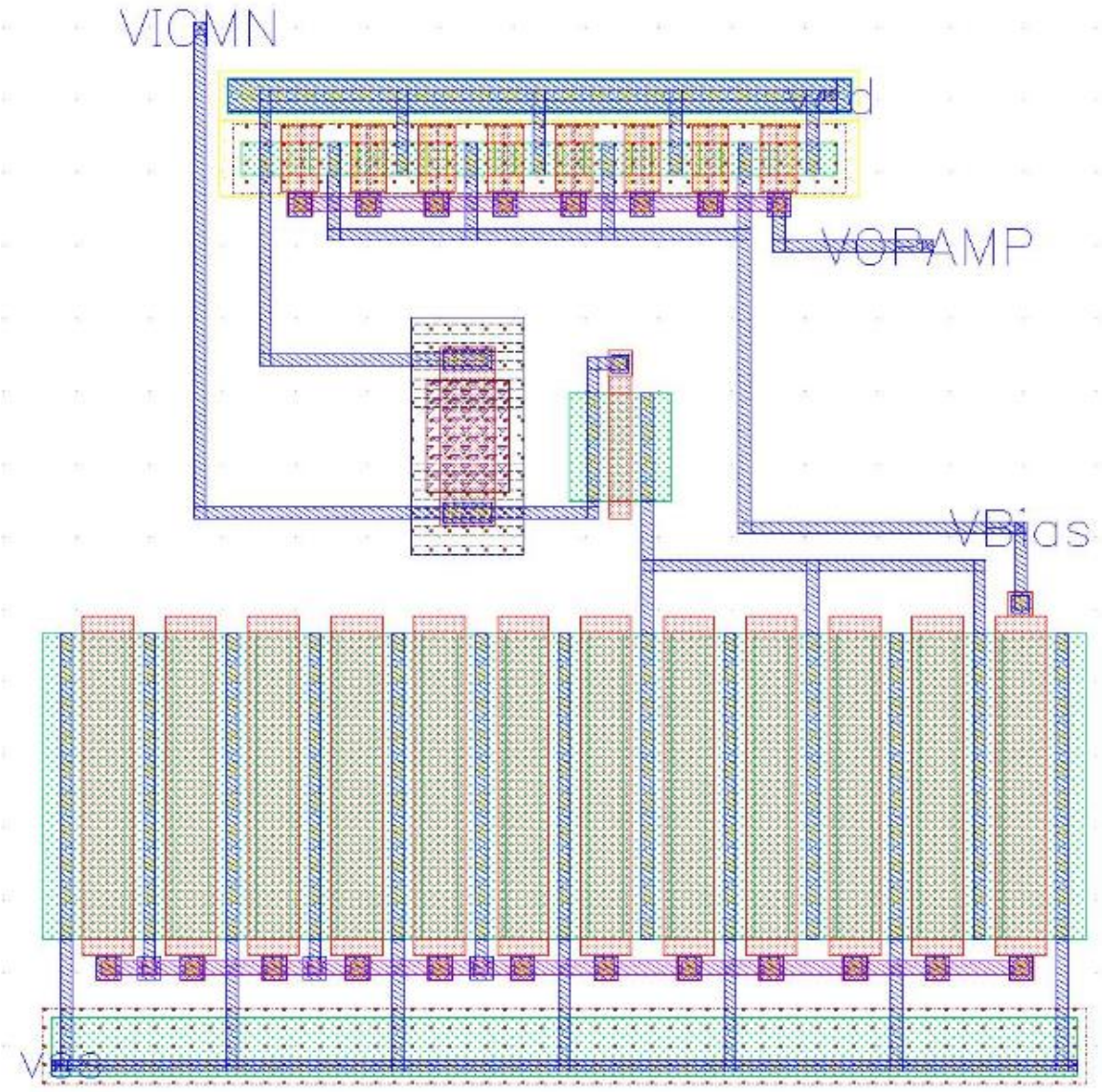


Figure 5-5 Replica circuit layout

5.3. Assembled Bias Circuit Layout Design

The assembled Bias circuit Layout is observed in **Figure 5-6**, the final dimension of this block was **49.15 x 52.65µm** (width x length) which results in **2587.74µm^2**. For the final PLL sub-module integration, this layout will be replicated to be placed in each of the CP branches.

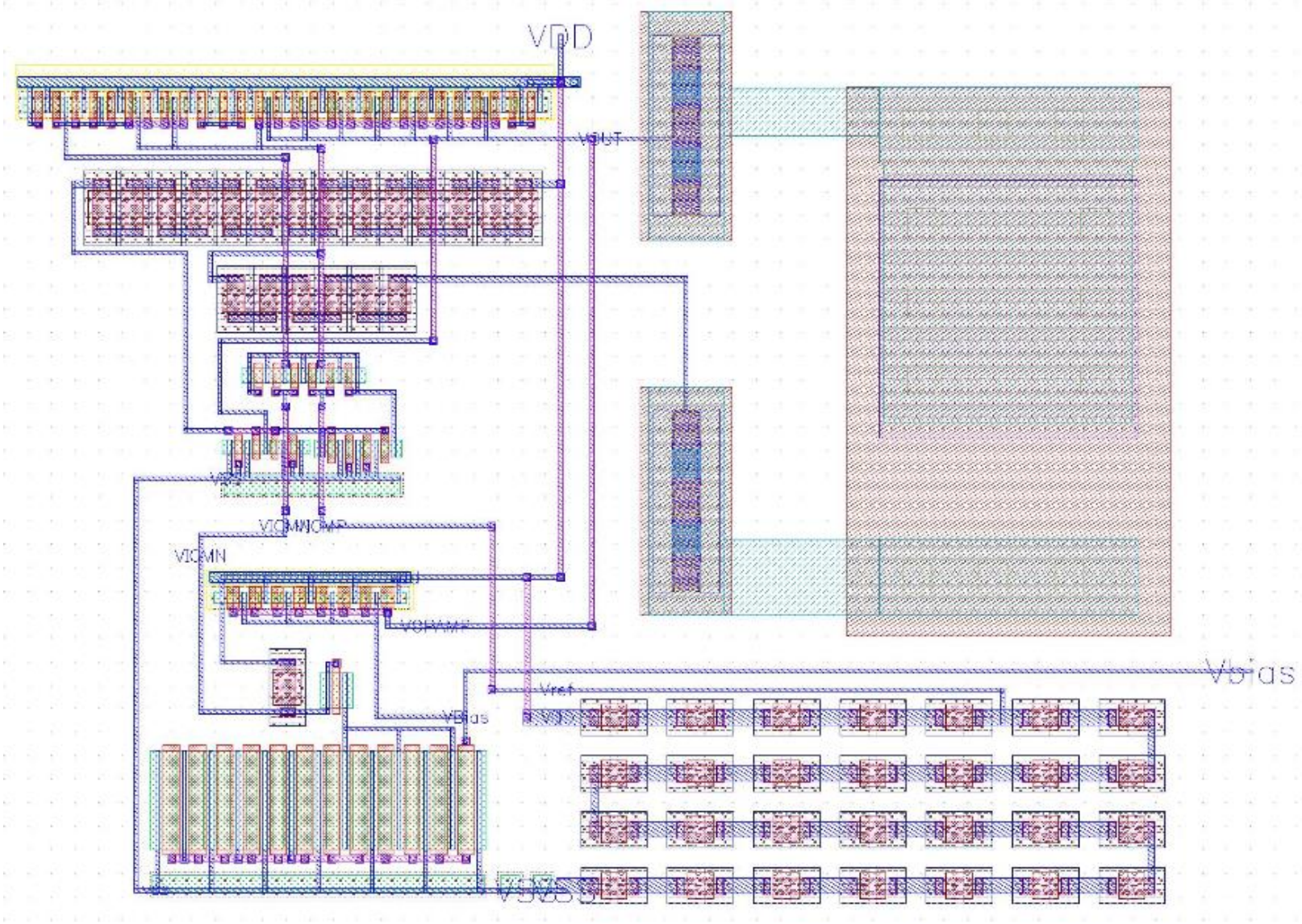


Figure 5-6 Assembled Bias circuit layout

6. Bias Circuit Post-Layout Verification

The assembled Bias circuit layout design was verified through the single set of design rules provided by Assura of Cadence. To perform the layout verification and parasitic extraction process the following tools were used: DRC (Design Rule Checking), LVS (Layout Versus Schematic), and QRC (Quantus Resistive-Capacitive).

6.1. DRC Assembled Bias Circuit Verification

The DRC verification allowed the evaluation of different design features, in the Bias circuit layout design the following DRC sub-classes were considered:

- DRC-Main. To check the dimension of interconnection and spacing between layers and devices.
- DRC-Antenna. To avoid antenna effect on interconnection lines.
- DRC-Density. To check uniform material (poly and metals) density across the chip for manufacturing requirements
- DRC-ESD. To check electrostatic discharge design rules.

Figure 6-1 shows an example of the resulting reports after performing each of the indicated DRC categories:

```
********************************************************************************

                  Assura Summary Report
@(#)$CDS: aveng_64 version av4.1:Production:dfII6.1.6-64b:IC6.1.6-64b.500.13.2 12/23/2015 11:53 (sjfnl732) $
sub-version 4.1_USR5, integ signature 2015-12-23-1118

run on fv00 from /media/Ext/sfw/ASSURA41/tools.lnx86/assura/bin/64bit/aveng on Mon Jul 23 21:06:53 2018
********************************************************************************

                  Run Summary

Total cells checked = 1
Total rules checked = 14282

Run time =  4.00 seconds
CPU time =  2.59 seconds
VM HWM   =  2334 Mbytes
Disk HWM =     0 Mbytes
Disk end =     0 Mbytes
Eman HWM =     0 Mbytes

                  End of Summary Report

********************************************************************************
```

Figure 6-1 Assura DRC summary report on assembled Bias circuit.

6.2. LVS Assembled Bias Circuit Verification

For the Bias circuit, the LVS verification confirmed the matching between the schematic view and layout view. In this checking, information, nets, devices, and parameters between schematic and layout were compared to detect rule errors. After fixing the emerged issues, the Virtuoso layout editor sends a message that confirms the correct evaluation (see **Figure 6-2**).

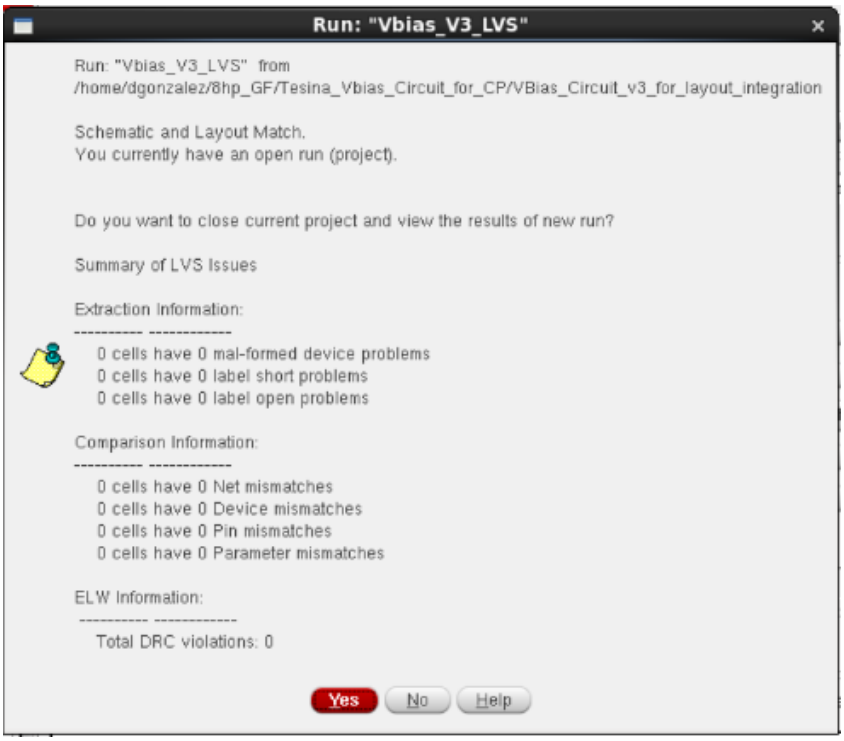


Figure 6-2 Assura LVS successful evaluation message.

6.3. QRC Assembled Bias Circuit Verification

The latest verification for Bias circuit is the parasitic extraction, the use of QRC allowed to extract all effects of parasitic devices (capacitor, resistors, and inductors), which could be merged with the original netlist. In other words, all parasitics are not designed but they are present, therefore must be taken into consideration.

Figure 6-3 shows the extracted view resulting from the QRC. This view will be used in performing the post layout simulation to compare the pre- and post-layout simulation results.

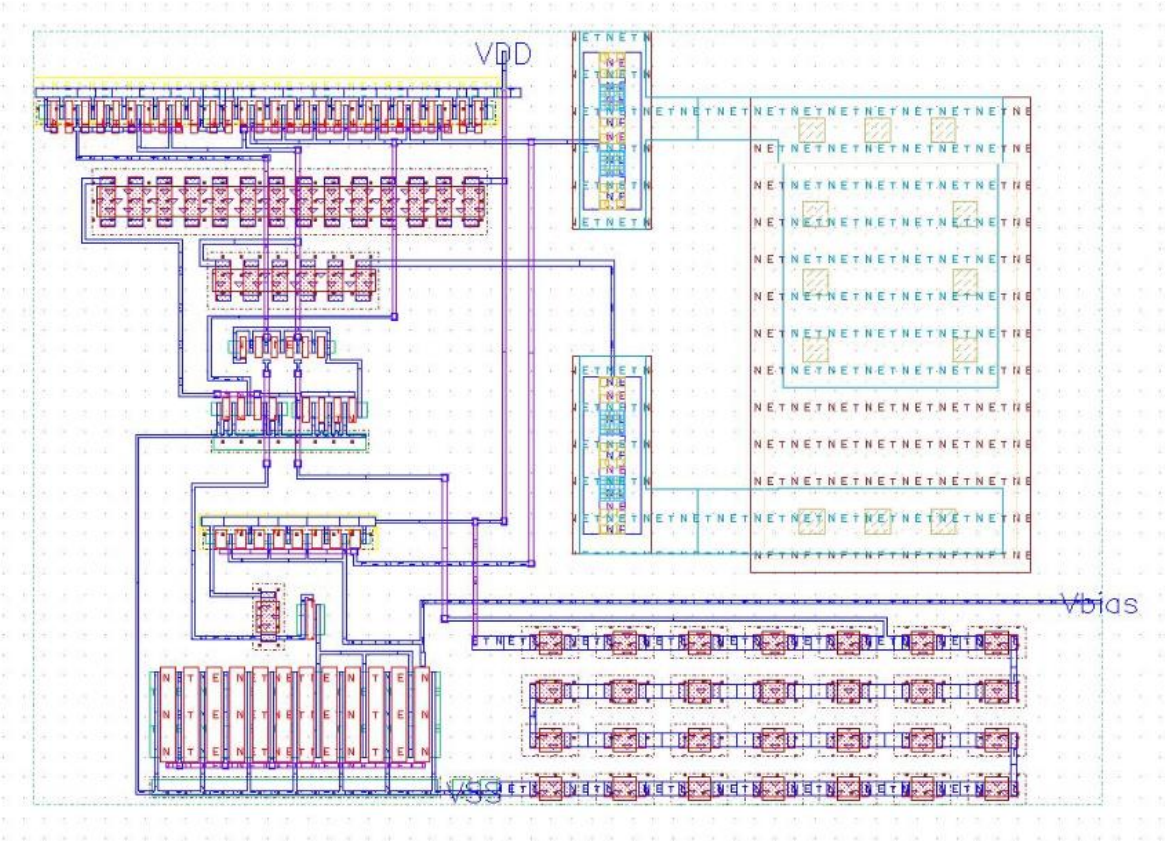


Figure 6-3 Extracted view from QRC.

6.4. Post Layout OTA Circuit Verification

After layout design rule verification, the performance of the OTA circuit is evaluated using the test-bench observed in **Figure 6-5**. In this test-bench, the pre and post layout OTA circuits are evaluated to compare the DC and AC response. **Figure 6-4** shows the transient response for VOCM signal, a difference of **39.08 mV (-5.45%)** is observed after layout optimization.

The AC response comparison is observed in **Figure 6-6**, a gain difference of **1.09 dB (-2.75 %)** is the final achievement after layout optimization. In regards to the phase (**Figure 6-7**), there are no differences between the pre and post layout plots.

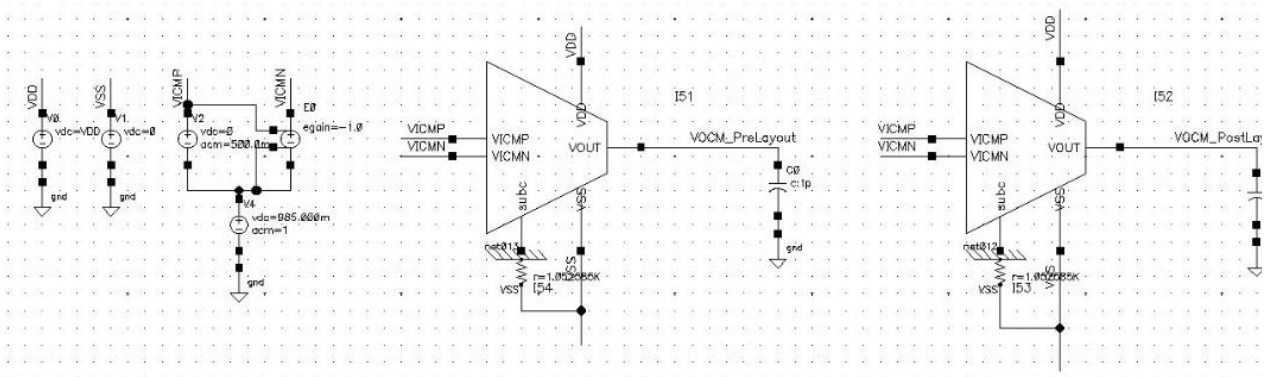


Figure 6-5 Two stage OTA test bench for post-layout verification.

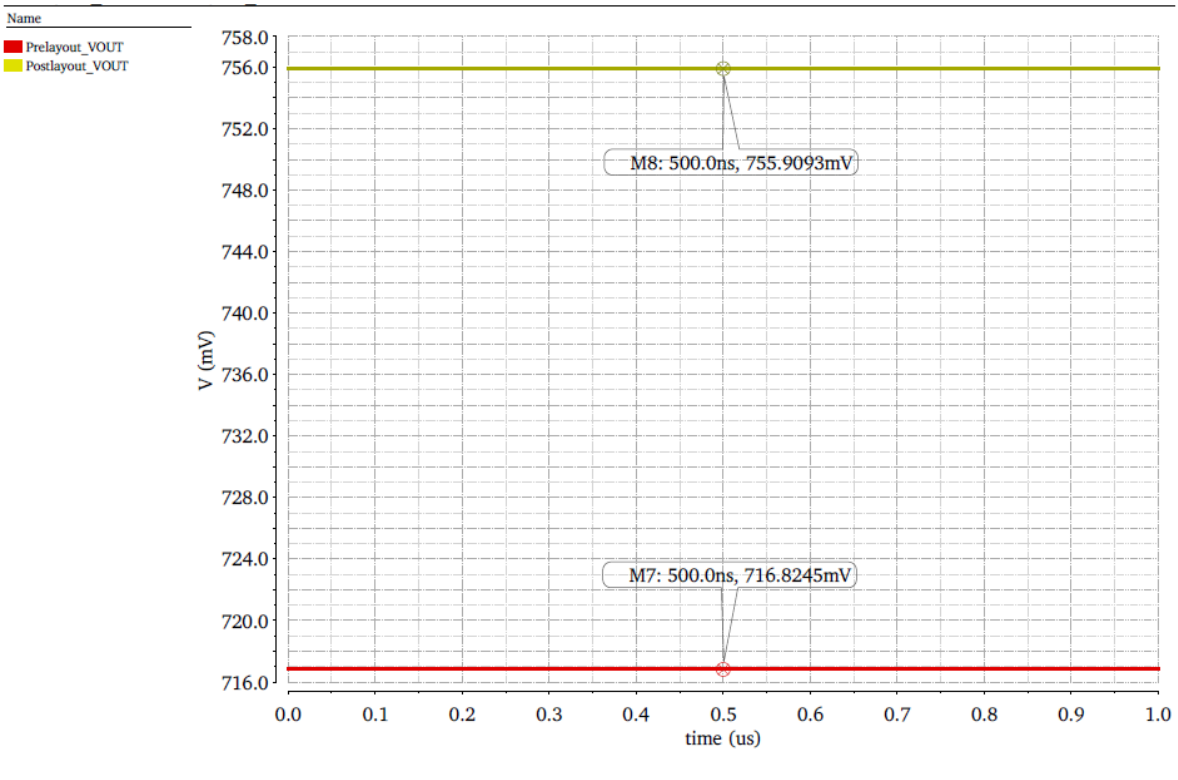


Figure 6-4 Two stage OTA VOCM signal pre and post layout comparison.

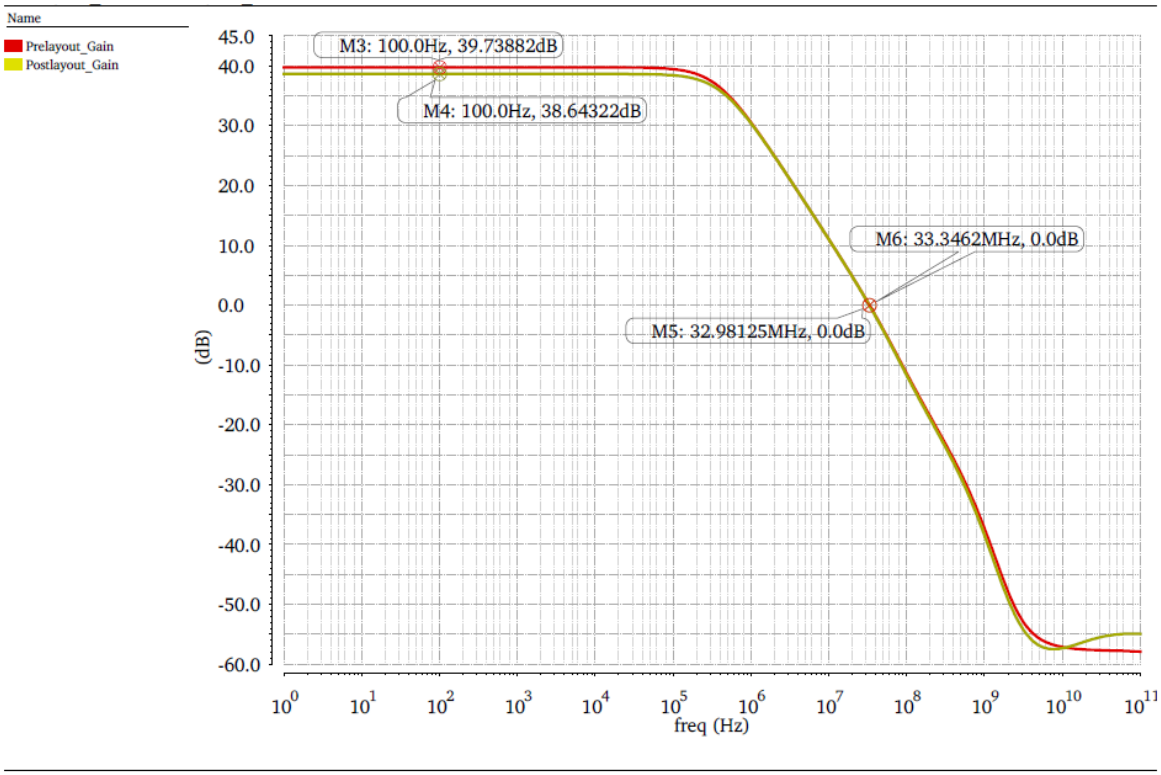


Figure 6-6 OTA pre and post layout comparison for AC response.

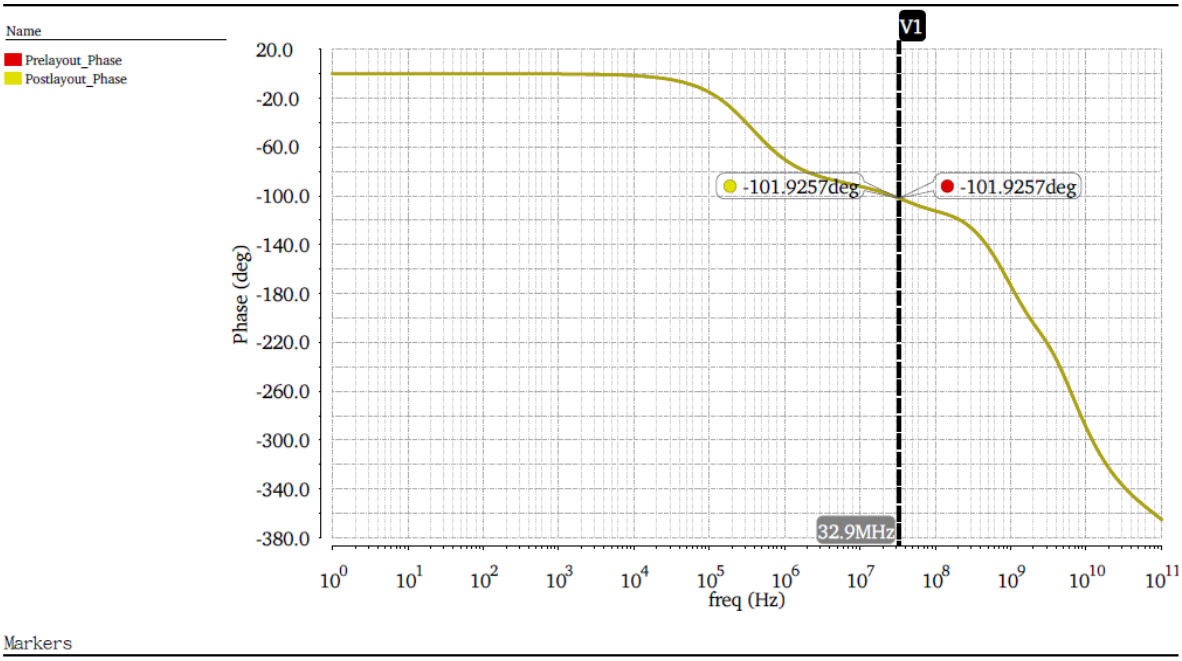


Figure 6-7 Two stage OTA pre and post layout phase comparison in AC response.

6.5. Post Layout Assembled Bias Circuit Verification

Layout verification for Bias circuit was completed using the test bench showed in **Figure 6-8**, in this test bench the only stimulus applied was VDD/VSS performing a DC analysis during 1us (same as the circuit shown in **Figure 4-9**), the pre-layout circuit was also added to compare both responses. The transient response for bias voltage is observed in **Figure 6-9**, after layout optimizations, the post-layout response reaches **331.01 mV** versus a pre-layout response of **334.66 mV**, this represents a difference of -**3.64 mV,** which means a deviation of -**1.08%.**

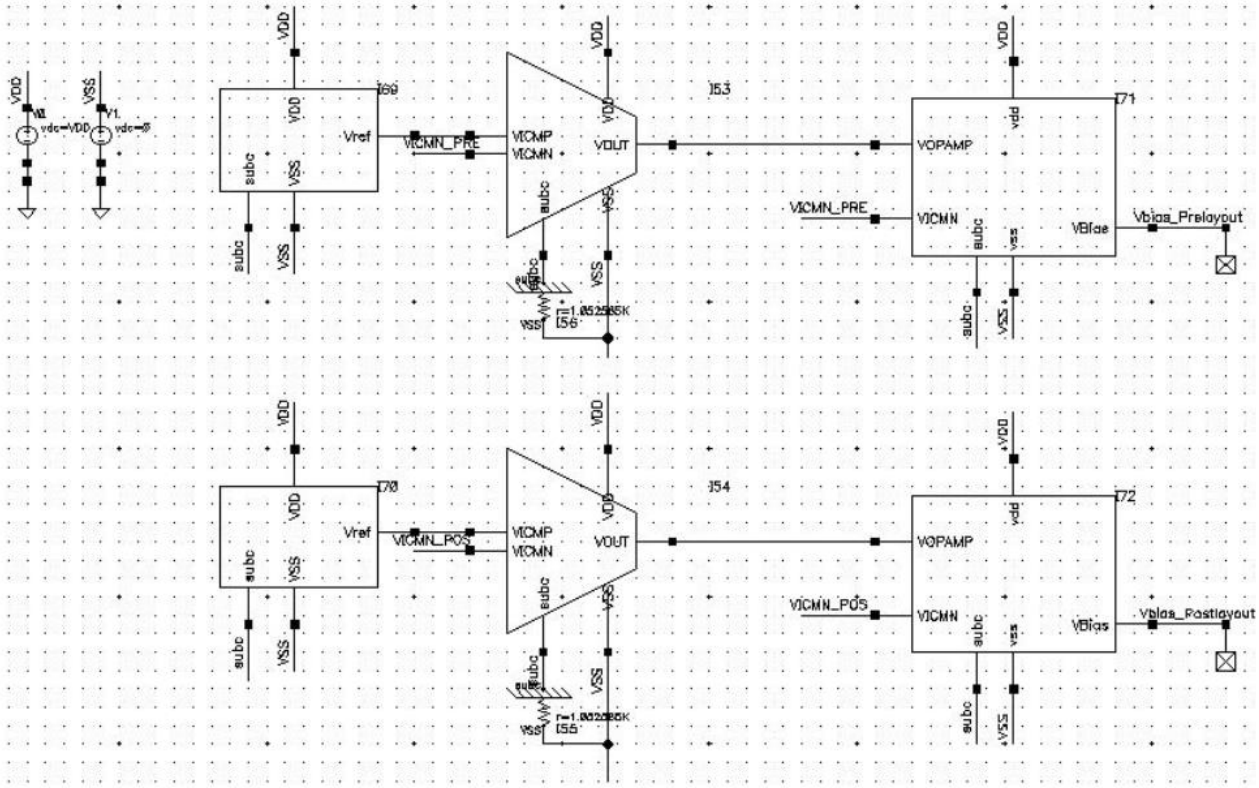


Figure 6-8 Vbias test bench for post-layout verification.

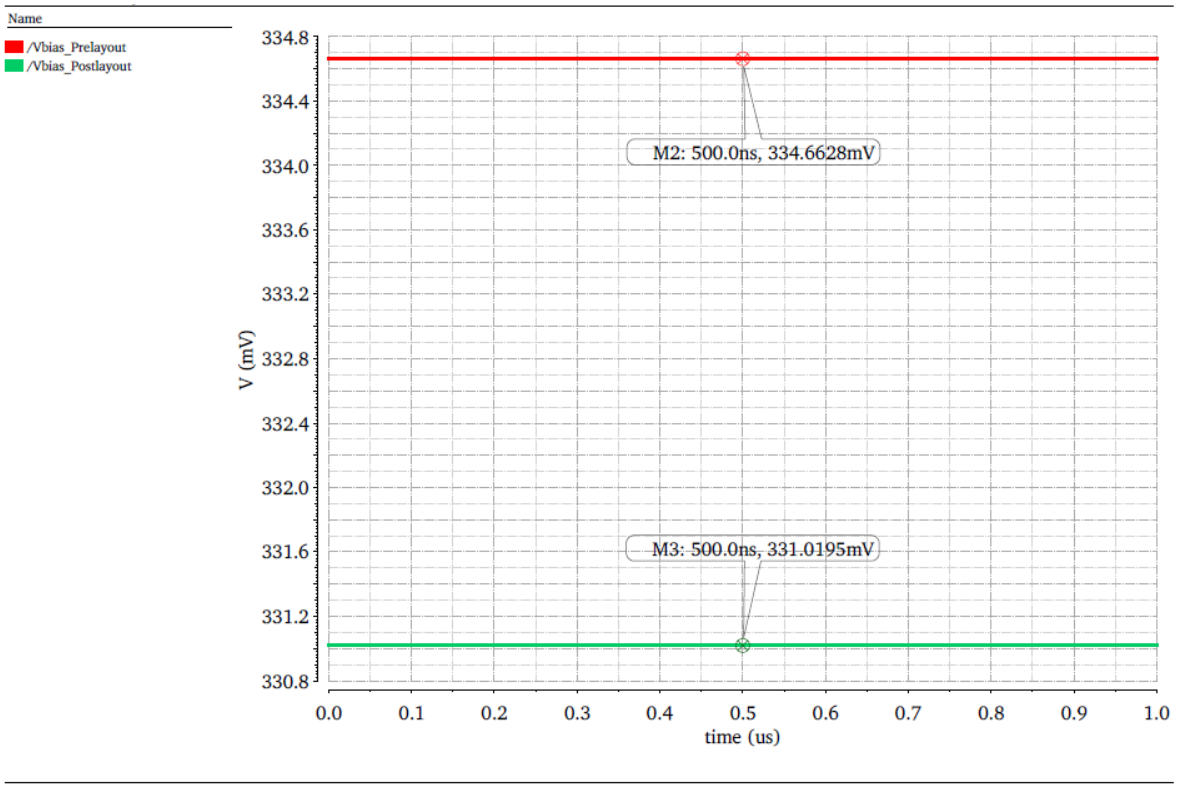


Figure 6-9 Vbias signal pre and post layout comparison.

6.6. Post Layout Bias Circuit Verification Integrated to CP

The final verification of Bias circuit was performance when it is assembled to the CP circuit. **Figure 6-11** shows the test bench used for pre and post layout simulation, the test bench parameters are the same used in chapter 4 (see **TABLE IV**) using a differential square waveform during 500 ns of DC analysis. The evaluated behavior of this Bias-CP circuit was the current charge and discharge curves (**Figure 6-10** and **Figure 6-12** respectively). Additionally, the behavior of dynamic current is compared (see **Figure 6-13**).

Post layout signals respect to pre-layout shows a difference for charge stage of **32.70 mV** which represents a decrement of **-3.78%** (measurement taken at the large delta detected between pre and post layout signals). For the discharge stage, the major increment detected was **34.67 mV (10.17%)**. Finally, the observed difference for dynamic current was **4.47 µA (-4.43%).**

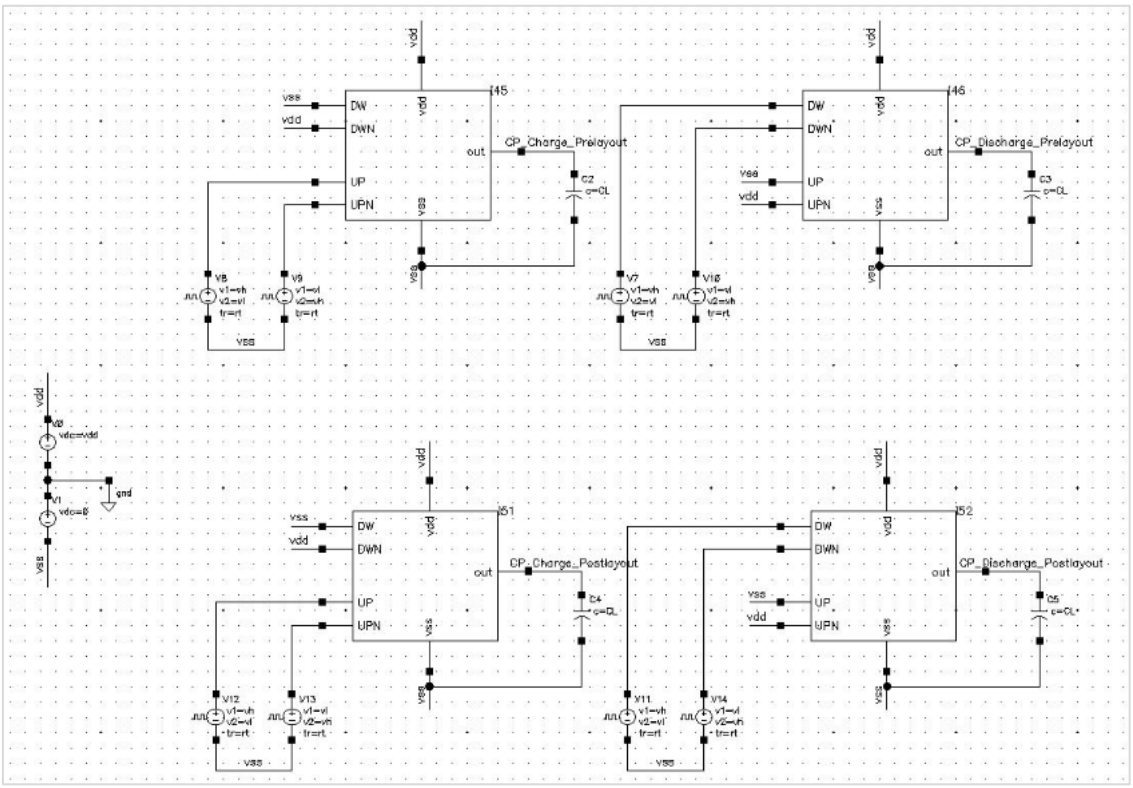


Figure 6-11 Vbias test bench for post-layout verification.

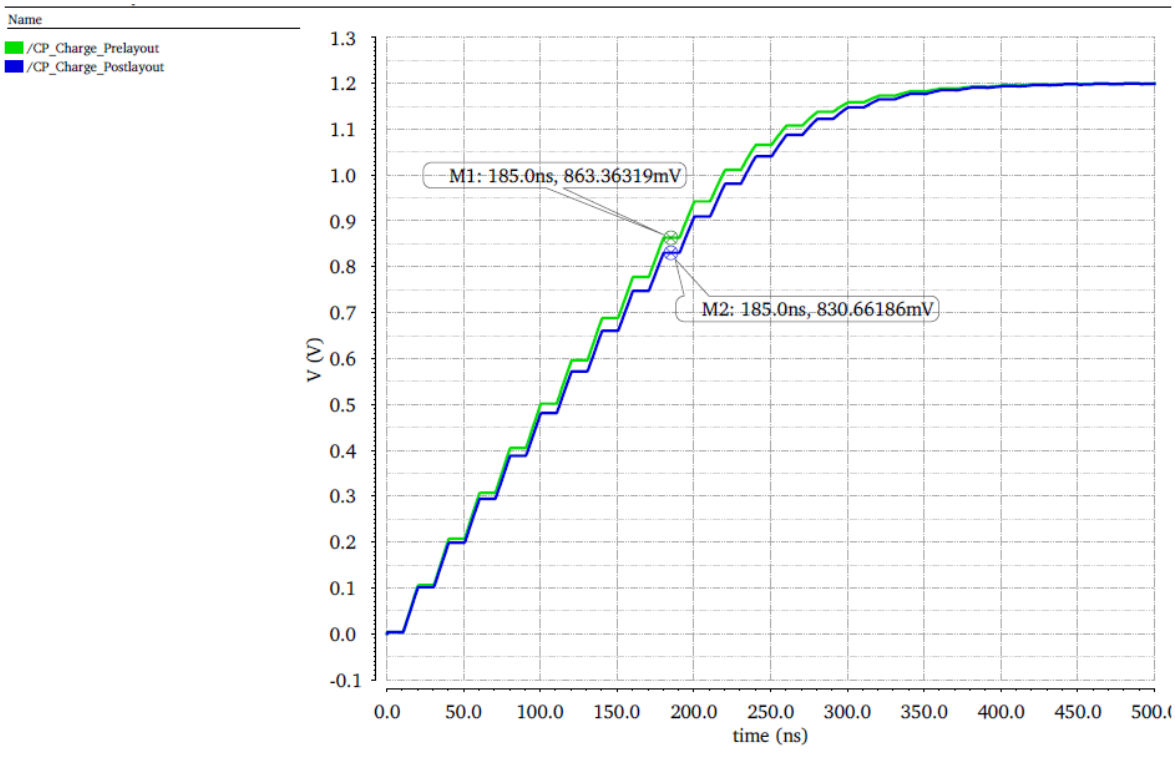


Figure 6-10 CP circuit charge stage pre and post layout comparison.

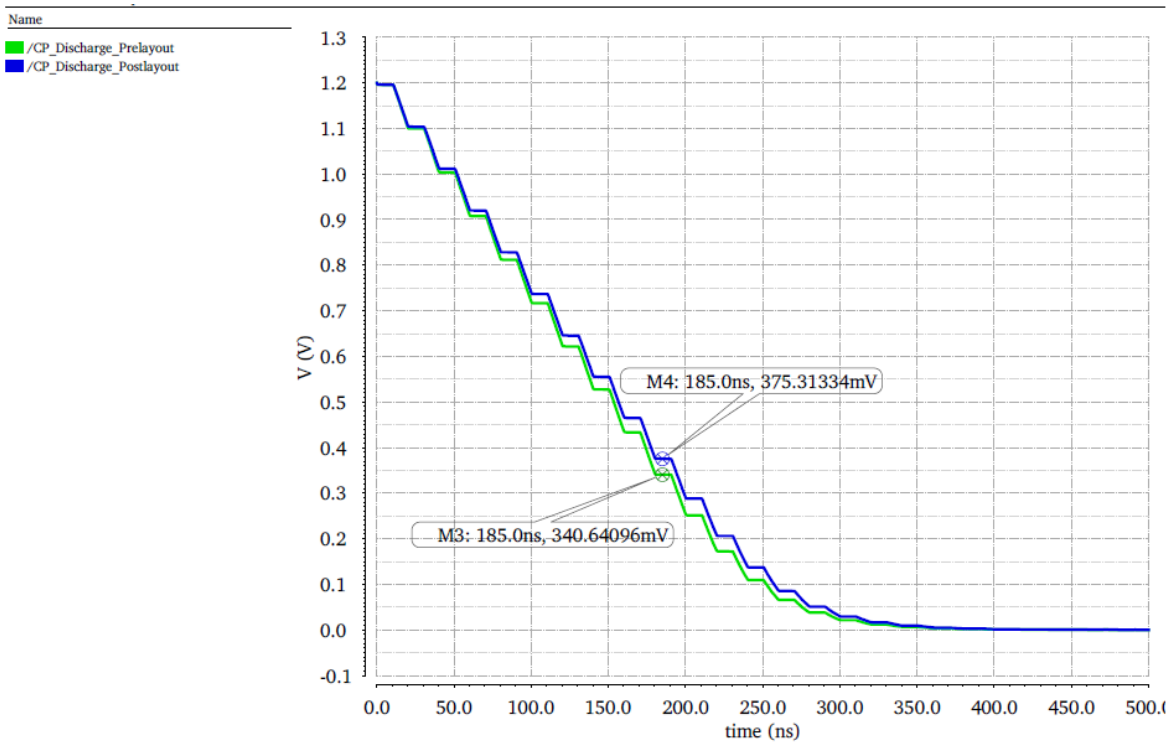


Figure 6-12 CP circuit discharge stage pre and post layout comparison.

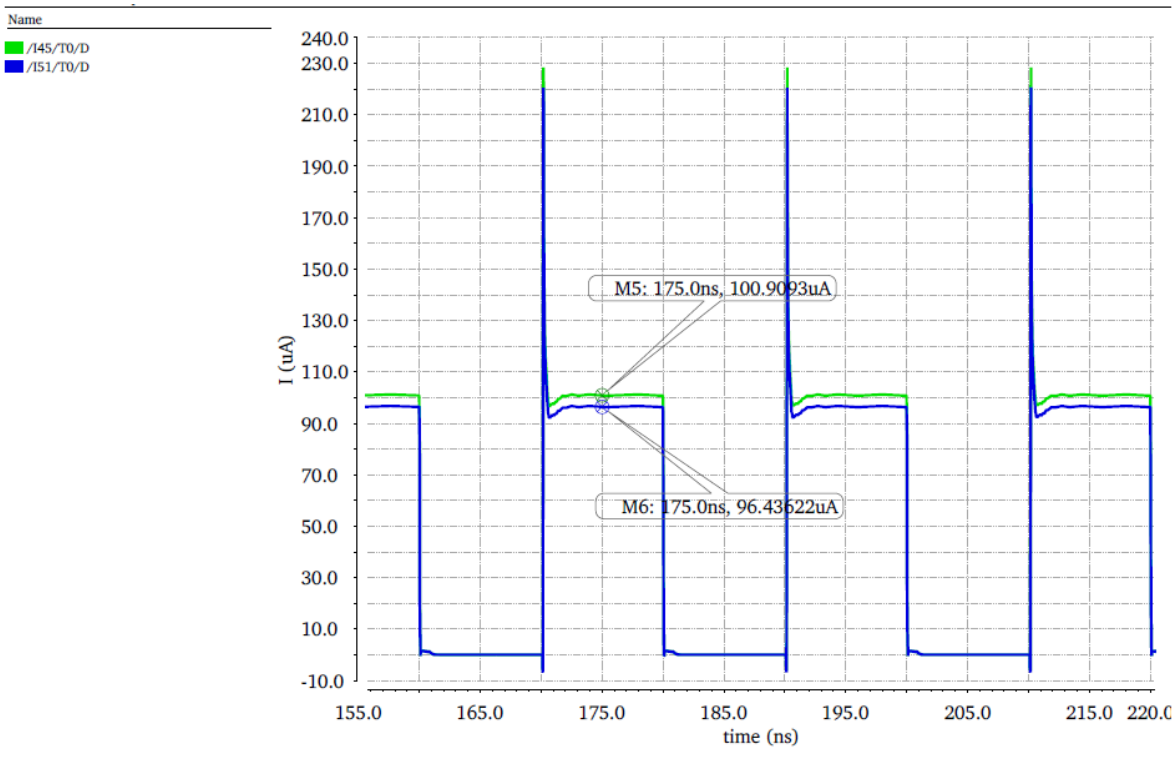


Figure 6-13 CP branch dynamic current pre and post layout comparison.

6.7. Figures of Merit of Bias Circuit Design.

As a final remark, the **TABLE VIII** show a design targets comparison versus the final results. As previously was indicated in chapter 3, the largest difference obtained in GBW will not affect the CP performance due to low frequency (DC) application.

TABLE VIII
BIAS CIRCUIT FIGURES OF MERIT

Figure of Merit	Design Target	Final Results	Delta
Two Stage OTA Gain	40 dB	38.64 dB	-3.40%
Two Stage OTA GBW	40 KHz	33.34 MHz	-16.65%
Bias Voltage	335 mV	331.01 mV	-1.19 %

As well as was presented throughout this work, the final comparison between the ideal performance of CP and the Bias circuit integrated to CP is observed in **TABLE IX**. Charge and discharge are symmetric curves, however numerically the discharge process appears with a higher variation, but this is because of low voltage values registered during signal captured are proportionally smaller.

TABLE IX
BIAS CIRCUIT INTERGRATED TO CP FINAL COMPARISON

Figure of Merit	CP Design Reference*	Final Results*	Delta
Charge Stage Voltage	856.66 mV	830.66 mV	-3.03%
Discharge Stage Voltage	347.77 mV	375.31 mV	7.91%
Dynamic Current	99.92 µA	96.37 µA	-3.55%

**Reference measurements were taken at 185us for charge/discharge voltage and 175us for dynamic current during 500ns of transient simulation.*

Conclusion

In this document, we have presented the design of Bias Voltage circuit integrated to a Charge Pump circuit in 130nm BiCMOS technology using GLOBALFOUNDRIES cmrf8hp process design kit and Cadence Virtuoso tools. Although the implemented architecture is widely used in many analog applications, the CP circuit dependency triggered the target specifications and consequently leads to create a customized design. The Bias circuit based on the CP topology allowed the use of a replica circuit that keeps the same transistors sizes to track the current CP's branch variation then locking the required Bias voltage of CP circuit.

During the design process, some challenges were faced:

- The proposal of the correct size of C_C capacitor in the OTA circuit is crucial to obtain an adequate GBW, and then the proper GBW defines a suitable value for bias current which finally defines an acceptable transistor size.
- The proper value definition of the VICM and VOCM to give enough voltage budget to maintain all transistors working on saturation region. PVT demonstrates the need to satisfy the relation between V_{DS} and Vdsat using a considerable voltage margin.
- Once the relation between C_L and C_C is satisfied, a trade-off between the GBW and C_C was created through the transconductance value. At the same time transconductance defined the bias current and size of transistors. That is, even though the CP application required a low frequency (DC) signal, it was necessary to increase the GBW specification to accomplish the described trade-off.

The presented design can be considered as a good start point, but certainly, there are many areas of opportunity for improvement, among them one can mention the following:

- The use of an OTA self-cascode topology could provide at least 50% more voltage gain to give fast compensation to the CP current variations.
- The replacement of the bias resistor (passive load) by two-array transistors connected as a diode (active load) would allow maintaining a proper bias voltage over process variations.

Appendix

A. 130 BICMOS TECHNOLOGY CHARACTERIZATION

To use complex MOSFET models used by simulation programs is one of the main obstacles for analog circuit design. The key parameter extraction is the process which gives to the circuit designers the start point for preliminary hand calculation. The initial calculation of this work was based on the BSIM3v3 Key Parameter Extractions for Efficient Circuit Designs [11].

The test bench used for 130nm BiCMOS key parameter extraction is observed in **Figure** A-14, this process is performed for n and p-mos devices, so the voltage and current sources are accordingly located. To guarantee to be in saturation, the dimension ratios of mosfet are set in 1, then, in order to cover all physical and electrical dependences effects, the (W/L) are varied as 1/1, 2/2, 5/5, 10/10, 20/20, 50/50, and 100/100, while bias current is swept from 1uA to 200uA.

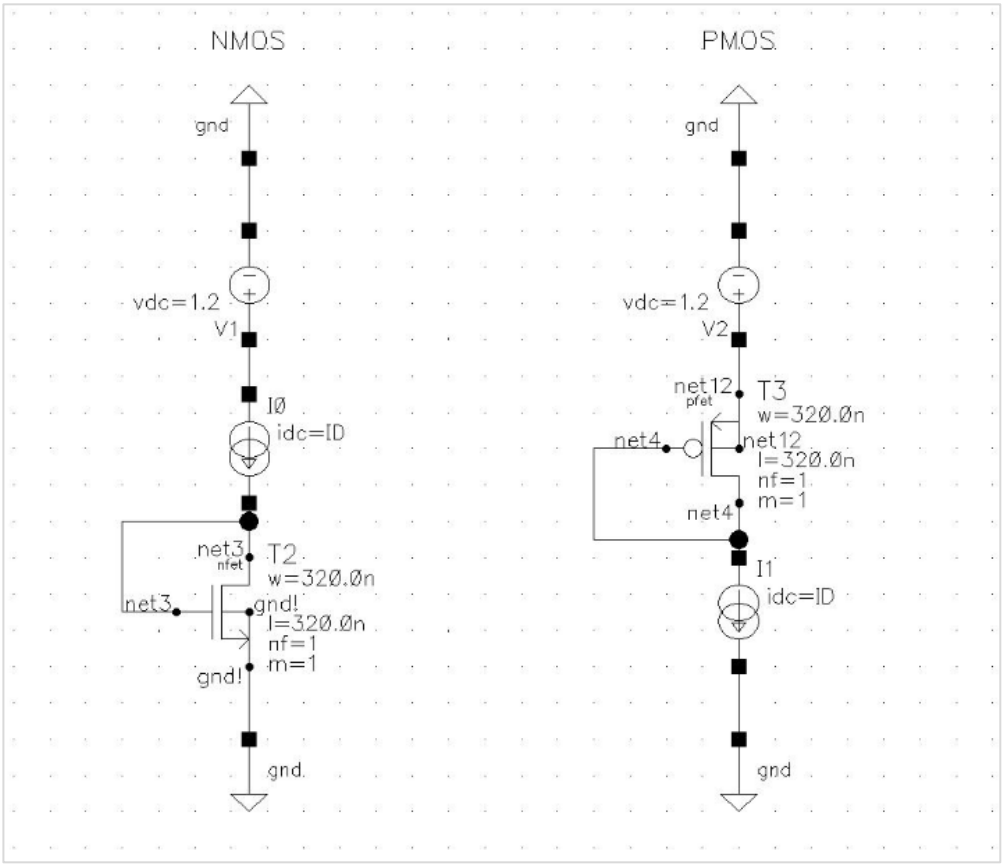


Figure A-14 Test bench for 130nm BiCMOS key parameter extraction.

The K parameter (transconductance) is extracted from the Betaeffective (B_{eff}) as:

$$K = \mu_O C_{OX} = \frac{B_{eff}}{W_{eff}/L_{eff}} \quad \text{(A-1)}$$

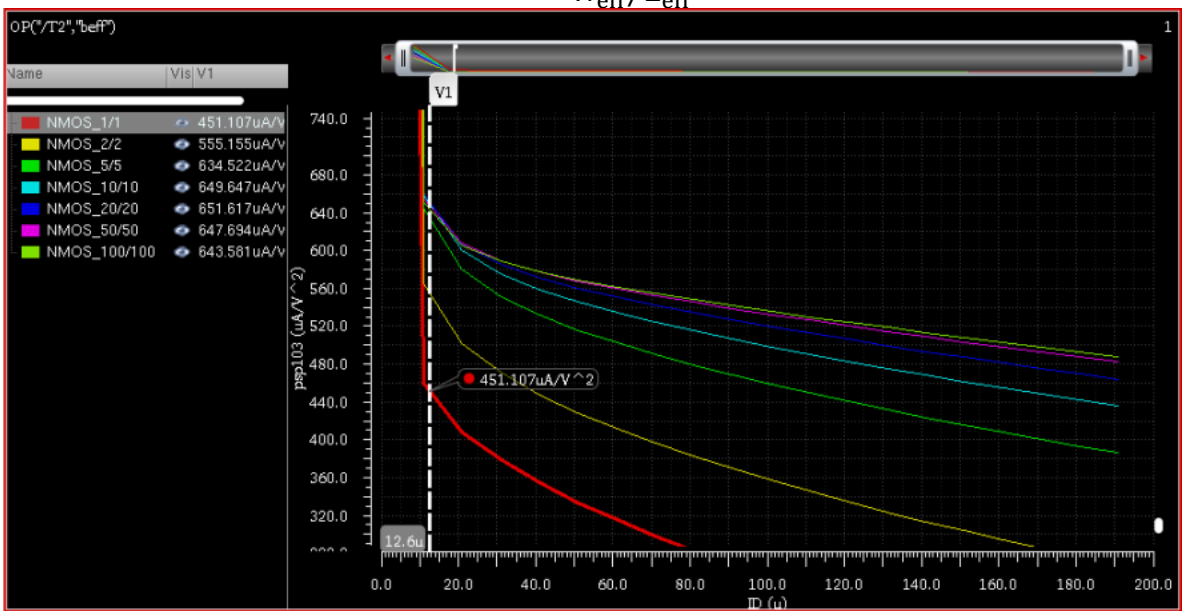


Figure A-15 KN (NMOS) graph for 130nm BiCMOS technology.

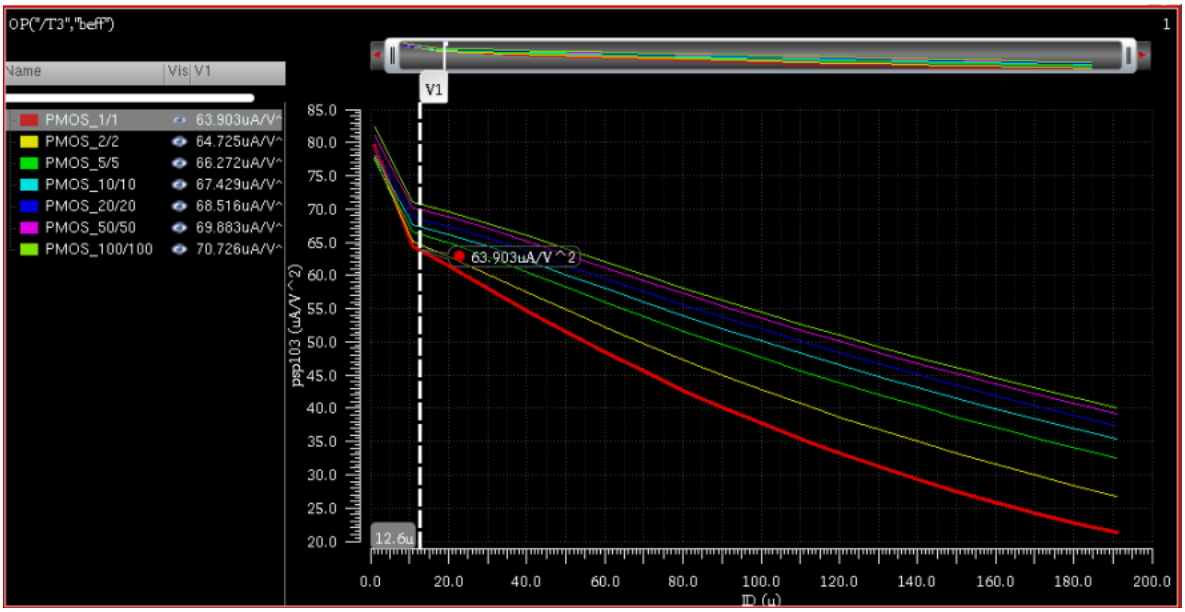


Figure A-16 KP (PMOS) graph for 130nm BiCMOS technology.

Figure A-15 and **Figure A-16** show the K_N (NMOS) and K_P (PMOS) plots for 130nm BiCMOS technology. For Bias circuit design, the selected value for L was 320nm, so the (W/L) ratio 1/1 is the reference for each parameter, then, the I_D selected in each graph was $I_B/2$, so the approximated value chosen for a reference was ID≈12.6 µA.

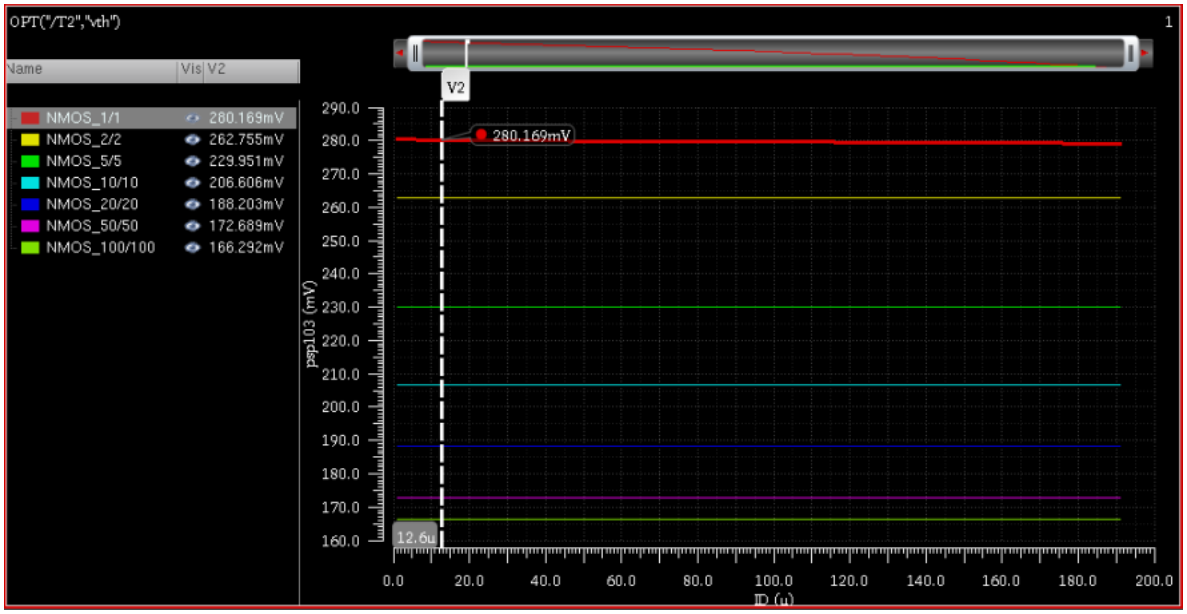


Figure A-17 V_{TH} (NMOS) graph for 130nm BiCMOS technology.

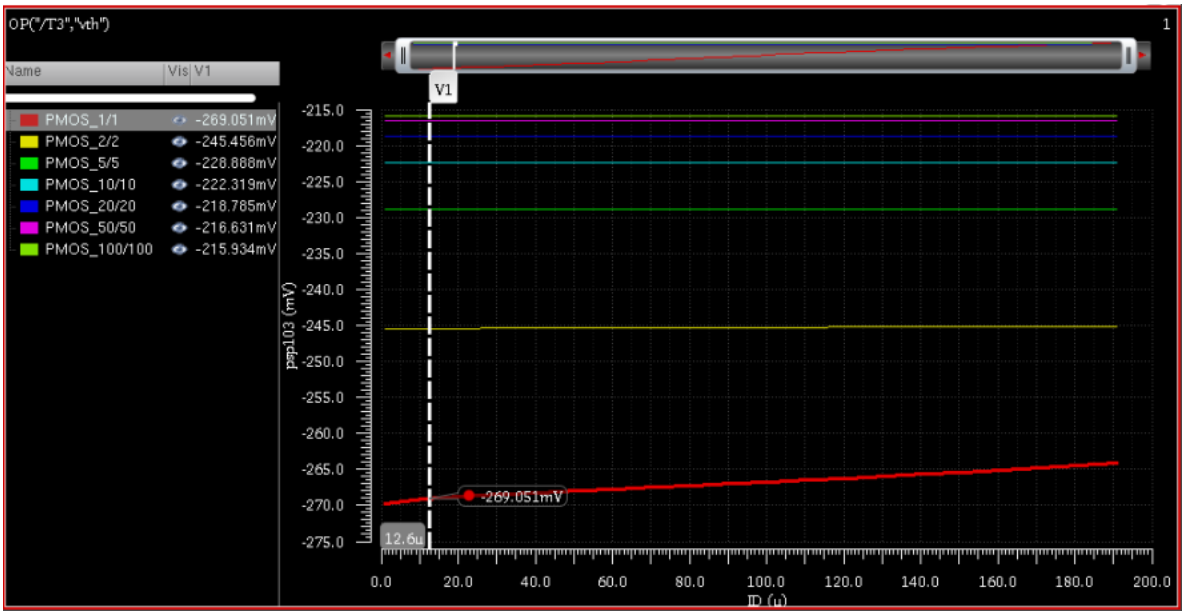


Figure A-18 V_{TH} (PMOS) graph for 130nm BiCMOS technology.

Figure A-17 and **Figure** A-18 shows the VTH parameter for NMOS and PMOS respectively, **Figure** A-19 and **Figure** A-20 show the extraction of λ parameter, this last parameter is based on the following equation:

$$\lambda = \frac{G_{DS}}{I_{DS}} \tag{A-2}$$

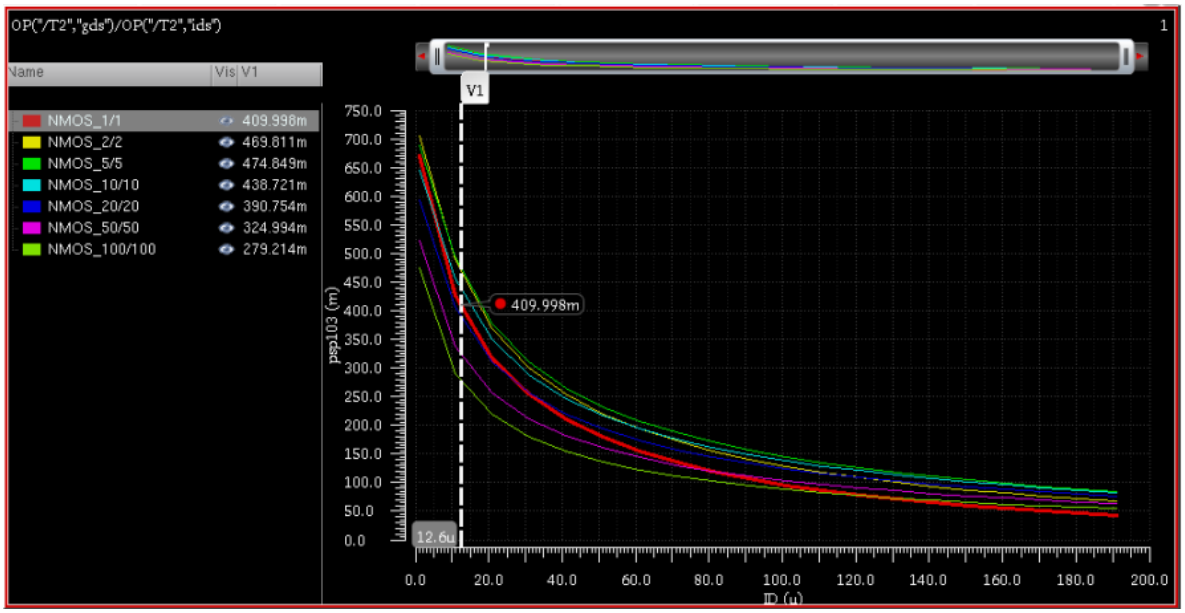


Figure A-19 λ(NMOS) graph for 130nm BiCMOS technology.

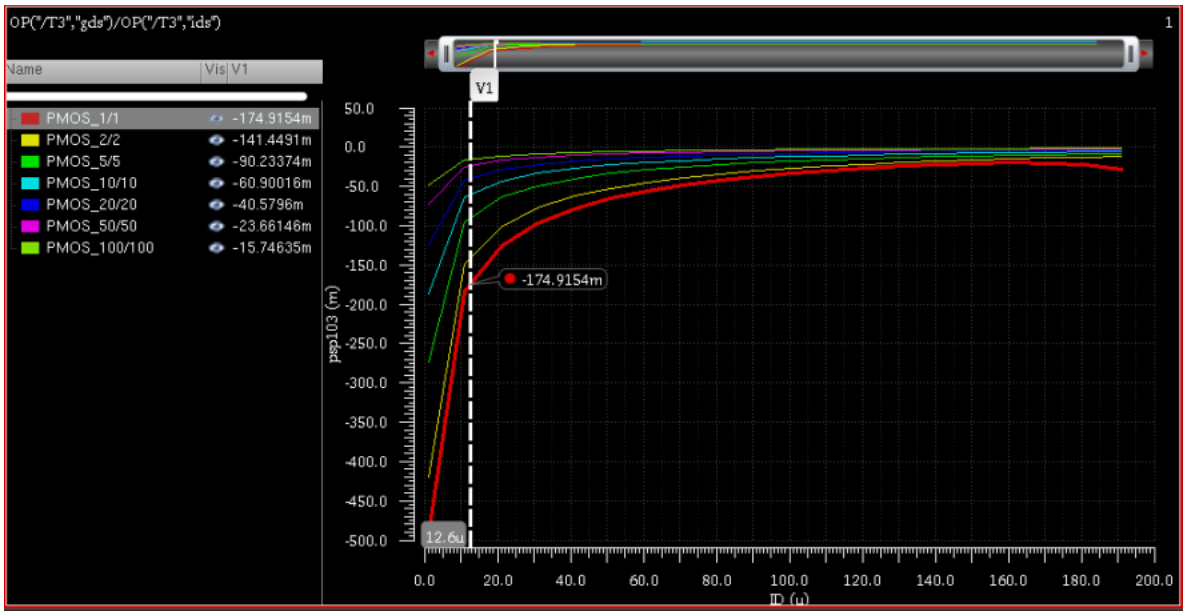


Figure A-20 λ(PMOS) graph for 130nm BiCMOS technology.

TABLE X shows a summary of the extracted parameters used in this work, these are the reference for the initial hand calculation (see Chapter 3).

TABLE X
130NM BICMOS DESIGN PARAMETERS

Parameter	NMOS	PMOS
$K\ (uA/V^2)$	451.107	63.903
$V_{TH}\ (mV)$	280.169	-269.051
$\lambda\ (m)$	409.998	-174.915

B. RESISTIVE VOLTAGE REFERENCE (PROGRESSIVE DETERMINATION VALUES)

$$N = \frac{V_{DD}}{V_X} \qquad \text{(A-3)}$$

$$M \approx \frac{V_{REF}}{V_X} \qquad \text{(A-4)}$$

N: Number of resistors (entire value).

V_X: the voltage variation (increment/decrement) between nodes.

V_{REF}: Voltage Reference (VICM)

M: Number of nodes whose value measured respecting Vss has the VICM (entire value).

N \ M	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
1	1200																													
2	600	1200																												
3	400	800	1200																											
4	300	600	900	1200																										
5	240	480	720	960	1200																									
6	200	400	600	800	1000	1200																								
7	171.43	342.86	514.29	685.71	857.14	1028.6	1200																							
8	150	300	450	600	750	900	1050	1200																						
9	133.33	266.67	400	533.33	666.67	800	933.33	1066.7	1200																					
10	120	240	360	480	600	720	840	960	1080	1200																				
11	109.09	218.18	327.27	436.36	545.45	654.55	763.64	872.73	981.82	1090.9	1200																			
12	100	200	300	400	500	600	700	800	900	1000	1100	1200																		
13	92.308	184.62	276.92	369.23	461.54	553.85	646.15	738.46	830.77	923.08	1015.4	1107.7	1200																	
14	85.714	171.43	257.14	342.86	428.57	514.29	600	685.71	771.43	857.14	942.86	1028.6	1114.3	1200																
15	80	160	240	320	400	480	560	640	720	800	880	960	1040	1120	1200															
16	75	150	225	300	375	450	525	600	675	750	825	900	975	1050	1125	1200														
17	70.588	141.18	211.76	282.35	352.94	423.53	494.12	564.71	635.29	705.88	776.47	847.06	917.65	988.24	1058.8	1129.4	1200													
18	66.667	133.33	200	266.67	333.33	400	466.67	533.33	600	666.67	733.33	800	866.67	933.33	1000	1066.7	1133.3	1200												
19	63.158	126.32	189.47	252.63	315.79	378.95	442.11	505.26	568.42	631.58	694.74	757.89	821.05	884.21	947.37	1010.5	1073.7	1136.8	1200											
20	60	120	180	240	300	360	420	480	540	600	660	720	780	840	900	960	1020	1080	1140	1200										
21	57.143	114.29	171.43	228.57	285.71	342.86	400	457.14	514.29	571.43	628.57	685.71	742.86	800	857.14	914.29	971.43	1028.6	1085.7	1142.9	1200									
22	54.545	109.09	163.64	218.18	272.73	327.27	381.82	436.36	490.91	545.45	600	654.55	709.09	763.64	818.18	872.73	927.27	981.82	1036.4	1090.9	1145.5	1200								
23	52.174	104.35	156.52	208.7	260.87	313.04	365.22	417.39	469.57	521.74	573.91	626.09	678.26	730.43	782.61	834.78	886.96	939.13	991.3	1043.5	1095.7	1147.8	1200							
24	50	100	150	200	250	300	350	400	450	500	550	600	650	700	750	800	850	900	950	1000	1050	1100	1150	1200						
25	48	96	144	192	240	288	336	384	432	480	528	576	624	672	720	768	816	864	912	960	1008	1056	1104	1152	1200					
26	46.154	92.308	138.46	184.62	230.77	276.92	323.08	369.23	415.38	461.54	507.69	553.85	600	646.15	692.31	738.46	784.62	830.77	876.92	923.08	969.23	1015.4	1061.5	1107.7	1153.8	1200				
27	44.444	88.889	133.33	177.78	222.22	266.67	311.11	355.56	400	444.44	488.89	533.33	577.78	622.22	666.67	711.11	755.56	800	844.44	888.89	933.33	977.78	1022.2	1066.7	1111.1	1155.6	1200			
28	42.857	85.714	128.57	171.43	214.29	257.14	300	342.86	385.71	428.57	471.43	514.29	557.14	600	642.86	685.71	728.57	771.43	814.29	857.14	900	942.86	**985.7**	1028.6	1071.4	1114.3	1157.1	1200		
29	41.379	82.759	124.14	165.52	206.9	248.28	289.66	331.03	372.41	413.79	455.17	496.55	537.93	579.31	620.69	662.07	703.45	744.83	786.21	827.59	868.97	910.34	951.72	993.1	1034.5	1075.9	1117.2	1158.6	1200	
30	40	80	120	160	200	240	280	320	360	400	440	480	520	560	600	640	680	720	760	800	840	880	920	960	1000	1040	1080	1120	1160	1200

$V_{X\,(mV)}$

C. VDSAT APPROACH FOR DESIGN PURPOSES

In this work, an important parameter that was assumed during the design stage (chapter 3) was the saturation voltage (V_{Dsat}). Taking into account the two stage OTA topology used on Bias circuit (**Figure A-21**), it is possible to deduce that the first stage of the OTA has the largest route from VDD to VSS (three MOSFET either M3-M1-MB2 or M4-M2-MB2), so, the available budget in terms of voltage for these transistors is VDD/3, this means, each transistor would have 400 mV as budget for its own V_{DS}.

Given the condition to keep saturated each transistor **(A-5)**, the determination to propose 200 mV as V_{Dsat} was only the purpose to ensure that V_{Dsat} has a half of the available voltage budget for V_{DS}.

$$V_{DS} > V_{GS} - V_{TH} = V_{dsat} \tag{A-5}$$

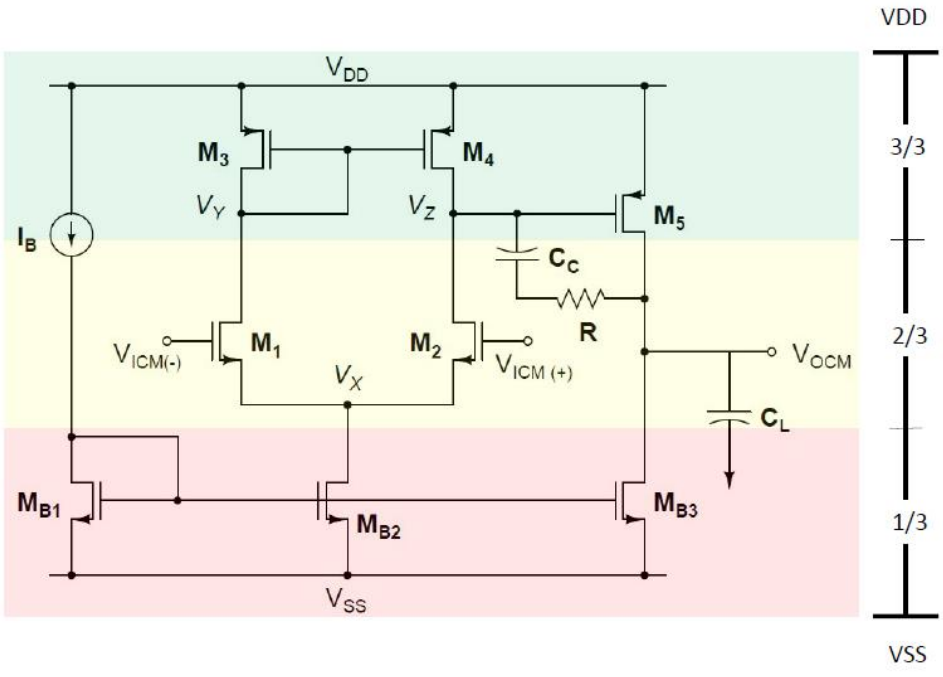


Figure A-21 Two stage OTA supply distribution.

D. PVT CORNERS FOR OTA AND BIAS CIRCUIT

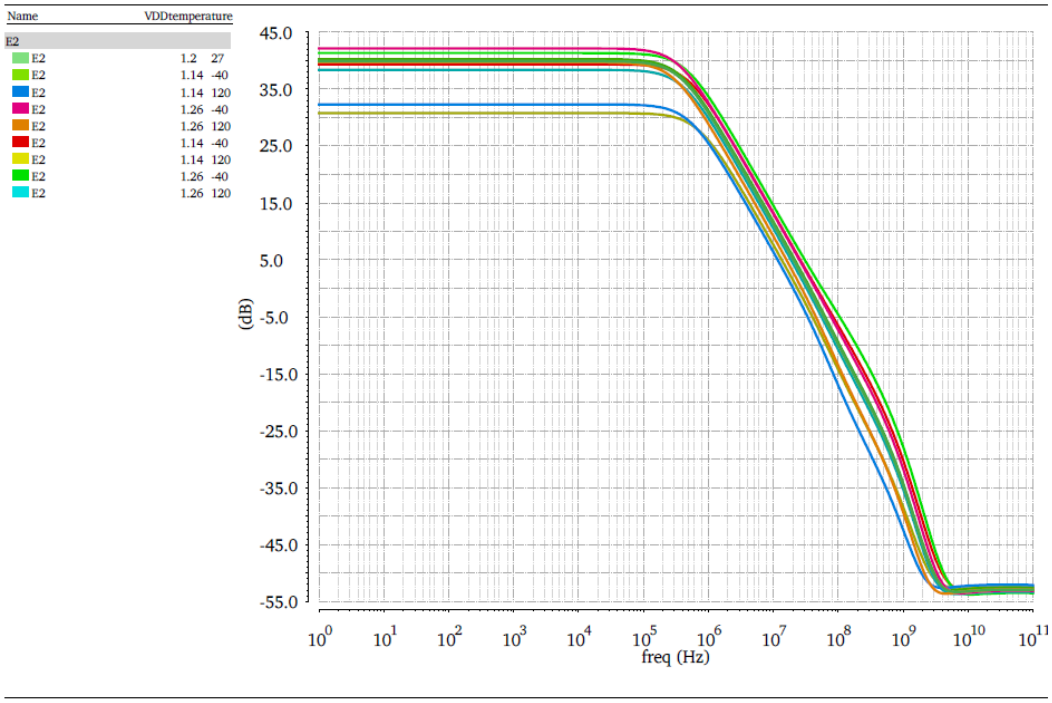
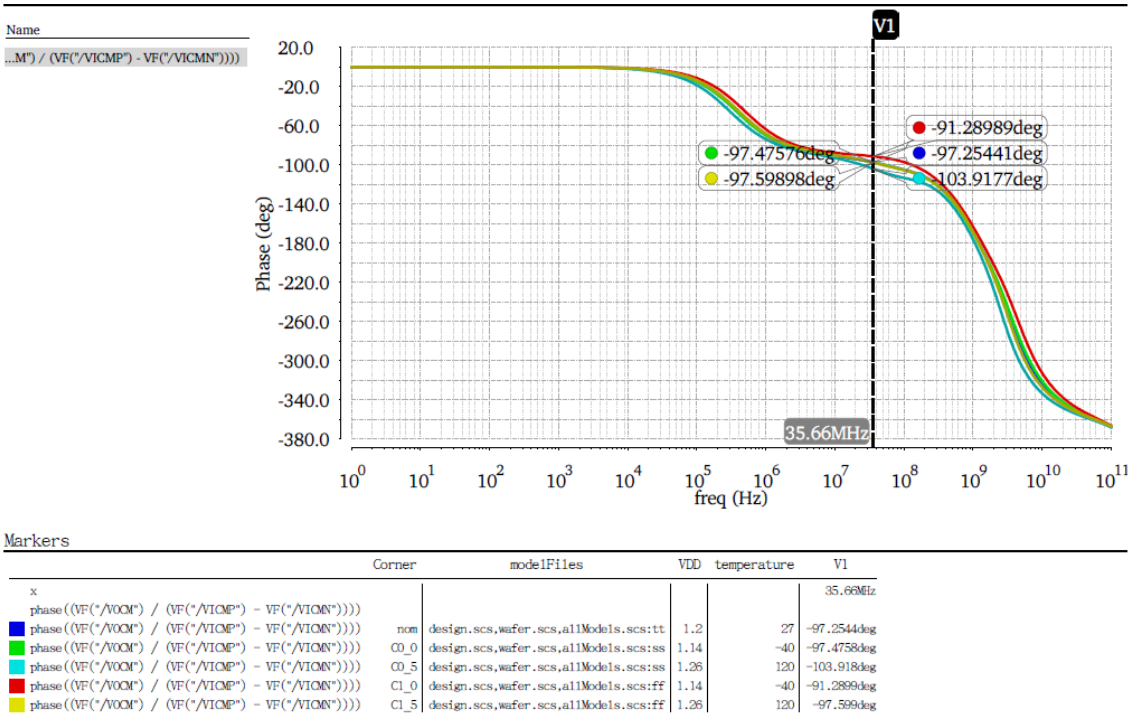


Figure A-22 OTA PVT AC response.



		Corner	modelFiles	VDD	temperature	V1
x						35.66MHz
phase((VF("/VOCM") / (VF("/VICMP") - VF("/VICMN"))))						
phase((VF("/VOCM") / (VF("/VICMP") - VF("/VICMN"))))	nom		design.scs,wafer.scs,allModels.scs:tt	1.2	27	-97.2544deg
phase((VF("/VOCM") / (VF("/VICMP") - VF("/VICMN"))))	C0_0		design.scs,wafer.scs,allModels.scs:ss	1.14	-40	-97.4758deg
phase((VF("/VOCM") / (VF("/VICMP") - VF("/VICMN"))))	C0_5		design.scs,wafer.scs,allModels.scs:ss	1.26	120	-103.918deg
phase((VF("/VOCM") / (VF("/VICMP") - VF("/VICMN"))))	C1_0		design.scs,wafer.scs,allModels.scs:ff	1.14	-40	-91.2899deg
phase((VF("/VOCM") / (VF("/VICMP") - VF("/VICMN"))))	C1_5		design.scs,wafer.scs,allModels.scs:ff	1.26	120	-97.599deg

Figure A-23 OTA phase PVT AC response.

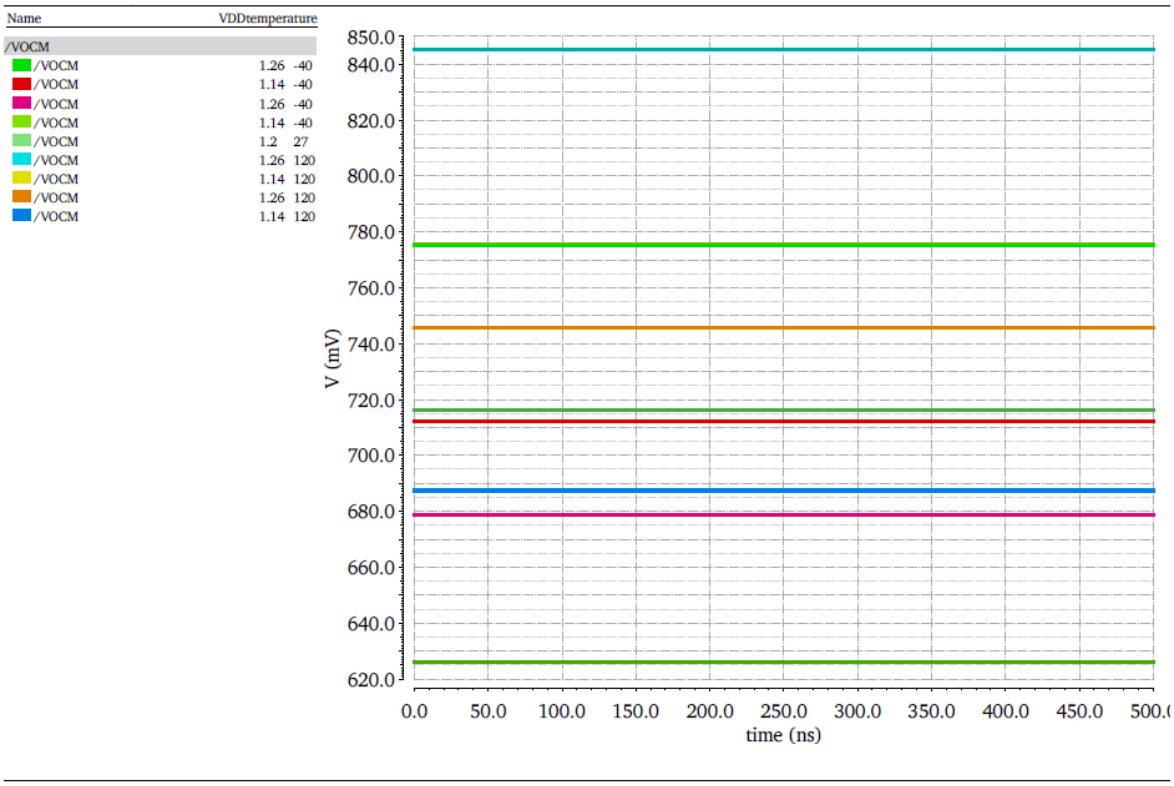


Figure A-24 OTA VOCM PVT DC response.

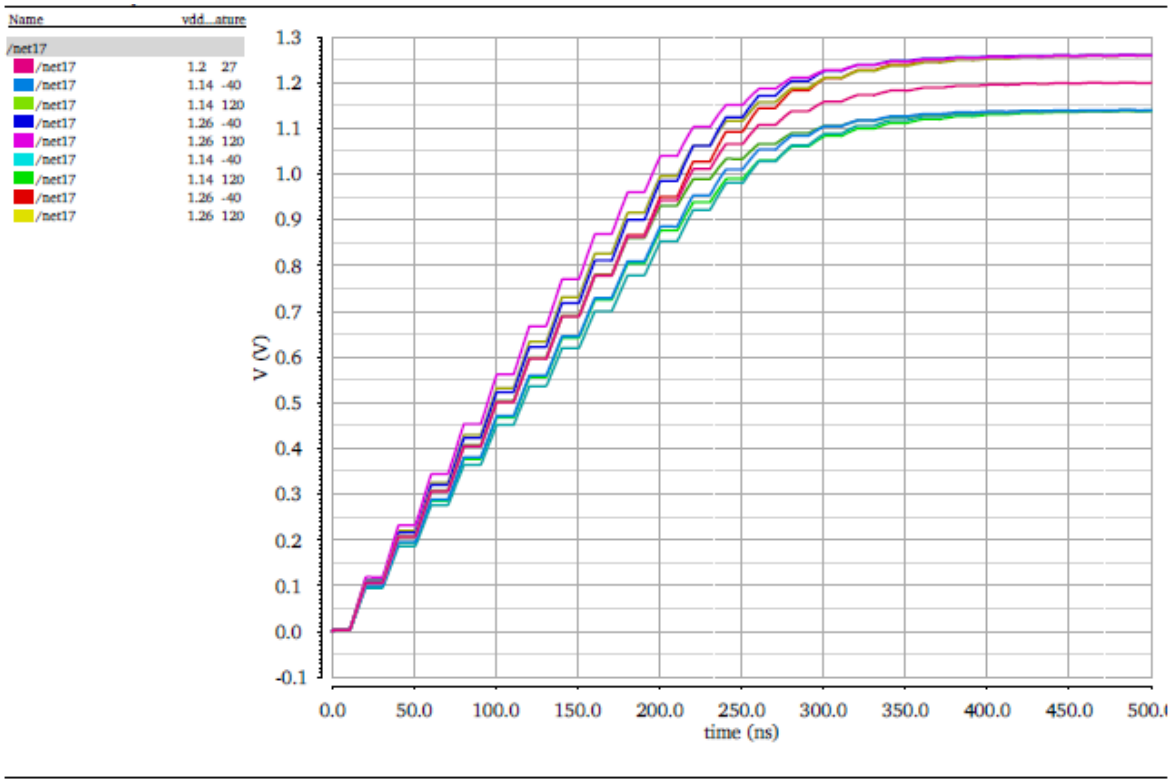


Figure A-25 CP circuit charge stage PVT.

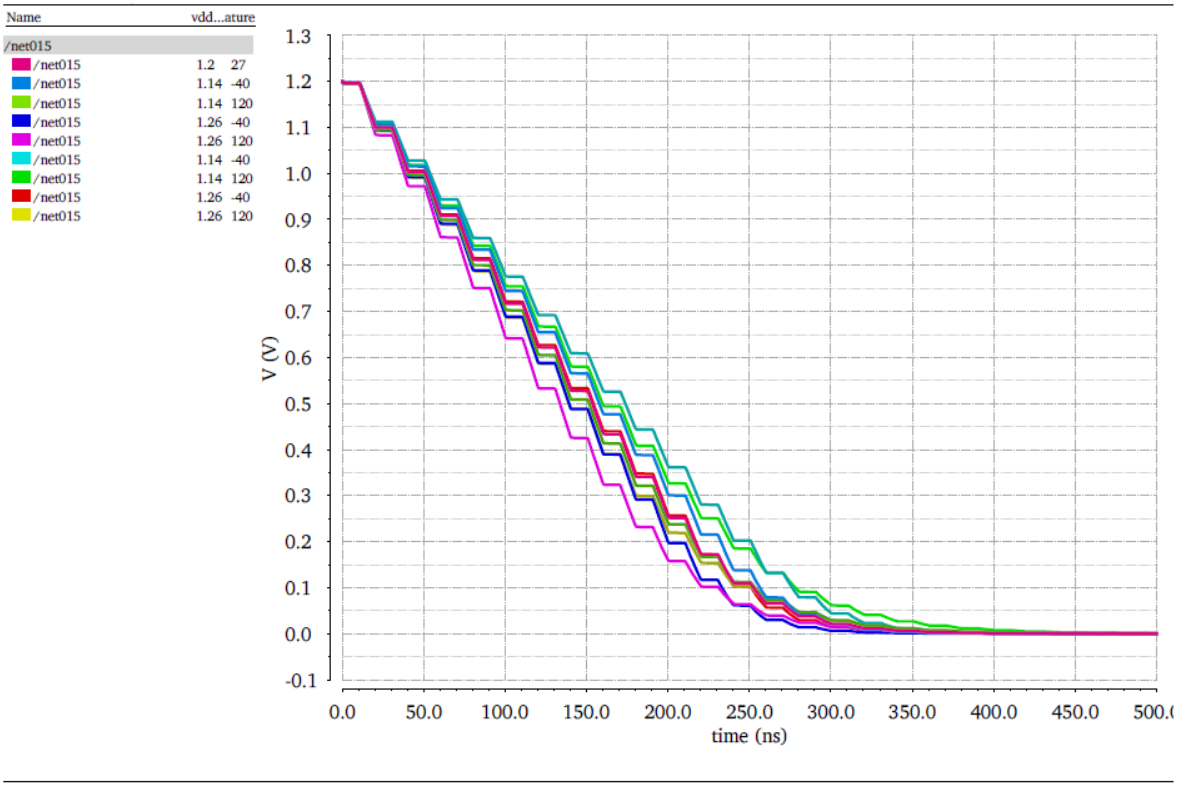


Figure A-26 CP circuit discharge stage PVT.

E. PLL BLOCK SPECIFICATION

The requirements to develop the PLL design are shown below:

- 1.2V power supply
- PLL generates clock signals up to 800.0 MHz (Max. 1.0 GHz)
- One clock output with 8 phases @800MHz (Phases: 0º,45º, 90º, 135º, 180º, 225º, 270º and 315º)
- Max. output skew of 60ps
- Internal and external PLL Feedback
- Ambient temperature range: 0C to +70C
- Spread spectrum compatible
- 60 ps max cycle-cycle jitter
- 10 ps max I/O Phase Jitter
- 10 ps max static phase offset (SPO)
- 60 ps max output–output skew
- PLL Lock time < 10us
- Current Consumption < 20mA
- Output Duty Cycle = 50% +/- 1%
- Rise & Fall time: 100ps
- Output Load = 10pF per output
- Vx = VDD/2 +/- 1%

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