A Programmable CMOS Voltage Controlled Ring Oscillator for Radio-Frequency Diathermy On-chip Circuit

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Abstract— **In this work we present the design of a digitally controlled ring type oscillator in 0.5 µm CMOS technology for a low-cost and portable radio-frequency diathermy (RFD) device. The oscillator circuit is composed by a low frequency ring oscillator (LFRO), a voltage controlled ring oscillator (VCRO), and a logic control. The digital circuit generates an input signal for the LFO, which generates a voltage ramp that controls the oscillating output signal of the VCRO in the range of 100 KHz to 1 MHz. Simulation results show that the proposed circuit exhibits controllable output characteristics in the range of 100 KHz – 1 MHz, with low power consumption and low phase noise, making it suitable for a portable RFD device.**

Index Terms— low-frequency oscillator, voltage-controlled oscillator, ring oscillator, radio-frequency diathermy, RFD.

I. INTRODUCTION

RADIO frequency diathermy (RFD) is a therapeutic technique that utilizes nonionizing electromagnetic radiation to induce localized heat inside the patient's body [1], [2],which is used for healing some kind of muscular illness. Devices used in RFD comprise a voltage controlled oscillator (VCO) among others building blocks [3], [4]. The frequency operation of these devices is tuned in the range of hundreds of kHz to few MHz [2], so that a stable frequency in a wide tuning range is one of requirements for VCOs of RFD devices. Other important design specifications for VCOs of on-chip RFD devices are: low power consumption, small layout area, low phase noise, and low power supply noise. There are many monolithic VCO architectures based on LC tank showing good performance for high frequency applications, however, the ring VCO topologies are preferred because they are more reliable and suitable for the wide tuning range, smaller layout area, lower dissipated power, and less design complexity than LC tank counterpart [5], [6], [7], but they are more prone to noise [7]. However, the low phase noise performance of ring oscillators can be improved by using differential VCO structures [7].

In this work, we present the design of a CMOS circuit for a portable RFD device, composed by a low frequency ring oscillator (LFRO), a voltage controlled ring oscillator (VCRO) and a digital control circuit. The circuit is designed to generate a square signal with a frequency in the range of 100 kHz to 1 MHz using 0.5 µm On-Semiconductor process parameters. Simulation results show that the proposed circuit exhibits controllable output characteristics in the range of 100 kHz – 1 MHz, making it suitable for a portable RFD device. In section IV conclusions are done.

II. PRINCIPLE OF THE PROPOSED PROGRAMMABLE VCRO

Figure 1 presents the proposed programmable VCRO circuit to generate four frequency sweep ranges. The control circuit allows change the frequency of the LFRO circuit in an exact way by mean of two bits. The LFRO generates a ramp signal that control the sweep frequency range (100 kHz - 1 MHz) of the VCRO circuit, also the repetition time for this frequency sweep. The RFD chip can start with a frequency sweep of 100 kHz to 1 MHz and any of these four repetition times: continuous, 1 s, 0.2 s, and 0.08 s. Actually, detailed information of this block is deliberately not provided because a patent registration of this prototype is in progress[1].

The schematic of the LFRO is shown in Fig. 2. This LFRO is implemented with 5-stages of current starved delay cells connected on a loop. In the basic cell, transistor N_2 connected to the source of transistor N_1 is the element that controls the delay time (t_d) of the cell, through its variable on-resistance ($r_{on2} = 1/[k_p(W/L)_2(V_{cntl\text{-}LFO} - V_{Th})]$) and the overall capacitance at drain node of N_1 in the inverter [8].

The oscillation frequency of the LFRO is given by

$$f_{osc} = \frac{1}{2Nt_d} \tag{1}$$

where N is the number of delay cells, and t_d is the delay time. The delay time of each inverter stage is given by [9]

$$t_d = \frac{V_{osc}C_L}{I_{cntl}} \tag{2}$$

where V_{osc} is the oscillation amplitude, I_{cntl} is the current controlled by transistor N_2, and C_L the overall parasitic capacitance at drain node ($C_L = C_{gsp1} + C_{dsp1} + C_{dbp1} + C_{dsn1} + C_{gdn1} + C_{dbn1} + C_{dgn2} + C_{dsn2} + C_{dbn2} + C_{gdp2} + C_{gsp2} + \ldots$). Then combining (1) and (2) we have

A. Corres-Matamoros is with Cormat Inc., Zapopan, 45079 Mexico (e-mail: antoniocorres@cormat.mx). E. Martínez-Guerrero (e-mail: margres@iteso.mx) and J. E. Rayas-Sánchez (e-mail: erayas@iteso.mx) are with the Department of Electronics, Systems, and Informatics, ITESO – The Jesuit University of Guadalajara, Tlaquepaque, Jalisco, 45604 Mexico.

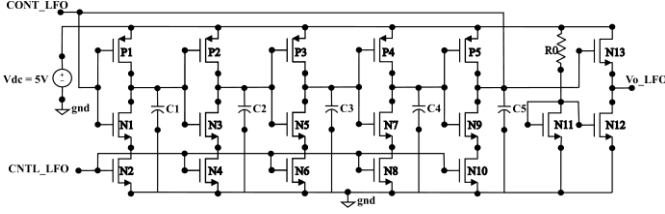Fig. 1.   Block diagram of oscillator with programmable frequency range.

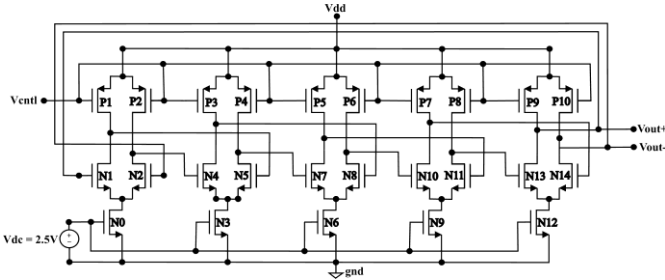Fig. 2.   Schematic of the low-frequency ring oscillator (LFRO) circuit [8].

Fig. 3.   Schematic of the voltage-controlled ring oscillator (VCRO) circuit [7].

$$f_{osc} = \frac{I_{cntl}}{2NV_{osc}C_L} \qquad (4)$$

due to power supply and temperature perturbations, and noise generated in other building blocks, it is expected that ring oscillator will suffer variations in respect to its f_{osc} nominal value. The effect of power supply and temperature perturbations are manifested as variation of the rising and falling pulse edges which is referred as jitter [10]. On the other hand, noise effect is manifested as alterations in both the amplitude and frequency of oscillation. Amplitude noise is less important because the non-linearities that affect the amplitude of oscillation also stabilize the amplitude noise [11]. By contrary, due to the fact that the phase noise is a random deviation in frequency it affects the zero crossing points of the time-dependent waveform of the oscillator in a random way, hence a variation of oscillation frequency could be present. Therefore phase noise become an important design consideration in selecting the oscillator architecture. It has been reported that differential architectures are less prone to phase noise [7], [10], [11].

As above mentioned, power consumption is an important design consideration. Power consumption is composed by static part and dynamic one. In general, static power

consumption is due only to the leakage current and it is very small and negligible as compared to dynamic power consumption. However, the dynamic power consumption occurs due to the short circuit currents and switching currents. The average power dissipation in an N-stage CMOS ring oscillator circuit is

$$P_{avg} = nNV_{DD}C_L f_{osc} \qquad (5)$$

where P_{avg} is average power, C_L is the overall capacitance at drain node of the inverter, V_{DD} is supply voltage and f_{osc} is frequency of oscillation.

According to (4), the oscillation frequency can be controlled by varying the I_{cntl}, if assuming the number of stages N, and C_L are fixed. It is also evident from (4) and (5) a tradeoff between frequency oscillation and power consumption: low frequencies require large C_L values, and low power consumption requires smaller C_L values. Indeed at very low frequencies power consumption is insignificant so, we can use large values of C_L. Nevertheless parasitic C_L is relatively low ($<<$ 1 pF). In order to get the required t_d (8.3 ms – 100 ms) for a frequency range of 1 Hz to 12 Hz we connect an external capacitor C_{delay} = 6 pF, that becomes in the new C_L at each output node of inverters. The size ratio of transistors of delay in cell LFRO were calculated to get a discharge ramp much slower than the charge ramp, so that the sweep of frequencies was much more gradual. The resulting values were $(W/L)_n$ = 1.5 µm/10.0 µm, and $(W/L)_p$ = 10.0 µm/0.6 µm. A voltage buffer at the output of LFRO is added in order to provide a current gain in the oscillating signal. In this buffer R_0 = 1 kΩ, $(W/L)_{n11,n12}$ = 1.5 µm /0.6 µm and $(W/L)_{n13}$ = 100 µm/0.6 µm.

As far as VCRO concerns, this was implemented with 5-stages of differential delay cells with alternated connections (Fig. 3). With this type of connection it is expected a reduction of phase noise [7]. In the basic delay cell, P_1 and P_2 are pMOS transistors that operates from deep triode region to saturation region, when its gate to source voltage (V_{O-LFO}) is varied to get the desired output frequency of oscillation, N_1 and N_2 are nMOS transistors whose input voltage provoques operation in triode region and saturation region, N_0 is the nMOS transistor used to provide a constant current source, so it operates in a saturation region. Here P_1 and P_2 are sized in order to act as a variable resistor controlled by V_{O-LFO} input. As the V_{O-LFO} become more positive the resistance of P_1 and P_2 transistor increases, thus raising the time constant at the output and lowering the operating frequency at the output.

Here again, the frequency oscillation is given by (1). Now, the delay time is defined in terms of the equivalent RC circuit of the delay cell as follows

$$t_d = \frac{C_L}{K_p(W/L)_{1,2}(V_{DD} - V_{o\_LFO} - |V_{Thp}|)} \qquad (5)$$
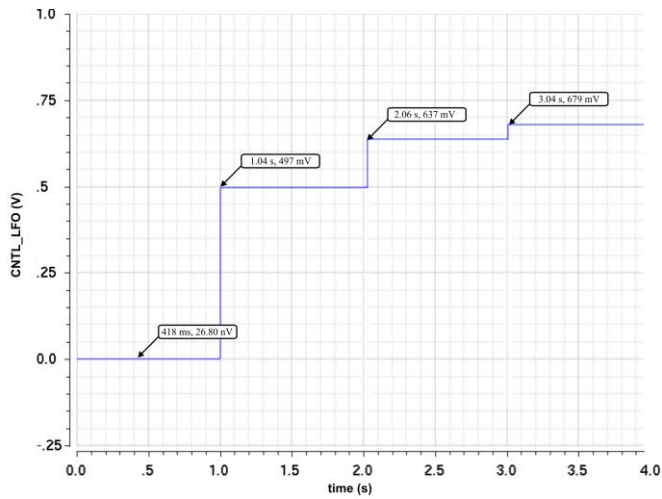
Fig. 4. Transient response of the digital control circuit for the different values of *A* and *B* inputs.
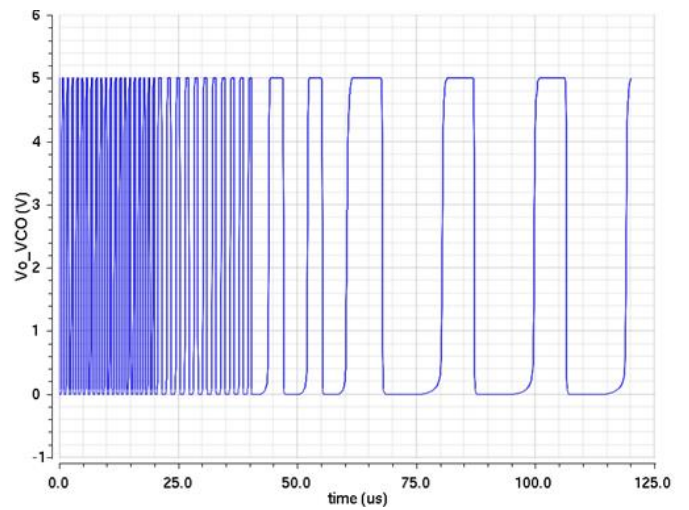

Fig. 7. Transient response of the VCRO circuit for the different modes of the digital logic control.
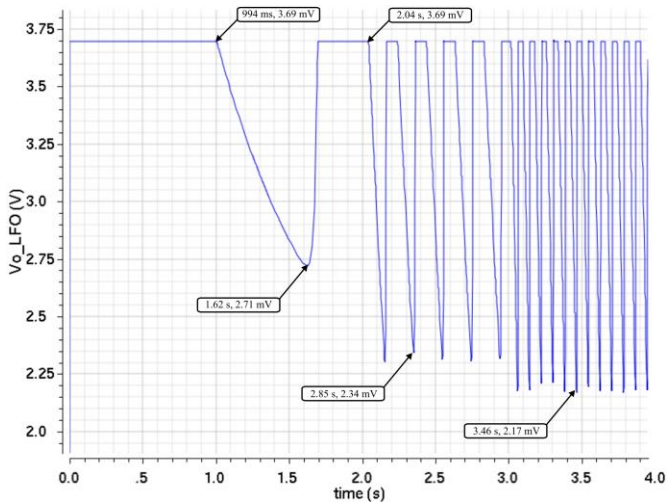

Fig. 5. Transient response of the LFRO circuit for the different values of the CNTL_LFO input.
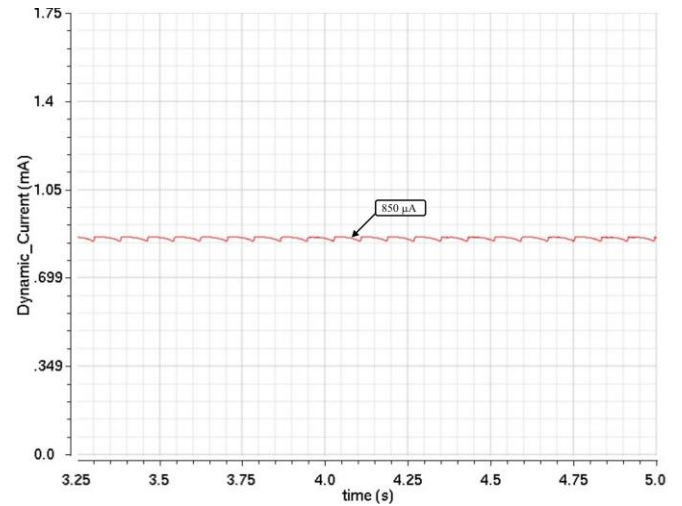

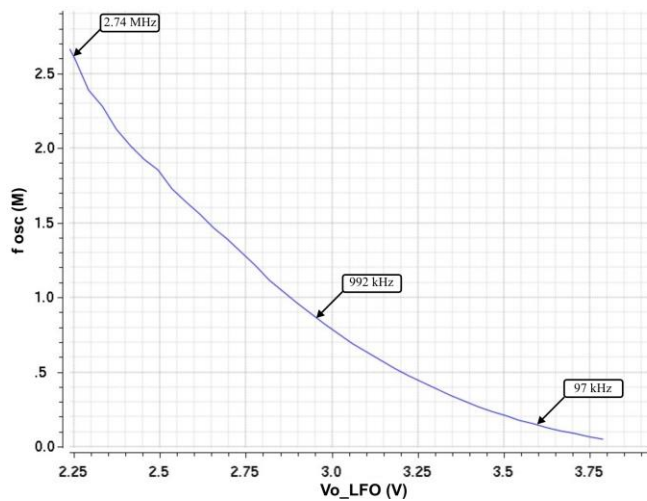Fig. 8. Average current consumption of the programmable VCRO circuit.

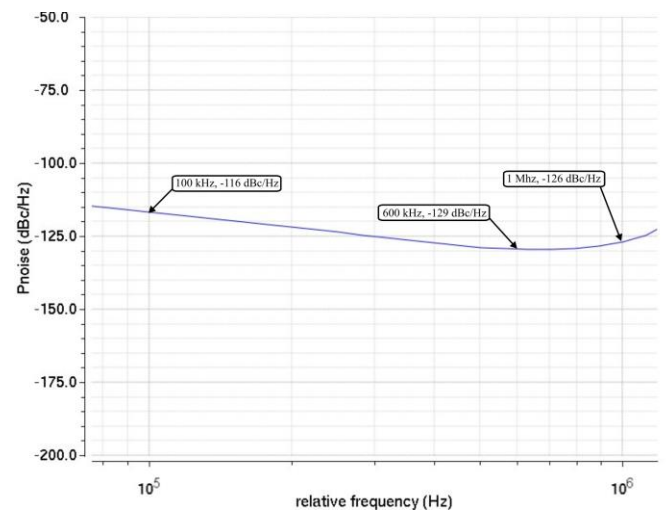Fig. 6. Tuning range of the VCRO circuit.

Fig. 9. Phase noise of the VCRO circuit.

where k_p is a transconductance parameter, V_{Thp} is threshold voltage, $(W/L)_{1,2}$ is the aspect ratio of pMOS transistors, and

V_{DD} is power supply. From (5) it is evident that for getting high values of t_d, $(W/L)_{p1,p2,n1,n2} < 1$. Here we have used $(W/L)_{p1,p2} = 1.5\ \mu m/10.0\ \mu m$, and $(W/L)_{n1,n2} = 1.5\ \mu m/10.0\ \mu m$, and $(W/L)_{n0} = 1.5\ \mu m/10.0\ \mu m$ to achieve $t_d = 2\ \mu s - 0.2\ \mu s$ (for each stage) corresponding to 100 kHz – 1 MHz frequency range of VCRO circuit.

III. Simulation results and discussions

Simulations of the designed circuit were made in Spectre from Cadence using the OnSemiconductor Process Design Kit (PDK). Fig. 4 shows the transient response of the digital control circuit. This response was obtained changing the logic values of the inputs *A* and *B* of the block Digital_control_LFO (Fig. 1) every second. The output is the level voltage that activates the four different frequencies of the LFRO circuit (Fig. 2). With 26 mV in the input CNTL_LFO a constant signal (no frequency) with 3.6 V of amplitude is generated at the output Vo_LFO, with 497 mV an output signal with 980 mVpp of amplitude and a frequency of 1 Hz is generated, similarly with 637 mV an output signal of with 1.35 Vpp of amplitude and a frequency of 5 Hz is generated, and finally with 679 mV an output signal of 1.52 Vpp of amplitude and a frequency of 5 Hz is generated.

Figure 5 shows the output signal Vo_LFO of the LFRO circuit, these four different ramp signals will generate four different frequency sweeps in VCRO circuit and different repetition time of these frequency sweeps. It can be seen a circuit discharge time bigger than the circuit charge time, this kind of ramp signal will produce that the VCRO will pass from the maximum operation frequency to the minimum operation frequency in a gradual mode.

Figure 6 shows the tuning range of the VCRO circuit from 97 kHz to 2.74 MHz, for a Vo_LFO voltage range from 2.25 V to 3.69 V. It represents a wide range of operation frequencies for RFD applications [1]. Out of this range the signal can not be considered for RFD applications [12].

Figure 7 presents an example of the output signal of the VCRO circuit, with a frequency sweep from 50 kHz to 1 MHz. This signal needs to be amplified to get a correct signal that can be used directly in patients for healing injured muscle tissues, as do not portable commercial RFD equipment [4].

Figure 8 presents the average current consumption of 850 µA of the entire circuit, as can be noticed, the proposed circuit has an average power consumption of 4.2 mW. This power consumption meets the requirements only for the blocks designed and presented in this work. The amplification block will have a large power consumption compared with the power consumption of this work.

In Fig. 9 we can see a phase noise decreasing linearly from of -116 dBc/Hz at 100 kHz to -129 dBc/Hz at 600 kHz, then an increase of -126 dBc/Hz at 1 MHz of useful frequency range. The phase noise indicated that VCRO circuit generates a stable signal in frequency terms to get the expected results in medical therapy [1].

IV. Conclusions

In this paper we have presented the design and simulation results of a programmable CMOS VCRO circuit intended for RF diathermy. Our VCRO generates a signal with a controllable amplitude and frequency in the tuning range of 100 KHz to 1 MHz. It includes a LFO structure based on current starved delay cells with variable resistors to get frequencies as low as 1 Hz. It also includes a VCO structure with differential delay cells to minimize phase noise, with minimal (W/L) ratios in order to minimize power consumption and layout area. The digital control circuit employed in our VCRO generates four different operation modes with two input signals for the LFO circuit. Simulation results show 850 µW of average power consumption of the complete designed circuit, as well as a phase noise in the range of -116 dBc/Hz to -126 dBc/Hz in the desired frequency range, meeting the requirements for commercial RFD devices.

Acknowledgement

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