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Reconfigurable FIR Filter Coefficient Optimization in Post-Silicon Validation to Improve Eye Diagram for Optical Interconnects

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***Abstract*— Enhanced small form-factor pluggable (SFP+) is a specification for a new generation of optical modular transceivers. The devices are designed for use with small form factor (SFF) connectors, and offer high speed and physical compactness. SFP+ modules require high-quality ASIC/SerDes transmitters (Tx) because IEEE and fibre channel standards place strict requirements on the optical interface, and linear/limiting SFP+ module types have Tx paths that do not correct for timing jitter. This introduces a design challenge to guarantee performance over process, temperature, and voltage (PVT) conditions. Adjusting the Tx equalization across PVT and different interconnect channels can be a time-consuming task in post-silicon validation. In order to overcome this problem, this paper proposes a direct optimization method based on a suitable objective function formulation to efficiently tune the Tx equalizer and optimize the eye diagram to successfully comply with industrial specifications.**

***Index Terms* — equalization, Ethernet, eye diagram, FIR, HSIO, ISI, optimization, post-silicon validation, signal integrity, SFP, tuning, transmitter.**

I. Introduction

The development of high speed Internet has driven data-transmission technology to fully commercialize on 10 Gbps data rates. One of the key components in the physical layer (PHY) is the transceiver module, which enables transmit and receive operations at the end of each fiber optic link. Transceiver modules, such as some Ethernet protocols like 10-Gigabit Small Form Factor Pluggable (XFP/SFP) and Enhanced SFP (SFP+), are regulated by specifications that ensure consistency between suppliers with requirements for eye mask measurements. These eye mask definitions specify transmitter (Tx) output performance in terms of voltage amplitude and time to ensure far-end receivers (Rx) can reliably recognize the two logic levels in the presence of timing noise and jitter [1]. However, as technology moves towards higher data rates, inter-symbol interference (ISI) has a significant impact on signal integrity and timing, which results in poor eye diagrams [2]. ISI is defined as one logic symbol interfering with a subsequent symbol; it is typically caused by channel impairments such as frequency dependent losses [3], mode conversion, and multiple reflections due to characteristic impedance discontinuities. In order to mitigate ISI and other undesired effects, adding pre-emphasis and de-emphasis circuits at the Tx is extensively used to adjust the signal prior to the influence of the channel [4]. Because of their inherent stable response and easily achievable linear phase property, the finite impulse response (FIR) filter is commonly used for emphasis circuits [4]. The core operations in FIR filters involves multiplication and accumulation of filter coefficients with the input digital data, and those can be realized using as many multipliers and adders as the number of filter coefficients, respectively [5]. Per IEEE standard for Ethernet section 5, clause 77 [6], the equalization for SFP+ Tx may be accomplished with a feed-forward equalizer (FFE) 3-tap FIR filter, where C_m, C_0 and C_p represent the three filter coefficients.

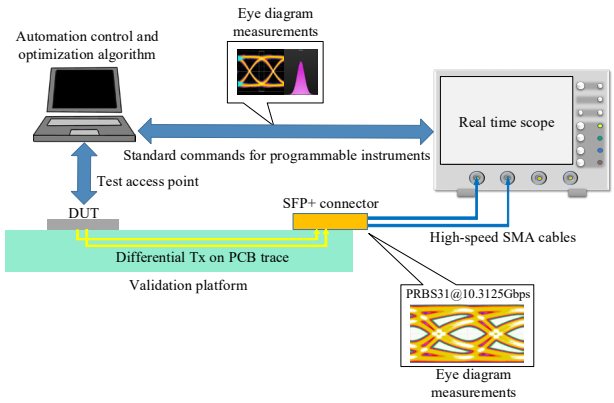

Fig. 1. Test setup for SFP+ Tx optimization.

The output signal of the FIR filter is represented as

$$y(t) = \sum_{i=0}^{N} c_i x\left(t - iT_d\right) \quad (1)$$

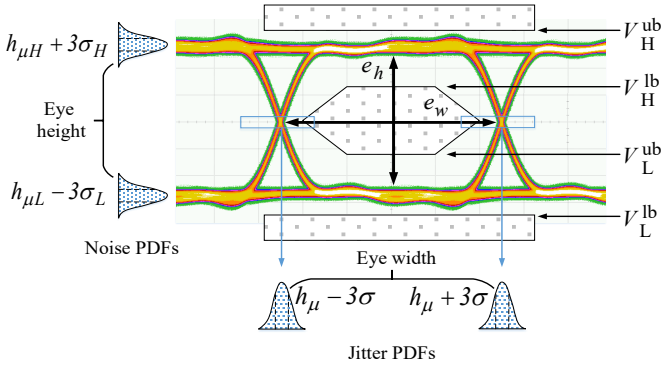

Fig. 2. Eye diagram and mask.

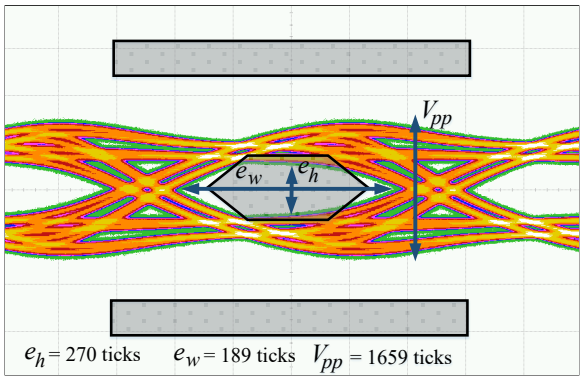

Fig. 3. Eye diagram over mask before optimization.

where c_i are the tap coefficients, N is the total tap number, and the delay per tap T_d is 1 unit interval (UI). The filter response can be adjusted by controlling the tap number and coefficients values.

Many simplifications in the FIR design implementation can be made when the coefficients are constant. However, FIR filters with reconfigurable coefficients are required in many application scenarios [7], where the filter order can be dynamically changed depending on the amplitude of both the filter coefficients and the inputs. These filters are useful for equalization techniques in high-speed input/output (HSIO) links to cancel any undesired effect, such as Tx jitter, attenuation or ISI, among others [8]. SFP+ Tx FIR filter is not self-adaptive, and then tuning is required during post-silicon validation. The current post-silicon practices to perform the coefficients tuning are based on an exhaustive enumeration method that consumes a large amount of validation time and resources. A recent work [9] proposed a new methodology based on an empirical algorithm that improves substantially the time for SFP coefficients tuning, but still requires days to obtain a set of optimal coefficients values. There have been several FIR filter coefficients optimization techniques reported in the literature [5], [7], [10]; however, all of these techniques are applied only at design simulation level.

In this paper, we propose a simple yet efficient optimization technique for a reconfigurable FIR filter used in a SFP+ Tx, by defining an effective objective function and by using direct numerical optimization in a post-silicon validation platform.

Our paper is organized as follows. Sections II and III describe the system test setup and system measurements, respectively. An overview about post-silicon tuning is presented in Section IV. The objective function formulation and the optimization procedure are presented in Section V. Finally, Sections VI and VII present the results obtained and our conclusions, respectively.

II. System Test Setup

The test setup is shown in Fig. 1. The eye diagram of the device under test (DUT) is measured at the end of the SFP+ connector using subminiature (SMA) cables connected to a high-speed, real time oscilloscope. The oscilloscope must have enough bandwidth capabilities to measure at least the 5th harmonic of the incoming signal and capabilities for S-parameters de-embedding to eliminate cables insertion loss. A computer executes the algorithm using a fully automated control by accessing the DUT through the test access points (TAP) registers for the FFE coefficients, sending instruments commands for eye diagram, jitter and histogram measurements on the scope.

III. System Measurements

An eye diagram is a useful tool for understanding signal impairments in the PHY of HSIO data systems, verifying Tx output compliance, and revealing the amplitude and time distortion elements that degrade the bit error rate (BER) for diagnostic purposes. Histograms are used to statistically analyze time and amplitude data of eye diagrams, offering important computational information when observing impairments in HSIO signals. The definition for eye height is derived from computing the difference between the inner 3σ points on the inside of the histograms of the one and zero levels, as shown in Fig. 2, where σ is the standard deviation of the histograms. The eye width is essentially the effective distance between the inner two 3σ points on the time histograms. To compute jitter, the time variances of the rising and falling edges of an eye diagram at the crossing point are captured, as shown in Fig. 2. The time histogram, shown below the eye pattern, is analyzed to determine the amount of jitter. The peak-to-peak jitter is defined as the full width of the histogram, meaning all data points present.

IV. Post-Silicon Tuning

As process technologies scale down, traditional circuit design methodologies are challenged by the problem of silicon process variation. Different techniques exist to maximize the parametric yield based on statistical design for analog circuits, and these techniques usually fall into two categories: design-time optimization and post-silicon tuning [11].

Design-time optimization techniques explore the design space at system-level and device-level to maximize the yield for analog circuits. However, accurate simulations for non-

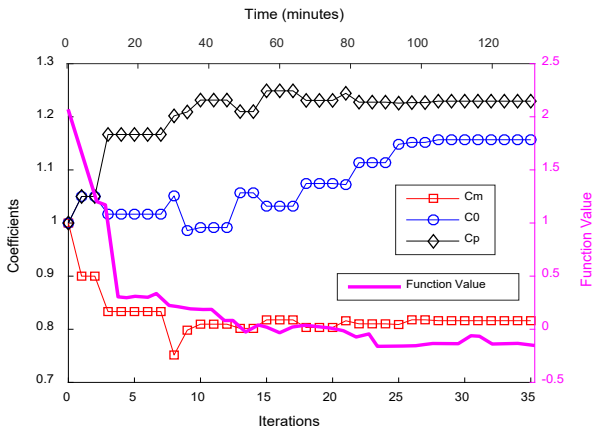

Fig. 4. Normalized coefficients responses and function values across iterations.

linear circuits, which are dominant in digital CMOS circuits, are computationally very expensive given the complexity of the system involved. Transistors are coupled with the IC interconnects, whose electrical properties cannot be ignored in deep submicron design [12]. On the other hand, post-silicon tuning in analog design has been widely adopted to confront the silicon process variation. Tunable elements are proposed to adjust the analog circuit performance after chip fabrication [13], [14]. These tunable elements provide a way to reconfigure I/O links in post-silicon to cancel out the effects of system channels' variability [8]. PHY tuning settings include: parameters of an equalizer at the Tx, Rx, or both; the clock and data recovery circuit settings; the variable gain amplifier; baud-spaced FFE in the Tx, and the bias voltages or currents values, among others [15]. A typical system may have hundreds of combinations of just equalization parameter values. Finding the optimal PHY settings that guarantee the BER required by an industrial specification is called PHY tuning. In the worst case, this means sweeping all possible combinations of all PHY settings, which is prohibitive in the post-silicon validation time frame [15].

V. Objective Function Formulation and Optimization

Let $\boldsymbol{R}_E \in \Re^3$ denote the signal integrity system response, which consists of the eye amplitude histogram mean high $h_{\mu H}$, the histogram mean low $h_{\mu L}$, and the total jitter J_T on the eye diagram,

$$\boldsymbol{R}_E = \boldsymbol{R}_E(\boldsymbol{x},\boldsymbol{\psi}) = \left[h_{\mu H}(\boldsymbol{x},\boldsymbol{\psi}) \quad h_{\mu L}(\boldsymbol{x},\boldsymbol{\psi}) \quad J_T(\boldsymbol{x},\boldsymbol{\psi})\right]^T \quad (2)$$

This signal integrity system response is a function of the PHY tuning settings $\boldsymbol{x} \in \Re^N$ (FIR tap coefficients), and the operating conditions $\boldsymbol{\psi}$ (voltage and temperature). The eye height $e_h \in \Re$ is obtained from,

$$e_h(\boldsymbol{x},\boldsymbol{\psi}) = h_{\mu H}(\boldsymbol{x},\boldsymbol{\psi}) + 3\sigma_H + h_{\mu L}(\boldsymbol{x},\boldsymbol{\psi}) - 3\sigma_L \quad (3)$$

where σ_H and σ_L are the standard deviation of the histogram mean high and the histogram mean low, respectively.

Since we want to maximize the eye diagram, our initial objective function consists of $-e_h$, however as the eye width is a function of the total jitter J_T, we must consider J_T in the objective function formulation.

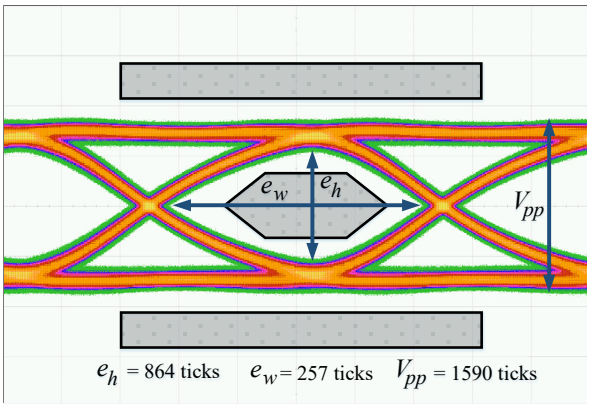

Fig. 5. Eye diagram over mask after optimization.

The e_h and J_T must be scaled by weighting factors w_1, w_2, $\in \Re$ such they become comparable. The values of these weighting factors can be selected by using initial e_h, and J_T measurements.

Therefore, the objective function is defined as

$$u(\boldsymbol{x}) = -w_1\left[e_h(\boldsymbol{x},\boldsymbol{\psi})\right] + w_2\left[J_T(\boldsymbol{x},\boldsymbol{\psi})\right] \quad (4)$$

with w_1, and w_2 are calculated from

$$w_1 = \frac{2}{\frac{1}{k}\sum_{i=1}^{k} e_h(\boldsymbol{x}^{(i)})} \quad (5)$$

$$w_2 = \frac{1}{\frac{1}{k}\sum_{i=1}^{k} J_T(\boldsymbol{x}^{(i)})} \quad (6)$$

where $\boldsymbol{x}^{(i)}$ are k randomly distributed base points for initial measurements of eye height and total jitter.

The optimization problem for the signal integrity system is

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} u(\boldsymbol{x}) \quad (7)$$

with $u(\boldsymbol{x})$ defined by (4).

We will now modify the optimization problem such that the optimal set of coefficients maximizes the eye diagram without exceeding the mask limits. The new optimization problem can be defined through a constrained formulation,

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} u(\boldsymbol{x}) \text{ subject to } l_1(\boldsymbol{x}) \le 0,\ l_2(\boldsymbol{x}) \le 0 \quad (8)$$

with

$$l_1(\boldsymbol{x}) = (h_{\mu H} + 3\sigma_H) - V_H^{ub} \quad (9)$$

$$l_2(\boldsymbol{x}) = V_L^{lb} - (h_{\mu L} - 3\sigma_L) \quad (10)$$

where $V^{ub}{}_H$ and $\underline{V}^{lb}{}_L$ are the eye mask specification limits: voltage high upper bound, and voltage low lower bound, respectively. A more convenient unconstrained formulation can be defined by adding a penalty term, as

$$U(\boldsymbol{x}) = -u(\boldsymbol{x}) + \rho_0^l \left|L(\boldsymbol{x})\right|^2 \quad (11)$$

where $L(\boldsymbol{x})$ is the eye mask limit penalty function, defined as

$$L(\boldsymbol{x}) = \max\{0, l_1(\boldsymbol{x}), l_2(\boldsymbol{x})\} \quad (12)$$

The optimal solution depends on the value of the penalty

coefficient $\rho_0^l \in \Re$,. We define ρ_0^l as

$$\rho_0^l = \frac{|u(\boldsymbol{x}^{(0)})|}{\left|\max\{l_1(\boldsymbol{x}^{(0)}), l_2(\boldsymbol{x}^{(0)})\right|^2} \quad (13)$$

where $\boldsymbol{x}^{(0)}$ is the starting point. Then, our objective function to optimize eye diagram and meet eye mask specification is

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} U(\boldsymbol{x}) \quad (14)$$

with

$$U(\boldsymbol{x}) = -w_1\left[e_h(\boldsymbol{x},\boldsymbol{\psi})\right] + w_2\left[J_T(\boldsymbol{x},\boldsymbol{\psi})\right] + \rho_0^l\left|L(\boldsymbol{x})\right|^2 \quad (15)$$

We aim at finding the optimal set of FIR coefficients values $\boldsymbol{x}^*$ by solving (14) using the Nelder-Mead method [16].

VI. Results

A pseudo-random bit sequence (PRBS) of length $(2^{31} - 1)$ - PRBS31 - is considered the standard for stressing HSIO circuits to achieve a confidence level in the operating margins of a product. PRBS31 provides a stressful environment to detect random jitter (RJ), sinusoidal jitter (SJ), ISI, and crosstalk. When the input signal to the FIR becomes a PRBS31 with a data rate of at 10.3125Gbps, the resultant eye diagram is shown in Fig. 3. Since the FFE tap coefficients are not properly equalized, the eye diagram is significantly distorted, with an eye height and eye width of 270 ticks and 189 ticks, respectively. Such e_h and e_w levels are so low that do not meet the required eye mask. Fig. 3 also shows the zero crossing points on the horizontal axis are not compressed enough, leading to high jitter measurements. In terms of the vertical axis, the voltage peak-to-peak is 1,659 ticks, which translates into wider noise histograms. Hence, we are looking to optimize the Tx equalization coefficients as a way to compensate for the channel effects, achieving an specifications compliant eye diagram.

Through the optimization process defined in Section V, we arrive to a set of Tx coefficients in just 35 iterations, as shown in Fig. 4. The optimized equalization coefficients improve substantially with an e_h and e_w, as shown in Fig. 5, being now 864 ticks and 257 ticks, respectively, which corresponds to an improvement of 252% on eye diagram area as compared to that one with the initial coefficients. The efficiency of this approach was also demonstrated by a significant time reduction on post-silicon validation. While the traditional process requires 4 days for a complete optimization using an exhaustive approach, the method proposed here can be completed in just 2 hours.

VII. Conclusion

We proposed a direct optimization approach to find the best Tx FIR filter settings to counteract ISI and other undesired effects in high-speed data transmission. The optimal set of FFE tap coefficients are determined by numerical optimization of an objective function expressed in terms of the required specifications on eye mask. Subsequently, the optimized coefficients are evaluated by measuring the real eye diagram of the physical system, showing a great mitigation of the ISI effects, and accelerating the typical required time for Tx coefficients tuning. Our approach allows fulfilling in an efficient manner strict IEEE and fibre channel standards as applied to high-speed interconnects based on optical interfaces, significantly enhancing current industrial practices in this arena.

Reference

[1] ANRITSU (2010). *Understanding Eye Pattern Measurements*, application note no. 11410-00533 (revision A) [Online]. Available: https://www.anritsu.com

[2] S. H. Hall, G. Hall, and J. A. McCall, *High-Speed Digital System Design:A Handbook of Interconnect Theory and Design Practice*, Hoboken NJ: Wiley 2000.

[3] W.-D. Guo, F.-N. Tsai, G.-H. Shiue, and R.-B. Wu, "Reflection enhanced compensation of lossy traces for best eye-diagram improvement using high-impedance mismatch," *IEEE Trans. Adv. Packag.*, vol. 31, no. 3, pp. 619-626, Aug. 2008.

[4] H. Higashi, S. Masaki, M. Kibune, S. Matsubara, T. Chiba, Y. Doi, H. Yamaguchi, H. Takauchi, H. Ishida, K. Gotoh, and H. Tamura, "A 5-6.4-Gb/s 12-channel transceiver with pre-emphasis and equalization," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 978-985, Apr. 2005.

[5] K. S. Reddy, S. K. Sahoo, "An approach for FIR filter coefficient optimization using differential evolution," in *Int. J. Electron. Commun. (AEÜ)*, 2015, vol. 65, no. 1, pp. 101–108

[6] *IEEE Standard for Ethernet*. IEEE Standard 802.3-2015.

[7] M. Kumm, K. Möller, P. Zipf, "Reconfigurable FIR Filter Using Distributed Arithmetic on FPGAs," in *IEEE Int. Symp. Circuits and Systems (ISCAS)*, Kuala Lumpur, Malaysia, May 2013.

[8] F. Rangel-Patino, A. Viveros-Wacher, J. E. Rayas-Sanchez, E. A. Vega-Ochoa, I. Duron-Rosales, and N. Hakim, "A holistic methodology for system margining and jitter tolerance optimization in post-silicon validation," in *IEEE MTT-S Latin America Microw. Conf. (LAMC)*, Puerto Vallarta, Mexico, Dec. 2016, pp. 1-3.

[9] M. A. Dhanesh and J. Mendoza-Bonilla, "Ethernet SFI Transmitter Optimization," in *Intel 11th Joint Seminar on Signal and Power Integrity*, Santa Clara, CA, Jan. 30, 2017.

[10] Y. S. Cheng, Y. C. Lai, and R. B. Wu, "Optimization of FIR filter to improve eye diagram for general transmission line systems," in *Design, Automation & Test in Europe Conference & Exhibition*, Dresden, Germany, April 2010, pp. 1321-1324.

[11] W. Yao, Y. Shi, L. He, S. Pamarti, "Joint Design-Time and Post-Silicon Optimization for Digitally Tuned Analog Circuits," in *2009 IEEE/ACM Int. Conf. on Computer-Aided Design*, San Jose, CA, Nov. 2009, pp. 725-730.

[12] Z. Wang, J. Zhu, "Transistor-Level Static Timing Analysis by Piecewise Quadratic Waveform Matching," in *Design, Automation and Test in Europe Conference and Exhibition*, Washington, DC, March 2003, pp 1026–1031.

[13] H. Huang and E. K. F. Lee, "Design of low-voltage CMOS continuous time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1168-1177, Aug. 2001.

[14] G. Miller, M. Timko, H.-S.Lee, E. Nestler, M. Mueck, and P. Ferguson, "Design and modeling of a 16-bit 1.5msps successive approximation adc with non-binary capacitor array," in *Proc. Int. Great Lakes Symp. on VLSI*, Washington, D. C, April 2003, pp. 161 - 164

[15] C. Gu, "Challenges in post-Silicon validation of high-speed I/O links," in *Proc. Intl. Conf. on Computer-Aided Design (ICCAD), IEEE/ACM*, San Jose, CA, Nov. 2012, pp. 547-550.

[16] J. C. Lagarias, J. A. Reeds, M. H. Wright, and P. E. Wright, "Convergence properties of the Nelder-Mead simplex method in low dimensions," *SIAM J. on Optimization*, vol. 9, no. 1, pp. 112–147, 1998.