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A Holistic Methodology for System Margining and Jitter Tolerance Optimization in Post-Silicon Validation

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***Abstract* — The optimization of receiver analog circuitry in modern high-speed input/output (HSIO) links is a very time consuming post-silicon validation process. Current industrial practices are based on exhaustive enumeration methods to improve either the system margins or the jitter tolerance compliance test. In this paper, these two requirements are addressed in a holistic optimization-based approach. We propose an innovative objective function based on these two metrics. Our method employs Kriging to build a surrogate model based on system margining and jitter tolerance measurements. The proposed method is able to deliver optimal system margins and guarantee jitter tolerance compliance while substantially decreasing the typical post-Si validation time.**

***Index Terms* — margining, jitter tolerance, equalization, optimization, post-silicon validation, Kriging.**

I. Introduction

Equalization (EQ) techniques are used in high-speed input/output (HSIO) links to cancel any undesired effect such as transmitter (Tx) jitter, attenuation or inter-symbol interference (ISI), among others [1], [2]. The current industrial practices to perform the EQ knobs tuning are based on an exhaustive enumeration method that consumes a large amount of the post-silicon validation schedule and resources [3]-[5]. To perform knob tuning, either receiver (Rx) eye diagram margins [6] are measured and optimized, or jitter tolerance (JTOL) tests [7] are executed until measurements comply with the link specifications. Then, a trade-off analysis is done to arrive at a single set of EQ values that satisfy both test scenarios.

This paper presents a holistic approach to concurrently optimize Rx system margins and JTOL, by defining an objective function that combines both type of measurements, and by using a Kriging surrogate-based modeling approach to efficiently perform optimization.

The paper is organized as follows. Section II describes the system test setup. Section III provides a summary of the system measurements. An overview on knobs tuning is presented in Section IV. The objective function formulation is presented in Section V and the surrogate model and optimization technique are described in Section VI. Finally, Sections VII and VIII present the results obtained and our conclusions, respectively.

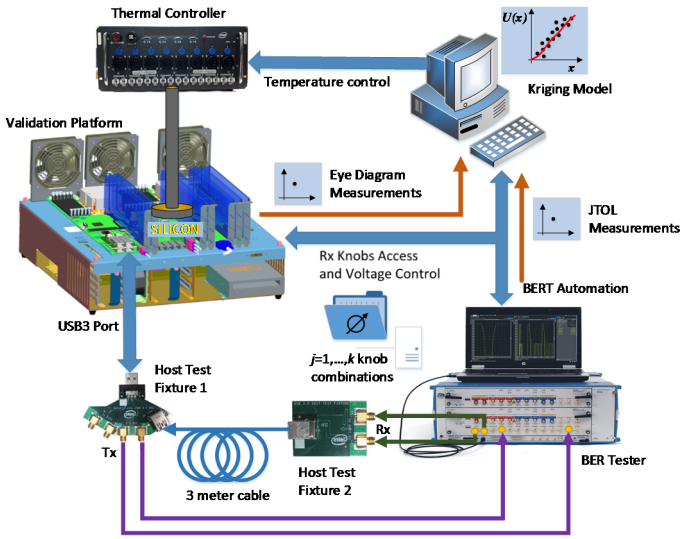

Fig. 1. The holistic methodology test setup for USB system margining and JTOL optimization.

II. System Description

The test setup is shown in Fig. 1. We stress the Rx with a bit error rate (BER) tester, sending a USB3 compliant pattern including all jitter impairments as per specification. The channel configuration is set as "far-end" using test fixtures and a 3-meter cable. The host computer is capable of accessing Rx knobs and sending commands to the BER tester in order to increase the jitter amplitude and frequencies. Then, we record system margins and sweep the jitter amplitude at the specification frequencies to obtain JTOL results.

III. System Measurements

There are two main measurements that are being used during the knobs tuning process at post silicon validation: system margins and JTOL measurements.

A. System Margins Test

Measuring system margins involves determining how the BER of a specific bus changes when several environmental and operating conditions are varied. The method consists on adjusting the silicon operating conditions (voltage, temperature), then measure the Rx's width and height of the functional eye diagram by adjusting a specific on-die design for test (DFT) hook until the eye opening has been shrunk to a point where the Rx detects errors or the system fails.

B. Jitter Tolerance Test

By encoding the clock into the data stream, the clock and data recovery (CDR) circuitry guarantees that the clock and data are in phase when the jitter frequency is in the bandwidth of the CDR. However, if there is high frequency jitter in the data stream, the CDR may not track the data and the jitter may cause bit errors. The goal for JTOL testing of an Rx architecture is to verify that it can operate at a target BER when operating under worst case signaling conditions. The Rx under test must have the capability to tolerate a stressed signal without errors in the decoded patterns during a certain amount of time. The pass/fail criterion is given by the specification limits, known as mask.

IV. Knobs Tuning

There are several knobs available in the physical layer design for both the Tx and Rx, which aim to compensate for the channel effects on the HSIO link. Those knobs typically include: parameters of an equalizer at the Tx, Rx or both; parameters of the CDR circuitry; variable gains in amplifiers; voltage bias or currents, etc. The process of setting the knobs to the optimum value that guarantee the BER required by an industrial specification to achieve optimal system performance is called knobs tuning.

V. Objective Function Formulation

Let $\boldsymbol{R}_{\mathrm{m}} \in \Re^2$ denote the electrical system margins response, which consists of the width and height of the functional eye diagram,

$$\boldsymbol{R}_{\mathrm{m}} = \boldsymbol{R}_{\mathrm{m}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = \left[e_{\mathrm{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \quad e_{\mathrm{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right]^T \tag{1}$$

where $e_{\mathrm{w}} \in \Re$ and $e_{\mathrm{h}} \in \Re$ are the width and height of the eye diagram. We aim at finding the optimal set of knobs coefficients to maximize the functional eye diagram area. Therefore, the initial objective function is given by

$$u(\boldsymbol{x}) = \left[e_{\mathrm{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right]\left[e_{\mathrm{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] \tag{2}$$

The eye width and height are function of the knobs ($\boldsymbol{x}$), the operating conditions ($\boldsymbol{\psi}$), and function of the devices ($\boldsymbol{\delta}$). Based on the operating conditions and devices, the eye diagram can be decentered with respect to the eye-width (asymmetry e_{wa}), eye-height (asymmetry e_{ha}) or both. Hence, the objective function must consider the asymmetries. The area of the eye diagram and the asymmetries must be scaled by weighting factors $w_1, w_2, w_3 \in \Re$ such they become comparable. Hence, a better objective function is defined as

$$\begin{aligned} u(\boldsymbol{x}) = {} & w_1\left[e_{\mathrm{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right]\left[e_{\mathrm{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] - w_2\left[e_{\mathrm{wa}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] \\ & - w_3\left[e_{\mathrm{ha}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] \end{aligned} \tag{3}$$

The optimization problem for system margining is then defined as,

$$\boldsymbol{x}^* = \arg\max_{\boldsymbol{x}} u(\boldsymbol{x}) \tag{4}$$

The holistic approach is realized by adding a JTOL penalty function to the optimization problem, such that the optimization finds a set of EQ knobs settings that maximize the functional eye diagram and simultaneously satisfies the JTOL specified mask. The JTOL system response, $\boldsymbol{R}_{\mathrm{J}} \in \Re$, consists of measurements of the sinusoidal jitter amplitude,

$$\boldsymbol{R}_{\mathrm{J}} = \boldsymbol{R}_{\mathrm{J}}(\boldsymbol{x},\boldsymbol{\psi}) = S_{\mathrm{JA}}(\boldsymbol{x},\boldsymbol{\psi}) \tag{5}$$

where S_{JA} is the sinusoidal jitter amplitude. The optimization problem is then defined as

$$\boldsymbol{x}^* = \arg\max_{\boldsymbol{x}} u(\boldsymbol{x}) \quad \text{subject to } \boldsymbol{g}(\boldsymbol{x}) \le 0 \tag{6}$$

where $\boldsymbol{g}(\boldsymbol{x})=S_{\mathrm{JAspec}}-S_{\mathrm{JA}}$; S_{JAspec} is the JTOL spec mask.

Considering (3), we can define an optimization problem that covers both the electrical margining system and the JTOL system responses by maximizing

$$U(\boldsymbol{x}) = u(\boldsymbol{x}) - r_0^g \left\|\boldsymbol{G}(\boldsymbol{x})\right\|_2^2 \tag{7}$$

where $\boldsymbol{G}(\boldsymbol{x})$ is the JTOL penalty function defined as,

$$\boldsymbol{G}(\boldsymbol{x}) = \max\{\boldsymbol{0}, \boldsymbol{g}(\boldsymbol{x})\} \tag{8}$$

The optimal solution depends on the value of the penalty coefficient $r_o^g \in \Re$. Therefore, the overall (holistic) objective function is defined as

$$\begin{aligned} U(\boldsymbol{x}) = {} & w_1\left[e_{\mathrm{w}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right]\left[e_{\mathrm{h}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] - w_2\left[e_{\mathrm{wa}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] \\ & - w_3\left[e_{\mathrm{ha}}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] - r_0^g \left\|\boldsymbol{G}(\boldsymbol{x})\right\|_2^2 \end{aligned} \tag{9}$$

VI. Surrogate Model and Optimization

To solve (9), we consider an optimization algorithm that uses Kriging as the surrogate-based approximation method.

A. Design of Experiments

Kriging's numerical stability requires that the points being selected for fitting be spread as far as possible from each other. We selected a low discrepancy sequence algorithm for the design of experiments (DOE), which guarantee to cover the space as uniformly as possible for the selected number of points.

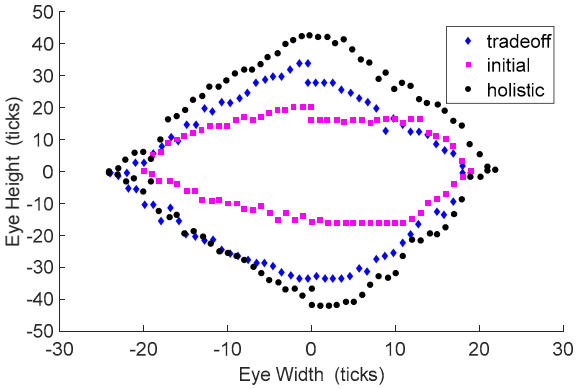

Fig. 2. Eye width versus eye height results: comparing the proposed methodology against the initial design and the trade-off approach.

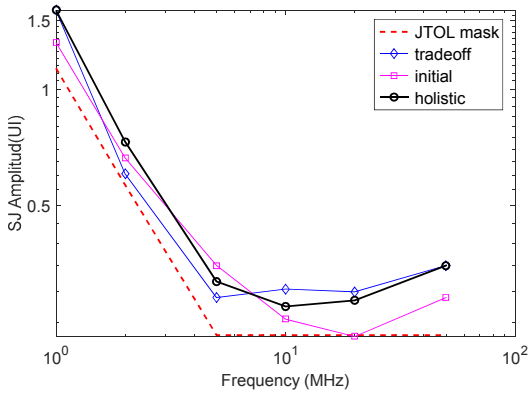

Fig. 3. Jitter tolerance (JTOL) testing results: comparing the proposed methodology against the initial design and the trade-off approach.

B. Kriging Modeling

Kriging is a reliable technique [8] already coded in a Matlab toolbox named DACE [9] that allows to set up and evaluate Kriging-based models in an efficient way.

We use the so-called ordinary Kriging [8] that estimates deterministic function f as

$$f_p(\boldsymbol{x}) = \mu + \varepsilon(\boldsymbol{x}) \;;\; E(\varepsilon) = 0 \;;\; \mathrm{cov}(\varepsilon(\boldsymbol{x}^i), \varepsilon(\boldsymbol{x}^j)) \neq 0 \forall i, j \quad (10)$$

where μ is the mean of the response at base points ($\boldsymbol{x}$), and ε is the error with zero expected value, and with a correlation structure being a function of a generalized distance between the base points. Once the Kriging model is built using a set of training data, the parameters of the model have to be estimated to give the best fit to the training data. For optimization purpose, we use the DACE toolbox that takes advantage of the Matlab optimization toolbox.

VII. Results

The holistic methodology proposed in this paper was tested in a post-silicon industrial environment, using an Intel server platform, comprised mainly of a CPU and a platform controller hub (PCH). The PCH is a family of Intel microchips which controls data paths and support functions used in conjunction with the Intel CPU through direct media interface (DMI). Within the PCH, our methodology was tested on a USB3 Super-speed Gen 1 HSIO link [10]. The channel topology is comprised of the Tx driver, the Tx based board transmission lines (TL), several via transitions, an I/O card connector, an internal cable that attaches a daughter card, followed by an external cable at which is attached at the other end another connector for the Rx I/O card, followed by another set of TL, and DC blocking capacitors at the Rx side of the device. The bandwidth limitations and inherent non-idealities of this system essentially result from the large amount of interconnects. Hence, we are looking to optimize the Rx equalization settings as a way to compensate for the channel limitations.

The Rx knobs settings obtained through the optimization process were verified by measuring both the Rx inner eye height/width and jitter tolerance of the PCH. The optimized knobs setting showed an improvement of 175% on eye diagram area as compared to the initial knobs setting, and a 34% improvement as compared with the traditional (tradeoff) approach, as shown in Fig. 2. Similarly, the jitter tolerance results showed a substantial improvement with margins well above the specification limit template, as seen in Fig. 3. The efficiency of this approach was also demonstrated by a significant time reduction on post-Si validation. While the traditional process requires days for a complete optimization, the method proposed here can be completed in a few hours.

VIII. Conclusion

Product complexity, performance requirements and time-to-market commitments have added tremendous pressure on post-Si validation. Therefore, validation teams have to continuously look for opportunities that make validation faster and cheaper. In this paper we demonstrated a holistic optimization approach that merges system margining and jitter tolerance measurements to optimize the receiver analog circuitry knobs during industrial post-silicon validation. The method uses Kriging to build a surrogate model for efficient optimization, and a novel objective function based on system margining and jitter tolerance measurements. Our experimental results, based on a real industrial validation platform, demonstrated the efficiency of our method to deliver optimal margins while guaranteeing jitter tolerance compliance, showing a substantial improvement for both system margins and jitter tolerance as compared with the current industrial practice, accelerating the typical required time for knobs tuning.

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