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Jitter Tolerance Acceleration Using the Golden Section Optimization Technique

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***Abstract*— Post-silicon validation of high-speed input/output (HSIO) links is a critical process for product qualification schedules of computer platforms under the current time-to-market (TTM) commitments. The goal of post-silicon validation for HSIO links is to confirm design robustness of both receiver (Rx) and transmitter (Tx) circuitry in a real application environment. One of the most common ways to evaluate the performance of a HSIO link is to characterize the Rx jitter tolerance (JTOL) performance by measuring the bit error rate (BER) through the link under worst stressing conditions. However, JTOL testing is very time-consuming when executing at specification BER, and the testing time is extremely increased when considering manufacturing process, voltage, and temperature (PVT) test coverage for a qualification decision. In order to speed up this process, we propose a new approach for JTOL testing based on the golden section algorithm. The proposed method takes advantage of the fast execution of the golden section search with a high BER, while overcoming the lack of correlation between different BERs by performing a downward linear search at the actual target BER until no errors are seen. Our proposed methodology is validated by implementing it in a server HSIO link.**

***Index Terms*— jitter, jitter tolerance, HSIO link, golden section, bit error rate, post-silicon validation.**

I. Introduction

Today advanced microprocessors and system on chip (SoC) must be compatible with many operating systems, hundreds of hardware devices, and software applications. The combined effects of increased product complexity, performance requirements, and time-to-market (TTM) commitments have added tremendous pressure on post-silicon validation. These challenges the validation teams to continuously assess their methodologies and look for opportunities to make validation faster and cheaper [1].

Post-silicon validation considers testing hundreds of silicon samples in realistic application environments, with the goal to check for robustness of the design by performing measurements on both receiver (Rx) and transmitter (Tx) circuitry of the high-speed input/output (HSIO) links. These measurements have to comply with electrical standards and ensure that the design can operate under worst stressing conditions [2]. One of the most common ways to measure the performance of a HSIO link is by measuring the bit error rate (BER) through the link [3]. The fewer the errors measured, the better the performance of the link. BER measurement is typically used to characterize the Rx jitter tolerance (JTOL) performance in order to determine compliance with the industry standard specifications, such as XAUI [4], PCIe [5], USB [6], and SATA [7]. The goal of JTOL is to verify that the Rx under test is capable to operate at a BER under worst case signaling conditions. The JTOL is usually measured with a BER tester instrument by sweeping the injected periodic jitter (J_P) amplitude across a range of frequencies until bit errors are detected. The test is considered to be passed when the measured error-free J_P amplitude is above the amplitude threshold defined by the protocol specification for each frequency point.

JTOL tests are very time-consuming when running at specification BER. For example, assuming a 95% confidence level and a target BER of 10^{-12}, it is necessary to transmit 3×10^{12} bits for each combination of J_P amplitude and frequency [8]. This roughly translates to 10, 8.3, and 6.3 minutes per testing point for USB3.0 [6], SATA3 [7], and PCIe3 [5], respectively. Therefore, a full JTOL test can take several hours. Even when JTOL tests are only executed on a few units, it takes a large amount of time to achieve appropriate process, voltage, and temperature (PVT) coverage for a qualification decision.

Some alternatives for JTOL test time reduction have been previously reported. In [9], a higher BER mask is presented as means to approximate a pass/fail criteria at a BER of 10^{-12} by slightly increasing the injected noise profile and executing the test at a BER of 10^{-10}. Another approach frequently used is to characterize the tolerated amplitude degradation between 10^{-10} and 10^{-12} tests. However, for both cases it is still needed to run a test at the spec BER to guarantee that the Rx passes the compliance test, mainly due to the lack of correlation between the 10^{-10} and 10^{-12} results. In [10], an extrapolation algorithm for JTOL is proposed. The goal of this extrapolation algorithm is to predict the jitter tolerance at low BER based on high BER region data with the objective to reduce the JTOL testing time. However, this algorithm fails when verified in a post-silicon validation compliance environment [11], as opposed to being used in high volume manufacturing testers. Under the high variation of measurements typically seen in system compliance tests, the linear regression of the Q factor [11] has a poor fit, which translates to poorly predicted values of J_P at low BER

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that do not correlate with real measurements.

This paper presents a new approach based on the golden section algorithm, which aims to accelerate the JTOL testing. The proposed method exploits the fast convergence of the golden section search with a high BER. The lack of correlation between different BERs is solved by performing a downward linear search at the actual target BER until no errors are seen. Our proposed approach is validated by testing it on a SATA HSIO links in a realistic server platform, demonstrating that the JTOL testing can be accelerated by more than an order of magnitude with respect to the current industrial practice.

The paper is organized as follows. Section II provides a brief description of post-silicon validation with emphasis in Rx and Tx compliance. Section III describes the JTOL testing. The proposed JTOL optimization is presented in Section IV. Finally, Sections V and VI present the results obtained and our conclusions, respectively.

II. Post-Silicon Validation

Post silicon validation is the stage from the product development of modern computer platforms where silicon is available at the laboratory and validation is performed by several groups or disciplines, such as functional validation (FV), bench design validation (BDV), and electrical validation (EV), among many others. All of these disciplines execute validation in parallel, each one focusing on different specifications, with the objective of qualifying a product over different operation conditions, process corners, and usage models [12].

Electrical validation focuses on the validation of several analog phenomena, such as the tuning of the so-called physical layer (PHY) [13], validation of the electrical parameters from the I/O links, power delivery, and clocks, as well as resilience to noise impairments such as crosstalk, inter symbol interference (ISI), etc.

HSIO interfaces have a Tx that sends a serial stream of bits with an embedded clock through a channel to the Rx. The Rx receives the incoming high-speed serial data, extracts the embedded clock, and determines a logical one or a logical zero for each bit received in the stream for further processing at the upper protocol layers.

Given that the data rate of HSIO interfaces is in the order of several gigabits per second (Gbps), the specifications associated to those interfaces regarding the timing budget is very stringent. This timing budget is reflected in several jitter specifications. On the Tx side, it is specified how much timing deviation the Tx can generate to consume the total jitter budget. Whereas on the Rx side, it specifies how much time deviation the Rx should tolerate before a false detection occurs. As noted in [14], "The traditional guaranteed by design paradigm cannot be applied anymore". Hence, the chip maker companies invest a lot of resources to do an exhaustive validation on the tight timing specifications to ensure their design and chip quality.

Many HSIO standards define the jitter performance at the BER of 10^{-12}, which requires a very long time to get a statistical valid measurement. Testing a representative number of parts on different operation conditions can increase the time exponentially, which cannot be afforded for the reduced validation times, which are continuously aimed to be reduced to achieve a competitive TTM. Hence, the need of suitable optimization algorithms to reduce the Rx JTOL testing time without compromising the quality on the validation becomes highly relevant.

III. Jitter Tolerance Testing

Jitter is the variation in time of a periodical signal [15]. In general, jitter sources are classified as random jitter (JR) and deterministic jitter (J_D), which combined form the total jitter (J_T). HSIO links specifications require the measurement of jitter components, which can be done by using different techniques, such as time interval error (TIE) measurement, jitter histograms, JTOL, and BER bathtub, among others. To perform a JTOL test, each protocol specification defines a calibration procedure prior to the JTOL execution. This procedure defines the specific jitter components injected to the test pattern, which remain constant throughout the JTOL test, such as J_R and ISI, while J_P is varied in both amplitude and frequency. The JTOL response R_J can therefore be defined as

$$R_J = u(J_P, f) \tag{1}$$

where J_P is the periodic jitter amplitude injected by the BER tester, and f is the frequency of the periodic jitter. The evaluation of u implies sending a certain amount of bits from the BER tester, receiving the data stream at the Rx of the device under test (DUT), looping back the data to the Tx of the DUT, and receiving it once again at the BER tester to check for bit errors. The equipment then computes the BER and returns a PASS if the measurement is above the target BER, or FAIL if there were more errors than those allowed to comply with the target BER. Therefore, u is a discrete function with continuous variables, and R_J is digital, since it can only have a PASS or a FAIL value. Given that there is usually a well-defined frontier between J_P values that yield a PASS and J_P values that yield a FAIL, u can be considered a unimodal function. Also, for a fixed value of f, the problem of finding the largest value of J_P that yields a PASS becomes a unidimensional optimization problem.

IV. JTOL Optimization

The proposed algorithm to optimize the JTOL testing time is divided in two main stages: 1) execution of a linear search method based on the golden section [16] at a high BER, typically 10^{-11}, and 2) a downwards search at the compliance BER, i.e. 10^{-12}, starting from the value obtained from the previous step. This technique clearly takes advantage of the fast execution of the golden section search with a high BER, while overcoming the lack of correlation between different BERs by performing a downward linear search at the actual target BER until no errors are seen.

A. Golden Section Search

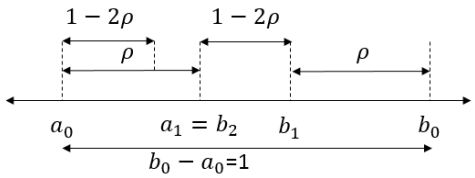

Fig. 1. Nature of the range reduction of the golden section algorithm.

The golden section search algorithm is one of the most widely used unidimensional search methods. It aims to find the minimum value of a unimodal function f: $\Re \rightarrow \Re$. In order to do so, it is necessary to delimit the search points of the function to [a_0, b_0], as shown in Fig. 1, defined as the lower bound (*lb*) and upper bound (*ub*) search points. To reduce the range of uncertainty, the function is evaluated in intermediate points, a_1 and b_1, which are symmetrically selected by applying the golden section rule in such a way that a_1 is at a distance of ρ to a_0 and $(1-\rho)$ to b_0 while b_1 is at a distance of $(1-\rho)$ to a_0 and ρ to b_0, where $\rho = (3-\sqrt{5})/2$ is the so-called golden ratio. The range reduction is then accomplished by comparing the function evaluations of the intermediate points. If $u(a_1) < u(b_1)$, the minimum value must be in the new range of [a_0, b_1]; however, if $u(a_1) \geq u(b_1)$ then the minimum value lies in the range [a_1, b_0]. This process is iterated, as depicted in Fig. 2, until the following stopping criteria is met:

$$\left(\alpha^{ub} - \alpha^{lb}\right) \leq \varepsilon_{\text{step}} \tag{2}$$

where $\varepsilon_{\text{step}}$ is defined as either the minimum J_P increment allowed by the BER tester or the known measurement to

$$\begin{aligned}
&\alpha_j^a = \alpha_j^{lb} + \rho\left(\alpha_j^{ub} - \alpha_j^{lb}\right)\\
&\alpha_j^b = \alpha_j^{lb} + (1-\rho)\left(\alpha_j^{ub} - \alpha_j^{lb}\right)\\
&\text{evaluate } u\left(\alpha_j^a\right) \text{and } u\left(\alpha_j^b\right)\\
&\text{repeat until } \textit{StoppingCriteria}\\
&\quad \text{if } u\left(\alpha_j^a\right) = \text{PASS} \wedge u\left(\alpha_j^b\right) = \text{FAIL}\\
&\qquad \alpha_{j+1}^{ub} = \alpha_j^b ; \alpha_{j+1}^{lb} = \alpha_j^{lb}\\
&\qquad \alpha_{j+1}^b = \alpha_j^a ; \alpha_{j+1}^a = \alpha_{j+1}^{lb} + \rho\left(\alpha_{j+1}^{ub} - \alpha_{j+1}^{lb}\right)\\
&\qquad u\left(\alpha_{j+1}^b\right) = u\left(\alpha_j^a\right)\\
&\qquad \text{evaluate } u\left(\alpha_{j+1}^a\right)\\
&\quad \text{else if } u\left(\alpha_j^a\right) = \text{PASS} \wedge u\left(\alpha_j^b\right) = \text{PASS}\\
&\qquad \alpha_{j+1}^{lb} = \alpha_j^a ; \alpha_{j+1}^{ub} = \alpha_j^{ub}\\
&\qquad \alpha_{j+1}^a = \alpha_j^b ; \alpha_{j+1}^b = \alpha_{j+1}^{lb} + (1-\rho)\left(\alpha_{j+1}^{ub} - \alpha_{j+1}^{lb}\right)\\
&\qquad u\left(\alpha_{j+1}^a\right) = u\left(\alpha_j^b\right)\\
&\qquad \text{evaluate } u\left(\alpha_{j+1}^b\right)\\
&\quad j = j+1\\
&\alpha^* = \left(\alpha_j^{lb} + \alpha_j^{ub}\right)/2
\end{aligned}$$

Fig. 2. Pseudo code implementation of the golden section algorithm.

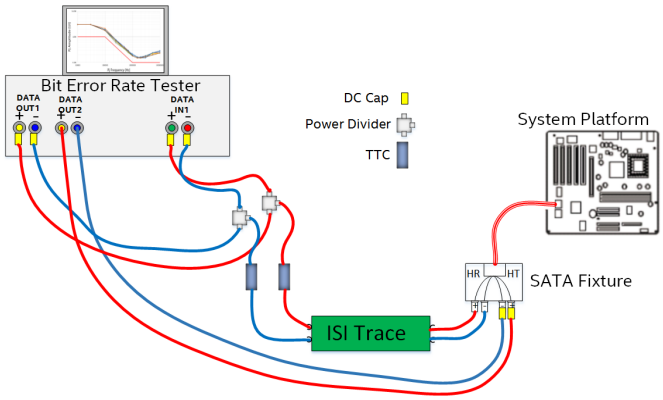

Fig. 3. SATA JTOL test setup.

measurement variability. In JTOL, the evaluation of the function returns a PASS or FAIL response from the BER test at a certain J_P and f. Therefore, the decision of which search range to discard is based on the possibility to approach on every iteration the actual boundary between the PASS and FAIL responses, which is our optimal point. The value returned by the algorithm, α^*, is the average between the upper bound and lower bound points from the last iteration.

B. *Downwards Search*

The second stage of the proposed algorithm performs a search starting from α^* from the previous stage, but now executing at the compliance BER. The search is performed in a downwards direction, meaning that the J_P is decremented in linear steps equivalent to $\varepsilon_{\text{step}}$ (or a percentage of $\varepsilon_{\text{step}}$ in accordance to precision used in the traditional method) until no errors are seen, or in other words, until the BER test passes. The range reduction achieved by the golden section search allows to decrease the number of evaluations in the downwards search. Typically only one to three evaluations are needed at the compliance BER, thus the overall test time is dramatically reduced.

V. Test Case

Our proposed methodology is tested in the SATA3 HSIO link embedded in an Intel platform controller hub (PCH) on a server platform [2].

The JTOL setup for SATA is comprised of a system platform which includes the DUT and a SATA connector, as well as a SATA3 Fixture, a SATA ISI Channel, two transition time converters (TTC), two power dividers and DC blocking capacitors, as shown in Fig. 3. During the Rx JTOL test, the BERT pattern generator sends a compliance test pattern with added jitter through the compliance channels. Prior to running the test, the port should transition to loopback state. Once in loopback, the data received from the DUT is compared to the data generated and errors are counted by the BERT.

The JTOL execution following our proposal takes 5.29 hours to complete 3 repetitions at five different frequency points, as compared to the 72.59 hours that the traditional method requires. In other words, our proposal is more than 13.7 times faster than the traditional approach to reach a

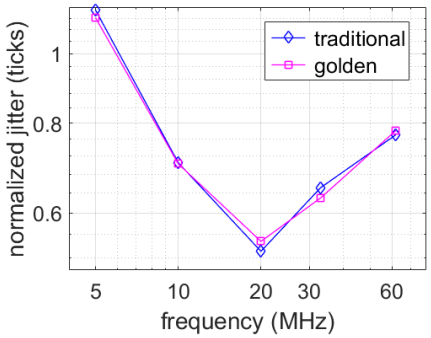

Fig. 4. SATA JTOL results for the traditional approach and the proposed golden section algorithm implementation, .

comparable solution, as shown in Fig. 4.

VI. Conclusions

The golden section search algorithm has proven its effectiveness on reducing the execution time compared with the traditional method; it is more than 13.7 times faster without compromising the accuracy on the measurements. Even though the algorithm was tested on the SATA standard as a proof of concept, the golden section search algorithm could easily be ported to be used on other standards, such as XAUI, PCIe, and USB3, among others. The incorporation of the golden section search algorithm to the post silicon JTOL tests will allow, on one hand, reducing the TTM by getting the evaluation of the silicon sooner, and on the other hand, increasing the validation quality by achieving more unit coverage or PVT conditions at low execution cost.

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