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INTEGRATION OF TRANSISTOR AGING MODELS ACROSS DIFFERENT EDA ENVIRONMENTS

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TÍTULO: **Integration of Transistor Aging Models Across Different EDA Environments**

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A mí familia

Summary

This thesis proposes an approach to consistently integrate transistor aging degradation models across different electronic design automation (EDA) environments, and studies the differences between the modeling approaches typically used to describe transistor degradation. First, an introduction to aging mechanisms in metal-oxide-silicon (MOS) transistors is provided, along with a description of the degradation effects: hot carrier injection (HCI) and bias temperature instability (BTI). Next, the degradation models typically used for circuit level simulation are reviewed along with the general aging simulation flow, explained in detail with the help of an example using the circuit simulator HSPICE. Afterwards, the problems associated with the built-in degradation models offered by the EDA vendors are discussed, revealing the necessity of implementing user defined models in order to achieve consistent aging simulations throughout different EDA environments, an important issue for semiconductor foundries wishing to deliver dependable process design kids (PDK) to integrated circuit (IC) designers. Application program interfaces (API) are a set of C-based data structures and functions that allow the implementation and integration of custom model into circuit simulators. This thesis analyzes the APIs offered by three major EDA vendors, in addition to the open model interface (OMI) API. Subsequently, a simulation study using examples of degradation models compares the aging simulation results obtained after their implementation in three different APIs and tested in two different circuit simulators, demonstrating the possibility of achieving consistent aging simulations results. Finally, this thesis analyzes and compares two modeling approaches used to describe transistor degradation: model card adaptation and subcircuits, highlighting the implications that these two modeling approaches have in aging simulation outcome and performance.

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Introduction

The continued scaling down of metal-oxide-silicon (MOS) technologies has been a driving factor of the growth and success of the semiconductor industry. In the past decades, semiconductor fabrication technologies continuously achieved smaller transistor channel lengths, which allowed increasingly higher integrated circuit densities and more powerful features and functionalities. However, since the submicron range was exceeded, reliability of MOS devices has become a major concern. Physical effects that could be neglected in the past, due to their limited influence, are now causing significant aging of the devices, degrading the performance of transistors.

In order to ensure the lifetime reliability of transistors, semiconductor foundries need to characterize and model the degradation effects that impact their technology and make this information available to the integrated circuit (IC) designers, with the purpose that degradation issues can be assessed and solved during the design phase. This thesis focuses on the integration of aging models into the major electronic design automation (EDA) circuit simulation tools, specifically on the possibility to achieve consistent degradation models across different EDA tools and between different modeling approaches.

Chapter 1 serves as an introduction to the main MOS transistor aging mechanisms, describing how scaling down of transistors geometry created the conditions for a more significant degradation. Furthermore, the general characteristics of the bias temperature instability (BTI) and hot carrier injection (HCI) degradation effects are presented.

Chapter 2 describes the aging models used for circuit level simulation, with special attention given to the typical empirical ansatzes used to model HCI and BTI, which are developed from wafer-level degradation measurements data, obtained following standardized procedures to characterize semiconductor technology degradation. Additionally, the general aging simulation flow is presented and discussed with the help of a detailed example, using the circuit simulator HSPICE.

Chapter 3 reviews the problems associated with the built-in degradation models offered by the EDA tools and focusses on the application program interfaces (API) making possible the implementation of custom models in the different EDA tools, since the integration of user-defined

degradation models enables the possibility for semiconductor foundries to offer consistent aging degradation behavior across multiple simulators. Additionally,, Chapter 3 shows the results of a simulation study in which hot carrier injection (HCI) and negative bias temperature instability (NBTI) aging models were implemented and integrated into two different simulation environments using specific APIs as well as the open model interface (OMI) API.

Chapter 4 starts by describing the characteristics of the modeling approaches used to describe transistor degradation. Aging degradation models are not standardized, and can vary significantly in their complexity and capabilities. Degradation models are typically defined using two approaches: either by degrading parameters of the transistor's model card, or by recreating the aged behavior in a subcircuit. Chapter 4 continues with the definition of example HCI and NBTI degradation models using both approaches, designed to have the same direct current (DC) behavior, and finishes with a simulation study comparing the impact that these modeling approaches have on an aging simulation result and its performance.

The author wishes to express his gratitude and sincere appreciation to Dr. José Ernesto Rayas-Sánchez, full professor and director of research in the Computer-Aided Engineering of Circuits and Systems group at ITESO; not only for his guidance and invaluable feedback, but specially for his patience and disposition to supervised this work, despite the difficulties associated with me working in another country.

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1. Aging Mechanisms in CMOS Technologies

1.1. Introduction

Since the implementation of the first transistor in the 1940s [Bardeen-49], the microelectronics industry has grown immensely and has been shaping and accelerating the technological development of our society so strongly, that it becomes difficult to think of an aspect of modern life where its influence is not noticeable. One key aspect that has allowed the industry to grow is the positive effects that result from scaling down a semiconductor device, improving performance and costs [Thompson-06]. An integrated circuit that is scaled down has a larger packaging density and higher working speeds [Taur-97].

In a MOS transistor, the electric field in the silicon substrate below the gate, created when a voltage is applied, is used to control the current flow from drain to source. If the dimensions of a transistor are reduced by a factor α, the same electric field conditions can be achieved by reducing the applied voltage along the key dimensions of the transistor and increasing the dopants concentration in the substrate [SRINIVASAN-04]. The constant-electric-field scaling maintains the same electric field intensity by reducing the transistor dimensions and voltage by a factor of $1/\alpha$, and increasing the doping by α. As a result, the density is improved by a factor of α^2, due to smaller dimensions of the device and the wiring. This reduction in the device dimensions also increases the speed of the transistor due to a decrease in the parasitic capacitances and shorter propagation distances. The power density remains constant even if the number of circuits is increased.

Constant-electric-field scaling, although valid, is nowadays not widely used because it requires a departure from standard voltages levels and reduces the operation voltages. Furthermore, scaling down both the applied voltage and the threshold voltage results in an increase of the stand-by leakage current. To address this, a non-constant-field scaling has been used, where the electric-field intensity changes by a factor ε. The applied voltage is then given by ε/α, which allows a slower scaling of the voltage. However, non-constant-field scaling differs from the ideal description above, and lifetime reliability issues start to become more evident in smaller

technologies, especially when the transistor channel lengths are smaller than 1 micrometer and the gate oxide thickness t_{ox} is on the range of a few angstroms. In a non-constant-field scaling, the electric field in the substrate increases and power dissipation scales slower than the device area [Huff-06], [Davari-95], resulting in higher power densities and temperatures, which accelerates known aging or failure mechanisms such as electro-migration, thermal cycling, dielectric breakdown, bias temperature stressing, tunneling injection, etc. Ultimately, the lifetime of the devices is reduced and the failure rate increases as the technologies are scaled down.

Some aging mechanisms, such as the time dependent dielectric breakdown (TDDB), are called destructive because they lead to a complete malfunction of the transistor. Non-destructive mechanisms, such as bias temperature instability (BTI) or hot carrier injection (HCI), modify the characteristics of the transistor without leading to an immediate malfunction of the device. However, this can degrade its performance and characteristics, altering expected behavior of the transistor, which could lead to a circuit or system level failure [Chouard-12]. This thesis dissertation will be focused on the integration of aging models into electronic design automation (EDA) software for reliability simulations. Therefore, this chapter will discuss the main non-destructive mechanisms affecting CMOS technologies and the effects they have in the performance of MOS transistors.

1.2. Bias Temperature Instability (BTI)

Bias temperature instability (BTI) has become one of the biggest reliability challenges for CMOS technologies. It is generally understood that BTI happens due to the creation of interface traps and oxide charges when the transistor is in strong inversion at elevated temperatures [Schroder-11], [Grasser-11]. Although negative bias temperature instability (NBTI) in p-MOSFETS has been known for many years, it only gained importance when the transistors reached the submicron range and its contribution to the overall device degradation became significant [Tae-Hyoung-13], [Hussin-11]. Positive bias temperature instability (PBTI) degradation can also be seen in n-MOSFET devices, as described below.

1.2.1 Negative Bias Temperature Instability (NBTI)

The required conditions to observe NBTI degradation in p-MOSFETS are: stress voltage at the gate, high temperatures (usually ranging from 80 to 150 °C), and grounded drain, source, and bulk. NBTI produces an increment in the threshold voltage and degradation of the mobility and transconductance, resulting in a reduction of the saturation current I_{Dsat}. The forward and reverse saturation currents degrade identically. This symmetry shows that the degradation observed is not related to channel carrier transport mechanisms. The degradation produced by NBTI indicates a build-up of charges at the insulator-substrate interface (Si/SiO_2). In general, it is understood that the electric field, in combination with the elevated temperatures, produces a breaking of SiH bonds at the insulator-substrate interface, which results in the creation of interface traps and positive charges in the oxide. One important characteristic of NBTI degradation is that it has a recovery effect. After the stress is removed, the damage in the device recovers, leading to a reduction in the threshold voltage shift. The recovery effect occurs quickly, needing only a few seconds after the stress is removed, although the NBTI degradation may need considerably longer stress times [Schroder-11], [Huard-06]. This difference in the time constants of the degradation and recovery effect makes the time delay between stressing the device and measuring the degradation critical because it can result in inaccurate measurements of the threshold voltage shift caused by NBTI [Varghese-05].

One theory widely seen in the literature trying to explain the microscopic origin of NBTI degradation is the reaction-diffusion (RD) model. In this model, a reaction phase is responsible for creating interface traps at the insulator-substrate interface, with a linear dependency on the stress time. The hydrogen released during the reaction phase then diffuses from the interface into the oxide, with an exponential time dependency [Schroder-11]. Although the RD model was considered to be correct for many years, later research showed that this model fails to fully describe NBTI [Grasser-11]. The physical explanation of NBTI is still not fully understood and lies beyond the scope of this chapter. In [Grasser-11], a detailed description of the RD model deficiencies can be found, showing that there is a charge-trapping mechanism present in NBTI degradation. For small devices, it can be seen that recovery occurs in discrete steps, which is not consistent with a process control by diffusion. Instead, this behavior resembles the charge trapping mechanisms observed in random telegraph noise. This charge trapping mechanism creates switching oxide traps

that contribute to the shift in threshold voltage and charge-pumping current. Further explanation of the switching traps mechanism can be found at [Grasser-12] and a successfully implemented compact model for NBTI using this principle can be found at [Giering-16].

1.2.2 Positive Bias Temperature Instability (PBTI)

Analogue to NBTI in p-MOSFETs, positive bias temperature instability (PBTI) degradation can be seen in n-MOSFET devices when a positive voltage stresses the device at high temperatures. PBTI was considered negligible for SiO2 or SiON oxide technologies, however, since the introduction of materials with high relative dielectric permittivity (high-κ materials), PBTI degradation became noticeable. The physical understanding of the mechanisms causing PBTI are less known in comparison with NBTI and the literature discussing PBTI is limited [Guo-15]. It is believed to be caused by charge trapping in the high-κ layer [Chouard-12]. Unlike NBTI, the degradation does not occur at the insulator-substrate interface and, due to the presence of intermediate SiO2 layers in the insulator stack, PBTI degradation occurs at a distance from the inversion channel, mainly affecting the threshold voltage while the mobility remains almost unaltered [Sa-05], [Zhao-11].

PBTI in p-MOSFETS or NBTI in n-MOSFETS can occur in accumulation mode, however it is uncommon in CMOS devices since it requires reversed sign voltages at the gate and there is no control over the I_{Dsat} current. Although accumulation is possible under some scenarios in analog circuits, BTI degradation in accumulation mode it is not considered to be a reliability issue at the moment [Chouard-12].

1.3. Hot Carrier Injection (HCI)

Hot carrier degradation affects both p-MOSFET and n-MOSFET devices. Scaled down MOS devices have small gate length, thin oxide insulator layers, and high doping concentrations, creating conditions for hot carrier generation. In a MOS transistor, once the inversion layer is created, a drain voltage will accelerate carriers from drain to source. Some of the carriers can gain sufficient kinetic energy to overcome the insulator-substrate interface potential barrier [Kueing-

Long-85]. This so-called hot carriers can create electron-hole pairs by impact-ionizing when they collide with the lattice. They can also get trapped, generating interface states or oxide defects. As a result, HCI degrades the transistor causing shifts in important electrical characteristics, such as threshold voltage, sub-threshold voltage swing, transconductance or current factor β [Maricau-13]. HCI degradation is asymmetrical, resulting in higher insulator degradation around the drain region. HCI typically occurs between the channel pinch-off and drain junction when the transistor is in strong inversion [Schroder-11], and generates both positive and negative charges simultaneously. For technologies in nanometers range, HCI degradation effects can be seen without the presence of an inversion layer, i.e., when the transistor is switched off. This effect is known as non-conductive HCI (NHCI) or off-stage HCI degradation [Holzhauser-00], [Muehlhoff-02].

The lucky electron model (LEM) is a well-known HCI model, widely used in reliability simulation, that has been able to predict the HCI degradation for CMOS technologies down to 0.25µm [Schroder-11]. LEM has not provided a direct proof or description of the all the physical mechanism causing HCI, rather, it is based on probabilistic arguments to determine the injection of channel electrons into the gate oxide [Hasnat-96], [Jungemann-96]. In the LEM, the shift in threshold voltage ΔV_{th}, the shift in sub-threshold current swing ΔS, and transconductance g_m are proportional to the total number of interface states induced by hot carriers and linearly correlated among themselves [HU-85]. The time dependence relation of ΔV_{th}, is proportional to t^n , with values for n ranging between 0.5 and 0.75.

For technologies under 0.25 µm an energy driven model (EDM) has been proposed, which includes effects such as electron-electron scattering. In the EDM, bias dependences are determined by the energy dependences of the scattering rate, and not by the number of interface states [Rauch-05]. To make transistors more robust against HCI degradation, fabrication techniques such a lightly doped drained (LDD) and doubled-diffused drained have been developed, although HCI degradation still takes place [Pfiester-88], [McPherson-06].

1.4. Conclusions

Technology scaling has allowed CMOS devices to continuously achieve performance improvements and economic success, but not without a price. The extremely small geometrical

dimensions of transistors in modern CMOS technologies have created the necessary conditions for degradation mechanisms to arise and comprise their lifetime reliability. Aging mechanisms, such as BTI and HCI, are the focus of discussion in state-of-the art reliability research because, due to their complexity, full understanding of the microscopic physical phenomena is missing. Nevertheless, different models have been proposed that, to some extent, describe these mechanisms and the influence they have on the transistors' behavior. This chapter serves as a first point of contact with aging mechanisms in CMOS technologies, describes their main characteristics, and offers the possibility to understand the conditions in which they occur. This, in turn, provides the necessary context for the work that will be undertaken in this thesis, which will focus on the integration of these models into EDA environments.

2. Modelling and Simulation of Aging Effects in CMOS Circuits

2.1. Introduction

Emerging applications, such as autonomous driving and Industry 4.0, demand for integrated circuits (ICs) with an enormous computing power at a very high reliability. These diametrical requirements should be considered early in an IC development project and incorporated into the design phase to ensure meeting the product specifications, especially for circuits intended to work in hostile environments or with high safety regulations, such as in the aerospace or automotive industries. Circuit-level aging simulations are a particular feature in electronic design automation (EDA) tools that allow the analysis and verification of potential lifetime reliability issues in ICs. Aging simulations make possible the inspection of a circuit's behavior after long operation times and are available in multiple tools and EDA environments. Their efficacy depends strongly on the accuracy and correctness of the models used to describe the degradation of the transistors.

Many important questions may arise when a team or a designer wishes to analyze lifetime reliability using aging simulations for the first time. Which degradation mechanism affect the technology employed for the design? Which models describe better aging degradation? How can these models be used in a simulation? How to do an aging simulation? Does the EDA environment to be used offers aging simulation capabilities?

This chapter intents to help answering some of these questions by giving an introductory overview into the modeling and simulation of aging effects. Section 2.2 describes the typical degradation models used for simulation and Section 2.3 discusses the aging simulation capabilities offered by different EDA vendors. An example of a simulation flow is presented in Section 2.4. The reports concludes with Section 2.5.

2.2. Aging Models for Circuit Level Simulation

Important electrical characteristics of field effect transistors (FETs), such as drain current or threshold voltage, change gradually over (operation) time due to bias temperature instability (BTI) and hot carrier injection (HCI) degradation mechanisms. This aging effect occurs as a result of the gradual accumulation of charges inside or near the gate oxide dielectric. Since such a change in the FET behavior impacts the performance of an IC design, and ultimately threatens the proper functioning of electronic devices, the development of adequate degradation models and their inclusion in circuit-level aging analysis has become essential. BTI is a major concern for p-channel FETs (PFETs), also known as negative BTI (NBTI). Large negative gate-source voltages and elevated temperatures trigger the capture of channel carriers into pre-existing or newly generated defects in the gate dielectric oxide. A reduction in gate-source voltage (V_{gs}) leads to a partial recovery of the degradation. An analog positive (PBTI) effect occurs in n-channel FETs, although less pronounced. HCI affect both FET types, whereas a high lateral electric field accelerates the carriers in the channel and a fraction of them becomes fast enough to destroy hydrogen-passivated bonds at the oxide interface. Depending on the inversion state, i.e. on V_{gs}, the destruction of this bonds can be an individual or collective effort of carriers. The temperature dependency of HCI can be complex, since the acceleration of carriers involve several scattering processes with different time dependencies.

In the semiconductor industry, it is a common practice to use empirical models for both NBTI [Aono-05], [Yang-06] and HCI [Lorenz-09], [Tyaginov-14], which fit experimental degradation data. Different organizations, both national and international, work on the standardization of reliability methods. Standards describing the procedures to measure BTI and HCI degradation in FETs can be found among the wafer level reliability JEDEC standards, such as JESD28A [JEDEC-01] , JESD60A [JEDEC-04a] and JESD90 [JEDEC-04b]. The JEDEC standards are responsibility of the JEDEC Solid State Technology Association, the standardization division of the Electronic Industries Alliance. JEDEC standards are among the most referred standards in Europe and USA [Bisschop-07].

The measurement of aging degradation in FETs is performed by employing elevated voltages or temperatures because the aging effects accelerate with elevated electrical or thermal stresses [Afacan-16]. Performing the measurements under normal operation conditions would be

highly impractical, since several months, or even years, would be necessary to observe the degradation caused by the aging mechanisms. JESD90 describes an accelerated stress and test methodology to measure device parameters changes due to NBTI in a single PFET. Although it is possible to have NBTI degradation during channel conduction, the standard only covers NBTI under a symmetric voltage stress condition with the channel inverted ($V_{gs} < 0$) and drain source voltage $V_{ds} = 0$ (no channel conduction). V_{gs} should be selected in such a way that to avoid a dielectric breakdown due to a high vertical gate oxide electrical field. NBTI measurements must be carried out at elevated temperatures and under direct current (DC) stress conditions. Similarly, JESD28A describes a methodology for the measurement of HCI degradation in a single NFET, where electrical stressing should be perform under DC bias conditions. The maximal V_{ds} stress is determined by the breakdown region of the characteristic curve of the NFET. The maximum V_{ds} should be determined at the V_{gs} producing the worst degradation, typically considered as the value at which the maximum substrate leak current occurs.

The general stress procedure for both standards is shown in Fig. 2-1. First, a transistor with geometrical dimensions and device parameters within the technology requirements is selected. Then, an initial characterization in linear and saturation regions is performed. The device parameters of interest shall be recorded and used to determine the shifts caused by the aging degradation. Typical parameters taken into consideration include: linear drain current IDLIN, saturation drain current IDSAT, maximal linear transconductance GMAX, and constant-current threshold voltage VTHI. The initial characterization, if successful, is followed by a stress-measurement cycle. For NBTI, voltages should by applied in the following order: first the drain voltage and second the gate voltage. The stress begins when the gate voltage has been applied at the intended stress temperature. In HCI, bulk voltage is applied first, gate voltage second, and finally the drain voltage. In both cases, the stress continues until the stress time for the interval is achieved. The voltages should be removed in reverse order. Typical NBTI and HCI degradation follow a power law function with time in a logarithmic scale, therefore, recommended stress intervals are at least ½ decade time steps. After each stress interval, a transistor characterization is performed, recording the same device parameters as in the initial characterization. The devices should be stressed until the specified failure criterion has been reached. If this is not possible due to the long times required, devices should be stressed until the collected data makes possible a linear logarithmic extrapolation.

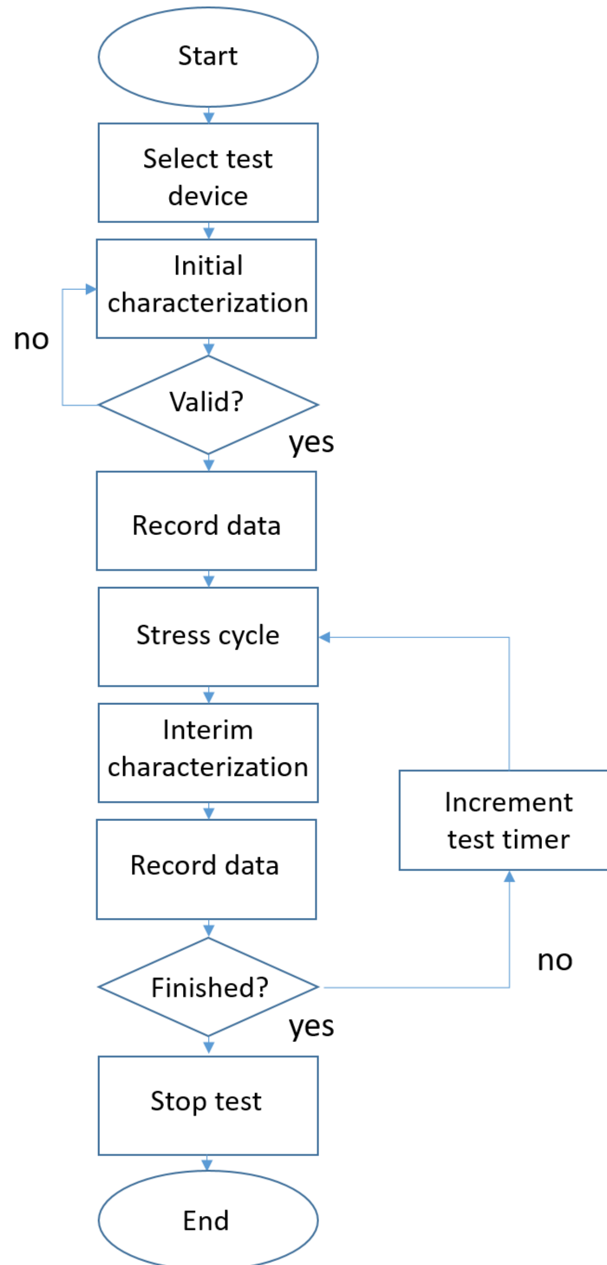


Fig. 2-1 NBTI and HCI stress test procedure [JEDEC-01], [JEDEC-04b].

Experimental constant-stress degradation data is typically fit to ansatzes similar to [JEDEC-04a], [JEDEC-04b]:

$$\Delta_1(V,T,t) = Aexp\left(\frac{E_{aa}}{kT}\right)V^m t^n \tag{2-1}$$

with a power low dependency in voltage, with exponent m, and in time, with exponent n, as well as an Arrhenius temperature dependency with activation energy E_{aa}.

The ansatz in (2-1) can be generalized in order to include the saturation of degradation observed experimentally, with a saturation level represented by *1/β*:

$$\Delta_2(V,T,t) = \frac{\Delta_1(V,T,t)}{1+\beta\Delta_1(V,T,t)} \tag{2-2}$$

It is possible to extend the degradation measurement techniques to include transient or RF bias conditions [Sasse-08]. This is, however, very challenging and could lead to a degradation enhancement influenced by the measurement setup due to carrier injection [Scholten-11], [Bellens-90].

Since transistors typically work in time-varying bias conditions, a conversion of the DC degradation models into time-varying models is necessary. This is usually done with a quasi-static approximation, in which the time-varying bias condition is treated as a sequence of DC bias conditions. This approximation has been used in power law models similar to (2-1). In [Scholten-11], a method is discussed to find a relationship between DC and time-varying bias conditions for different types of DC degradation formulas. Table I shows the quasi-static time-varying equivalent for some DC models.

Despite their limitations, empirical models based in constant-bias characterization standards are widely used in industry. As mentioned before, the complexity of the models increases

TABLE I
EXAMPLES OF THE CONVERSION FROM DC DEGRADATION FORMULAS TO DEGRADATION FORMULAS VALID UNDER TIME-VARYING BIAS [11]

DC bias	Quasi-static equivalent
Power Law	
$\Delta Deg(t) = C \cdot (f(Vi) \cdot t)^n$	$\Delta Deg(t) = C \cdot \left[\int_o^t (f(Vi(\hat{t}) \cdot d\hat{t})\right]^n$
Saturated Power Law	
$\Delta Deg(t) = \frac{P_{max}}{1+\left(\frac{t}{\tau(Vi)}\right)^{-\alpha}}$	$\Delta Deg(t) = \frac{P_{max}}{1+\left(\int_0^t \frac{d\hat{t}}{\tau(Vi(\hat{t}))}\right)^{-\alpha}}$
Logarithmic Law	
$\Delta Deg(t) = C \cdot ln\left(1+\frac{t}{\tau(Vi)}\right)$	$\Delta Deg(t) = C \cdot \ln\left(1+\int_0^t \frac{1}{\tau(Vi(\hat{t}))} \cdot d\hat{t}\right)$

if a more detailed representation of the physical phenomena is desired. In general, degradation models can be extended to improve accuracy and include additional features. For example, adding the recovery effect to BTI [Grasser-12], [Giering-16] and variability [Kaczer-10]; voltage-dependent time exponents [Kerber-09]; or full dependency on V_{gs} and V_{ds} for HCI [Tyaginov-14].

2.3. Overview of Aging Simulation in Modern Electronic Design Environments

Different EDA vendors offer circuit-level aging simulation capabilities integrated into their tools. In this chapter we concentrate in three of the most important EDA vendors in industry: Cadence, Synopsys, and Mentor Graphics. The general aging simulation flow is depicted in Fig. 2-2 Flow of circuit-level aging simulations. and, in principle, is the same for all EDA tools, despite particular differences between the simulators. First, a transient simulation is perform using a "fresh netlist", which represents the circuit at time 0 and assumes particular usage or load scenarios, often referred to as "mission profiles". From the transient simulation, the stress conditions per FET are extracted in terms of voltages, currents and temperatures. Degradation models use the stress information for each individual FET, along with its physical characteristics, such as width and length, to calculate the degradation that each FET suffers due to the degradation mechanisms. The degradation is then mapped or converted into adjustments of selected parameters of the underlying transistor model. With the adjusted parameters, an "aged netlist" is generated to represent the circuit after a pre-defined time of operation. A simulation using the aged netlist allows the analysis of the performance for the "aged" circuit. With this information, the circuit

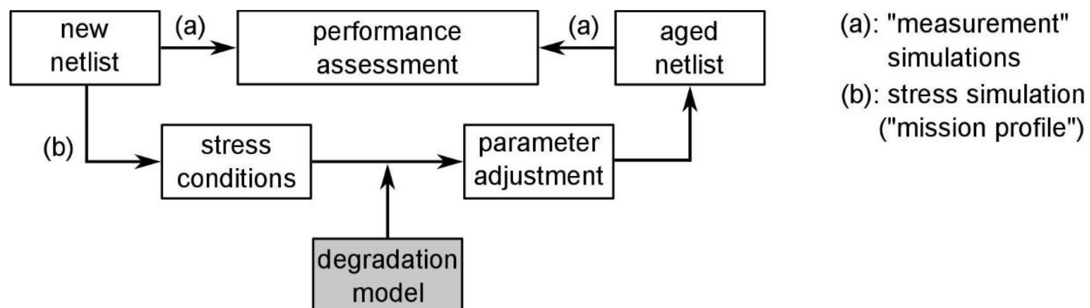
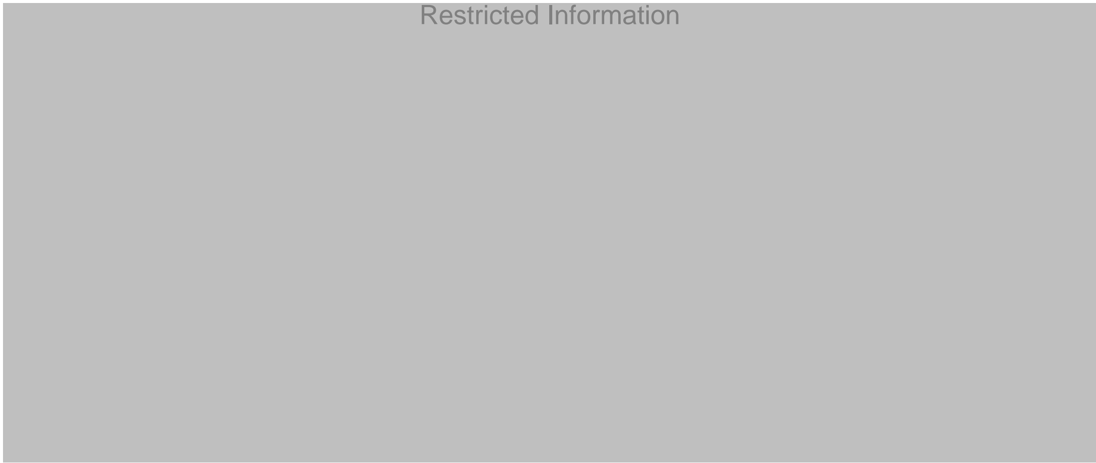


Fig. 2-2 Flow of circuit-level aging simulations.

TABLE II
MOSFET MODELS SUPPORTED BY DIFFERENT EDA TOOLS



designer can determine if the circuit still behaves between the design specifications, hence assessing the circuit lifetime reliability.

[1] Spectre circuit Simlator v14.1, Cadence Design Systems, Inc., 655 Seely Avenue, San Jose, CA,2014
[2] Virtuoso® RelXpert Reliability Simulator v15.1, Cadence Design Systems, Inc. 655 Seely Avenue, San Jose, CA,2015
3 HSPICE Version O-2018.09-1, Synopsys, Inc., 690 East Middlefield Road, Mountain View, CA October 2018.
[4] HSPICE Version O-2018.09-1,Synopsys, Inc., 690 East Middlefield Road, Mountain View, CA October 2018
[5] HSIM Version C-2009.06,Synopsys, Inc., 690 East Middlefield Road, Mountain View, CA June 2009
[6] ELDO Release 2018.4, Mentor Graphics Corporation, 8005 SW Boeckman Road Wilsonville, OR 2018

The MOSFET models supported by the different EDA tools are summarized in Table II.

2.4. Aging Simulation in HSPICE

In order to offer a better understanding on reliability analysis using EDA tools, this section presents an example of an aging simulation using the simulator of Synopsys: HSPICE. This example only explains how to run an aging simulation and details on how user-defined models are integrated into the simulator will be discussed in a future report. Fig. 2-3 Netlist in HSPICE with an MOSRA aging analysis. shows a netlist with a MOSRA reliability analysis. It is important to emphasize that aging simulations always have to be performed along with a transient (.tran)

```
* MOSRA TEST *
* Original Netlist *
vdd 1 0 2
mp1 3 2 1 1 p1 l=0.1u w=10u ad=5p pd=6u as=5p ps=6u
mn1 3 2 0 0 n1 l=0.1u w=5u  ad=5p pd=6u as=5p ps=6u
mp2 4 3 1 1 p1 l=0.1u w=10u ad=5p pd=6u as=5p ps=6u
mn2 4 3 0 0 n1 l=0.1u w=5u  ad=5p pd=6u as=5p ps=6u
mp2 2 4 1 1 p1 l=0.1u w=10u ad=5p pd=6u as=5p ps=6u
mn3 2 4 0 0 n1 l=0.1u w=5u  ad=5p pd=6u as=5p ps=6u

.model p1 pmos level=54 version=4.5
.model n1 nmos level=54 version=4.5

* MOSRA aging analysis

.model p1_ra mosra level=101

.appendmodel p1_ra mosra p1 pmos

.mosra reltotaltime=1e8
```

Fig. 2-3 Netlist in HSPICE with an MOSRA aging analysis.

analysis. In HSPICE, the first step is to declare the aging model. This is done using the command `.model` and declaring the type as MOSRA. For example, the statement `.model p1_ra mosra level=101`, creates a model named `p1_ra`, which is linked to the MOSRA aging model identified with the number 101, in this case, a user-defined model. MOSRA's own degradation models are identified as level 1 or 3.

Once the aging model has been declared, it is necessary to indicate to the simulator, using the command `.appendmodel`, to which transistor model card the aging model will be associated to. The statement `.appendmodel p1_ra mosra p1 pmos`, indicates that the aging model `p1_ra` will degrade the transistor model named `p1` of the type `pmos`. The final step is to activate the reliability analysis with the command `.mosra` and declaring the time at which the degradation should be calculated.

For this example, a 130 nm BSIM4 Predictive Technology Models (PTM) for bulk complementary metal-oxide-semiconductor (CMOS) [NIMO-06] will be used. PTM provides open, accurate, and customizable models that are compatible with circuit simulators.

The degradation mechanisms will be modeled with a saturated power law (2-2) and using the quasi-static approximation described in Table I. NBTI degradation is mapped to the PFETs as a shift in the BSIM4 parameter *VTH0* according to:

$$VTH0_{aged} = VTH0_{fresh} - \Delta vth0 \qquad (2\text{-}3)$$

taking (2-1) with $\Delta vth0 = \Delta_1$, $A = 2.915$, $E_{aa} = -0.2$, $m = 3.5$, $n = 0.15$ and (2-2) with $\beta = 3$.

HCI degradation is also modeled with a saturated power law and mapped to the BSIM4 parameter $\mu 0$:

$$\mu 0_{aged} = \mu 0_{fresh} - \Delta\mu 0 \qquad (2\text{-}4)$$

using (2-2) with $\beta = 13$,

$$\Delta\mu 0 = \Delta_1 = A \cdot exp\left(\frac{C}{V_{ds}}\right) t^n \qquad (2\text{-}5)$$

where $A = 3.215$, $C = 8.15$ and $n = 0.12$.

These aging models will be used to analyze the aging degradation effects in two ring oscillators (RO) of 3 and 21 stages. The MOSRA aging simulation in HSPICE has been used to measure the oscillation frequency of the ring oscillator as they aged due to degradation mechanisms.

Fig. 2-4 shows the frequency degradation in a 3-stage RO due to the HCI aging model defined (2-4) in and (2-5). Similarly, Fig. 5 shows the frequency degradation in a 21-stage RO due to the NBTI aging model. The *x*-axis is in logarithmic scale, and show the variation of the frequency of the ring oscillator up to 10^9 seconds. As a quick reference, 10 years are equal to 3.154×10^8 seconds.

Although this is a generic example, and the degradation models have not been characterized to represent the actual degradation of a real transistor, it shows the impact that the aging mechanisms could have in a real design and how an IC designer can make use of an aging simulation to analyze the negative effects of degradation mechanisms.

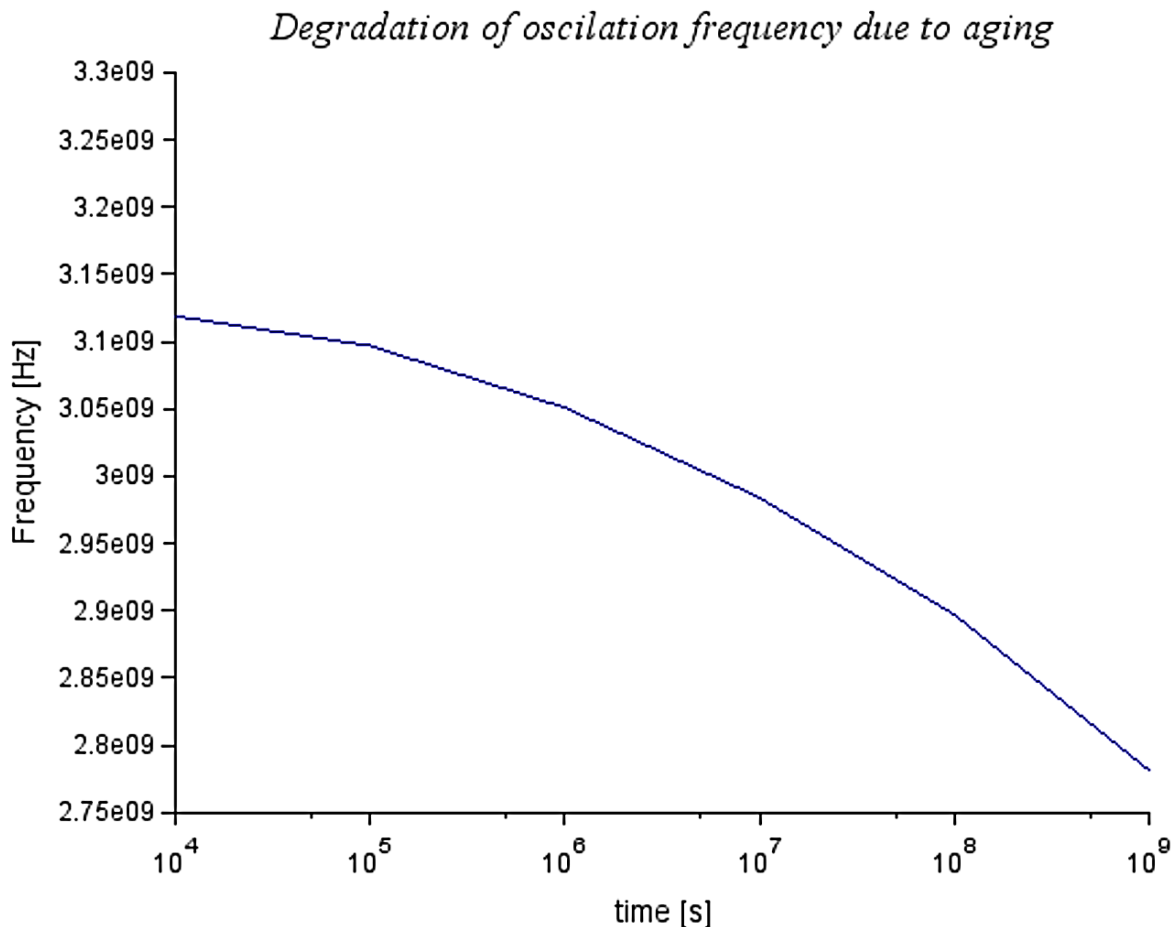


Fig. 2-4 Oscillation frequency degradation of the 3-stages RO under HCI aging.

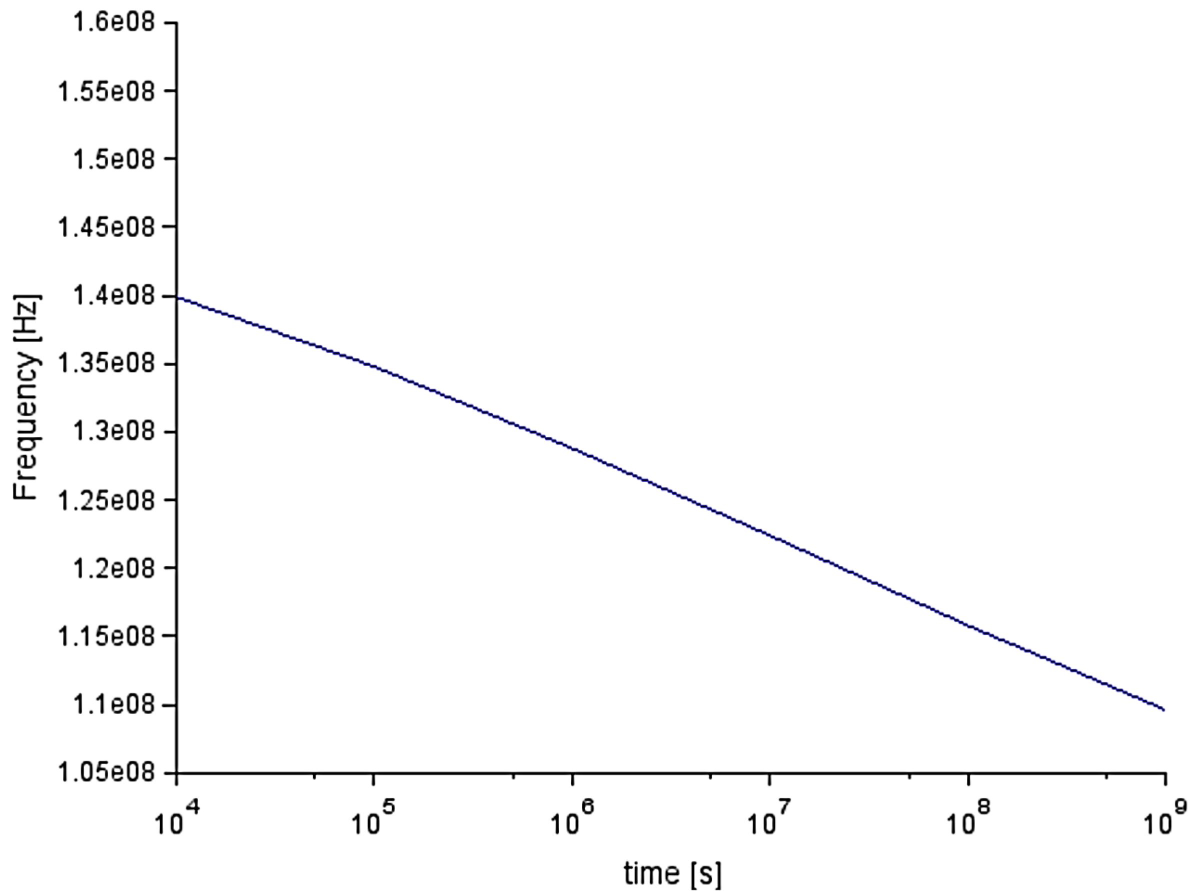


Fig. 2-5 Oscillation frequency degradation of the 3-stages RO under HCI aging.

2.5. Conclusions

Integrated circuits will behave differently after long operation times as a result of degradation mechanisms primarily affecting the gate oxide dielectric in the field effect transistors. In this chapter, a brief overview of the degradation mechanism HCI and BTI was presented and accompanied by a discussion of the models typically used for circuit-level aging simulation and a summary of the aging simulation capabilities in different EDA tools. Finally, the reader is introduced into the circuit-level aging simulation flow by the means of an example that shows the effects that HCI and NBTI may have in the oscillation frequency of two ring oscillators. The aging simulation performed uses generic degradation models implemented in HSPICE.

3. Integration of Aging Models into Multiple EDA Environments

3.1. Introduction

Aware of the importance lifetime reliability has gained in the electronics industry with the steady development of sub-micron semiconductor technologies, electronic design automation (EDA) vendors offer aging simulation capabilities integrated into their simulation flows, together with built-in degradation models and the possibility to implement custom models. The integration of user-defined degradation models enables the possibility for semiconductor foundries to offer consistent aging degradation behavior across multiple simulators. Although the main EDA tools provide built-in transistor degradation models within their aging simulation flow, it can be a difficult task to determine their adequacy for a given semiconductor technology. Since there are not standard transistor degradation models, each EDA tool provides its own models, which can vary in complexity and level of accessibility. Furthermore, the extraction procedures of the degradation model parameters are not necessarily public, making it hard to estimate the cost and effort to characterize the degradation of the transistors without engaging with the EDA tool provider or signing an NDA.

For these reasons, it seems almost impossible to have consistent aging simulations in multiple design environments using built-in models. This is an important issue for semiconductor foundries, which are responsible of characterizing their technologies and providing a consistent Process Design Kit (PDK) to their customers. Design teams doing aging simulations with built-in models in different EDA environments can obtain different degradation results under the same stress conditions and for the same technology. Implementing custom models can overcome these disadvantages. Besides the built-in models, EDA tools provide an application program interface

(API) that allows the implementation of user-defined transistor aging models into their simulation flow.

This chapter provides an overview of the APIs that make possible the usage of custom models in the main EDA tools and discusses the steps needed to achieve their consistent integration. It also presents a simulation case implementing aging models of hot carrier injection (HCI) and negative bias temperature instability (NBTI) into two different simulation environments.

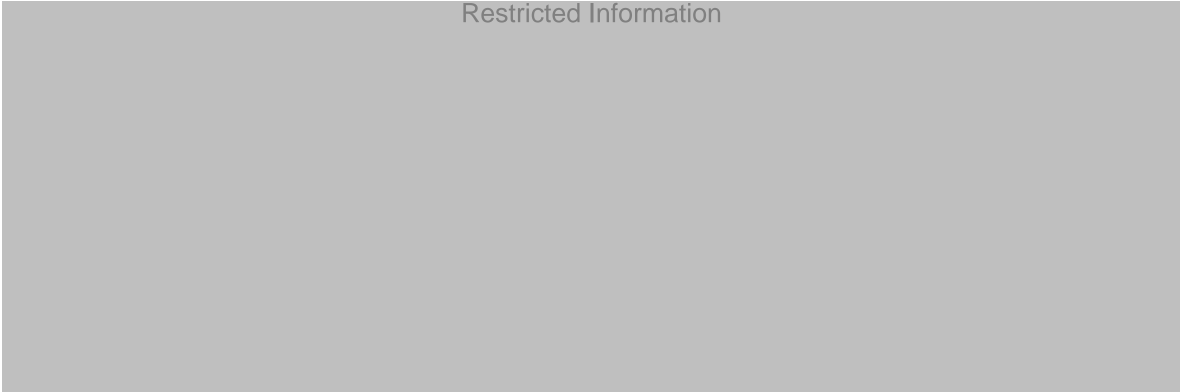
The rest of this chapter is organized as follows. Section 3.2 describes how an API makes possible the integration of custom models into an EDA simulation flow. Section 3.3 discusses the steps followed to consistently implement an aging model across different EDA environments. Section 3.4 presents the results obtained after successfully integrating an aging model example into different simulators. Finally, Section 3.5 concludes this chapter.

3.2. Implementation of User-defined Degradation Models into EDA Environments

User-defined degradation models can be integrated into a simulation flow using the APIs provided by the EDA tools, which are a set of data structures and functions in the programing language C, enabling the implementation of the mathematical description of an aging model, in addition to the exchange of information with the circuit simulator. During a “fresh” simulation, the model has access to the stress conditions for each transistor (temperature, voltages, or currents), the reliability control statements from the netlist, and the model card parameters. The model uses that information to calculate the degradation of each transistor in the circuit being simulated. Next, the degradation information is sent back to the simulator, which uses it to perform a second simulation with the aged or degraded transistors.

There are different ways of depicting aged transistors for aging simulations. The most common option is to degrade parameters of the underlying transistor’s model card to change its electrical characteristics and match the behavior of the aged transistor. Another option is to use a subcircuit, with voltage and current sources around the original transistor, to represent a degraded

TABLE III
AVAILABLE APIs IN THE MAIN EDA TOOLS



behavior. In some tools, it is possible to directly degrade internal electrical characteristics of the transistors, for example, the drain to source current or the transconductance.

Similarly to the built-in aging models, APIs are tool specific. Table III summarizes the APIs available in the different EDA environments, along with the degradation mapping options they offer. Efforts to provide a standard interaction between simulator and aging models have materialize in the emerging Open Model Interface (OMI), developed by the Compact Model Coalition, a working group devoted to the standardization of SPICE models [SI2-18a]. The OMI is an open interface for compact SPICE modeling to support extension to standard compact models, including reliability aging modeling [SI2-18b]. Since the details of the internal architecture of the APIs shown in Table III are not public, only some details of the available OMI API are discussed, with the intention to give an overview of the internal characteristics of an API (data structures and functions) that allow the implementation of an aging model.

3.2.1 Data Structures for Aging Modeling in the OMI API

The OMI API provides several data structures with different purposes, such as giving access to general simulation information, to specific data for each transistor instance, or to store intermediate results of the aging model. Table IV summarizes the main data structures necessary for the implementation of an aging model.

3. INTEGRATION OF AGING MODELS INTO MULTIPLE EDA ENVIRONMENTS.

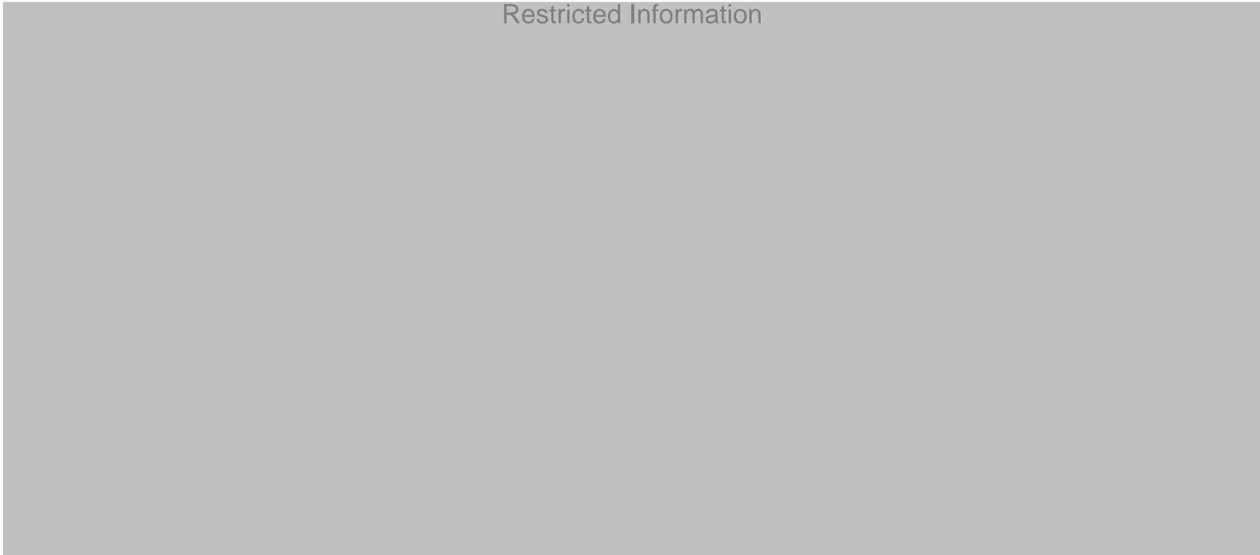


Fig. 3-1 Definition the omiBSIM4CoreData data structure in the OMI API.

TABLE IV
BASIC OMI API DATA STRUCTURES USED FOR AGING MODELING

Restricted Information

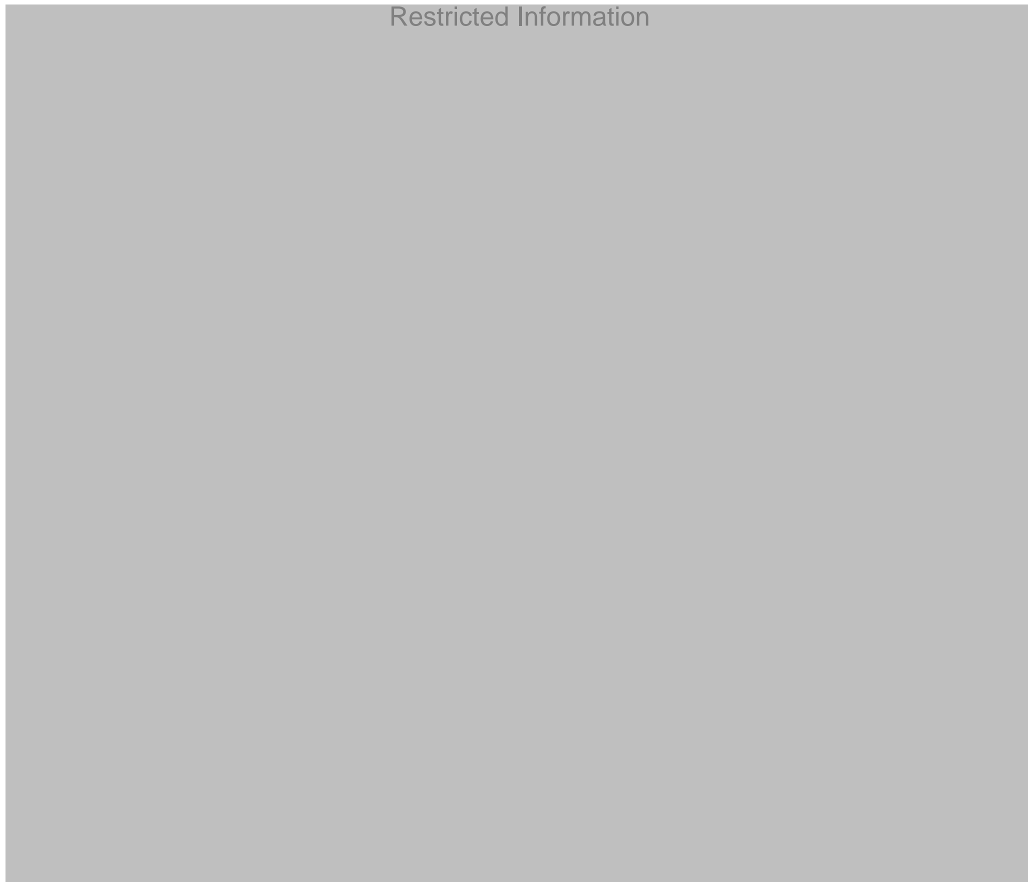
3.2.2 Interface Functions for Aging Modeling in the OMI API

A set of functions allows the interaction between the OMI and the simulator as well as the control of the OMI flow. A subset of functions of interest for the implementation of an aging model is summarized in Table V.

The basic aging model simulation flow in the OMI consists of three steps, each executed by an API function:

a) Age Integration.

TABLE V
BASIC OMI API FUNCTIONS USED FOR AGING MODELING



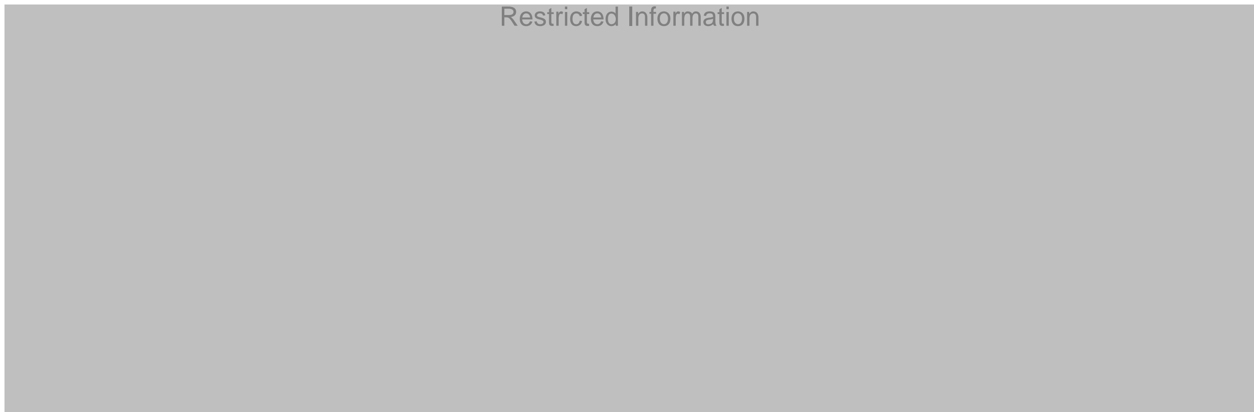


Fig. 3-2 Declaration of aging model flow functions for BSIM4 in the OMI API.

b) Age Extrapolation.

c) Degradation Mapping.

The complete OMI flow and its interaction with the simulator goes beyond the implementation of an aging model, therefore, other functions and data structures are necessary for a full interaction between the OMI API and the simulator, but they exceed the scope of this chapter. The information about the whole OMI API flow can be found at [SI2-18b].

3.3. Consistent Integration of Degradation Models In Multiple EDA Environments

User-defined degradation models open the door to consistent aging simulations across different simulators. As discussed in Section II, EDA tools offer their own APIs, allowing the

model integration into their aging simulation flows. It is also possible to integrate the model using the OMI API for EDA environments supporting it, [redacted] [redacted]. Although different APIs share the same basic working principle, they have several differences in their internal architecture and complexity. Additional differences can be found in the simulation flows among EDA tools.

In order to achieve the goal of integrating an aging model into different simulators, a significant effort is required to get access to the necessary API documentation and source codes as well as studying them in detailed to understand their capabilities, limitations, and interactions with the simulator. Therefore, it is convenient to have a clear procedure guiding the steps needed to achieve a simulation-ready aging model.

A proposed methodology is presented in Fig. 3-3. The first step is to analyze the mathematical description of the degradation model and clearly define its requirements:

a) Determine the information the model will need from: the simulation environment (temperature, voltages or currents); the netlist (aging model parameters or simulation control settings) or the transistor model card ("fresh" model card parameters). It is

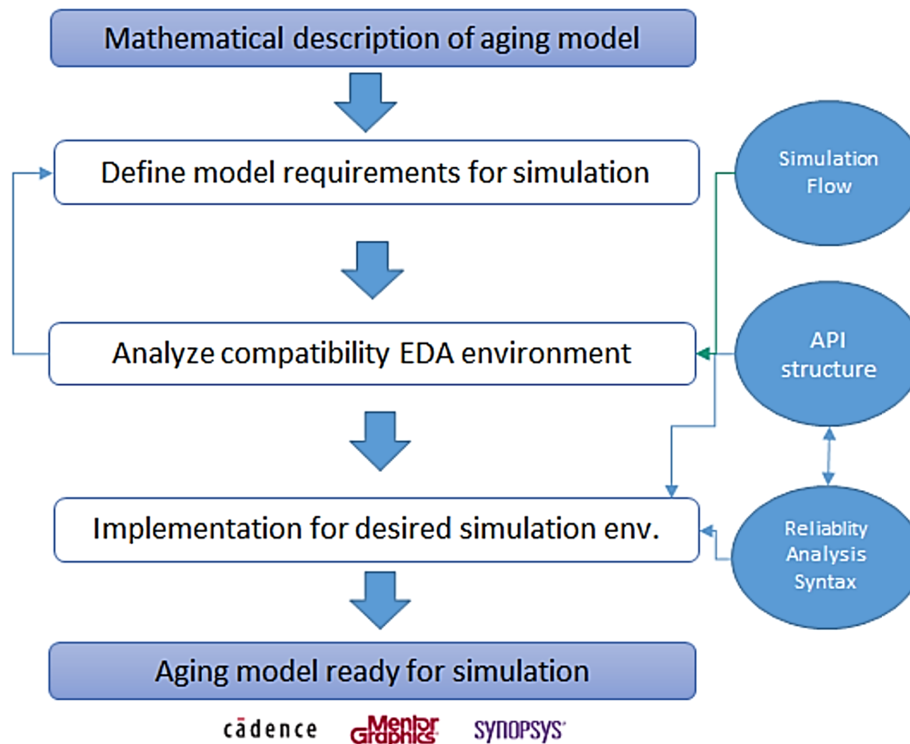


Fig. 3-3. Steps followed to integrate aging models into different EDA environments.

also important to determine in which stage of the aging simulation flow the information will be required.

b) Determine the information the model will give back to the simulator in function of how the degradation is mapped.

c) Consider simulation features offered by the simulator (Monte Carlo analysis, gradual degradation in multiple steps or load information from file) as well as the transistor compact models supported.

Once the model requirements are defined, it is necessary to analyze the compatibility of the model requirements and the desired API.

To clarify the importance of this analysis, let us assume two relatively simple degradation models. Model A describes the aging of a BSIM4 transistor as a reduction of the carrier mobility, in function of temperature T, gate to source voltage V_{gs}, drain to source voltage V_{ds}, and the transistor´s length L and width W:

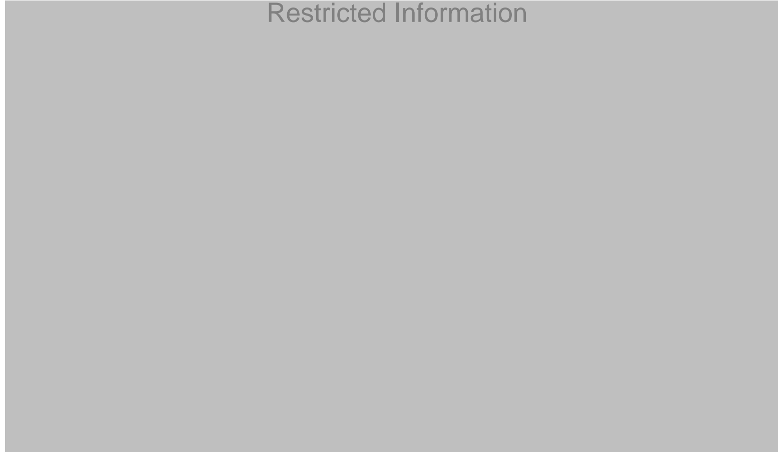
$$Deg_A = \Delta\mu_o = f(T, Vgs, Vds, L, W) \quad (3\text{-}1)$$

and degradation model B describes the aging of a BSIM3 transistor as a shift in the drain to source current I_{ds}, in function of the same variables as in (3-1):

$$Deg_B = \Delta I_{ds} = f(T, Vgs, Vds, L, W) \quad (3\text{-}2)$$

Both models describe the degradation using typical stress conditions: temperature T, device voltages (V_{gs}, V_{ds}), and dimensions (L, W), which are available in the data structures of all the APIs described in Table I, as well as in the OMI API.

TABLE VI
RESULTS OF COMPATIBILTY ANALYSYS TO DETERMINE THE IMPLEMENTABILITY OF AGING MODELS



3.4. Simulation Study And Results Comparison

This section presents the results of the implementation of the hot carrier injection (HCI) and negative bias instability (NBTI) degradation models described in Chapter 2, for a 130 nm BSIM4 Predictive Technology Models (PTM) in CMOS technology [NIMO-06]. These models have been integrated into the simulators SPECTRE, from Cadence, and HSPICE, from Synopsys, using their tool-specific APIs (URI and MOSRA API respectively), along with the OMI API. In the following discussion, the simulators will be referenced as “Simulator 1” and “Simulator 2”, respectively.

A simulation study was first designed, consisting of aging simulations performed on single NFET and PFET devices, to analyze the degradation of electrical characteristics of the transistors, as well as circuit simulations containing multiple transistors, specifically 3- and 21-stage ring oscillators (ROs). For the single device simulations, the PFET transistor is stressed with a temperature T = 175 °C and $V_{gs} = -1.2$ V, and the electrical characteristics observed are:

a) the degradation of a specific threshold voltage VTHI, defined as the value of V_{gs} causing an $I_{ds} = 100\times10^{-9}\,(W/L)$ A, and
b) and IDLIN, defined as I_{ds} at $V_{gs} = -1.2$ V and $V_{ds} = -0.05$ V.

Similarly, the NFET transistor is stressed at room temperature T = 27 °C with V_{ds}= 1.2 V, observing:

c) the maximum transconductance GMAX, measured at V_{ds} = 0.05 V

d) and IDLIN, defined as I_{ds} at V_{gs} = −1.2 V and V_{ds} = −0.05 V.

The continuous lines in Fig. 3-4 show the evolution over time of the degradation of the PFET's VTHI and IDLIN under NBTI, obtained from both simulators, using the intrinsic API as well as the OMI API. Fig. 3-4 also shows the difference between the degradation results obtained with distinct APIs, after arbitrarily selecting Simulator 1 with the OMI API as a reference value. Equivalently, Fig. 5 shows the results of GMAX and IDLIN degradation in the NFET under HCI.

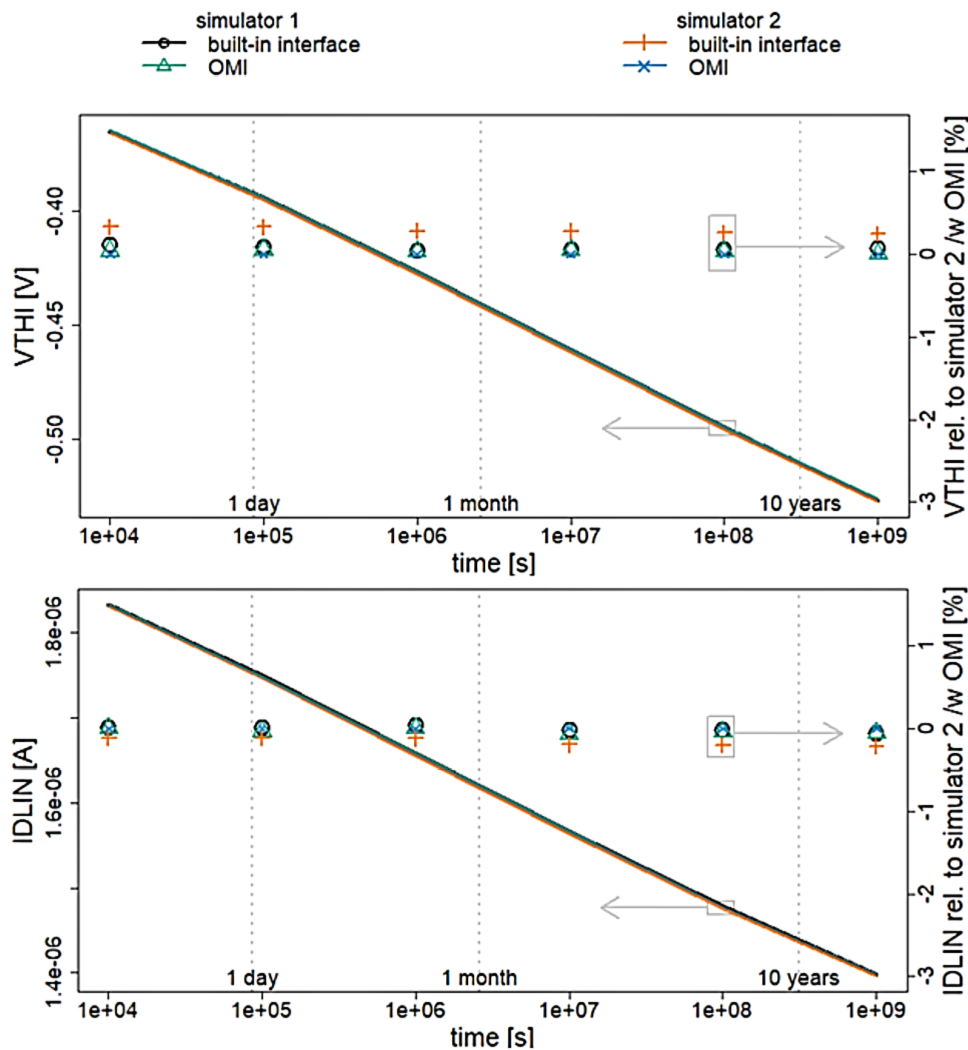


Fig. 3-4 VTHI and IDLIN degradation of PFET under NBTI.

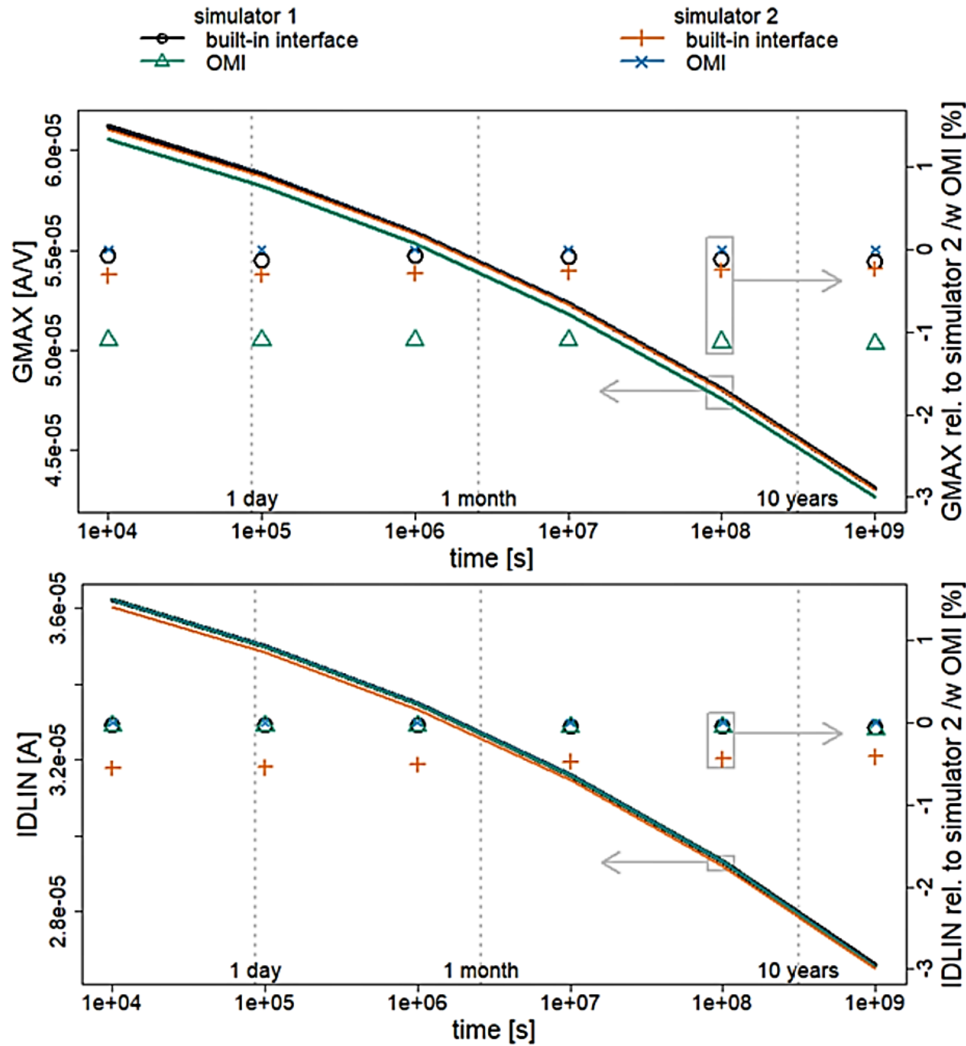


Fig. 3-5 GMAX and IDLIN degradation of NFET under HCI.

The difference in the results are clearly below 1%, with the exception of GMAX degradation in the NFET, in which the maximal difference is around 1%. Nevertheless, the results can be consider practically identical.

Continuing with this study, the 3- and 21-stage ring oscillators operate at V_{dd} = 1.2 V and are forced into oscillation by applying reasonable initial conditions. The 3-stage RO is aged under HCI at room temperature, while the 21-stage RO is aged at T = 175 °C under NBTI. Fig. Fig. 3-6 and Fig. 3-7 show the frequency degradation of these circuits, respectively. Once again, the figures show the measured degradation in the simulation (continuous lines) as well as the difference between the implementations, where a maximal deviation within 1.5% can be seen for the 3-stage RO, and around 1% for the 21-stages RO. The difference between the results can be decreased

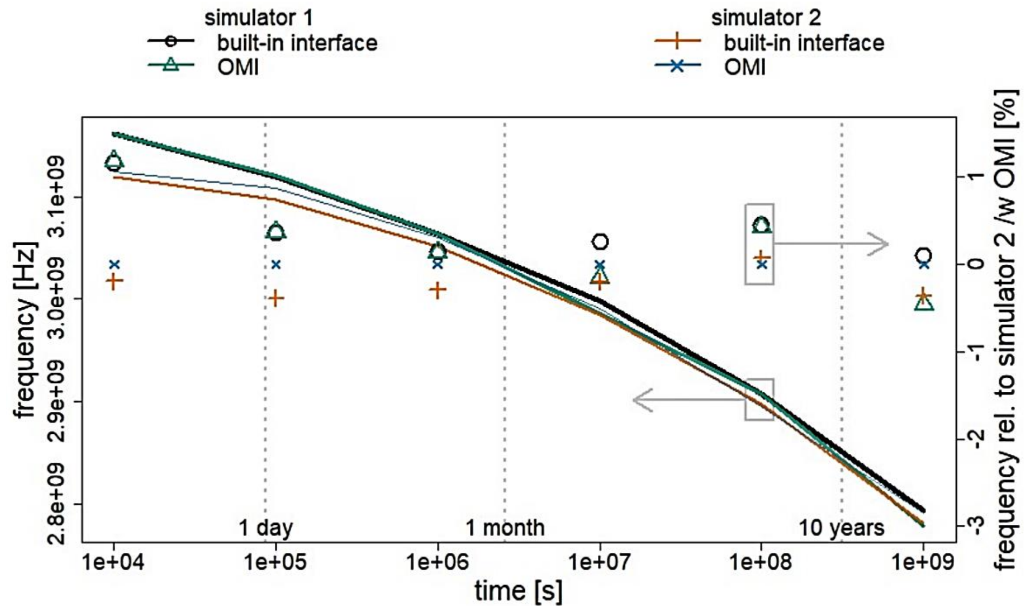


Fig. 3-6 Frequency degradation of 3-stage ring oscillator (RO) under HCI aging.

further by fine tuning the simulator accuracy, considering time discretization in the transient analysis and the measurement and control options used in the simulation.

The results showed in this section have been published as a poster presentation in the TuZ 2019 workshop [Velarde-19].

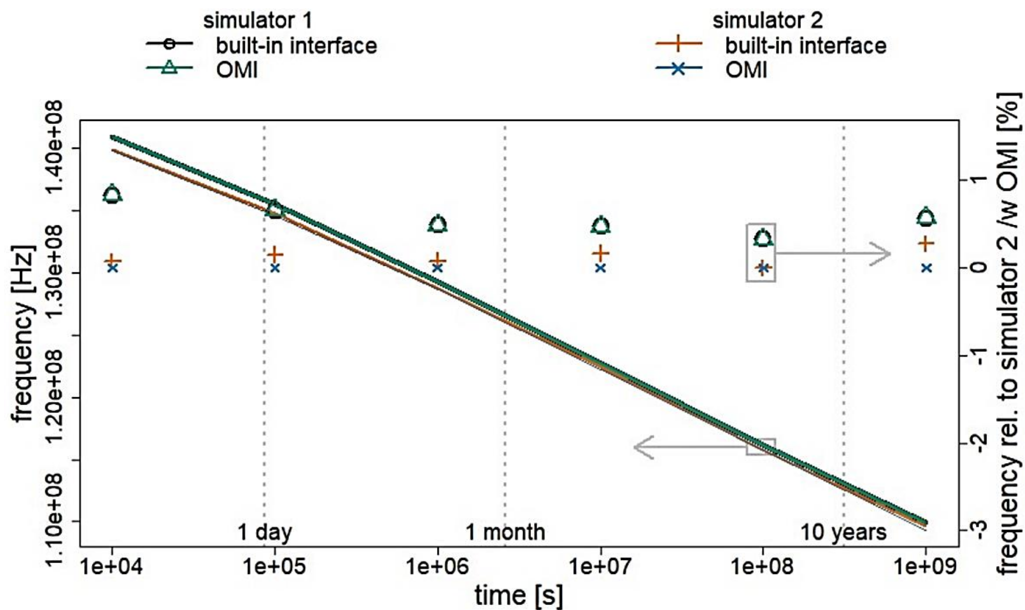


Fig. 3-7 Frequency degradation of 21-stage RO under NBTI aging.

3.5. Conclusions

The assessment of the lifetime reliability for integrated circuit (IC) designs can be performed before manufacturing using circuit level aging simulations with appropriate degradation models. The importance of these simulations, and their underlying models, is expected to rise due to multiple emerging application fields requiring complex designs in advanced technology nodes used in hazardous conditions, as well their growing usage in safety critical industries such as the automotive and aerospace industries. Semiconductor foundries, responsible for characterizing their technologies, face two challenges regarding lifetime reliability. First, they need to define reasonable degradation models based on their measured data, balancing accuracy, complexity, and characterization effort. Second, it is important for the foundries to ensure the consistency of the models delivered in their process design kit (PDK), so they yield identical results in the different electronic design automation (EDA) environments they support. This chapter focused on the implementation of degradation models in different EDA environments by using their built-in application programming interfaces (APIs) as well as the emerging standard interface OMI API. Using standard modeling approaches for negative BTI (NBTI) and hot carrier injection (HCI), a simulation study was performed to analyze the feasibility of a consistent implementation of aging models across various EDA tools. The degradation results obtained in two different simulators are practically identical, with differences in the calculated degradation of the electrical parameters below 1% for single transistor simulations, and between 1% and 1.5% in simulations with multiple transistors. A more detailed analysis of performance differences between the APIs and the simulators considering more complex models or larger circuits are topics for future work.

4. Comparison of Modeling Approaches for Transistor Degradation

4.1. Introduction

The relevance of reliability issues in semiconductor technologies has increased since the length of the transistor channel achieved the submicron range and the influence of well-known degradation mechanisms, such as bias temperature instability (BTI) and hot carrier injection (HCI), which started to alter the electrical behavior of the transistors, creating a significant aging effect [Tae-Hyoung-13], [Hussin-11]. The main electronic design automation (EDA) vendors incorporate aging simulation capabilities into their design environments, allowing the assessment of a circuit's lifetime reliability, but the accuracy and effectiveness of an aging simulation depends strongly in the aging model describing the transistors degradation.

HCI and BTI degradation models serve as a link between the physical degradation measured at wafer level and the circuit simulator. Aging degradation is typically described as the shift in different electrical figures of merit (FOM), such as: threshold voltage (VTH), maximum transconductance (GMAX), linear and saturation current (IDLIN and IDSAT), among others. The FOMs are recorded after stressing the device during the wafer level reliability (WLR) characterization. Typically, a stress-measure-stress procedure, clearly defined in industrial standards [JEDEC-01], [JEDEC-04b], is followed to characterize the degradation of a given semiconductor technology. The experimental data obtained by the characterization process can then be used to fit empirical models, or to validate physics based degradation models.

Two main approaches are typically used to model aging effects for FETs in an aging simulation. In a model card approach, the degradation of the transistor's FOMs is mapped into shifts of selected parameters of the transistor's underlying model card. In the second approach, the electrical behavior of a "fresh" transistor is altered by adding voltage and/or current sources within a subcircuit [Gielen-13].

This chapter gives a general examination of the two degradation modeling approaches and analyzes the influence that these modeling approaches have in the simulation performance,

especially as the complexity of a circuit increases.

The rest of chapter is organized as follows. Section 4.2 describes the characteristics of the modeling approaches and discusses their differences. In Section 4.2, example degradation equations are used to develop aging models for both modeling approaches. Section 4.4 contains a simulation study using ring oscillators (ROs) with varying number of stages, to evaluate the performance of the models in a circuit level simulation. Finally, Section 4.5 encloses the conclusions of the report.

4.2. Modeling approaches for Transistor Degradation

The two basic approaches typically used to represent transistor's degradation in a circuit level simulation are conceptually illustrated in Fig. 4-1. A representation of the model card adaptation, where the characteristics of the FET itself are changed by modifying parameters of the underlying transistor model card, is shown in Fig. 4-1a. Similarly, Fig. 4-1b represents a subcircuit model, which consists of controlled current and (or) voltages sources placed around the unaltered FET, mimicking its degraded electrical behavior [Gielen-13].

In order to develop a FET aging model using the model card approach, it is necessary to select reasonable parameters of the transistor compact model (e.g., BSIM3, BSIM4, PSP) to capture the degradation. For simple degradation models, it is possible to select parameters based on the understanding of the transistor compact model equations. For example, in a first approximation, the parameter representing the long-channel threshold voltage at zero substrate bias, VTH0, can be selected to depict the impact of BTI on V_{th}. Similarly, it would be reasonable to select the low-field carrier mobility parameter, U0, to capture the shifts in IDSAT due to HCI

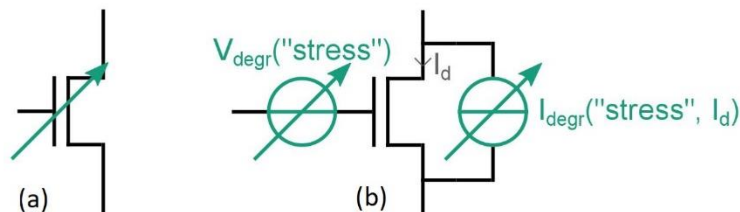


Fig. 4-1 Basic approaches to model FET degradation: (a) model card adaptation; (b) subcircuit model (example simplified from [Gielen-13]).

degradation.

After the selection of the model card parameters, a vector function ***f*** mapping the degradation of the selected FOM to shifts or deviations in model card parameters has to be determined. Although ***f*** might not be explicitly known, its inverse can be evaluated by circuit simulation. Additional FOMs, such as GMAX or IDLIN, could be taken into account by considering further model card parameters, such as RDSW, VSAT, AGS, DSUB, LPE0, NDEP [Pieper-17], naturally increasing the dimensionality of ***f***. For a proper selection of reasonable parameters in complex models, it is useful to do a sensibility analysis to extract the influence different model card parameters have on the relevant FOMs.

In the case of the subcircuit modeling approach, the original FET model remains unchanged and the description of the degradation can be done independently from the underlying compact model type or version, as well as its internal parametrization. To accurately capture first-order and

TABLE VII
PROPERTIES OF DEGRADATION MODELS BASED ON MODEL CARD ADAPTATIONS AND SUBCIRCUITS

Model card adaptations	Subcircuits
Does not introduce new nodes to simulation netlist	Introduces new nodes and/or branches into simulation netlist,
Model cards cannot be shared between FET instances in simulations of aged netlist due to individual degradation	Model cards can be shared between FET instances in simulations of aged netlist
Make use of physics built into underlying compact model, potential inaccuracies when the underlying compact model is not able to capture the true degradation physics	Model has to capture degradation physics in the subcircuit definition
Requires re-calibration after updates to nominal models	Independent of type and parametrization of the nominal compact model
Introduces implicit device geometry and temperature dependencies from the mapping ***f***	Geometry and temperature dependencies need to be explicitly defined

higher-order impacts of FET degradation, the controlled sources surrounding the transistor may have multiple dependencies to the stress conditions (e.g., voltages, currents, temperature, time, etc.) and bias conditions. The complexity of these dependencies increases with the number of FOMs considered in the model. For example, in the subcircuit model shown in Fig. 1b, the current I_{degr}, flowing in the opposite direction of the drain current I_d, is controlled by stress conditions and the fresh I_d. It is possible to find the dependencies needed to generate an I_{degr} representing the degradation of the saturation current IDSAT, but these will be different if I_{degr} should also model IDLIN degradation. These dependencies, especially with further FOMs, could be non-linear and dramatically increase the model complexity. Table VII summarizes the basic properties of the two modelling approaches previously discussed.

4.3. Definition of Aging Models for Different Approaches

To compare the two aging modelling approaches discussed in Section II, a simulation study based on the aging degradation equations described in Chapter 2 is performed. These example models were developed for a 130 nm predictive technology model (PTM), with a BSIM4 model card [NIMO-06]. The models were originally conceived for model card adaptions, so they need to be modified such that the same equations can be used for both degradation modelling approaches.

In the PFET NBTI degradation model, the shift in threshold voltage $\Delta vth0$ defined in Chapter 2 depends on the applied gate to source voltage V_{gs}, the temperature T and the stress time t, as follows:

$$\Delta vth0 = \frac{\Delta_1}{1 + \beta\Delta_1} \tag{4-1}$$

and

$$\Delta_1 = A exp\left(\frac{E_{aa}}{kT}\right) V_{gs}^m t^n \tag{4-2}$$

with $A = 0.2915$, the activation energy $E_{aa} = -0.2$, $m = 3.5$, $n = 0.15$, $\beta = 3$ and k is the Boltzmann constant.

For the model card adaptation, the degraded model card value $VTH0_{aged}$ is:

$$VTH0_{aged} = VTH0_{fresh} - \Delta vth0 \tag{4-3}$$

and representing the nominal model card value as $VTH0_{fresh} = -0.321$.

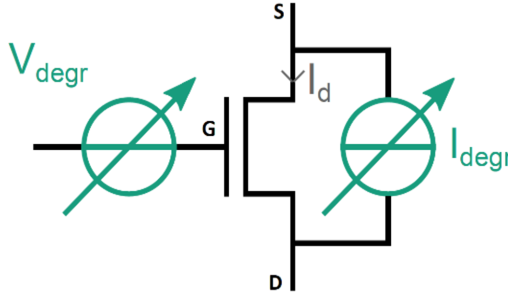


Fig. 4-2 Subcircuit used to model NBTI degradation in the PFET.

Fig. 4-2 shows the subcircuit used to model the NBTI degradation in the PFET. For the voltage source at the gate,

$$V_{degr} = -\Delta vth0 \tag{4-4}$$

with ΔV_{th} defined by (4-1) and (4-2), and for the current source:

$$I_{degr_NBTI} = \mathrm{C_{nbti}}(\Delta vth0, \mathrm{T}) \cdot \mathrm{I_d} \tag{4-5}$$

where C_{nbti} is a constant, whose value depends on the calculated ΔV_{th0} and the circuit temperature T. The voltage source V_{degr} is sufficient to model the degradation of VTH, which is the goal of the degradation model. The current source $I_{degr,NBTI}$ must be added to achieve the same DC characteristics obtained with the model card model, since the parameter VTH0 affects the threshold voltage and the drain current by influencing the effective carrier mobility [Hu-03].

The NFET HCI model defined in [7] calculates $\Delta\mu_0$ as a function of stress time t and the applied drain to source voltage V_{ds} using a saturation equation as in (4-1), with:

$$\Delta_1 = A \cdot exp\left(\frac{C}{V_{ds}}\right) t^n \tag{4-6}$$

where $A = 1.215$, $C = 8.15$, and $n = 0.12$. In the model card approach, the degraded parameter U0 is defined as:

$$\mu0_{aged} = (1 - \Delta\mu0) \cdot \mu0_{fresh} \tag{4-7}$$

with the nominal parameter $\mu0_{fresh} = 0.05928$.

The subcircuit depicted in Fig. 4-3 has been selected to model the NFET HCI degradation, with the current source implemented as:

$$I_{degr_HCI} = C_{HCI}(\Delta\mu0, T) \cdot I_d \tag{4-8}$$

where the constant C_{HCI} depends on the calculated degradation and the temperature. The HCI subcircuit model does not include a voltage source at the gate, since the BSIM4 parameter U0 mainly affects I_d, so the current source in (4-8) appears sufficient. Although the model card based

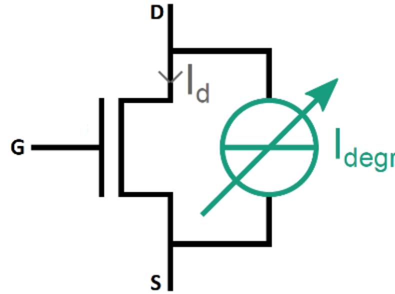


Fig. 4-3 Subcircuit used to model HCI degradation in the NFET.

HCI model does not considers temperature, the underlying compact model has implicit temperature dependencies, so they needed to be modelled in the subcircuit based model to achieve the same degraded behavior, hence the temperature dependency in C_{HCI}.

An inverter using the NFET and the PFET transistors is implemented to verify the DC behavior of both models. In a DC simulation, a sweep of the inverter input from logic 0 to logic 1 is carried out at different temperatures and with different degradation values. Fig. 4-4 shows a

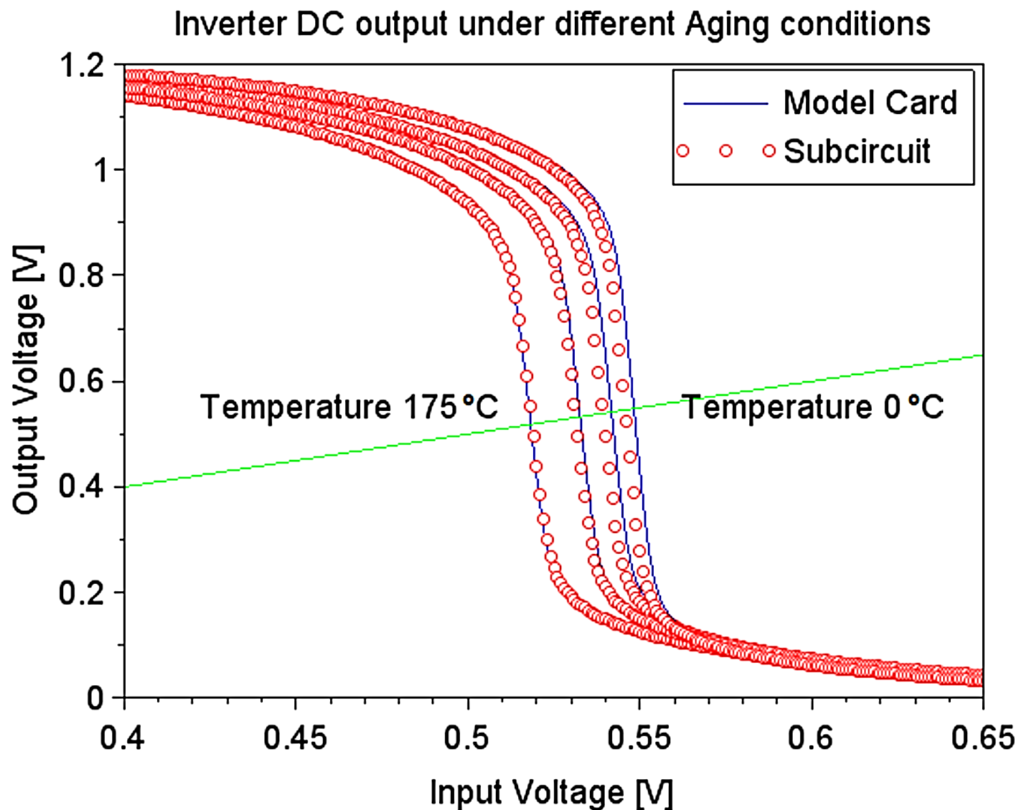


Fig. 4-4 Input (green line) and output waveforms (blue lines and red circles) from DC simulations of fresh and aged inverter instances with model card adaptation and subcircuit model.

comparison of the output waveforms obtained with both models, showing a good agreement between the two approaches over a wide temperature range.

4.4. Comparison of Simulation Performance of the Aging Modeling Approaches

To study the impact of the degradation modeling approach on an aging simulation performance, especially when the number of transistors (and nodes) increases, aging simulations are performed in various inverter ring oscillators (RO) with different number of inverters. In these simulations, the degradation over time of the oscillation frequency *f*, and the power consumption *P*, are measured. For a nominal transient simulation at $T = 27$ °C, the oscillation frequency for a 21-stage R0 is $f = 0.448$ GHz, with a power consumption of $P = 62.41$ μW. The corresponding values for a 501-stage RO are $f = 18.55$ MHz and $P = 63.07$ μW.

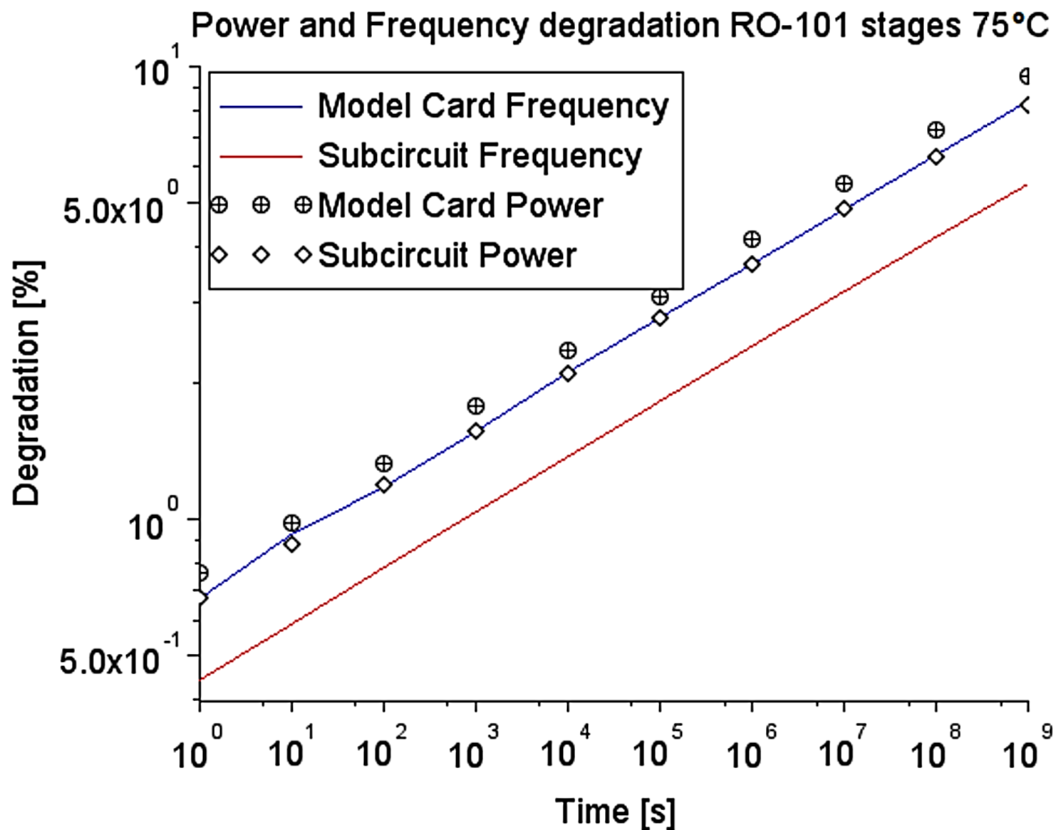


Fig. 4-5 Degradation of oscillation frequency and power consumption over time for a 101-stage RO at $T = 75$ °C.

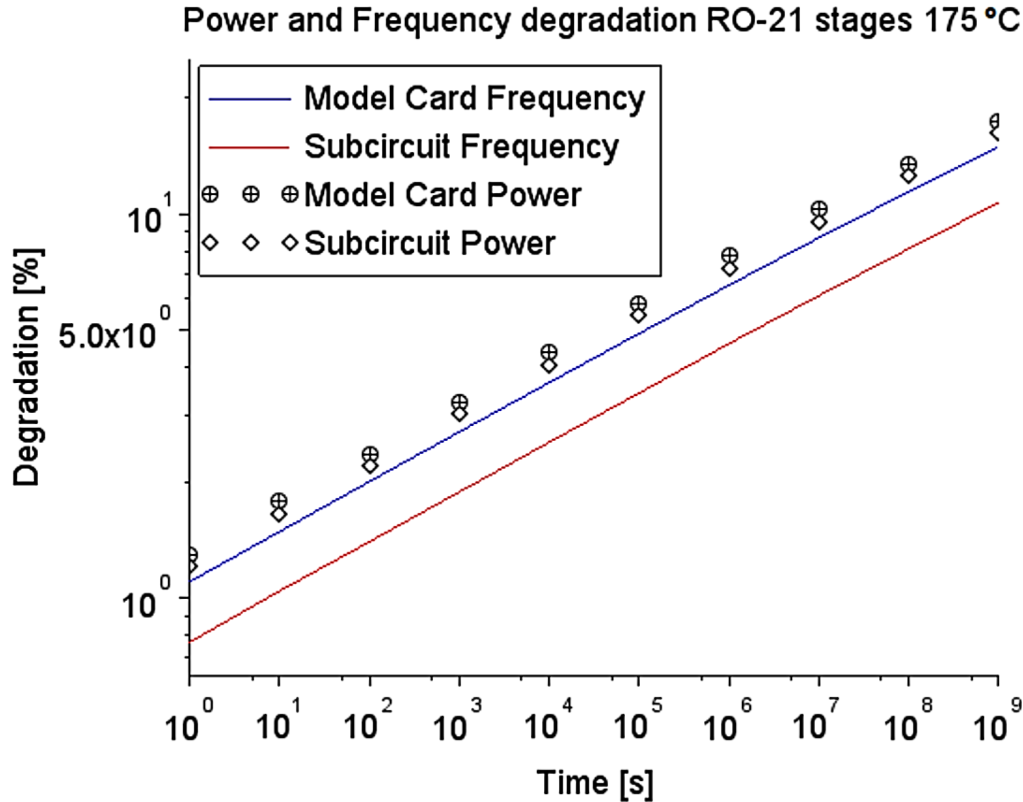


Fig. 4-6 Degradation of oscillation frequency and power consumption over time for a 21-stage RO at T =175 °C.

First, the degradation results of both approaches are compared. Fig. 4-6 shows f and P degradation for a 21-stage RO under NBTI and HCI aging mechanisms at T = 175 °C. Similarly, Fig. 4-5shows the degradation results for a 101-stage RO at T = 75 °C. The aging simulations have been carried out at high temperatures to make the NBTI effect more significant.

In both cases, the model card approach predicts larger degradation that the subcircuit based model. For example, the frequency degradation for the 21-stage RO at $t = 10^8$ s is ~11.5 % for the model card approach, but only ~8 % for its subcircuit counterpart. These differences have been seen throughout different simulations and number of RO stages.

In Section 4.3, the models were designed to have identical DC behavior, without considering any parasitic or capacitive effects that may affect transient simulation. In the model card approach, VTH0 is increased to model NBTI degradation, but this also increases parasitic FET capacitances [Hu-03], leading to a different performance. To achieve identical transient behavior between the two model approaches, a deeper analysis of the effects of VTH0 is needed.

Furthermore, measurements of the real frequency degradation of the RO would be needed to verify the actual behavior and determine if parasitic effects need to be considered.

To analyze the impact of the modeling approach in the simulation runtime, the transient simulation times of aging simulations have been analyzed for ROs with different number of stages, from 21 to 501. On a standard server computer, 100 aging simulations for each RO were carried out and the mean simulation time recorded. All the simulations were performed under a particular stress scenario, with T = 175 °C, bias voltage V_{DD} = 1.2 V, and stress time t_{stress} = 10^5 s.

The mean simulation time for the nominal 21-stage RO is 1.31 s. The mean simulation time for the aged circuit with the model card approach shows no significant increase. For the subcircuit approach, simulation time is 1.44 s (+11%). For the 501-stages RO, the mean simulation times is 262 s for the nominal circuit, 336 s for the aged circuit with the model card approach and 431s for the aged circuit with the subcircuit approach. For the 501-stage RO the subcircuit approach shows a significant increase in the mean simulation time as compared to the nominal simulation (+65%) and the aged simulation with the model card (+28%).

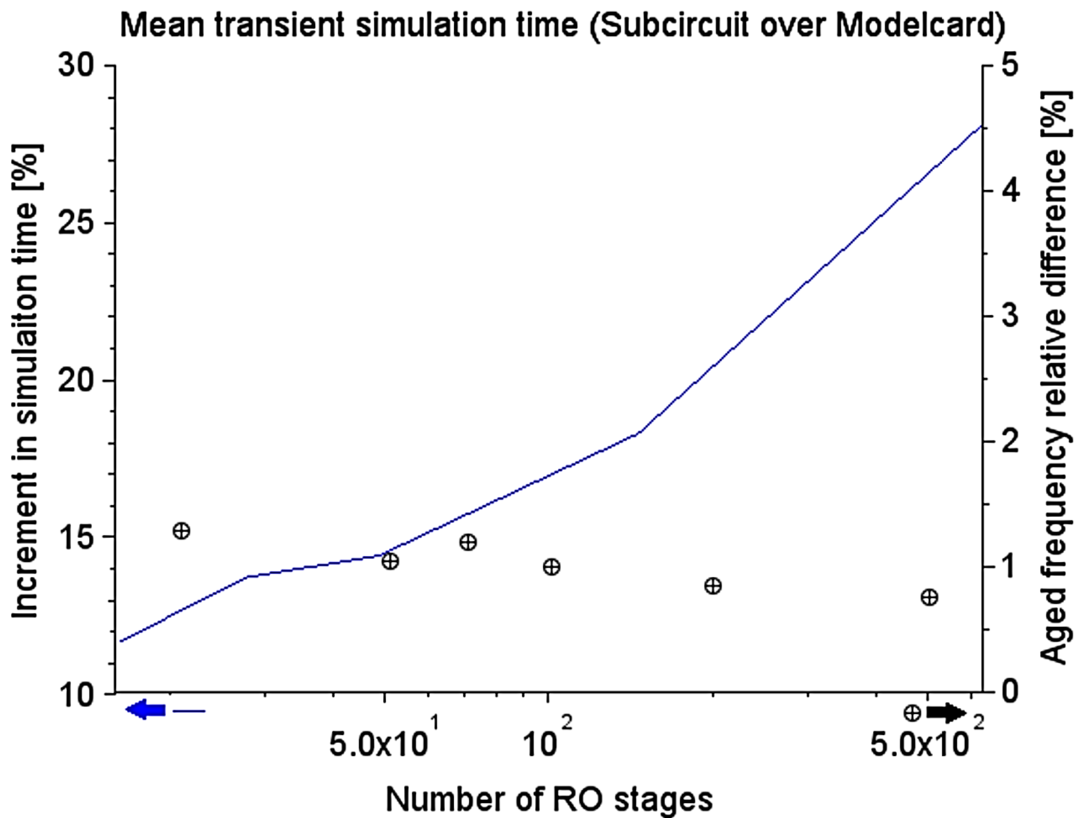


Fig. 4-7 Increase of mean simulation time (subcircuit over model card, blue line) and relative difference in degraded frequency against number of RO stages (circles crossed). Stress conditions are: V_{DD} = 1.2 V, T = 175 °C and t_{stress} =10^5 s.

Fig. 4-7 shows the increase in the mean transient simulation time of the subcircuit approach over the model card approach. The additional nodes introduced in the circuit by the subcircuit models affect the simulation performance of the aged circuit as compared to model card version, showing worst performance as the complexity of the circuit grows. Fig. 4-7also shows the relative difference between the two approaches in the aged frequency *f*. A decrease in the relative difference can be seen as the number of R0 stages increases and *f* decreases, reducing the impact of the parasitic capacitances built in the model card approach due to the use of VTHO. In this study, 100 simulations were executed to mitigate the influence of external factors such as server loading and utilization, nevertheless, they still influence the simulation performance. The results described in this chapter will be presented in a conference paper at the 49th European Solid-State Device Research Conference (ESSDERC), in Krakow, Poland [Lange-19].

4.5. Conclusions

Field effect transistors (FET) degrade over time due to known mechanisms such as negative bias temperature instability (NBTI) and hot carrier injection (HCI). Aging simulations at circuit level allow integrated circuits (IC) designers to analyze the impact degradation effects have in the performance and lifetime reliability of a particular IC design. The critical element in an aging simulation is the degradation model, which determines the behavior of an aged FET due to given stress conditions.

This chapter discussed the differences between two modeling approaches. The main disadvantage of the subcircuit approach over the model card approach is the introduction of extra nodes into the simulation, which has an impact in the simulation performance. The model card approach makes uses of the built-in equations of the transistor compact model, which introduces geometry and temperature dependencies into the degradation model.

Using examples of NBTI and HCI degradation equations, models using the two approaches were developed to have identical direct current (DC) behavior, since degradation models are based on DC stress conditions. Nevertheless, when these models were used in transient simulations with switching circuitry, the models showed a significantly different behavior. This is most likely due to the change in the parasitic capacitances of the transistor’s compact model introduced by the

degradation of model card parameters, such as VTH0 or U0. Future work should look into detail how FETs degrade under non-DC stress conditions to develop an accurate model for real application scenarios.

The simulation performance of the modelling approaches was analyzed using ring oscillators (ROs) of different number of stages. As expected, the introduction of extra nodes in the subcircuit approach lead to longer transient simulation runtimes for the aged circuit as compared to the model card approach; the increment of simulation time grows as the number of transistors in the circuit increases, showing increments in mean simulation times up to ~28% for a 501-stage RO.

Conclusions

The work presented in this thesis focused on the consistent integration of aging degradation models into different electronic design automation (EDA) environments by implementing user-defined models exploiting the different application program interfaces (API) available for the major EDA simulators. More specifically, the present thesis studied the API's offered by Cadence, Mentor Graphics, and Synopsys for their respective circuit simulators, SPECTRE, ELDO and HSPICE, in addition to the independent Open Model Interface (OMI). Example HCI and NBTI degradation models were implemented in Cadence and Synopsys own API's, as well as the OMI, and were simulated in SPECTRE and HSPICE, showing coherent results among the different simulators and APIs.

Further contributions from this thesis work include an analysis and comparison of the two main approaches used to model transistor degradation: degrading selected parameter in the model card or using subcircuits. HCI and NBTI models were designed to achieve matching DC behavior and their performance was compared in a simulation study using ring oscillators with different number of stages. It was shown that despite identical DC behavior between the two approaches, a significant difference was observable when comparing the frequency degradation of the ring oscillators. This discrepancy is due to the change in parasitic capacitances introduced in the model card approach, which degraded model card parameters, affecting also the values of the parasitic capacitances. Additionally, a significant difference in the transient simulation time was observed in the subcircuit approach, showing longer simulation times due to the introduction of extra nodes and branches.

Further potential work could focus on the study of aging degradation under transient or AC stress, in order to achieve more robust and exhaustive empirical degradation models for transient simulations, and to better understand the effects transistor degradation have under time varying stress conditions. Although the OMI is an important step towards standardization, the first version of the OMI is still limited. Further work could also study the improvements in the next version of the OMI API, in order to determine if it could be appropriate to use it exclusively in the implementation of degradation models for different simulators, which is currently not the case.

Appendix

A. LIST OF INTERNAL REPORTS

[1] F. A. Velarde-González and J. E. Rayas-Sánchez, “Aging mechanisms in CMOS technologies,” Internal Report *CAECAS-18-06-R*, ITESO, Tlaquepaque, Mexico, Apr. 2018.

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