INSTITUTO TECNOLÓGICO
Y DE ESTUDIOS SUPERIORES DE OCCIDENTE

Reconocimiento de validez oficial de estudios de nivel superior según acuerdo secretarial 15018, publicado en el Diario Oficial de la Federación el 29 de noviembre de 1976.

Departamento de Electrónica, Sistemas e Informática

DOCTORADO EN CIENCIAS DE LA INGENIERÍA


# ANÁLISIS Y OPTIMIZACIÓN DEL DISEÑO DE REDES DE ENTREGA DE POTENCIA MEDIANTE MODELOS SUSTITUTOS PARA APLICACIONES DE SERVIDORES DE CÓMPUTO EN LA NUBE

Tesis que para obtener el grado de

DOCTOR EN CIENCIAS DE LA INGENIERÍA

presenta: Felipe de Jesús Leal Romo

Director de tesis: Dr. José Ernesto Rayas Sánchez

Tlaquepaque, Jalisco. Septiembre de 2020

DOCTOR EN CIENCIAS DE LA INGENIERÍA (2020) ITESO, Tlaquepaque, Jal., México

**TÍTULO:** **Análisis y optimización del diseño de redes de entrega de potencia mediante modelos sustitutos para aplicaciones de servidores de cómputo en la nube**

**AUTOR:** Felipe de Jesús Leal Romo
Ingeniero en Electrónica y Sistemas de Comunicación Digital (Universidad Autónoma de Aguascalientes, México)
Maestro en Diseño Electrónico (ITESO, México)

**DIRECTOR DE TESIS:** José Ernesto Rayas Sánchez
Profesor Numerario del Departamento de Electrónica, Sistemas e Informática, ITESO
Ingeniero en Electrónica (ITESO, México)
Maestro en Sistemas Electrónicos (ITESM Campus Monterrey, México)
Doctor en Ingeniería Eléctrica (Universidad McMaster, Canadá)
*Senior*, IEEE

**NÚMERO DE PÁGINAS:** xxviii, **118**

ITESO – The Jesuit University of Guadalajara

Department of Electronics, Systems, and Informatics

DOCTORAL PROGRAM IN ENGINEERING SCIENCES


# SURROGATE-BASED ANALYSIS AND DESIGN OPTIMIZATION OF POWER DELIVERY NETWORKS FOR CLOUD COMPUTING SERVER APPLICATIONS

Thesis to obtain the degree of

DOCTOR IN ENGINEERING SCIENCES

Presents: Felipe de Jesús Leal-Romo

Thesis Director: Dr. José Ernesto Rayas-Sánchez

Tlaquepaque, Jalisco, México
September 2020

PHD IN ENGINEERING SCIENCES (2020) ITESO, Tlaquepaque, Jal., Mexico

**TITLE:** **Surrogate-based Analysis and Design Optimization of Power Delivery Networks for Cloud Computing Server Applications**

**AUTHOR:** Felipe de Jesús Leal-Romo
Bachelor's degree in electronics engineering (*Autónoma de Aguascalientes*, Mexico)
Master's degree in electrical engineering (ITESO, Mexico)

**THESIS DIRECTOR:** José Ernesto Rayas-Sánchez
Department of Electronics, Systems, and Informatics, ITESO-The Jesuit University of Guadalajara
Bachelor's degree in electronics engineering (ITESO, Mexico)
Master's degree in electrical engineering (ITESM, Mexico)
Ph.D. degree in electrical engineering (McMaster University, Canada)
Senior, IEEE

**NUMBER OF PAGES:** xxviii, **118**

*To my wife, Melina, whose patience and understanding*
*have made this achievement possible*

# Resumen

A medida que el cómputo en la nube aumenta su modelo de uso, es muy importante que los proveedores y las compañías que brindan este servicio reduzcan su costo total de propiedad. Analizando detenidamente las oportunidades de reducción de costos, una de las áreas de oportunidad más prometedoras es el consumo de energía del servidor. Esto implica el diseño de un hardware robusto capaz de funcionar adecuadamente durante alta demanda de cómputo, evitando grandes cantidades de fuga de energía traducidas en disipación de calor, y por consecuencia, más energía gastada en mantener frescos los centros de datos. Tomando este contexto como punto de partida, el trabajo de los ingenieros de entrega de potencia (EP) adquiere más relevancia al proporcionar recomendaciones razonables que no aumenten el costo en la lista de materiales de los PCBs y los sustratos de empaquetado del silicio, maximizando el rendimiento y evitando un consumo excesivo de energía. En esta tesis doctoral, EP se presenta como una disciplina que implica decisiones balanceadas entre el rendimiento y el ahorro de costos. En la tesis se demuestra cómo la implementación del diseño de experimentos y el mapeo espacial pueden ser enfoques numéricos muy eficaces para ayudar a los ingenieros de EP a tomar decisiones más rápidas e informadas, al tiempo que se optimiza el diseño de redes de suministro de potencia (PDN, por sus siglas en inglés) para el servidor. Para lograr una optimización sistemática de la PDN, esta tesis doctoral propone una metodología general para implementar modelos sustitutos. Primero, explotando la extracción de parámetros del modelo circuital de una PDN para aproximar los perfiles de impedancia, y segundo, generando modelos sustitutos de caja negra que permitan una optimización rápida y confiable de la PDN. Para la generación de modelos sustitutos de caja negra, esta tesis compara cuatro diferentes técnicas de aprendizaje automático: Kriging, redes neuronales de regresión generalizada, modelos sustitutos polinomiales y máquinas de vectores de soporte. Los mejores metamodelos resultantes se explotan para una optimización rápida de la PDN en dos aplicaciones industriales distintas: un regulador de voltaje (RV) que implementa detección remota por medio de un sensor dual para aplicaciones de comunicaciones y almacenamiento, encontrando las resistencias y condiciones de carga optimas; y un RV multifase de una PCB de servidor, encontrando configuraciones de compensación óptimas para disminuir la cantidad de capacitores y al mismo tiempo evitar la pérdida de rendimiento del CPU.

# Summary

As cloud computing escalates its usage model, it is very critical for vendors and companies that provide this service to reduce the total cost of ownership (TCO). By looking thoroughly into cost reduction opportunities, one of the most promising areas of opportunity is computer server's power consumption. This means, the design of a robust hardware capable to perform adequately during high computing demand, avoiding large computer's burning power translated as heat dissipation, and in consequence, more power consumed to keep datacenters cool. By taking this precedent as a baseline, power delivery (PD) engineers' job is taking more relevance to provide reasonable recommendations that do not increase bill of materials (BOM) cost of motherboards and packages, and maximize performance avoiding excessive power consumption. In this doctoral dissertation, PD analysis is presented as a discipline that implies trade off decisions between performance and cost savings. It is demonstrated how the implementation of design of experiments (DoE) and space mapping (SM) can be very effective numerical approaches to aid PD engineers taking quicker and informed decisions, while optimizing the design of power delivery networks (PDN) for computer server's design. To achieve a systematic optimization of the PDN, this PhD dissertation proposes a general methodology to implement surrogate-based models. First, by exploiting parameters extraction (PE) for lumped circuit PDN model to fit impedance profiles, and second by generating black box surrogate-based models to enable fast and accurate optimization of the PDN performance. For black box surrogate-based models' generation, this dissertation compares four different machine learning techniques: Kriging, generalized regression neural networks (GRNN), polynomial surrogate models (PSM), and support vector machines (SVM). The best resultant metamodels are exploited for fast PDN optimization in two different industrial applications: a voltage regulator (VR) implementing dual power rail remote sensing, intended for communications and storage applications, to find the optimal sense resistors and loading conditions; and a multiphase VR of a server motherboard, by finding optimal compensation settings to decrease the number of bulk capacitors preventing CPU's performance loss.

# Acknowledgements

The author wishes to express his sincere appreciation to Dr. José Ernesto Rayas-Sánchez, professor of the Department of Electronics, Systems, and Informatics at ITESO, and director of research in the Computer-Aided Engineering of Circuits and Systems (CAECAS) group at ITESO, for his encouragement, expert guidance, and keen supervision as doctoral dissertation director throughout the course of this work. The author offers his gratitude to his managers Luis Barajas-Ruvalcaba and Fernando Bravo, from Intel Corporation, for their support during the development of this dissertation. He also thanks Dr. Esteban Martínez-Guerrero, Dr. Zabdiel Brito-Brito, Dr. Horacio Visairo-Cruz, and Dr. Roberto Murphy-Arteaga, members of his Ph.D. Dissertation Committee, for their interest, assessment, and suggestions.

Special thanks are due to Dr. Zabdiel Brito-Brito, from CAECAS research group at ITESO. It is the author's pleasure to acknowledge fruitful collaboration and stimulating discussions with his colleagues of CAECAS research group at ITESO – The Jesuit University of Guadalajara: Andrés Viveros-Watcher, Francisco Rangel-Patiño, José Luis Chávez-Hurtado, Rafael del-Rey-Acuña, Jorge Dávalos-Guzmán, and Edna Moreno-Mojica.

The author also thanks his peers and colleagues from Intel Corporation, for fruitful cooperation and helpful technical discussions: Marisol Cabrera-Gómez, Brenda Kunz Van Der Rosen, Paulina González-Soto, Carlos Sánchez-Ortíz, Carlos López-Limón, Daniel García-Mora, Jorge Velázquez-Maldonado, and many others.

The author gratefully acknowledges the financial assistance through a scholarship granted by the *Consejo Nacional de Ciencia y Tecnología* (CONACYT), Mexican Government, as well as the financial support provided by Intel Corporation.

Finally, special thanks are due to my family: my wife Melina, my mother in law, and my parents, for their understanding, patience, and continuous loving support.

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# List of Acronyms

| | |
|---|---|
| AC | Alternating Current |
| AI | Artificial Intelligence |
| ANN | Artificial Neural Networks |
| ANOVA | Analysis of Variance |
| ASM | Aggressive Space Mapping |
| BGA | Ball Grid Array |
| BOM | Bill of Materials |
| CCD | Central Composite Design |
| CCM | Continuous Current Mode |
| CPU | Central Processing Unit |
| CRAC | Computer Room Air Conditioning |
| DC | Direct Current |
| DCM | Discontinuous Current Mode |
| DCP | Data Center Pulse |
| DoE | Design of Experiments |
| DSC | Die Side Capacitor |
| EMI | Electromagnetic Interference |
| FCC | Federal Communications Commission |
| FEM | Finite Elements Method |
| FFD | Fractional Factorial Design |
| FIT | Finite Integration Technique |
| GRNN | Generalized Regression Neural Networks |
| GUI | Graphical User Interface |
| HSW | Hard Switching |
| HTA | High Ambient Temperatures |
| I/O | Input-Output |
| IDC | Internet Data Center |
| IPMI | Intelligent Platform Management Interface |
| IT | Information Technology |
| KPI | Key Performance Indicators |
| LDO | Low Dropout Regulator |
| LGA | Land Grid Array |
| LSC | Land Side Capacitor |
| MoM | Method of Moments |
| ODC | On-Demand Cooling |
| OLGA | Organic Land Grid Array |
| PCB | Printed Circuit Board |
| PD | Power Delivery |
| PDN | Power Delivery Network |
| PE | Parameters Extraction |
| PFM | Pulse Frequency Modulation |
| PI | Power Integrity |
| PID | Proportional Integral Derivative |

| | |
|---|---|
| PLL | Phase Locked Loop |
| PM | Power Manager |
| PSM | Polynomial Surrogate Models |
| PSN | Power Supply Noise |
| PSNIJ | Power Supply Noise Induced Jitter |
| PTAS | Power and Thermal Awareness Solution |
| PUE | Power Usage Effectiveness |
| PWL | Piecewise-Linear |
| PWM | Pulse Width Modulation |
| RLC | Resistor Inductor Capacitor |
| SDI | Software Defined Infrastructure |
| SM | Space Mapping |
| SSW | Soft Switching |
| SVM | Support Vector Machines |
| TCO | Total Cost of Ownership |
| VR | Voltage Regulator |
| VRM | Voltage Regulator Module |
| VRTT | Voltage Regulator Test Tool |

# Introduction

Personal computers and internet started to become more and more affordable to people in the 90's. The quest for high performance computing and large compute nodes became a need to solve complex problems and enable more business models, such as online shopping, social networking, storage in the cloud, etc. During the last fifteen years, the demand of large datacenters has become a need for many companies, with emblematic representatives such as Amazon, Google, Facebook, etc.

This business model was acclaimed and is well known as "cloud computing". As a result of the success of this business model, cloud computing is drastically exploiting datacenters performance and demanding for novel computer server's hardware development.

According to [Gartner-18], the hype cycle of cloud computing is categorized into five trends: democratized artificial intelligence (AI), digitalized ecosystems, do-it-yourself biohacking, transparently immersive experiences, and ubiquitous infrastructure.

The outcome of designing a server computer for data centers must provide an outstanding performance; while at the same time power consumption and power dissipation are contained in a very reasonable manner. This fact implies datacenters should not deliver a heavy carbon footprint contribution and costly bills of ownership to keep them up and running.

One way to measure the infrastructure's efficiency of a datacenter is by means of the power usage effectiveness (PUE) concept [Gough-15], which is expressed as the total data center energy use divided by the IT equipment energy use.

This ratio was designed to understand how many watts of power are used to supply power and provide cooling for the IT equipment for one watt of power used to run the computer. One interesting fact is that for outdated datacenters, PUE usually fluctuates between 2 or 3, which means that if PUE = 2, 50 % of the power is used for non-computational purposes such as air-cooling distribution, lights, etc. A PUE > 3 implies a very inefficient datacenter [Gough-15].

Hence, to improve the PUE of a datacenter, power delivery (PD) [Swaminathan-07] design plays a significant role by improving CPU's efficiency. The end goal of power delivery design is to ensure an adequate performance. When CPU is going through different workloads such as high computing stress (heavy load) or idle stages (light load), ensuring that the chip is reliable and the

voltage is stable (healthy silicon) [Pandit-10], [Oh-11], by looking into threshold voltage *vs.* CPU frequency is a major concern for power delivery engineers.

The most basic power delivery foundation based on the performance of a chip given by the impedance profile, $Z(f)$, of the power delivery network (PDN) [Swaminathan-04], from the voltage regulator up to the chip. The main goal of designing a suitable $Z(f)$ consist of keeping the impedance as low and flat as possible across a wide frequency range, which typically comprehends from a few Hz up to several GHz. Once the impedance profile is as flat and low as possible, this impedance profile is subdued to specific workload's stress ($di/dt$) in the time domain space to ensure that the maximum ($V_{max}$) and minimum ($V_{min}$) voltages are met for a given CPU state [Intel-14].

Having the above statements in mind, this type of assessments makes the job of a power delivery engineer very challenging. PD is considered a job that requires enough expertise and understanding of the PDN to make a judgement call between adding more ounces of copper, selecting an adequate voltage regulator solution, determining a balanced quantity of decoupling capacitors, etc. Many trade-off analyses are performed during pre-silicon stages to predict the end behavior of the physical PD implementation. Such PD trade-off analysis requires of many hours simulating complex PDN models in SPICE, which are extracted from the PDN physical model implemented in 2.5-D and 3-D CAD tools, making the whole process of PD assessment and recommendation very computationally intensive and time consuming.

Given the above scenario where intensive computing usage and long hours are typically required to get a solution space of the PDN, advanced numerical techniques such as surrogate-based optimization algorithms [Booker-99], space mapping [Bandler-04], [Koziel-08], design of experiments (DoE) [Montgomery-12], etc., as well as surrogate modeling approaches such as Kriging [Lebensztajn-04], artificial neural networks [Zhang-00], [Rayas-Sánchez-04], and support vector machines (SVM) [Angiulli-07], [Xia-06], among others, provide PD engineers of excellent tools to streamline the design process and give better guidance to layout designers and silicon teams. However, these advanced CAD techniques have not been widely exploited so far in the arena of power integrity and power delivery networks. Pioneer work, such as that by [Torun-18], [Cao-19], and [Rayas-Sánchez-20], have proposed the application of similar numerical techniques to this field, however, there is a lot of work left to do, by enforcing more and more the usage and application of these type of advanced CAD techniques for PDN industry applications.

This dissertation presents an exploration and implementation of different optimization techniques aided by surrogate-based models to design industry-oriented power delivery networks for high-performance computer servers typically applied in cloud computing. This doctoral dissertation is organized as follows.

Chapter 1 presents a brief review of the cloud computing business model and how it is closely related to power delivery design.

Chapter 2 gives a general context of the main power delivery concepts, the difficulties it faces now a days, and describes some fundamental design parameters and criteria, such as impedance profile, voltage droop, voltage regulator efficiency, gain margin, etc.

Chapter 3 covers two optimization techniques to design power delivery networks: design of experiments and space mapping.

Chapter 4 proposes a generic methodology to come up with reliable surrogate-based methods in order to enable accurate and fast power delivery simulation models for further design optimization.

In the General Conclusions, the most relevant remarks about this doctoral dissertation are summarized, based on the overall results of the proposed surrogate-based optimization methodology for server computer power delivery networks. It also briefly describes some future areas of implementation in pre-silicon design and post-silicon design to enhance power integrity and its predictability.

Finally, Appendix A shows the list of references of the fifteen internal research reports developed during the doctoral studies, and Appendix B shows the list of papers published during this same time period.

# 1. Power and Thermal Challenges for Cloud Computing Applications

In recent years, cloud computing started to become a relevant business model. For that reason, it is important to understand some business models adopted by customers and cloud service providers, including service and deployment models. Inherent to cloud computing implementation, it is equally important to review some of its trends, to comprehend upcoming challenges that cloud computing faces to maximize power savings from the server's computers development perspective. This chapter presents a summary of cloud computing, including its general concept, its business models, and main data center's performance indicators, finalizing with upcoming trends that represent challenges from the power delivery's (PD) point of view.

## 1.1. Introduction to Cloud Computing

Cloud computing as a concept is not new. The first person to introduce time-sharing concept and public computing utilization was John McCarthy in 1961 [IEEE-15]. Since then, computers and networks have evolved to make cloud computing a reality. Nowadays, datacenters are a large collection of high-performance computers co-allocated in huge facilities, allowing companies such as Google, Amazon, and others, to rent their resources for several different purposes. Because cloud computing is a wide topic, the scope of this chapter will be introductory. The chapter walks through the cloud computing concept and its five basic characteristics according to the National Institute of Standards and Technology (NIST). Once the concept is clarified, the chapter reviews cloud computing models. After the models, the chapter summarizes some facts of why cloud computing is a suitable and attractive business model. Then, as a fifth point, the chapter walks through some data center's infrastructure performance indicators. Finally, the chapter comments on challenges forecasted for computer server's development from the power and thermal perspective.

## 1.2. Cloud Computing Definition


Fig. 1.1 Representation of cloud computing concept. A ubiquitous server computer executing data mining, simulation, streaming, storage, etc., ordered by users.

According to NIST [NIST-15], "cloud computing is a model for enabling convenient, on-demand network access to a shared pool of configurable computing resources (*e.g.*, networks, servers, storage, applications, and services) that can be rapidly provisioned and released with minimal management effort or service provider interaction".

In recent years, cloud computing has been adopted as a business model, enabling companies, especially small and medium size ones, ubiquitous access to powerful resources, as illustrated in Fig. 1.1, rather than investing large amounts of their capital building and sustaining datacenter facilities.

From NIST's definition above, how then can we characterize cloud computing in a way that differentiates it from simple "networking?" The following five characteristics are useful in distinguishing cloud computing [NIST-15]:

a) On-demand self-service. A consumer can unilaterally have provision of computing capabilities, such as server time and network storage, as needed without requiring

human interaction with the service provider.

b) Broad network access. Capabilities are available over the network and accessed through standard mechanisms that promote use by different thin or thick client platforms, such as mobile phones, tablets, laptops, and workstations.

c) Resource-pooling. The provider's computing resources are pooled to serve multiple consumers using a multi-tenant model, with different physical and virtual resources dynamically assigned and reassigned according to consumer demand. There is a sense of location independence in that the customer generally has no control or knowledge over the exact location of the provided resources but may be able to specify location at a higher level of abstraction (*e.g.*, country, state, or datacenter). Some examples of such resources include CPU, data storage, memory capacity and network bandwidth.

d) Rapid elasticity. Capabilities can be reconfigured, in some cases automatically, to scale rapidly outward and inward in response to changing demand. To the consumer, the capabilities available for provisioning often appear to be unlimited and can be acquired at any time.

e) Measured service. This characteristic refers to the ability of cloud systems to automatically control and optimize resource utilization through monitoring,

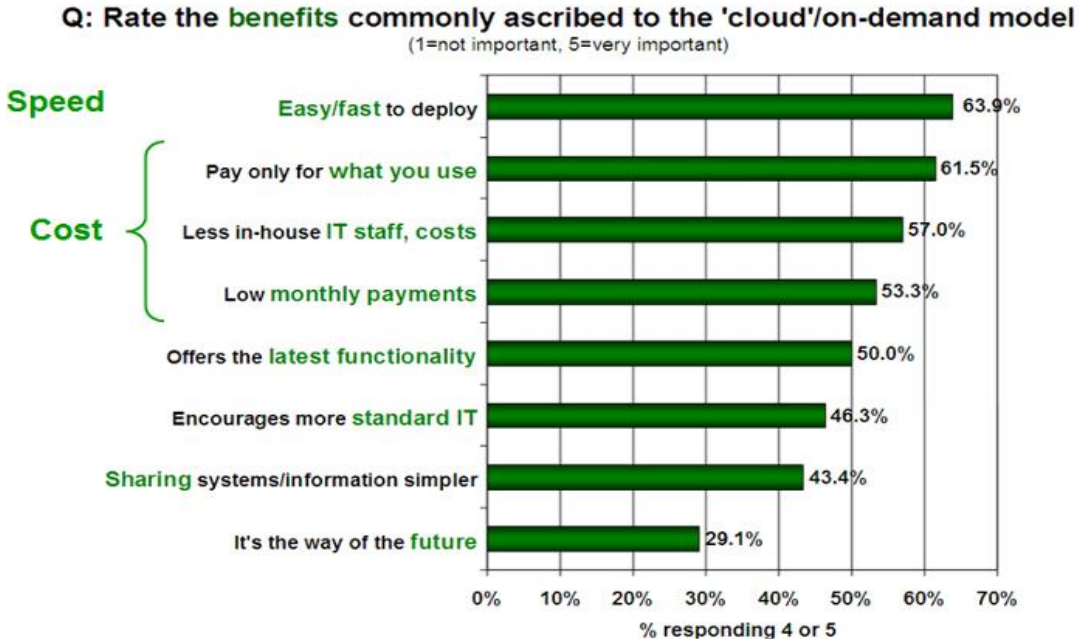


Fig. 1.2 Poll conducted by Oracle [Oracle-15a]. The chart shows that speed and cost are the two primary customer expectations.

measurement and reporting of cloud attributes. For example, storage capacity, processing power, network bandwidth, and number of active user accounts.

## 1.3. Cloud Computing Enablers as a Business Model

This section briefly describes the fundamental enablers and the trends that make cloud computing an interesting business model.

Along the last five years, polls conducted by different companies predict a rapid pace in the adoption of cloud computing models by the next 10 to 15 years. For example, Oracle is one of several pioneer companies and it is interested on a thorough understanding of cloud computing benefits as a model. For such reason, Oracle highlighted that speed and cost are two of the main benefits expected by customers [Oracle-15a]. Fig. 1.2 provides more detailed information in that regard.

Around 2010 and 2011, Intel and Oracle released an interesting forecast with the following

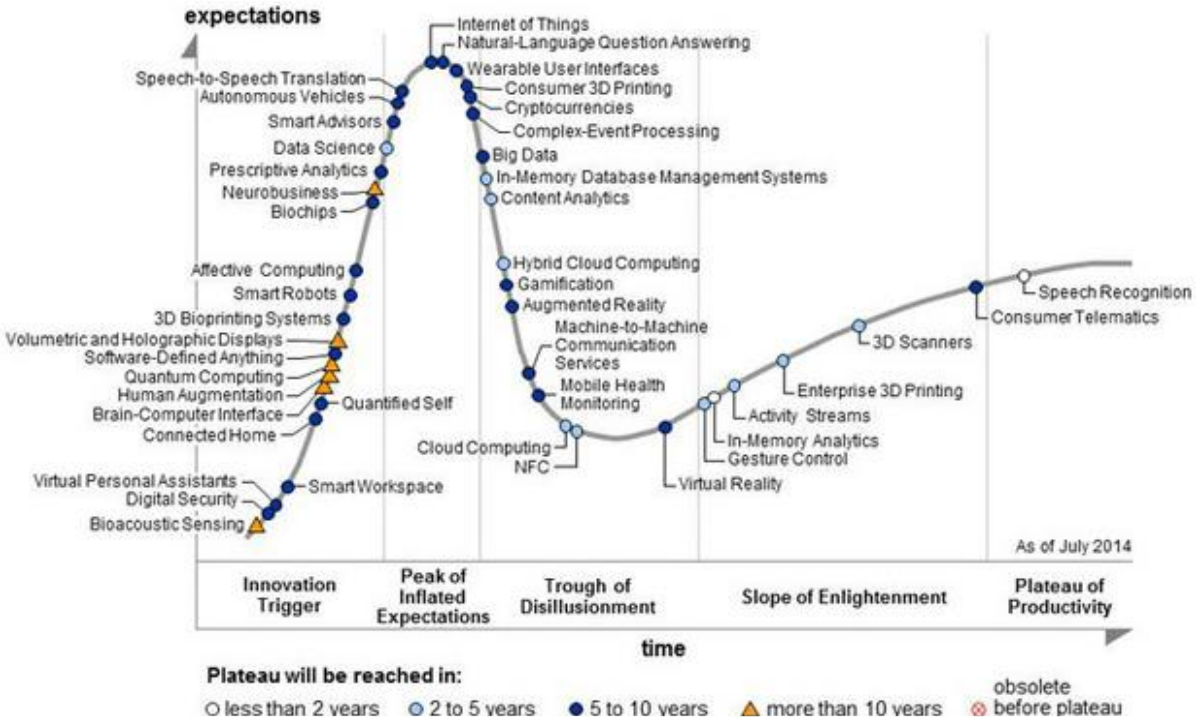


Fig. 1.3 Cloud computing is constantly evolving; three years later, in 2014, cloud computing shows a new hype (figure taken from [Trapp-Tech-15]). The new hype shows big data transitioned from “Innovation Trigger” to “Through of Disillusionment”.

cloud computing trends by the year 2015 [Oracle-15b]. By 2015, the Internet will connect 2.5 billion people and more than 15 billion devices.

1) In the following 10 years, the number of files enterprises deal with will grow by 75 times.
2) Datacenters consume more than 2 % of electricity in the USA.
3) Without dramatic efficiency improvements and the current technology, the equivalent of about 45 new coal plans will be needed to power datacenters by 2015.
4) For every 600 smartphones or 120 tablets, a new server is added.

Computing power will evolve drastically. Hence, big data [Intel-15a], [Gartner-15], [Trapp-Tech-15] and software defined infrastructure (SDI) [Gartner-15], [Trapp-Tech-15], [Kang-13], [Mambretti-14] are pretty much some of the hypes that companies are pursuing now a days, as depicted in Fig. 1.3 and Fig. 1.4.

Why big data and SDI? Big data addresses the critical need for cloud computing to extend beyond early, first-generation big data usage (primarily, search) to efficiently and effectively support big data analytics, including new high-productivity frameworks for advanced machine learning algorithms and for coping with the continuous ingest, integration, and exploitation of live

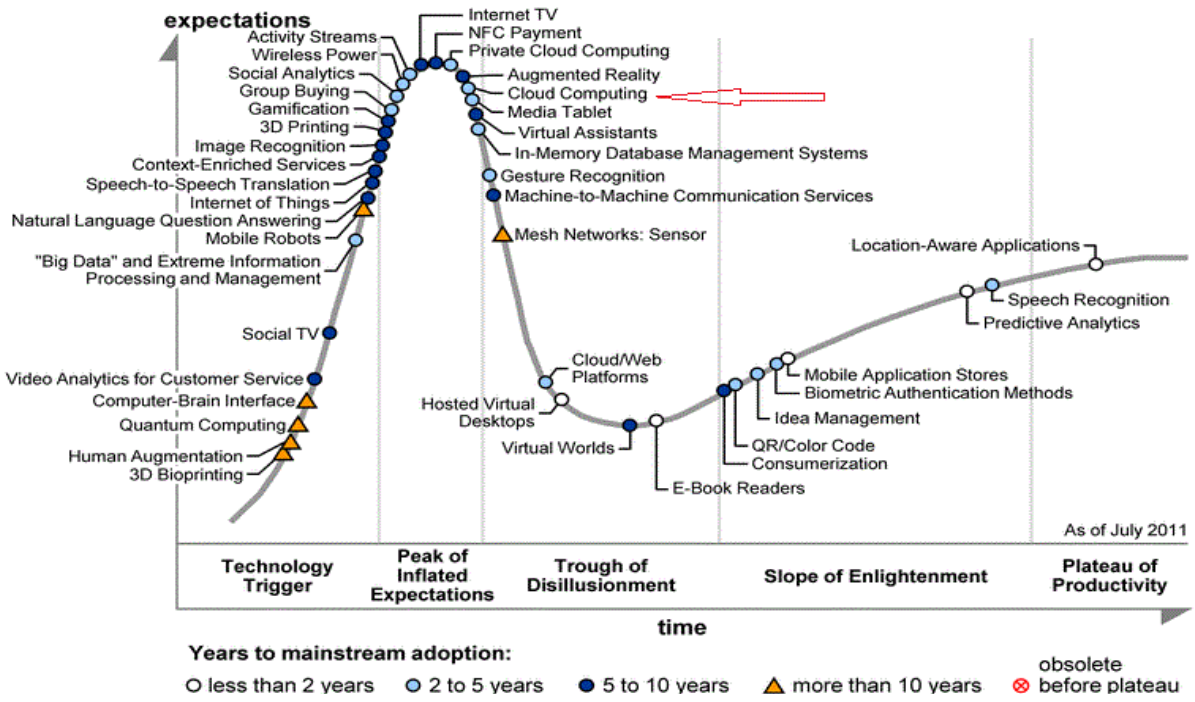


Fig. 1.4 Cloud computing hype from 2011 (figure taken from [Gartner-15]). Big data is seen as a technology trigger and cloud computing is seeing at the peak of inflated expectations.

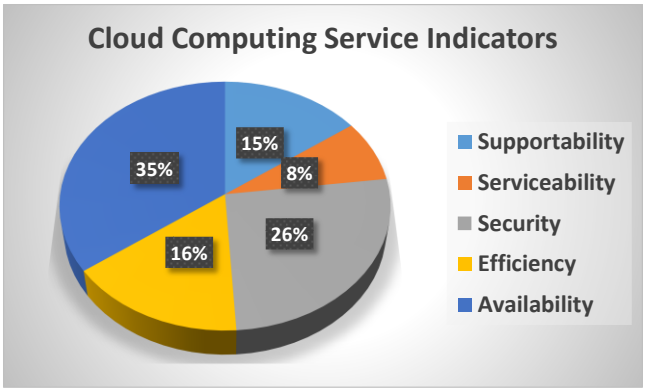


Fig. 1.5 Top five cloud computing service indicators requested by customers. Figure taken from [EMA-15].

data feeds, such as video streams or social networks [Intel-15]. On the other hand, SDI is in charge to monitor that servers are always utilized to their maximum workload, keeping them busy and ensuring uninterrupted service [Kang-13], [Mambretti-14].

Because of all the above, there are plenty of new opportunities to grow on cloud computing space, either as a research and development topic or as a business model.

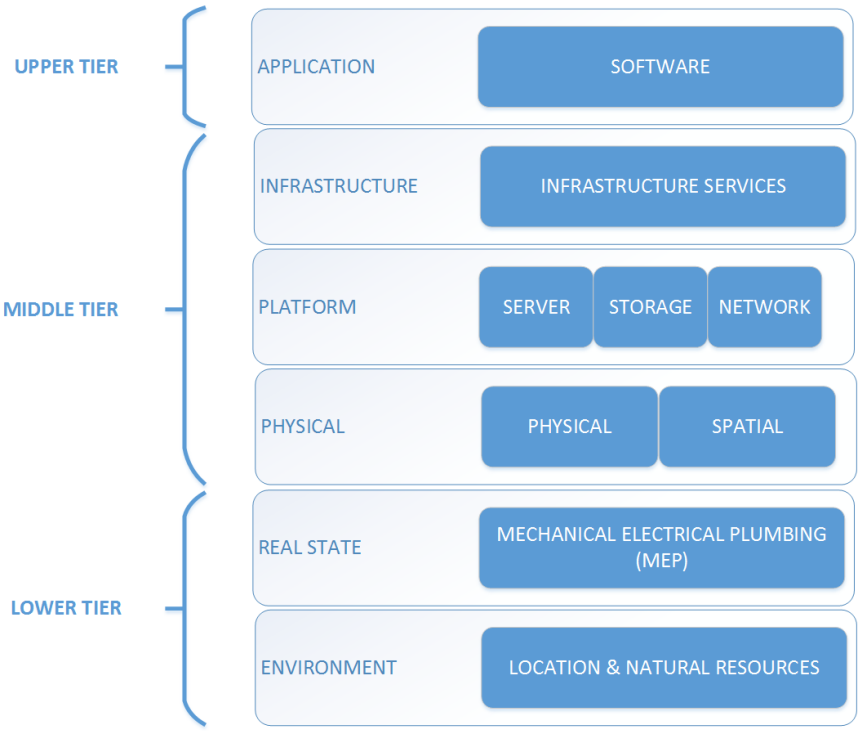


Fig. 1.6 Typical data center's infrastructure. Infrastructure comprehends three tiers from environment up to application. Environment managed by cloud service providers, while platform and application can be managed by customers depending on the cloud deployment usage model. Figure taken from [EMA-15]

## 1.4. Cloud Computing Performance Indicators and Infrastructure

Cloud computing service must fulfill some indicators requested by customers [EMA-15]. These indicators are measured based on cloud service availability, efficiency, security, serviceability, and supportability. As observed in Fig. 1.5, availability, efficiency, and security are highly ranked by customers.

To be able to supply service and comply with customer requests, cloud service providers need to ensure they have a robust data center infrastructure. According to Data Center Pulse (DCP) [EMA-15], the infrastructure of a data center comprehends three tiers; starting with facilities up to software as illustrated in Fig. 1.6. From Fig. 1.6, it is seen that hardware related components correspond to approximately two-thirds of data center's infrastructure. Then, it is easy to imagine hardware related can be one of the most troublesome performance indicators.

In 2010, Enterprise Management Associates, Inc. (EMA), conducted a research analysis to figure out which key performance indicators (KPIs) affected data center operation and management [EMA-15]. The research results (see Fig. 1.7) revealed that hardware/component failures were the most frequent contributing factors to operational performance, followed by vendor/remote related and change related. These top three KPIs were then applied to the DCP stack to view common areas of failures for data center operations and management. As it is revealed in the diagram, physical layer showed the most KPI contributing factors related to data center management performance as illustrated in Fig. 1.8. Combining with the platform and

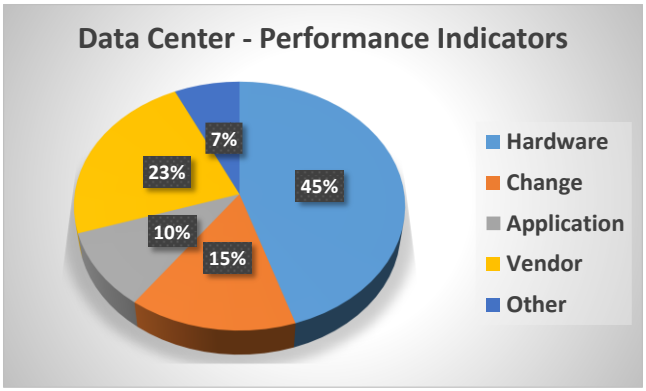


Fig. 1.7 Poll conducted by EMA. Pie chart reveals that one of the biggest performance problems in a data center comes from hardware failures. Figure taken from [EMA-15].

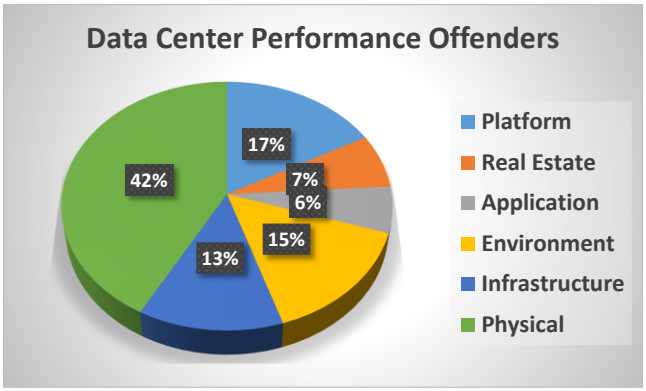


Fig. 1.8 Pie chart combining polls conducted by EMA and DCP reveal that physical tier. Figure taken from [EMA-15].

infrastructure layers, the mid-tier was one of the many contributing factors to data center performance measurement. That is, most of the data center management challenges are caused by complexities in the mid-tier, spanning from spatial, power and cooling, to network, storage and servers, to services and hosting. These areas are where information technology (IT) management needs to look to improve data center management.

## 1.5. Cloud Computing and Its Power and Thermal Challenges

As stated in [EMA-15], mid-tier represents many performance challenges in datacenters. In addition to that, a survey conducted in 2015 by Frost and Sullivan shows that data centers across the globe consume around 100 GWh of power and this consumption is expected to increase 30% by 2016 [Zhang-15a]. This means that several important challenges are coming for both regulatory entities and developers to converge into green energy facilities and reduce carbon footprint.

Cloud service providers and development enterprises are looking into innovative ways to increase efficiency in data centers, as depicted in Fig. 1.9 [Data-Dynamics-15]. From the hardware and SDI development perspective, cloud service providers are requesting optimized power management, thermal, and power consumption solutions to minimize their total cost of ownership (TCO).

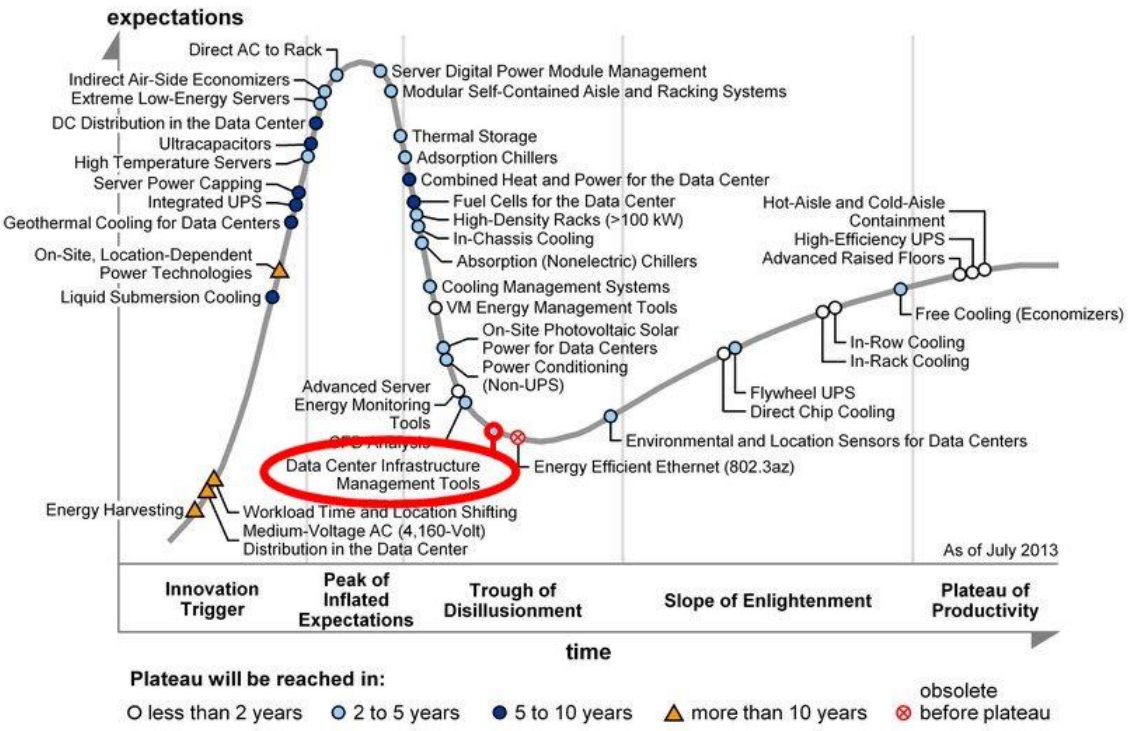


Fig. 1.9 2013's power and thermal hype cycle. Figure taken from [Data-Dynamics-15]. Several fronts are being explored such as high temperature servers and extreme low-energy servers.

### 1.5.1 Power Delivery *vs.* Power Consumption

Power delivery engineers must ensure platforms are energy efficient and dissipate less power. Since a large amount of power dissipation is translated into heat, then, a robust cooling solution must be employed in datacenter facilities to avoid over-heating of the platforms, which means larger facilities, more energy consumption, and a heavy carbon footprint.

To achieve an optimized platform power solution, power delivery engineers need to better understand which components play the major roles. For instance, if power delivery engineers are able to save 1 W per platform, if a company allocates 25,000 servers together in one facility, the company will be saving 25,000 W, which translates into energy savings and a drastic TCO reduction for the company, reducing also its carbon footprint to the environment. Hence, power delivery engineers must look into constructive ways to reduce the amount of voltage regulators employed into platforms [Intel-15b], as illustrated in Fig. 1.10, and maximize their efficiency.

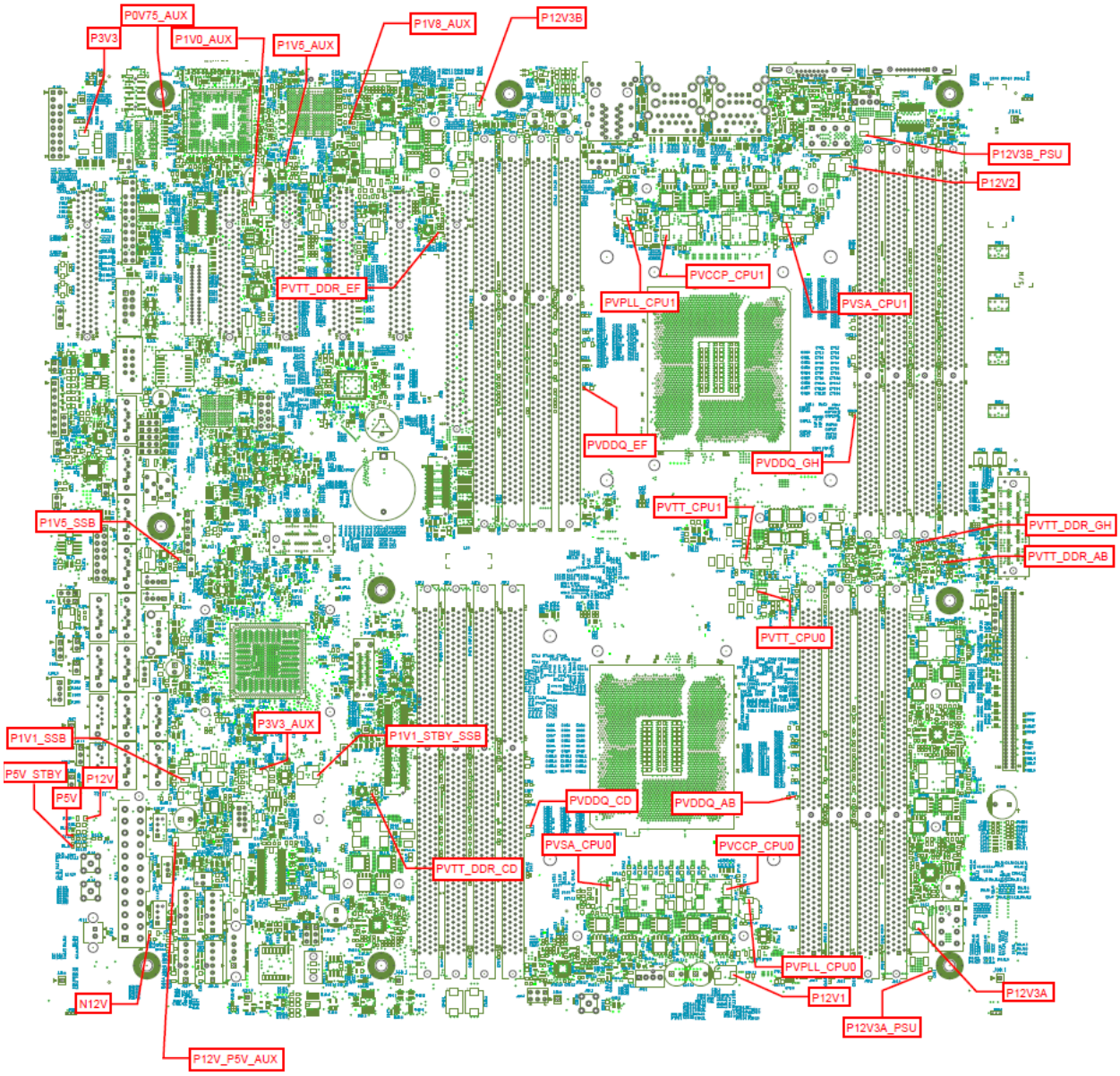


Fig. 1.10 Intel´s Romley platform from 2010, illustrating its power delivery solution [Intel-15b]. Red rectangles indicate different voltage regulators locations. It is seen that a very significant fraction of the total platform space is occupied by a power solution.

### 1.5.2 Cooling *vs.* Real Time Thermal Information

In most traditional internet data centers (IDC's), the operational temperature range continues to be between 18 °C to 23 °C or even lower. Hence temperature has a direct impact on IT's components reliability and performance (see Fig. 1.11). There are three reasons to explain

why conservative cooling settings continue to be used [Zhang-15a].

1) Conservative cooling settings (over cooling) to ensure all IT infrastructure is cooled to within equipment specifications. Because these specifications varied widely between different IT infrastructures, there is the potential to impact the reliability of certain IT equipment with high temperatures.
2) Traditional cooling control mechanisms and policies employed in datacenters are based on a limited number of distributed physical sensors on the ceiling of the cold and hot aisles. These sensor measurements cannot reflect the overall picture of a fluctuating temperature field. The non-uniform temperature distribution at server inlets caused by air flow patterns, recirculation or bypass air between hot and cold aisles, etc. are not picked up from ceiling sensors. Given the limitation of using just a few sensors to determine ambient temperature over the large and varied physical space of a data center, low temperature traditional air cooling is required.
3) Indirect connection between demand (server) and supply (computer room air conditioning - CRAC) in the traditional control policy. Different kinds of servers with different power densities and power distribution always means different cooling requirements (power variation, inlet air temperature, airflow volume). A CRAC unit cannot know and reflect the exact cooling demand directly based on changing server

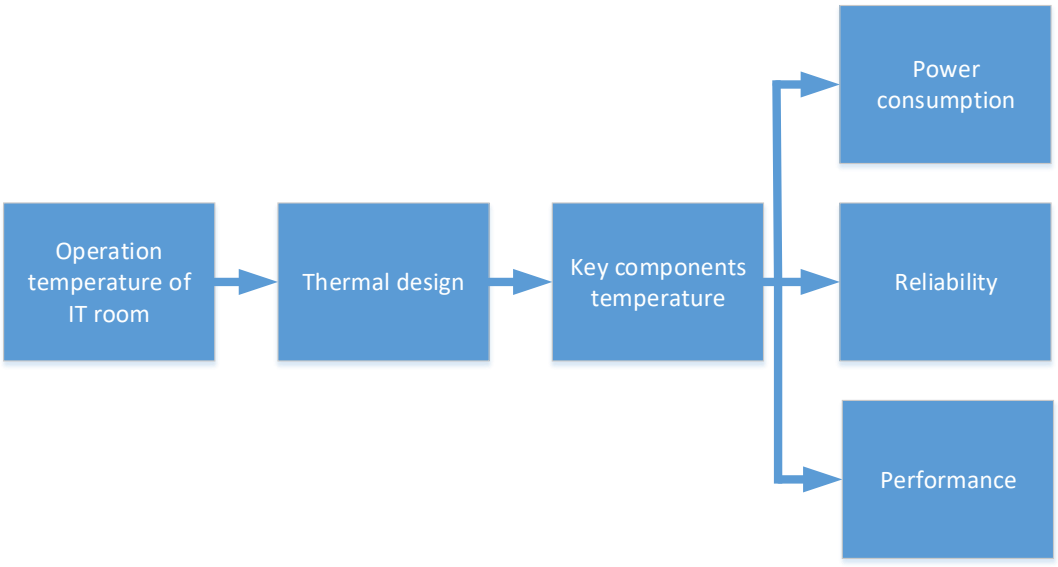


Fig. 1.11 Cooling solution in data centers has a direct impact on components reliability and performance. There is also a direct impact on TCO if power consumption is high. Figure taken from [Zhang-15a].

usage. For example, if a multi-server application workload increases, it causes a large power variation and subsequent increased thermal output. The traditional cooling control mechanism will not respond until the physical ceiling sensor notices the in-room air temperature rises and reports this to the BMS system. This longer response time causes a larger temperature oscillation range, and therefore a conservative operational temperature setting is needed to ensure the thermal safety of the data center equipment. Higher operational temperatures reduce that thermal headroom for equipment as well as reduce allowable temperature variations in an IDC. IDC operators have less response time to deal with any large power/thermal variation or IDC cooling infrastructure in the event of a failure.

One important trend for reducing power consumption is raising the operational temperature of an IDC. Higher ambient temperatures (HTA) have been shown to reduce power consumption based on more efficiently using CRAC units. But just raising the ambient inlet air temperature cannot be done by itself without looking at more effective ways of managing air control and delivery called on-demand cooling (ODC) [Zhang-15a]. For instance, in SDI, it is expected that power and thermal intelligence considers the placement of the specific workload, including workload provision and consolidation. Thus, the cloud software would be able to connect cooling and power facility to achieve better power and cooling management efficiency. Intel's PTAS (power and thermal awareness solution) catches metrics of temperature, airflow, CPU consumption etc. and allows users to run analytics to optimize datacenter management [Song-15], [Zhang-15b].

### 1.5.3 Power Management *vs.* Performance

One of the biggest challenges for data center operators today is the increasing cost of power and cooling as a portion of the total cost of operations. The cost of power and cooling has increased 400 %, and these costs are expected to continue to rise. In some cases, power costs account for 40 to 50 % of the total data center operation budget [Filani-08]. To overcome this constraint, data centers have three choices: expand power and cooling capacity, build new data centers, or employ a power management solution that maximizes the usage of existing capacity. For this reason, the power management approach bears close examination.

A typical data center power distribution hierarchy is designed to deliver a fixed amount of power to the room and then to each rack. The challenge of the data center operator is to determine the number of servers for each rack while ensuring that the overall rack power consumption does not exceed the limit. To do this, the operator must make certain assumptions about the maximum power consumption per server. For most data centers, there are two ways of determining this [Filani-08]:

1) Using server nameplate power value.

2) Using a derated nameplate value.

The server nameplate value, which is marked on the server by the manufacturer, is the maximum possible power value that the server can consume. Actual power consumption is typically much less that the nameplate power. While derating, as opposed to using nameplate value, can improve server density, it is obvious that both methods are not optimal, hence a better approach is needed.

Because the data center operator has no visibility into how much power each server is consuming at any given time, neither does he/she understand the power consumption pattern over time. Without that visibility, the operator or data center management software is unable to decide how much power to allocate to servers/racks based on actual need. A better approach is to allocate power and populate racks using the following steps [Filani-08]:

1) Monitor actual power consumption to understand average and peak power utilization for the server/rack.
2) Dynamically allocate power to groups of servers to maximize power/space utilization while staying within the power constraints determined by the power and cooling capacities.
3) Dynamically reallocate power when necessary to accommodate shifts in power needs of servers. To implement this dynamic power allocation approach, server platforms must address key power management requirements.

Power manager (PM) such as intelligent platform management interface (IPMI) [Intel-15c], is responsible for enforcing power management directives that can be specified for each server. This is done by monitoring the appropriate power and thermal sensors on the servers, and by controlling the appropriate components that allow the PM to control the servers' power consumption as directed.

The PM has three major components operating in a closed loop manner [Filani-08]: monitoring, policy engine, and control.

1) Monitoring module. Monitoring module is responsible for monitoring the sensors to determine if a new set of settings of the effectors needs to be enforced.
2) Policy engine. Policy engine decides a new set of controls based on the deviation of the actual power consumed from the limit and the utilization of various components.
3) Control module. Control module enforces the new settings as determined by the policy engine using mechanisms appropriate for that effect.

When the power consumption exceeds the power limit, the PM will choose a set of settings for various components (processor, memory controller, etc.) that effectively reduce the power consumption of the platform. When power consumption goes below the limit, any restrictive controls previously placed on the processor, memory, and other effectors are relaxed.

The PM can be deployed in various ways [Filani-08]:

1) As a firmware running on a dedicated microcontroller in the server.
2) As part of the baseboard management controller (BMC) that also performs other system management functions in the server.
3) As an agent in conjunction with the operating system.
4) As a combination of the above.

By implementing one of above deployment models, it is possible to save power up to 20 %. Also, there are initiatives to introduce new line of data center uninterruptable power supplies (UPS) that incorporate power management and monitoring technology. As an example, Eaton's 5x series are the first UPS with an embedded intelligent power manager (IPM) application, which is designed to support virtualized environments. IPM integrates with VMware's vCenter and Microsoft's System Center Virtual Machine Manager, and enables administrators to create granular power management policies, which can be used to control the power-up and shutdown of virtual machines to reduce power consumption [TechTarget-15].

### 1.5.4 Node Management *vs.* Efficiency

In combination with an enabled management console and servers, node manager provides the capabilities needed to efficiently and effectively manage power and thermals in a data center

or next-generation private cloud environment. The usage model is as follows [Intel-15d]:

1) Monitor. Track actual temperature and power usage directly from the server.
2) Limit. Control maximum node power to increase rack density and confidence.
3) Survive. Automatically reduce power to extend operations during power or cooling events.
4) Optimize. Use power data and strategic limiting to place workloads for maximum efficiency.

## 1.6. Conclusions

Cloud computing is an emerging model that is becoming rapidly adopted by governmental, industrial, and commercial entities. Big data and software defined infrastructure, among others, are just some of many engines that enable cloud computing as a suitable business model. Cloud computing forecasts several challenges for hardware and software developers as well as for regulatory entities. On the software side, developers must ensure enough security on the usage of the information as well as intelligent algorithms that maximize workloads of datacenters. On the other hand, regulatory entities must agree on the definition of the rules for the usage of cloud computing (NIST) and power consumption guidelines (American Society of Heating, Refrigerating, and Air-conditioning Engineers - ASHRAE). While for hardware developers, especially on the power and thermal side, customers are requesting optimized power delivery solutions to reduce their costs and guarantee uninterrupted service. There are plenty of new opportunities to enhance power and thermal analysis, enabling engineers to look into more reliable materials that handle higher junction temperatures, optimization methods to appropriately situate sensors, identifying critical variables that influence the most VR module design, and many more rules to enhance power management policies.

# 2. Power Delivery and Power Conversion Fundamentals

Technology is continuously evolving. One example of that is reflected by Moore's law [Moore-06], that estimates the time in which there will be a transition between one transistor technology size to another smaller one that enables more features to the end users, including higher data transmission rates, but at the same time usually dissipates more energy. From the last statement, the field of signal integrity (SI) plays a notable role, because it is critical to guarantee a reliable transmission of the data from point to point for high speed buses. One should ask, what happens to the buffer that transmits the data? How can we ensure the transistors will never fail for a certain operation, such as a wake up or sleep event? To answer those questions, it is important to put some attention on how the energy is being delivered to the buffer in order to turn it off or on, depending on the operation that needs to be performed.

Ensuring that power is well delivered in appropriate manner to the buffers requires a thorough study of the system [Yuan-11], [Swaminathan-04]. "Power Delivery", also referred as "Power Integrity" (PI), is a discipline in charge of understanding all the non-idealities of the channels that deliver the power to the buffers, and providing design recommendations to overcome any sudden change to the voltage due to transitions of loads under different conditions; for example a load-release, wake up, or sleep event when talking about input-output interfaces (I/O). This chapter briefly describes the main concepts related to power delivery design, the interactions that power delivery has across many different design teams, the elements that compose a power delivery network (PDN), and finally, it covers the main design guideline methods to deliver an optimum design recommendation that ensures a safe operation of the chip and low cost. These concepts are mainly based on the author's point of view from his industrial experience.

## 2.1. Power Delivery Basic Concepts

Power delivery is an engineering discipline that studies the channel and its non-idealities to deliver power from the supply, *i.e.* voltage regulator (VR), to the sources, *e.g.*, buffers on the

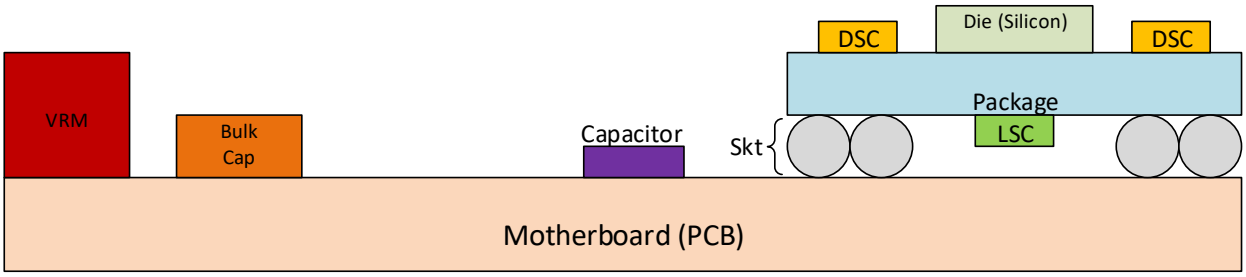


Fig. 2.1 Example of a server platform. Cross section shows each stage, from voltage regulator module (VRM) to die, including decoupling capacitors.

die, to maintain the voltage at a certain level, especially when there are events such as hibernation, turbo, wake up or sleep scenarios, that can potentially damage the transistors and increase power losses.

As stated earlier, PD oversees looking for an optimum design of the channel that delivers the power to meet performance of the chip. This is done by looking into several design aspects: cost, decoupling stages, voltage regulator module (VRM), chip requirements, package rules, PCB design guidelines, electromagnetic interference (EMI), etc. All these aspects contribute in some manner to the behavior of the PDN. One example of a PDN is illustrated in Fig. 2.1 for an Intel server product.

As observed in Fig. 2.1, the channel that delivers power is not a perfect transmission line. Along the way from the VRM to the die, there are many transitions in the corresponding characteristic impedance. Among other effects, all these transitions produce changes to the voltage, causing a degradation of the voltage supply mainly due to the inductance inherent to these stages and the abrupt change in the current ($V = L\ di/dt$).

Some of the main ingredients that comprehend a PDN [Swaminathan-04], [Swaminathan-07] include decoupling capacitors allocated over different areas, printed circuit board, package, die, VR, socket, among others. These elements are briefly described next.

### 2.1.1 Die/Chip

It is a piece of silicon that contains the logic circuits, equalization stages, phase locked loops (PLLs), etc., in charge of the operation of a chip which demands voltage. Typically, all current transitions on the die occur in less than tens of nanoseconds. These transitions are load changes. In the PDN terminology, a change on the load is called a *di/dt* event.

### 2.1.2 Capacitors

Capacitors are the main decoupling stages that react at different time slots to supply voltage to the source while the VR reacts to settle the voltage when occurs a change in the load. In the server platforms arena, capacitors can be classified as follows.

Capacitance on die. Capacitance on die ($C_{die}$) is the first decoupling stage that reacts in tens of nanoseconds when a *di/dt* event occurs. $C_{die}$ is the capacitance at silicon level and it is categorized into two different types: intrinsic and extrinsic. Intrinsic capacitance is related to the inherent capacitance given by the transistors, *e.g.*, gate-source capacitance. On the other hand, extrinsic capacitance is given on a certain area of the silicon with different via arrangements among the chip's metal layers on top of the transistors; they are provided on purpose to mitigate the *di/dt* change. These capacitors are usually in the range of femto-farads to hundreds of nano-farads.

Die side caps. Die side caps (DSC) are the capacitors outside the chip but still close enough to it, allocated on the surface of a package. These caps react also in tens to hundreds of nanoseconds and are in the range of micro-farads.

Land side caps. Land side caps (LSC) are located under the cavity of the package but still close to the die. These capacitors usually react in hundreds of nanoseconds and typically go from micro-farads to tens of micro-farads.

Printed circuit board (PCB) decoupling caps. These capacitors are usually allocated underneath the package cavity or even outside the package keep out zone. Usually, these caps are in tens to hundreds of micro-farads and react in hundreds of nanoseconds to single digits of micro-seconds.

Bulk capacitors. These capacitors are the biggest ones that belong to the PDN. These capacitors are allocated near to the VR and they represent the largest contribution of capacitance. Usually these capacitors go from hundreds of micro-farads to thousands of microfarads in some cases, and the average time they react is in microseconds to tens of microseconds.

### 2.1.3 Printed Circuit Board

Printed Circuit Board (PCB) is the element where most components are placed, such as latches, VRMs, chip, package, etc. It is made of metallic and dielectric layers. PCB contributes

with the majority of the PDN impedance, mainly inductance and resistance, and usually most of its contribution is seen in the range of Hz up to 1MHz. For relatively low frequency applications, PCBs are typically made of copper and FR4 dielectrics to keep their cost low.

### 2.1.4 Socket

The socket is mainly used for inventory and control of the platform. For Intel's server design, the socket is an electrical pins connection that makes possible to set the package on top of the PCB, usually a motherboard. It is very resistive and inductive, depending on the type of technology that is chosen. Some of the existing sockets are ball grid array (BGA), land grid array (LGA), organic land grid array (OLGA), etc.

### 2.1.5 Package

A package is like a PCB, but much smaller and denser. It also uses FR4 as dielectric, however, it uses different technology such as stacked via laminated core (SVLC) or core technology. The package is one of the main components that makes possible to convert the small ball grid arrangement at chip level to a larger ball grid arrangement at board level. Typically, it is one of the main stages where power delivery engineers spend most of their time to add decoupling stages to isolate as much as possible any coupling problem from one power rail to another, or from power rails to signal rails.

### 2.1.6 VRM

Voltage regulator module is the component in charge of providing voltage to the chip. They are based on many types of DC-DC converters, such as linear, step-down, step-up, etc.

## 2.2. Power Delivery Methodology

In order to meet performance and cost targets, power delivery engineers need to understand how the PDN behaves [Yuan-11], [Swaminathan-04], [Swaminathan-07]. For that reason, power

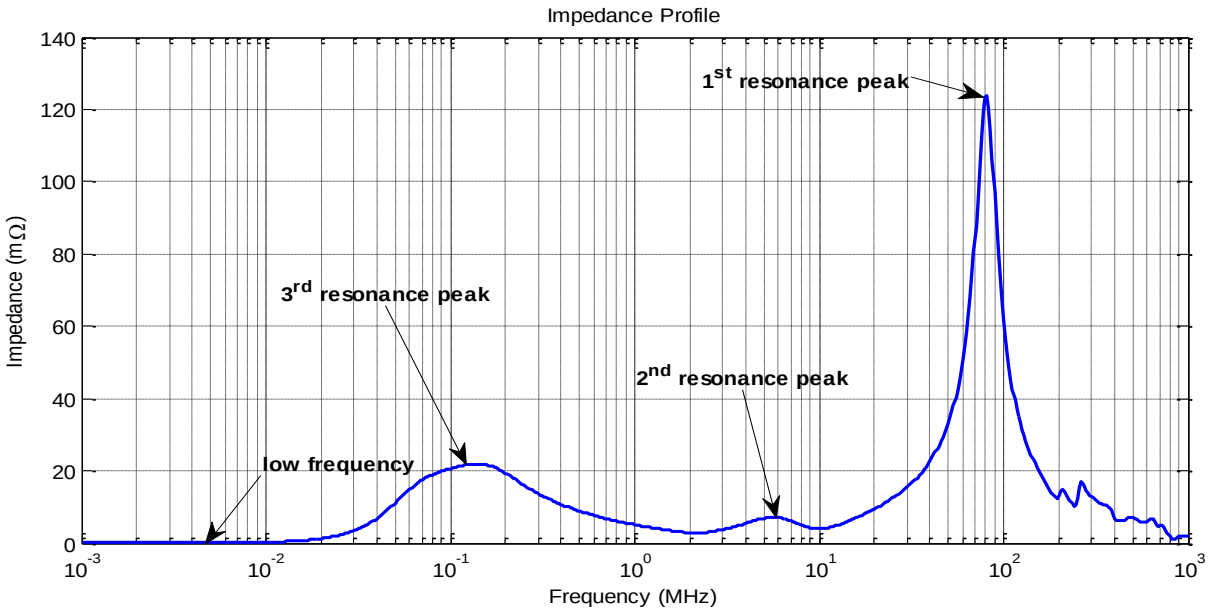


Fig. 2.2 Frequency domain analysis plot to understand the behavior of a PDN; also known as impedance profile. This plot illustrates different impedance levels along the frequency.

delivery engineers focus their attention primarily on the understanding of two main perspectives: impedance profile in different frequency ranges (frequency domain analysis), and time domain analysis [Pandit-10].

### 2.2.1 Frequency Domain Analysis

Frequency domain analysis of PDN is typically realized by the so called "Impedance Profile" technique. Fig. 2.2 illustrates a typical impedance profile plot, where a set of resonance (valleys) and anti-resonance (peaks) curves that describe the behavior of the PDN along a range of frequencies are shown. It is desired that the impedance profile keeps a flat behavior along the frequency ranges and a reasonably low impedance level.

From Fig. 2.2, it can be observed that the impedance profile is typically not flat. In that example there are three peaks that need careful attention. The impedance profile is usually read from right to left, so the first peak occurring typically at around 50-100 MHz identifies the interaction between the die, typically the $C_{die}$, and $R_{die}$ seen at the load and the inductance of the package.

The second peak, typically at around 1-50 MHz, corresponds to the interaction between the

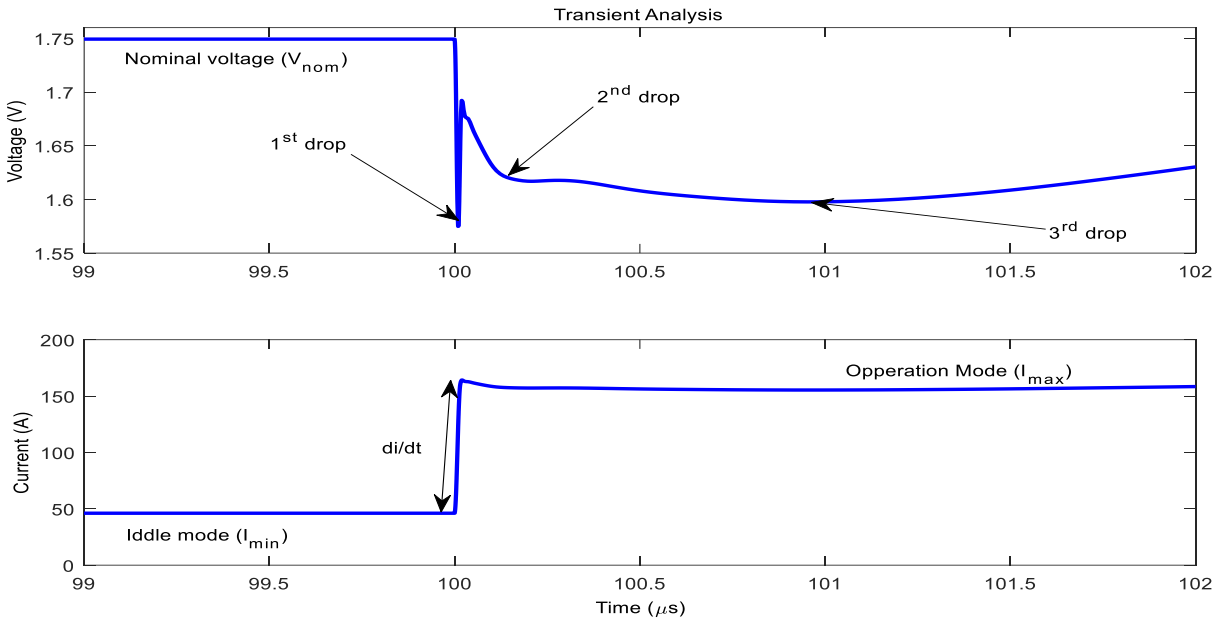


Fig. 2.3 Transient domain analysis plot depicting a voltage drop variation when there is a transition in the load from an idle stage to an operational stage.

LSC and the socket. The third peak (at around 100 kHz) is given by the inductance of the board and the bulk capacitors. Finally, the flat line at lower frequencies is practically considered DC and is the total resistance added from the PDN.

### 2.2.2 Time Domain Analysis

Time domain analysis is another key technique that enables engineers to understand how difficult it is to meet the minimum voltage target ($V_{min}$). This analysis is based on a set of *di/dt* events, wake up or sleep, or resonance scenarios provided by silicon teams. As an example, Fig. 2.3 depicts transient domain curves.

Similarly to the frequency domain analysis, the corresponding transient domain analysis also identifies three valleys; these valleys translate the peaks observed in the impedance profile plot to voltage drops. For example, the first drop is related to the first impedance peak at the most left-hand side and it is given in tens of nanoseconds. The second drop is related to the second impedance peak and is in the range of hundreds of nanoseconds, and third drop is given by the PCB and it is where the VR starts to react to settle the voltage due to the change in the load. First and second drops are primarily dominated by all the decoupling stages that contribute to avoid a

dramatic voltage drop, so during this time these droops are called AC droops. Once the VR starts to react to the voltage variation the drop becomes a DC drop.

## 2.3. Power Supply Noise Concept

To understand why PD engineers need to employ standard PD design methods, it is needed to comprehend from a high-level perspective what power supply noise is. Basically, power supply noise (PSN) can be seen as the undesired set of random signals (*e.g.* ripple that is transmitted from the supply VRM to the chip) causing potential violation of time margins (jitter), not meeting minimum voltage ($V_{min}$) or maximum voltage ($V_{max}$) at transistors level, later on translated as performance hit [Wong-06]. Since the nominal voltage is getting more and more reduced with every new transistors technology combined with load increments (*i.e.* large current variation in a short period of time, *di/dt*), it becomes more important to reduce as much as possible the noise induced from the voltage regulator onto the chip to guarantee suitable performance under any condition (*e.g.* power management stage, logic operation, etc.).

## 2.4. Target Impedance Method

Target impedance method was introduced at the end of the 90's by Smith et al. [Smith-99]. Basically, this method consists of looking for a desired target impedance that satisfies power supply impedance requirements across the whole frequency range based on a simple Ohm's law,

$$Z_{\text{target}} = \frac{V_s r}{I} \tag{2-1}$$

where $V_s$ is the voltage supply in volts, $r$ is the allowed relative ripple (usually in percentage), and $I$ is the current.

Since the VRM is far away from the chip, the current must travel across a large section of copper traces and discontinuities (vias, etc.), to reach the die under any loading condition. Because of this fact, it becomes imperative for PD engineers to add decoupling stages as close as possible to the die (see Fig. 2.1), in order to supply energy while the voltage regulator (VR) reacts by keeping the impedance profile as low as possible across the frequency range of interest. Adding several decoupling stages to the PDN implies that the impedance profile will not be flat along the

whole frequency range; and the PDN will see different voltage drops in the time domain as shown in Fig. 2.3.

### 2.4.1 Techniques to Extract PDN

PDN comprehends several elements such as bulk capacitors, PCB, package, decoupling capacitors, socket, etc. In order to build the impedance profile that best predicts the target impedance requirements, PD engineers build complex distributed models employing different circuital parameter extraction techniques.

One approach consists of separating the different components like package and board by decomposing each of them into several pieces [Auernheimer-04], as illustrated in Fig. 2.4, employing the partial-element equivalent circuits technique (PEEC) [Archambeault-01] that obtains the resistance, inductance, and the magnetic coupling factors (*K*). Once these parameters for package and PCB are obtained, it is possible to incorporate the socket, the die, and the decoupling stages to build a very large SPICE netlist. Even though this approach is very accurate

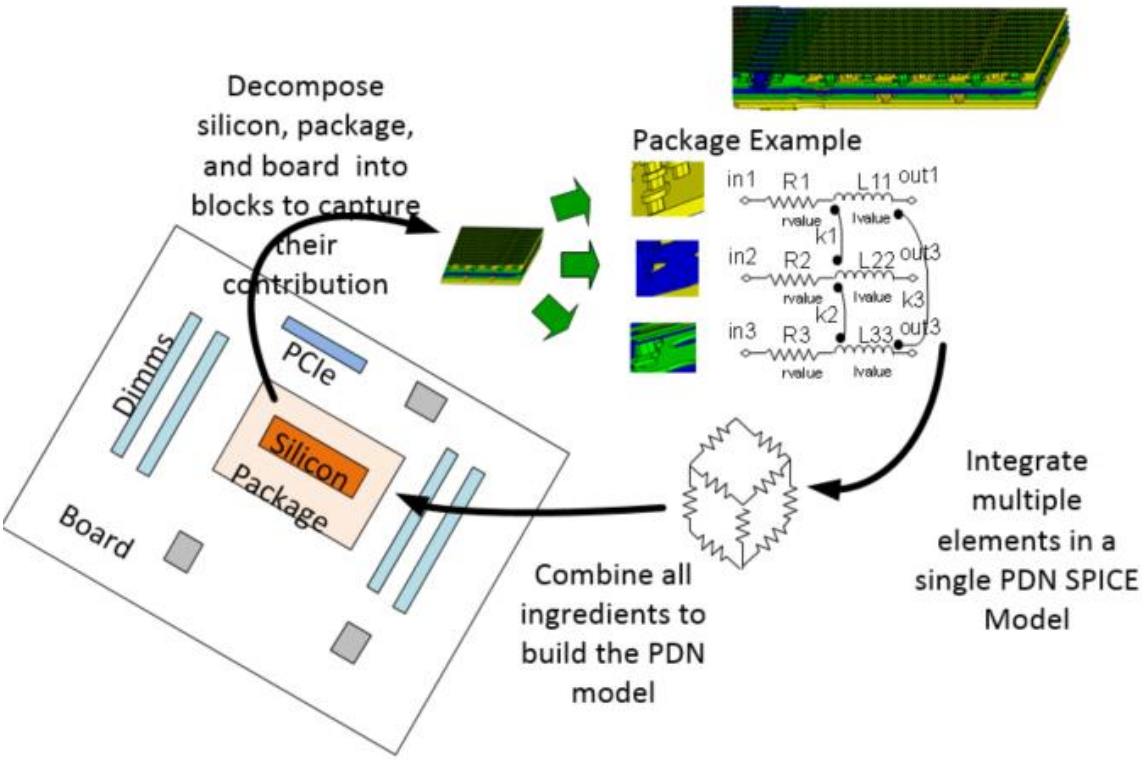


Fig. 2.4 PDN modeled by separating package and board to get parasitics *R*, *L* and coupled inductors (*K*) by employing PEEC technique to build a SPICE netlist.

for building PDN models, getting a too large netlist can be very time consuming and user prone error. More recent techniques take advantage of electromagnetic field simulators to enhance the PDN's extraction process.

### 2.4.2 Simulating Target Impedance

Once the PDN's SPICE netlist is set up and ready for simulation, PD engineers start looking into two main scenarios.

The first scenario consists of running an AC simulation sweep along a wide frequency range to verify the impedance profile is under desired target impedance expectations. As observed in Fig. 2.2, the impedance profile is not flat along the frequency range, and this is basically because of the interconnect structure and the decoupling stages added to the PDN. In order to further reduce the peaks observed at different frequencies, PD engineers can employ capacitor optimization, as in [Siming-13], to minimize as much as possible the parasitic effects inherent to the capacitors and their loop inductance, or even by adding more copper to the power rails.

Since impedance profile is not the only way to verify if PDN complies with target impedance specifications, PD engineers also have to look into time domain simulations, as depicted in Fig. 2.1, to check $V_{min}$ and $V_{max}$ specifications are not violated. These types of time domain simulations are usually represented by either current step or a switching current to quantify the peak to peak noise (see Fig. 2.5a and Fig. 2.5b).

## 2.5. Jitter Reduction Method

Since target impedance was adopted by many PD engineers, there have been multiple efforts to optimize the PDN by means of optimizing location and quantity of capacitors, to reduce the loop inductance associated, as well as to reduce cost, by looking into reduction of the target impedance [Fizesan-10], [Swaminathan-04] to be able to predict the behavior of PDNs at simulation level and achieve an impedance profile as flat as possible.

But what is the real impact to the chip when designing based on target impedance method? In the early 2000's, Rahal-Arabi *et al*. [Rahal-Arabi-02] found that when removing extrinsic $C_{die}$

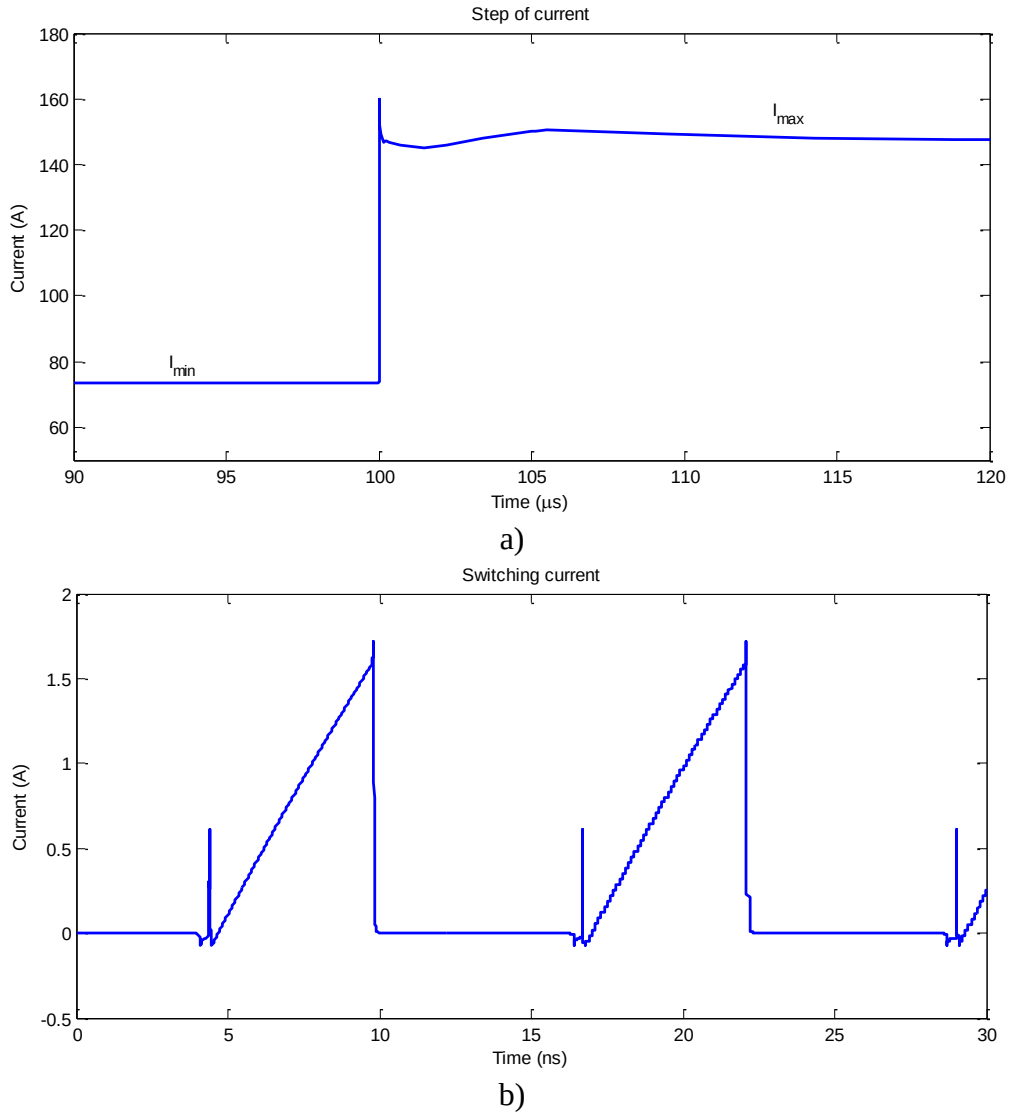


Fig. 2.5 Time domain analysis. Different loading conditions to excite the PDN: a) current step, and b) switching current.

from the chip the impact to the performance was almost negligible, although it was not possible to find a clear explanation to such phenomena. This problem without clear answer was the trigger for many authors [Yuan-11], [Wong-06], [Kantorovich-08], [Swaminathan-10] to focus their attention to understanding exactly the source of such phenomena. Later, jitter was discovered to be the major contributor that explained the small impact on performance observed in [Rahal-Arabi-02].

From signal integrity point of view, jitter is understood difference between two consecutive periods within *n* cycles [Yuan-11]. This set of signals are evaluated on the time domain and later are overlapped in a defined time window. Such overlap of the curves is seen as an eye on the oscilloscope. And this eye must be as open as possible, indicating that the signal is well transmitted

and is well understood by the buffer at the next stage. If the eye is almost closed, this means the signal is having problems to meet time margins or even to meet a desired amplitude, and this needs to be fixed.

Something similar occurs on the PD field. Since the chip has many power stages, the voltage regulator (VR) reacts to those stimuli coming from the chip. This process takes up to some microseconds to settle the VR voltage, because PDN is not uniform and the voltage tends to drop. That is why the PDN has multiple decoupling stages to avoid voltage drop as much as possible while the VR settles its voltage [Siming-13], without too much voltage fluctuation at the buffers of the chip.

This is why jitter prediction has started to dominate most of the design efforts to lower the power supply noise induced jitter (PSNIJ) to the chip in order to lower costs by a reasonable reduction of capacitance needed, which has been confirmed in the laboratory when target impedance is employed as the primary methodology to design a PDN.

### 2.5.1 Jitter Calculation

Jitter-based methodology goes beyond target impedance. Basically, this methodology consists of jitter margin calculation to optimize decoupling capacitance, while maximum performance is obtained by ensuring a good functionality of the clock. The method includes the estimation of discrete jitter noise [Kantorovich-08], [Swaminathan-10] coming from power supply noise, including other aspects like random jitter given by variation in the process, etc.

This methodology has been broadly studied across IO design because of the interaction with other devices [Yuan-11], while core jitter noise [Razmadze-13] is difficult to measure because all the logic is inside the CPU and is difficult to route external probe points.

### 2.5.2 Sources of Noise Induced Jitter

There are three possible root causes for jitter:

a) Power and return path design. Power and ground are treated as a non-uniform transmission lines that are subject to signal degradation, causing crosstalk and jitter noise. This makes necessary a careful design of power and return path transmission

lines [Laddha-08].

b) Crystal oscillator. One source of high jitter contributions is usually coming from the crystal oscillator, hence, a careful and a thorough design of the transmission line from the crystal to the die is needed.

c) Chip design. It consists of measuring the jitter on the clock [Wong-06], [Kantorovich-08], [Swaminathan-10], [Razmadze-13] in order to guarantee a proper functionality of the circuitry avoiding the usage of a large decoupling capacitance inside (extrinsic $C_{die}$) as well as PLL optimization.

## 2.6. Power Distribution System

Today's devices require different power delivery solutions. Power delivery networks comprehend also VR solutions (see Fig. 2.6). As an example, mobile devices (*e.g.* phones and tablets) focus on reduced cost and portability versus performance, contrary to what server computers attempt to achieve. Then, is possible to differentiate between two types of power distribution schemes [Dibene-14].

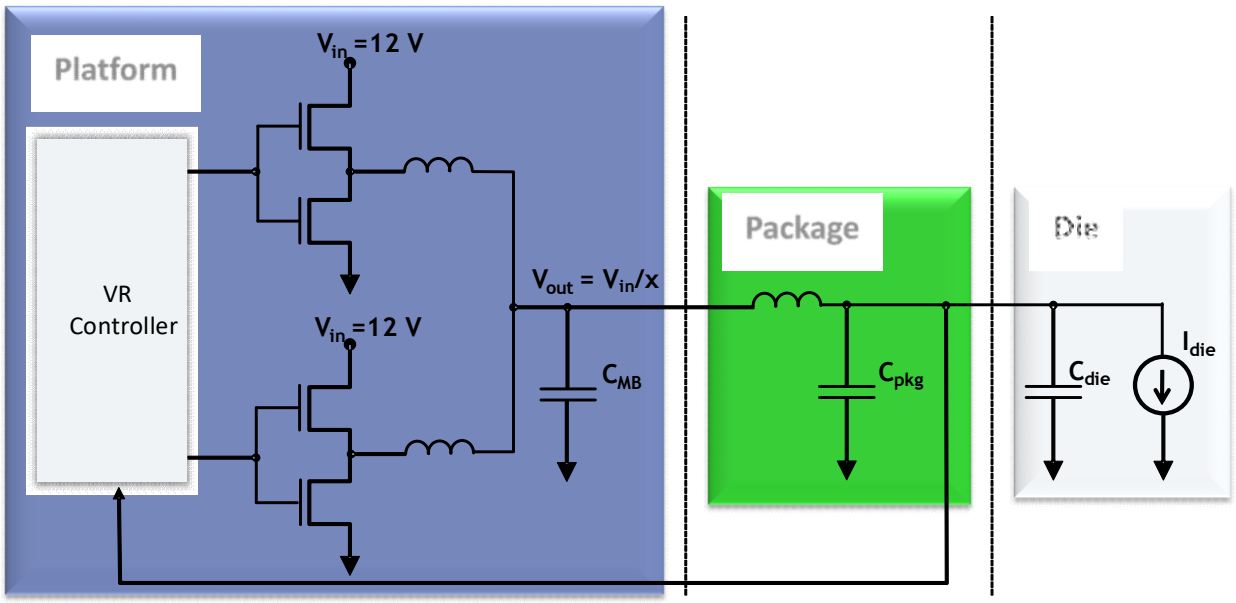


Fig. 2.6 Power delivery network emphasizing the voltage regulator (VR) module that supplies voltage to the die.

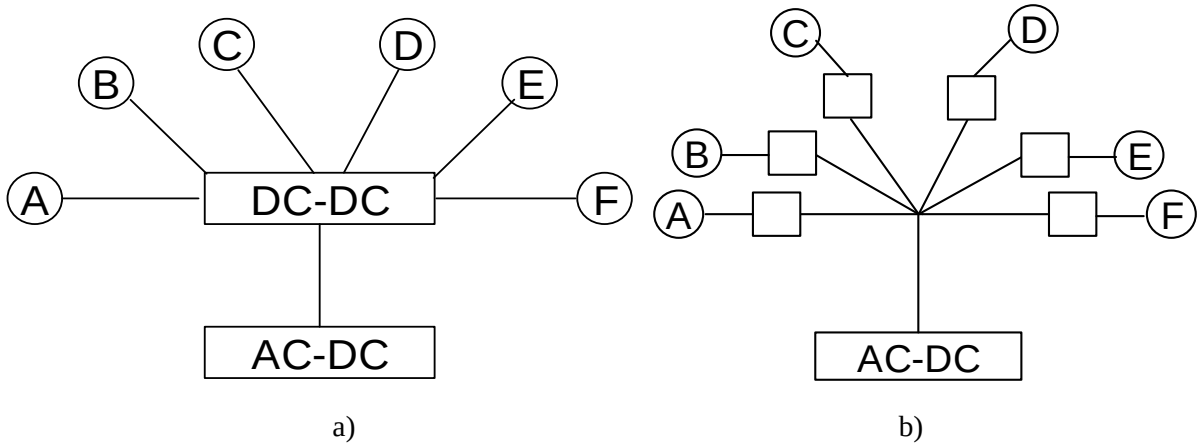


Fig. 2.7 Power distribution configurations: a) centralized mode suitable for mobile devices; b) distributed mode. Commonly used in systems where high performance is needed, like computer servers.

### 2.6.1 Centralized Power Distribution System

This type of scheme is preferred by mobile applications where power rail performance is typically less stringent. The architecture is usually concentrated in a specific location and the distance to components is short (see Fig. 2.7a). There can be few converters or a single device such as a power management integrated circuit (PMIC).

### 2.6.2 Distributed Power Distribution System

Systems demanded by high performance (*i.e.* speed, current amplitude, low ripple, etc.), require power conversion solutions to be spread throughout the board (see Fig. 2.7b). This type of application usually fits into computer servers where converters are placed in proximity to the loads. These converters often operate independently, with independent controllers.

## 2.7. Converters and their Topologies

Power conversion is a wide and spread area. There are linear voltage regulators, switching voltage regulators (AC-AC, AC-DC, DC-DC, and DC-AC), and many others [Cipriano-Dos-

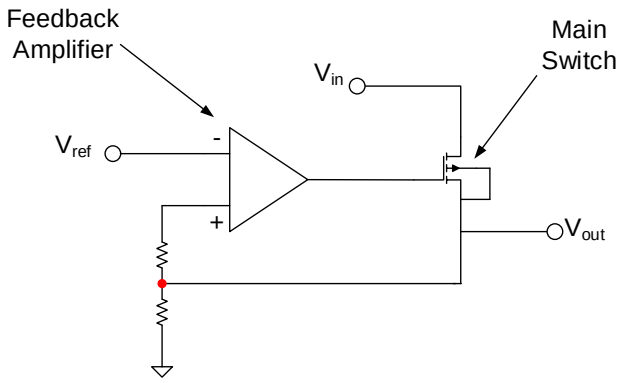


Fig. 2.8 Example of a linear voltage regulator topology, also known as LDO. It is noticed that the feedback control loop is simple.

Santos-15]. Each regulator defines its own topology and its own treatment; however, it is not within the scope of this work to study all of them. This chapter makes a brief overview of the most common regulators implemented in server computers.

### 2.7.1 Linear Voltage Regulator

Linear voltage regulators [Linear-Technology-13] are known also as low dropout regulators (LDOs). A simple example of an LDO is illustrated in Fig. 2.8.

Some features that make LDOs ideal for some server's applications are:

1) Provide step-down DC/DC conversion without the need of an external power inductor.
2) Offer simple and low-cost solutions, especially for low power applications with low current, where thermal stress is not critical.
3) Suitable for low noise and low ripple applications. The absence of switching elements yields small EMI problems and very high bandwidth.
4) Fast transient applications. These VRs have fast transient response, since their feedback is usually internal.
5) Low dropout, because output voltage is close to the input voltage.
6) Uniform efficiency along a wide load range. Absence of switches without need of external components, such as inductors, make power loss almost negligible.

On the other hand, LDOs can burn a lot of power if the difference between input voltage and output voltage is large. Because of a large voltage difference, efficiency gets reduced, as predicted by

$$\eta_{LR} = \frac{V_o}{V_{in}} \tag{2-2}$$

where $\eta_{LR}$ is the linear regulator's efficiency, $V_o$ is a desired DC output voltage, and $V_{in}$ is the input voltage from the AC-DC converter.

### 2.7.2 Switching Voltage Regulator

Opposed to LDOs, switching VRs tolerate a larger voltage difference between input and output voltages. However, their efficiency is not uniform among wide load ranges. Switching VRs have a wide range of topologies, being the main VR topologies: buck or step-down converter, boost or step-up converter, and buck-boost or inverting type converter.

Buck-boost is widely employed for silver box[1] in servers, while buck regulator is frequently implemented to supply different voltage DC levels for DDR, PCIe, QPI, UPI, Core, etc.

## 2.8. Basic Design Guidelines of Buck Regulators

Buck regulator is one of the most widely used application preferred by power conversion engineers for server computers. Their main figures of merit are shown in Table 2.1.

TABLE 2.1. SWITCHING BUCK REGULATOR FIGURES OF MERIT [DIBENE-14]

| Metric | Relative Comparison |
|---|---|
| efficiency | usually above 90 % |
| size | average, depending on application |
| ripple | good, depending on application (*e.g.* multi-phase and frequency of operation) |
| response time | good, particularly for multi-phase |
| ease of use | excellent (large base of suppliers for components) |
| cost | excellent (large base of suppliers for components) |
| system integration into platform | excellent (large base of suppliers for components) |

[1] Silver box is a typical terminology employed by designers in the power conversion field, it refers to desktop or server computer power supply

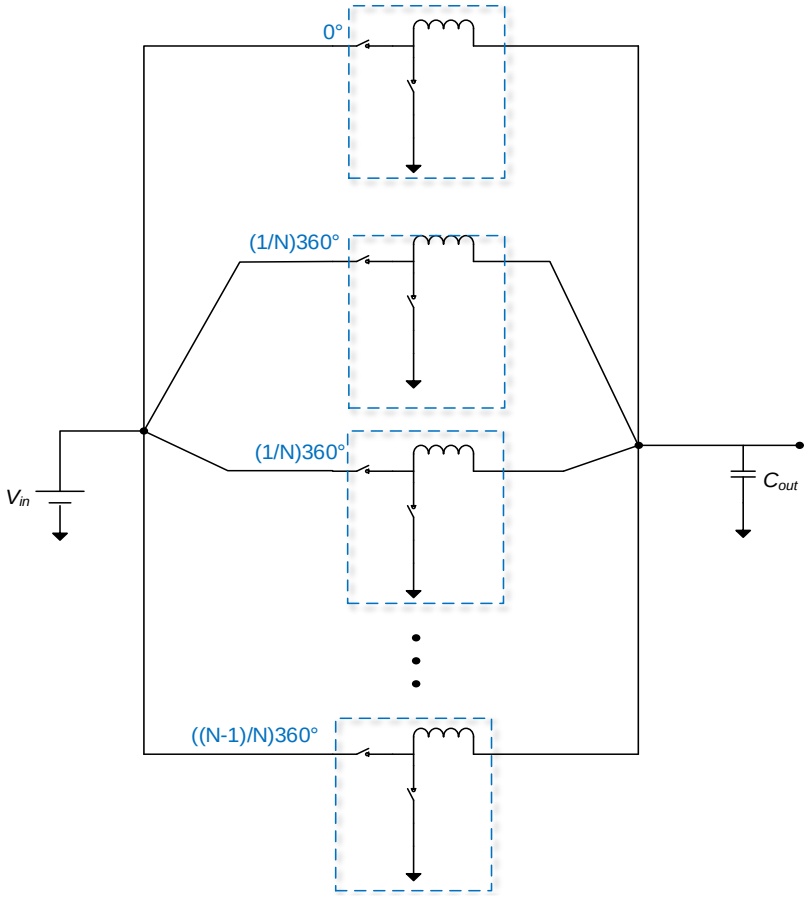


Fig. 2.9 Example of multiphase buck regulator. It is possible to reduce ripple noise by adjusting the voltage phase of the output inductors.

As mentioned in previous section, the buck regulator belongs to switching converters category and it tolerates larger voltage differences.

One important advantage of buck regulators is the flexibility to incorporate multiple phases [Peng-02] (see Fig. 2.9), where several inductors can be put in parallel and out of phase to significantly reduce output ripple and improve VR's efficiency. On the other hand, and compared to LDOs, buck's topology is more complex, and it requires external components, such as output inductors and their feedback control loop.

The feedback control loop can be implemented using several techniques, including pulse width modulation (PWM) [Freescale-14], pulse frequency modulation (PFM) [Freescale-14], and resonant circuitry [Yang-03]. A representation of a synchronous buck converter is illustrated in Fig. 2.10. Because of its architecture, buck regulator represents some challenges to power conversion designers [Dibene-14], [Lee-06]. The presence of switching devices generate switching

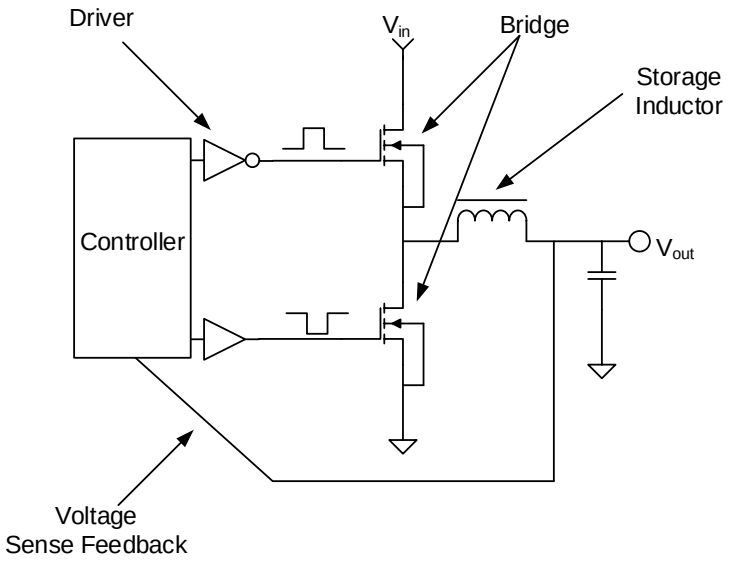


Fig. 2.10 An example of step-down converter including its feedback control loop. Synchronous switching conformed of two FETs [Dibene-14].

loss, and conductor losses have an efficiency hit, while external components, such as output inductors, generate inductor losses which increases ripple. Hence, a good understanding and a careful trade-off analysis needs to be performed to minimize the impact of these losses to the VR.

To minimize switching losses, designers have adopted different switching techniques such as hard switching (HSW) and soft switching (SSW) [Rathi-11], which take the VR to operate into continuous current mode (CCM), associated to SSW and discontinuous current mode (DCM) for HSW (see Fig. 2.11). Table 2.2. summarizes the trade-offs between the two switching techniques.

To minimize voltage ripple and ripple current impact, designers may choose carefully the inductor and the output filter (see Fig. 2.10). Primarily the ripple current at the output node depends on the size of the inductor, as follows

$$I_L = V_{in} \frac{D(1-D)}{L f_{switch}} \tag{2-3}$$

where $I_L$ is the ripple current at the load, $V_{in}$ is the input voltage, $L$ is the output inductor selected, $D$ is the duty cycle (the on-off period given by the desired output voltage divided by the input voltage $V_o/V_{in}$), and $f_{switch}$ is switching frequency of the transistors. Finally, the output voltage ripple equation is like (2-3), but its dependence is given by the size of the series capacitor and the parasitics associated to output inductors:

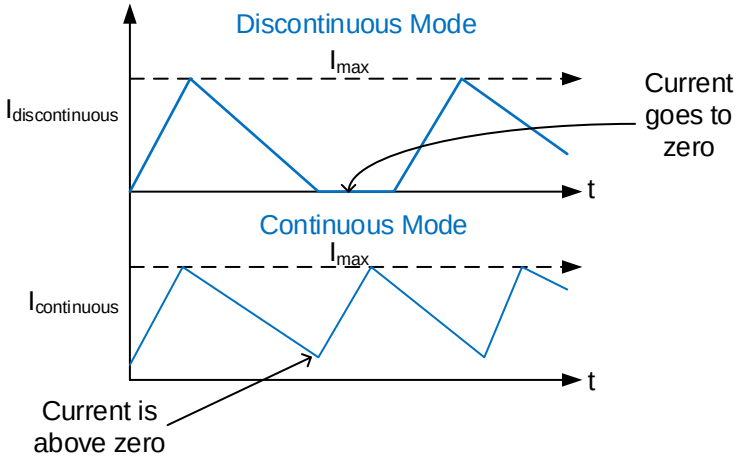


Fig. 2.11 Example of ripple current. Upper plot shows discontinuous current mode obtained with hard switching technique. Lower plot illustrates a continuous current mode obtained when soft switching technique is implemented.

TABLE 2.2. CONTINUOUS VS. DISCONTINUOUS CURRENT MODE TRADE-OFFS [RATHI-11]

| Metric | Hard Switching (DCM) | Soft Switching (CCM) |
|---|---|---|
| switching loss | severe | almost zero |
| overall efficiency | norm | possibly higher |
| heat-sinking requirement | norm | possibly lower |
| hardware count | norm | more |
| overall power density | norm | possibly higher |
| EMI problem | severe | low |
| *dv/dt* problem | severe | low |
| modulation scheme | versatile | limited |
| maturity | mature | developing |
| cost | norm | higher |

$$V_{ripple} \approx I_L ESR = V_{in} \frac{D(1-D)\tau_{RC}}{L f_{switch} C} \tag{2-4}$$

where $V_{ripple}$ is the desired output ripple, $I_L$ is the ripple current at the load, *ESR* stands for inductor's equivalent series resistance, $D$ corresponds to selected duty cycle, $V_{in}$ is the input voltage, $L$ is the selected inductor, $\tau_{RC}$ is the time constant given by inductors *ESR*, and finally $C$ is the output filter's capacitor.

## 2.9. Design Recommendations and Future Challenges

This section covers in a very general manner the most important power conversion metrics to design a step-down converter. Although the chapter covers step-down topology for server computers, these metrics might be applied almost identically to mobile applications as well. Table 2.3 summarizes some design practices suggested to get a good trade-off balance for power design. Even though these design guidelines are good practices, there are more facts and considerations that affect server computers power design.

### 2.9.1 Performance *vs.* Efficiency

Power loss from VR to the chip is not uniform, as seen in Fig. 2.12. This problem translates into current density crowding and thermal dissipation. Power management schemes aim at improving VR's efficiency selecting the best phase shedding configuration. In addition, multiphase VR, power delivery network solution, as well as an adequate selection of the output inductor contribute to reduce significantly power dissipation without sacrificing much chip's performance.

TABLE 2.3. POWER DELIVERY-POWER CONVERSION DESIGN GUIDELINES [DIBENE-14]

| Sources of noise | Mitigation Methods |
|---|---|
| low frequency ripple | Use multiple phases out of phase, use more low-frequency caps with lower ESR, lower impedance of power/ground plane pairs |
| FET switching noise | Lower slew rate of FETs, shift dead time of upper time and lower FETs, use of soft switching topology, use of high frequency decoupling at noise of FETs, reduce parasitic connections to main filter, lower loop impedance between output of main filter and power/ground connections of main FETs/drivers |
| parasitic ring-back | Use lower impedance path between main power train filter and FETs, use low impedance loop at same connection, reduce input parasitic from input filter to main power FET/drivers |
| power/ground plane noise | Lower impedance (typically lower inductance) between power and ground planes. Place high frequency decoupling capacitors across power and ground planes in regions nearest filter output of main power train filter |

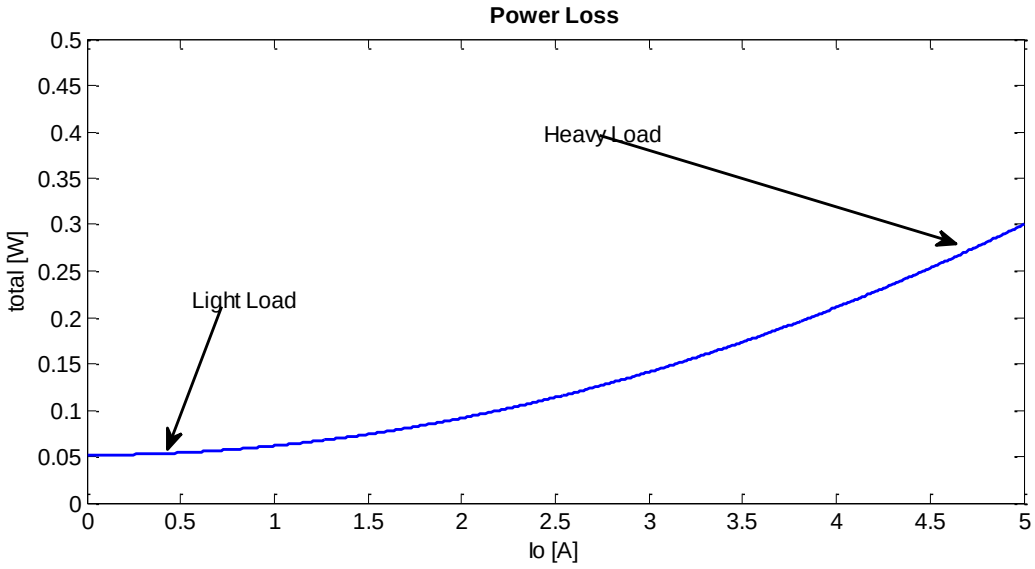


Fig. 2.12 Power loss illustration. Power loss is a metric that transfers directly into heat dissipation. At light loads *i.e.* less than 1 A switching, transistor and conductor losses dominate, while at heavy loads (larger than 1 A) inductor's DC resistance plays a significant role.

### 2.9.2 Simulation *vs.* Real World

How well simulation tools predict real world scenarios? Simulation tools and models employed during simulation must be validated against real measurements, following procedures similar to the ones exemplified in [Leal-Romo-17] and [Leal-Romo-18].

### 2.9.3 Area Constraints

Voltage regulator's physical area can occupy less space if VRs are designed to operate at high switching frequencies [Lee-06]. As illustrated in Fig. 1.10, each power rail needs of a different VR and PD solution. A dedicated VR solution occupies certain motherboard's real state area and the form factor server's rack prevents to increase the size of the motherboard. Considering that a CPU chip can have more than fifty power rails, it is important to find ways of combining rails that share same reference voltage with different voltage sensing schemes for real state savings.

### 2.9.4 Cost Reduction Opportunities

Seeking for cost savings in the bill of materials (BOM) is possible by looking into optimized PDNs [Amelifard-09], [Woojoo-15], with less VRs (*e.g.* IP consolidation, tree topology [Amelifard-07]), less layers count, less decoupling capacitors [Yuancheng-04], etc.

### 2.9.5 Active *vs.* Passive Cooling

It is necessary to assess refrigeration systems *vs.* air cooled solutions as part of the power management schemes and control mechanisms that regulate data center's temperature within the range of 18 °C to 23 °C, without impacting computer's performance. Refer to Section 1.5.2 and Section 1.5.3 for a broader explanation.

### 2.9.6 EMI Regulations

As part of the electromagnetic interference (EMI) and compatibility (EMC) regulations, it is especially necessary to evaluate filter's ability to attenuate high frequency noises, as well as front-end AC/DC board mounted converters [Lee-06]. Complying with Federal Communications Commission (FCC) regulations and other international entities is essential to ensure there are no interferences between devices and there is no hazard for living beings.

### 2.9.7 Electromigration

High current densities may produce thermal impact that deteriorates chip's reliability. It is important to have a robust heatsink and optimized layout solution to avoid high current crowding that may damage transistors or can melt the copper provoking short circuits.

### 2.9.8 Low *vs.* High Frequency Noise

Are buffers operating properly? Jitter noise must be considered in the design of robust power solutions to mitigate noise and other undesired EM effects in buffers [Leal-Romo-15]. Power delivery teams need to ensure that there are proper power isolations and good decoupling mechanisms to prevent any data corruption at the time CPU is performing operations.

### 2.9.9 Moore's Law

As transistors technology shrinks [Moore-06], power delivery teams deal with more leakage current from transistors, which makes PDN more challenging to design. In consequence, tighter voltage noise specifications are needed. This means lowering reference voltages to reduce large power losses, which causes very narrow voltage ranges.

## 2.10. Conclusions

Power delivery is a discipline that looks for an optimum design of the channel to keep the silicon healthy. Power delivery teams interact with several design teams that provide inputs, taking them as baseline assumptions to perform a thorough analysis of the PDN. Once simulations are concluded, power delivery engineers start looking for quality solutions that meet both performance and cost targets; this implies a continuous communication with design teams. A brief review of the main concepts and definitions related to power delivery was realized in this chapter. An in-depth understanding of the typical power delivery methodology and its equivalent models will be addressed in Chapter 4.

This chapter summarizes the two most widely used methodologies to analyze a PDN. The target impedance method is suitable for a quick analysis and general understanding of the behavior of the PDN; however, it represents some challenges to accurately predict the amount of decoupling capacitance needed, which is translated later into cost addition or overdesign of the PDN itself. A more recent methodology was also discussed, which consists of looking into power supply noise induced by jitter up to the silicon. However, although in this methodology it is more viable to accurately measure noise induced to I/O's and memory devices, core interfaces represent a challenge to measure it because of the difficulty to define external probe points.

Besides the advantages and disadvantages of these two techniques, there are still open questions that need to be addressed: how to design an efficient VRM? How can silicon teams predict realistic loading scenarios to avoid overdesign of the PDN? How can silicon and PD teams deal with leakage current? As transistor technologies move forward, new and unknown challenges might appear on the power conversion and the power integrity fields. A future work will cover basic power conversion concepts to design VRM for server platforms.

Also, this chapter reviewed some of the most important metrics to design switching DC-DC converters, specifically the buck regulator implemented on server computers design. Also, some of the most common switching techniques were explained. It is evident, that power conversion and power delivery are two areas that have close interaction. PDN has strong dependences on the VR solution and its metrics, while VR solution has a strong dependence with other areas such as thermal, EMI, etc. As silicon technology shrinks, it is evident that design power solution will become more stringent. On the power conversion side, it becomes necessary to comprehend better the power management schemes, switching techniques of the buck regulator to achieve larger bandwidth and higher efficiency, as well as to optimize the components needed, and VR's cost. On the other side, power delivery will look for cost-effective ways to mitigate noise added into the platform and deliver best VR performance. At the end, both disciplines aim to reduce coupling and jitter effects at chip level to improve efficiency and reduced cost. In Chapter 4, other areas of opportunity to optimize both VR and power distribution designs will be considered.

# 3. Design of Experiments and Space Mapping for Power Delivery Problems

Modern computer servers require cutting edge technologies to meet their expected high performance. Among several relevant disciplines, power delivery is a key player in this regard. Efficient and reliable statistical methods to reduce cost while keeping adequate server's performance is highly demanded from PD's perspective. This chapter addresses a feasible statistical methodology based on design of experiments (DoE) for evaluating platform's power delivery ingredients. Our methodology explores voltage regulator's intrinsic parameters, compensation networks, non-linear compensation parameters, and the quantity of bulk capacitors. Our statistical approach aims at identifying those variables with the largest impact on computer server's PD performance, as well as optimizing them at the system level while achieving cost reduction.

Also, this chapter describes the implementation of an optimization technique for designing structures simulated in 3D electromagnetic field solvers. A proof of concept is done by simulating a spiral inductor for its EM optimization. The optimization technique employed is based on space mapping (SM) methods, more specifically on the aggressive space mapping (ASM).

It is important to state that both methods described in this chapter are an expanded version of the papers [Leal-Romo-17] and [Leal-Romo-17a].

## 3.1. Motivation to Adopt DoE for Power Delivery Analysis

Server's performance imposes severe demands for higher bandwidths, low cost power solutions, and high computing performance. Thus, modern computer servers require cutting edge technologies to meet all the above expectations. In this regard, PD requires some tradeoff decisions to select an adequate voltage regulator, a suitable and affordable decoupling solution, and a robust stack up design to handle sharp load current demands, while keeping silicon under expected performance. Several authors have explored different PD methodologies, such as establishing target impedance across a wide frequency range to select the decoupling capacitor solution needed

by the power delivery network [Smith-99], [Pan-13], as well as time domain approaches [Rahal-Arabi-02] and jitter analysis [Yuan-11], [Swaminathan-10] for estimating voltage drop and voltage margins to come up with robust design solutions.

Industrial PD design is still considered an "art"; it is a heavily heuristic process and very dependent on engineer's expertise. Identifying which variables are most consequential to the PDN space is a highly complex task, usually performed in practice by parametric sweeps, exhaustive enumeration, and engineering knowledge and experience. To the best of our knowledge, formal statistical methodologies based on design of experiments (DoE) for the optimization of PDN is almost inexistent. The contribution of this chapter aims at filling that gap. This chapter primary focus on solving computer server's PD system by optimizing voltage regulator's tuning parameters as well as its bulk capacitors solution as documented in [Leal-Romo-17].

## 3.2. Modeling Power Delivery by DoE

DoE has been adopted in some disciplines closely related to PDN design, such as I/O's electrical validation and verification [Norman-03] and SI analysis [Matoglu-04], [HCL-12], where designers statistically assess cases to find the best channel configuration and the best equalization recipe to avoid loss of information from one buffer to another. However, PD has not taken full advantage of such methodologies.

Similarly to the SI and electrical validation realm, PD designers are looking for the best power channel's recipe capable of maintaining its voltage level within expected ratings under any loading circumstance. PD engineers typically require complex and detailed PDN simulation models to predict with enough accuracy the power channel's behavior, which makes simulation very computationally intensive, taking up to several days to obtain a PDN behavior.

From the above perspective, classical parametric sweeps and exhaustive enumeration are usually prohibitive. Here we propose using advanced DoE techniques, such as fractional factorial design (FFD) [Montgomery-12], hard to change factors with split-plot, etc., that significantly reduce the amount of simulations needed, enabling PD engineers to efficiently identify the most impactful variables within the PDN. In DoE, the objective is to obtain a behavioral model for a certain output of interest, such that it describes with enough accuracy the actual system's behavior. This behavioral approximation is typically implemented by a linear regression model,

$$y(\boldsymbol{x}) = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_{12} x_1 x_2 + \cdots + \varepsilon \tag{3-1}$$

where $y(\boldsymbol{x})$ is the system's output of interest, $\beta$'s are parameters to be determined during the DoE analysis, $x_1$, $x_2$, etc., are the model variables that represent the selected system factors *A*, *B*, etc., and $\varepsilon$ is the statistical error. Variables $x_1$ and $x_2$ are defined in a coded scale from –1 to +1 (low and high corner levels, respectively, for each factor), and $x_1x_2$ represents the interaction between $x_1$ and $x_2$.

To illustrate our methodology, we select a similar VR design to that one in [Xu-14] as the test vehicle to meet some silicon's minimum and maximum voltage requirements: $V_{min}$ = 1.5 V and $V_{max}$ = 2 V, under any loading condition (*di*/*dt*).

## 3.3. DoE for Power Delivery: Simulation Approach

Based on the VR design described in [Xu-14], the parameters investigated in the simulation are enlisted in Table I. We consider not only intrinsic VR compensation parameters, but also some VR's external factors [Leal-Romo-17]. For the first set of intrinsic parameters, we focus our study on the proportional-integral-derivative (PID) controller's variables ($k_i$, $k_d$, $k_p$), non-linear coefficients (*NL-C*), adaptive transient response (*ATR*), and auto-phasing schemes enabling and disabling VR's phases at some point in time ($A_{Ph}$). In the second set, we consider the quantity of bulk capacitors (*BlkC*) and the slew rate (*SR*) (here defined as the *di*/*dt* slope of the transition from

TABLE 3.1. VARIABLES USED TO BUILD THE FFD FOR SIMULATION SCENARIO

| Factor | Equivalent Variable | (–1) | (+1) |
|---|---|---|---|
| $A = (x_1)$ | $k_p$ | 100 | 250 |
| $B = (x_2)$ | $k_d$ | 250 | 450 |
| $C = (x_3)$ | $k_i$ | 100 | 250 |
| $D = (x_4)$ | $k_{fp}$ | 100 | 250 |
| $E = (x_5)$ | $A_{Ph}$ | no | yes |
| $F = (x_6)$ | *NL-C* | no | yes |
| $G = (x_7)$ | *ATR* | no | yes |
| $H = (x_8)$ | *BlkC* | 29% | 100% |
| $J = (x_9)$ | *SR* (1-1000 A/μs) | 200 | 800 |

TABLE 3.2. TEST BECH GENERATED TO COLLECT PDN VOLTAGE BEHAVIOR FROM PHYSICAL IMPLEMENTATION

| $k_p$ | $k_d$ | $k_i$ | $k_{fp}$ | $Atr_{h1}$ (s) | $Atr_{h2}$ (s) | *BlkC* (%) | *SR* (A/μs) |
|---|---|---|---|---|---|---|---|
| 100 | 250 | 100 | 100 | 0 | 0 | 29 | fast |
| 250 | 450 | 100 | 100 | 0 | 0 | 29 | slow |
| 100 | 250 | 250 | 100 | 0 | 0.5 | 29 | slow |
| 250 | 450 | 250 | 100 | 0 | 0.5 | 29 | fast |
| 250 | 250 | 100 | 250 | 0 | 0.5 | 29 | slow |
| 100 | 450 | 100 | 250 | 0 | 0.5 | 29 | fast |
| 250 | 250 | 250 | 250 | 0 | 0 | 29 | fast |
| 100 | 450 | 250 | 250 | 0 | 0 | 29 | slow |
| 100 | 250 | 100 | 100 | 0.125 | 0 | 29 | slow |
| 250 | 450 | 100 | 100 | 0.125 | 0 | 29 | fast |
| 100 | 250 | 250 | 100 | 0.125 | 0.5 | 29 | fast |
| 250 | 450 | 250 | 100 | 0.125 | 0.5 | 29 | slow |
| 250 | 250 | 100 | 250 | 0.125 | 0.5 | 29 | fast |
| 100 | 450 | 100 | 250 | 0.125 | 0.5 | 29 | slow |
| 250 | 250 | 250 | 250 | 0.125 | 0 | 29 | slow |
| 100 | 450 | 250 | 250 | 0.125 | 0 | 29 | fast |
| 250 | 250 | 100 | 100 | 0 | 0.5 | 100 | fast |
| 100 | 450 | 100 | 100 | 0 | 0.5 | 100 | slow |
| 250 | 250 | 250 | 100 | 0 | 0 | 100 | slow |
| 100 | 450 | 250 | 100 | 0 | 0 | 100 | fast |
| 100 | 250 | 100 | 250 | 0 | 0 | 100 | slow |
| 250 | 450 | 100 | 250 | 0 | 0 | 100 | fast |
| 100 | 250 | 250 | 250 | 0 | 0.5 | 100 | fast |
| 250 | 450 | 250 | 250 | 0 | 0.5 | 100 | slow |
| 250 | 250 | 100 | 100 | 0.125 | 0.5 | 100 | slow |
| 100 | 450 | 100 | 100 | 0.125 | 0.5 | 100 | fast |
| 250 | 250 | 250 | 100 | 0.125 | 0 | 100 | fast |
| 100 | 450 | 250 | 100 | 0.125 | 0 | 100 | slow |
| 100 | 250 | 100 | 250 | 0.125 | 0 | 100 | fast |
| 250 | 450 | 100 | 250 | 0.125 | 0 | 100 | slow |
| 100 | 250 | 250 | 250 | 0.125 | 0.5 | 100 | slow |
| 250 | 450 | 250 | 250 | 0.125 | 0.5 | 100 | fast |

minimum current $I_{min}$ to maximum current $I_{max}$). From Table 3.1, there are nine factors to

investigate, requiring a total of $2^9 = 512$ simulations when using full factorial design. However, we use the FFD technique to reduce the number of simulations by "confounding" some of these factors.

Returning to our simulation's test bench scenario, we selected a $2_{IV}^{(9-4)} = 32$ experiments. We use resolution IV since it is suitable for designs in which none of the main effects is an alias of another main effect or neither two-factor interactions, but two factor interactions are aliases between them. Typically, aliasing technique receives the name of "confusion of factors". Additionally, we use a factorial $2^{(9-4)}$ because only five of the main factors are not confounded, and they correspond to Yates order for generating the test bench, while the remaining four factors are obtained by the following generators [Montgomery-12]: $F = \pm BCDE$, $G = \pm ACDE$, $H = \pm ABDE$, and $J = \pm ABCE$.

The corresponding test bench to the 32 scenarios to collect $V_{min}$ and $V_{max}$ responses is given in Table 3.2. We carried out only time domain simulations in SIMetrix/Simplis[2] simulator to obtain test bench results from Table 3.2 under different VR and PD settings. Once results are collected,

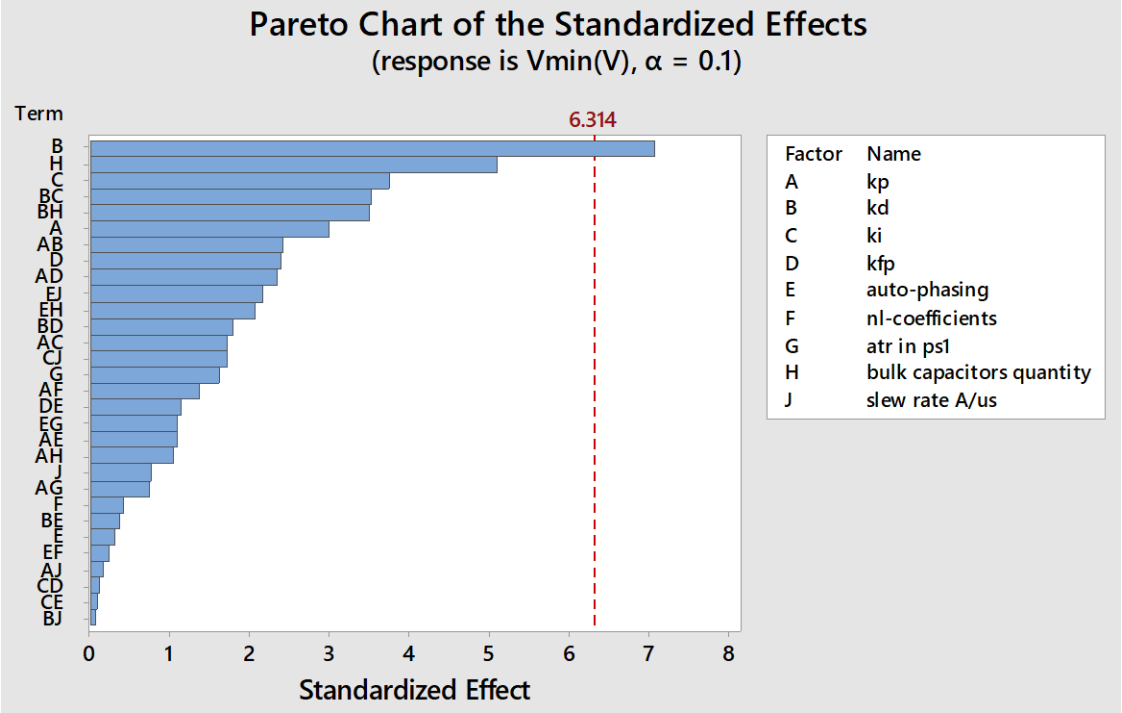


Fig. 3.1 Pareto's chart after performing ANOVA with a significance level of $\alpha = 10\%$ for $V_{min\_sim}$. Note that $k_d$ is the most dominant factor.

[2] SIMetrix/Simplis 7.20e (x64), Copyright © 2014 Simplis Technologies Ltd, 78 Chapel Street, Thatcham, Berkshire, RG18 4QN, UK, http://www.simetrix.co.uk/site/index.html

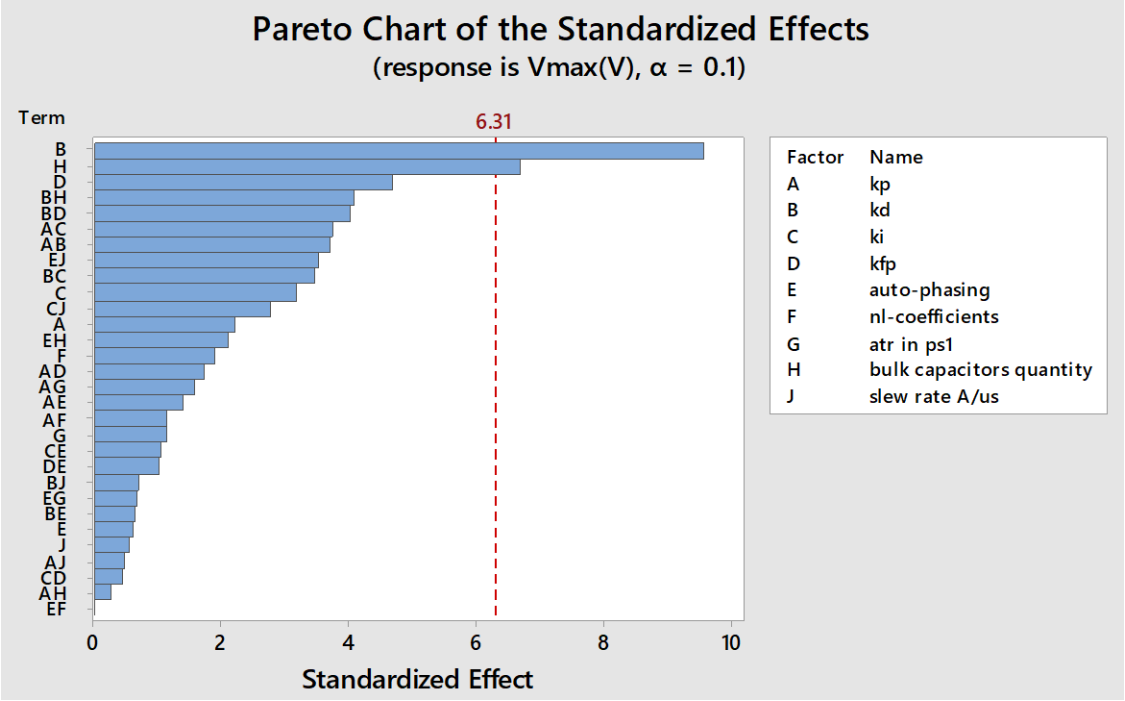


Fig. 3.2 Pareto's chart after performing ANOVA with a significance level of $\alpha = 10\%$ for $V_{max\_sim}$. Note that $k_d$ and *BlkC* are the most dominant factors.

an analysis of variance (ANOVA) is performed to get some linear regression equations at the output of interest, including its effects. Then, assuming a 10% confidence level, from Pareto's analysis (Fig. 3.1 and Fig. 3.2), it is possible to identify which variables are more important and hence simplify the equations obtained from ANOVA, yielding the following parameterized models for the minimum and maximum simulated voltages:

$$V_{min\_sim}(\boldsymbol{x}) \approx 0.960 + 0.001722x_2 \tag{3-2}$$

$$V_{max\_sim}(\boldsymbol{x}) \approx 2.791 - 0.00261x_2 - 0.0806x_8 \tag{3-3}$$

It is interesting to note that both model equations depend on a derivative parameter ($x_2$ = $k_d$), while $V_{max}$ adds one more dependency with the quantity of bulk capacitors ($x_8$ = *BlkC*).

## 3.4. DoE for Power Delivery: Physical Approach

Based on our findings obtained in Section 3.3, a laboratory verification with the same PD design on a physical platform implementation is conducted to validate if the dependencies are the same. Since the physical VR module has more parameters available for configuration, we focus our interest on similar parameters to those used in the simulation approach. Table 3.3 shows the

TABLE 3.3. VARIABLES USED TO BUILD THE FFD FOR PHYSICAL IMPLEMENTATION

| Factor | Equivalent Variable | (–1) | (+1) |
|---|---|---|---|
| $A = (x_1)$ | $k_p$ | 100 | 250 |
| $B = (x_2)$ | $k_d$ | 250 | 450 |
| $C = (x_3)$ | $k_i$ | 100 | 250 |
| $D = (x_4)$ | $k_{fp}$ | 100 | 250 |
| $E = (x_5)$ | $ATR_{h1}$ | no | yes |
| $F = (x_6)$ | $ATR_{h2}$ | no | yes |
| $G = (x_7)$ | $ATR_{\_kp}$ | 0 | 56 |
| $H = (x_8)$ | $k_{j\_atrl}$ | 0 | 56 |
| $J = (x_9)$ | *BlkC* | 29% | 100% |
| $K = (x_{10})$ | *SR* (1-1000 A/μs) | 200 | 800 |

codification for each factor. Following exactly the same DoE procedure used in Section 3.3, we generated 32 scenarios using the FFD technique as described in Table 3.4.

Since in the laboratory, where there are instabilities, the VR saturates, there were some scenarios unable to produce valid results. To solve this problem, we treated the statistical results as a generalized linear model to identify the most meaningful factors from the linear model equation (see Fig. 3.4 and Fig. 3.3). The resulting model equations describing system's behavior for the physical $V_{min}$ and $V_{max}$ are:

$$V_{min\_phy}(\boldsymbol{x}) \approx 1.3676 + 0.001826x_8 \tag{3-4}$$

$$V_{max\_phy}(\boldsymbol{x}) \approx 2.019 - 0.000047x_1 - 0.000297x_2 \tag{3-5}$$

where $x_8 = k_{j\_atrl}$ is one of the non-linear factors, while from PID's side, some compensation factors like $x_1 = k_p$ and $x_2 = k_d$ resulted meaningful. It should be noticed that the quantity of bulk capacitors is not among the most relevant factors for the physical implementation. This fact indicates that it would be possible to investigate a favorable scenario that reduces the quantity of capacitors needed. To validate that, we expanded our model to incorporate this additional factor, as follows:

$$V_{min\_phy}(\boldsymbol{x}) \approx 1.3676 + 0.001826x_8 + 0.000198x_9 \tag{3-6}$$

$$V_{max\_phy}(\boldsymbol{x}) \approx 2.019 - 0.000047x_1 - 0.000297x_2 - 0.000091x_9 \tag{3-7}$$

It is seen that this new DoE model is now dependent on the number of bulk capacitors, $x_9$.

TABLE 3.4. TEST BECH GENERATED TO COLLECT PDN VOLTAGE BEHAVIOR FROM PHYSICAL IMPLEMENTATION

| $k_p$ | $k_d$ | $k_i$ | $k_{fp}$ | $Atr_{h1}$ (s) | $Atr_{h2}$ (s) | $BlkC$ (%) | $SR$ (A/μs) |
|---|---|---|---|---|---|---|---|
| 100 | 250 | 100 | 100 | 0 | 0 | 29 | fast |
| 250 | 450 | 100 | 100 | 0 | 0 | 29 | slow |
| 100 | 250 | 250 | 100 | 0 | 0.5 | 29 | slow |
| 250 | 450 | 250 | 100 | 0 | 0.5 | 29 | fast |
| 250 | 250 | 100 | 250 | 0 | 0.5 | 29 | slow |
| 100 | 450 | 100 | 250 | 0 | 0.5 | 29 | fast |
| 250 | 250 | 250 | 250 | 0 | 0 | 29 | fast |
| 100 | 450 | 250 | 250 | 0 | 0 | 29 | slow |
| 100 | 250 | 100 | 100 | 0.125 | 0 | 29 | slow |
| 250 | 450 | 100 | 100 | 0.125 | 0 | 29 | fast |
| 100 | 250 | 250 | 100 | 0.125 | 0.5 | 29 | fast |
| 250 | 450 | 250 | 100 | 0.125 | 0.5 | 29 | slow |
| 250 | 250 | 100 | 250 | 0.125 | 0.5 | 29 | fast |
| 100 | 450 | 100 | 250 | 0.125 | 0.5 | 29 | slow |
| 250 | 250 | 250 | 250 | 0.125 | 0 | 29 | slow |
| 100 | 450 | 250 | 250 | 0.125 | 0 | 29 | fast |
| 250 | 250 | 100 | 100 | 0 | 0.5 | 100 | fast |
| 100 | 450 | 100 | 100 | 0 | 0.5 | 100 | slow |
| 250 | 250 | 250 | 100 | 0 | 0 | 100 | slow |
| 100 | 450 | 250 | 100 | 0 | 0 | 100 | fast |
| 100 | 250 | 100 | 250 | 0 | 0 | 100 | slow |
| 250 | 450 | 100 | 250 | 0 | 0 | 100 | fast |
| 100 | 250 | 250 | 250 | 0 | 0.5 | 100 | fast |
| 250 | 450 | 250 | 250 | 0 | 0.5 | 100 | slow |
| 250 | 250 | 100 | 100 | 0.125 | 0.5 | 100 | slow |
| 100 | 450 | 100 | 100 | 0.125 | 0.5 | 100 | fast |
| 250 | 250 | 250 | 100 | 0.125 | 0 | 100 | fast |
| 100 | 450 | 250 | 100 | 0.125 | 0 | 100 | slow |
| 100 | 250 | 100 | 250 | 0.125 | 0 | 100 | fast |
| 250 | 450 | 100 | 250 | 0.125 | 0 | 100 | slow |
| 100 | 250 | 250 | 250 | 0.125 | 0.5 | 100 | slow |
| 250 | 450 | 250 | 250 | 0.125 | 0.5 | 100 | fast |

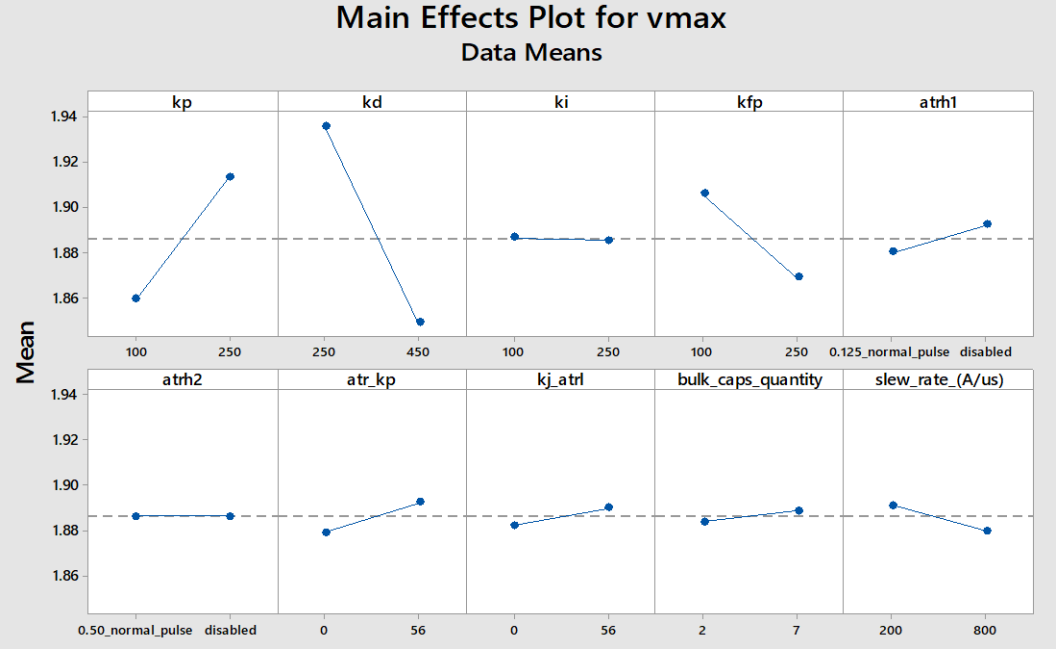


Fig. 3.3 Main effects on $V_{max\_phy}$ after performing ANOVA's generalized linear model analysis. Note that $k_p$ and are $k_d$ the most dominant factors.

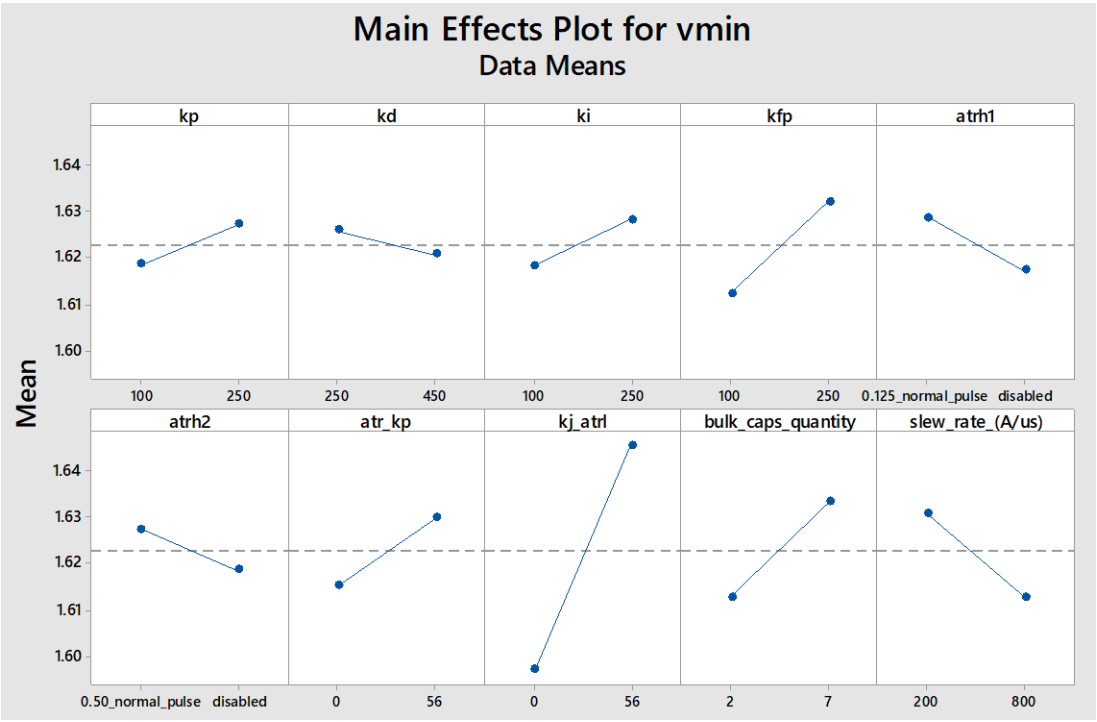


Fig. 3.4 Main effects on $V_{min\_phy}$ after performing ANOVA's generalized linear model analysis. Note that $k_{j\_atrl}$ is the most dominant factor.

## 3.5. System Optimization: Simulation and Laboratory

In the previous two sections, we described the methodology to find the most significant factors of a PD system in two scenarios: simulation and its physical implementation. As it is observed, there are some coincidences and discrepancies on the model equations obtained from the simulation and laboratory measurements.

Both scenarios indicate that a good PID compensation recipe is needed ($k_p$ and $k_d$ resulted significant factors), while the laboratory approach added one more non-linear parameter that needs fine tuning ($k_{j\_atrl}$). Also, in the case of the laboratory, the quantity of bulk capacitors was initially not too relevant, indicating a great opportunity to reduce costs. We adjusted our DoE linear regression model to include bulk capacitors as one more factor to consider in the physical PD optimization.

To optimize power delivery's system response from simulation and from the laboratory, we solve an optimization problem to find an optimal solution $\boldsymbol{x}^*$ that minimizes a suitable objective function $u(\boldsymbol{x})$ with respect to variables $\boldsymbol{x}$, exploiting our response surface model $y(\boldsymbol{x})$ [Montgomery-12] (see flow diagram in Fig. 3.5),

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} u(\boldsymbol{x}) \tag{3-8}$$

with the objective function defined as:

$$u(\boldsymbol{x}) = [V_{\min} - y(\boldsymbol{x})] + [y(\boldsymbol{x}) - V_{\max}] \tag{3-9}$$

Central composite design (CCD) [Montgomery-12] is one of various response surface modeling (RSM) techniques. CCD is composed of factorial design $2^k$ or FFD with $n_F$ runs, $2^k$ axial or star runs and $n_c$ central runs. The fundamental deployment of a CCD is based on sequential experimentation, *i.e.*, a $2^k$ design is used to adjust the first order model. Since such model usually presents lack of adjustment, then, axial runs are added to incorporate some quadratic terms in the model. In this chapter we selected CCD as the method to develop the RSM models.

From Fig. 3.5, the first optimization step uses steepest descent to establish the direction that maximizes system's performance. Finally, the second step consists of applying the CCD

technique to enhance the model around the optimal solution.

Table 3.5, summarizes our results before and after optimization for both scenarios (PD simulation and physical PD implementation). As observed in Table V, physical PD implementation needs 14% more capacitors than the simulation, although, still making feasible a 29% reduction of capacitors needed. Both scenarios (simulation and physical implementation) are evaluated under fast SR conditions before and after optimization.

From Table 3.5, silicon's $V_{min}$ and $V_{max}$ meet the required specifications, although, we need to ensure these results are valid from the VR's perspective. To ensure these results meet VR's voltage boundaries, we estimate the maximum and minimum VR output voltage allowed. The following equations estimate these requirements:

$$VR_{lb} = V_{nom} - (I_{max})(LL) - VR_{AC\_DC} \tag{3-10}$$

$$VR_{ub} = V_{nom} + (I_{max})(LL) + VR_{AC\_DC} \tag{3-11}$$

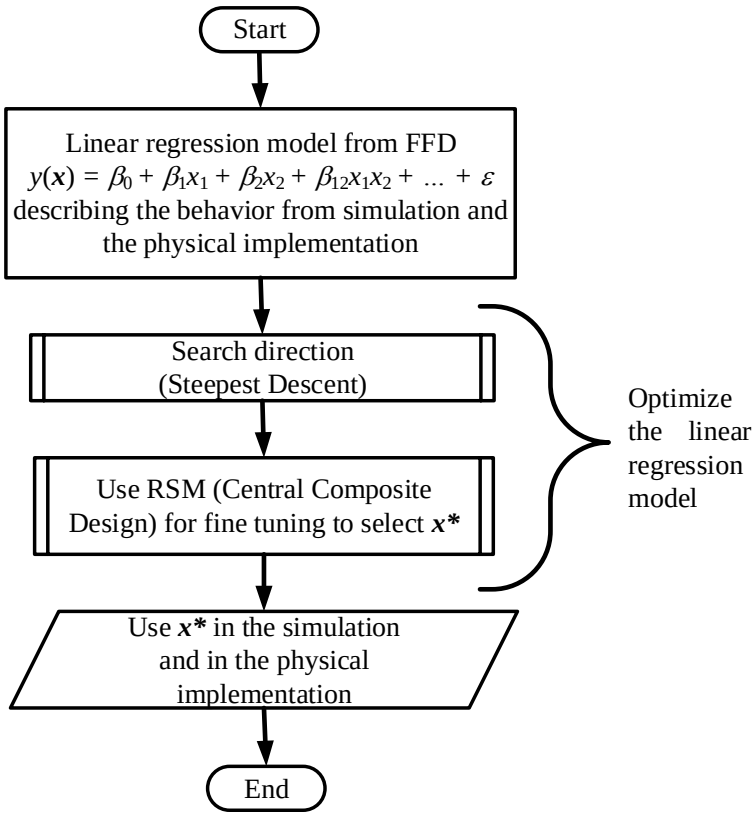


Fig. 3.5 Flow diagram illustrating the sequence followed in the implementation of RSM optimization technique.

TABLE 3.5. DOE RESULTING VOLTAGE LEVELS AND PEAK TO PEAK COMPARISON FOR SIMULATION AND PHYSICAL IMPLEMENTATION SCENARIOS BEFORE AND AFTER OPTIMIZATION

| Scenario | | $K_P$ | $K_D$ | $KJ_{\_ATRL}$ | *BLKC* | *SR* | $V_{MIN}$ (V) | $V_{MAX}$ (V) |
|---|---|---|---|---|---|---|---|---|
| simulation | before | 135 | 330 | N/A | 100% | FAST | 1.64 | 1.85 |
| | after | 135 | 275 | N/A | 57% | FAST | 1.57 | 1.89 |
| laboratory | before | 180 | 420 | 0 | 100% | FAST | 1.62 | 1.82 |
| | after | 124 | 450 | 38.5 | 71% | FAST | 1.58 | 1.88 |

where $VR_{lb}$ and $VR_{ub}$ are the VR output voltage boundaries (lower and upper bounds, respectively), $V_{nom}$ is the nominal voltage given for the power rail's channel, $I_{max}$ is the maximum current load, *LL* is the load line or equivalent resistance seen by the system[3], and $VR_{AC\_DC}$ is the AC plus DC tolerance the VR can support; for this particular case, $VR_{AC\_DC}$ = ±22 mV. Using (3-10) and (3-11), the calculated output voltage boundaries are $VR_{lb}$ = 1.58 V and $VR_{ub}$ = 1.98 V. Hence, from Table V, it is observed that optimization results are marginally meeting minimum and maximum VR's voltage boundaries.

## 3.6. Power Inductor Optimization

During the last three decades, CAD 2.5D and 3D electromagnetic (EM) field solvers have presented an exponential demand. Some of the most common computational techniques employed to solve such complex problems are finite elements method (FEM) [ANSYS-12], method of moments (MoM) [Keysight-08], and finite integration technique (FIT) [Microwaves101-15], among others. One of the most recent 3D FEM tools introduced to the market is Cadence® Sigrity™ PowerSI® 3D EM (PowerSI 3D, PSI-3D) [Cadence-16].

To achieve our objective, firstly we compared our 3D simulation results against results reported in a previous work [Eroglu-11]. Later, we described the development of a MATLAB driver to manipulate the geometry on the spiral inductor from the EM-solver PSI-3D. Finally, to achieve our desired inductance values, we employed the Broyden-based input space mapping algorithm, better known as aggressive space mapping (ASM) [Bandler-95], [Leal-Romo-12],

[3] The specific values of $V_{nom}$, $I_{max}$, and *LL*, are proprietary information from Intel Corporation.

[Rayas-Sánchez-16], [Leal-Romo-17a], as the selected optimization technique to fine tune the geometrical dimensions of the spiral inductor structure. This section describes the implementation of an optimization method to facilitate fine tuning of the geometry for a spiral inductor structure simulated in a 3D EM-FEM solver, namely, Cadence® Sigrity™ PowerSI® 3D EM.

## 3.7. Power Inductor Fine Model Implementation in PSI-3D

In this section we discuss the design of a 3D spiral inductor structure for high-power

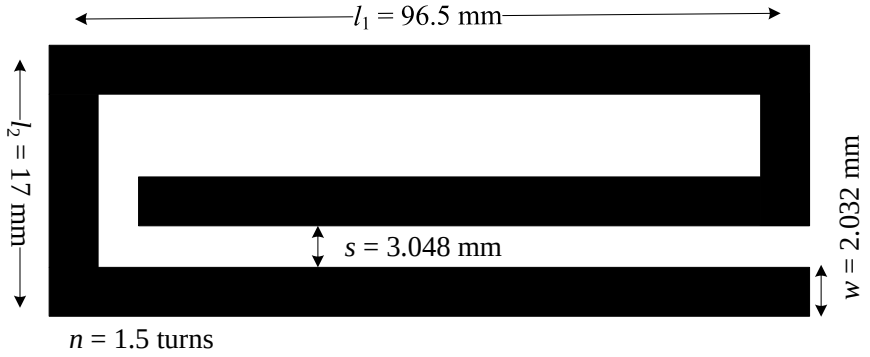


Fig. 3.6 Spiral inductor geometry and dimensions for high-power applications [Eroglu-11].

TABLE 3.6. SPIRAL INDUCTOR PHYSICAL PARAMETERS

| Variable Name and Units | Initial Value |
|---|---|
| $L_1$ (mm) | 96.5 |
| $L_2$ (mm) | 17 |
| $S$ (mm) | 3.048 |
| $W$ (mm) | 2.032 |
| $H$ (mm) | 2.54 |
| $t$ (mm) | 0.03048 |
| $n$ (turns) | 1.5 |
| $\varepsilon_r$ ($Al_2O_3$) | 9.8 |
| $\rho$ (CuAu) | 0.7066 |
| $\sigma$ (S/m) | $5.8 \times 10^7$ |
| $\tan\delta$ | 0.0001 |

applications in PSI-3D[4], which will be used as our fine model to optimize its geometrical dimensions. To perform such task, we decided to base our design on inductor 5 from [Eroglu-11], which is illustrated in Fig. 3.6. The parameters and material properties of the inductor structure are described in Table 3.6. A 3D view of the spiral inductor structure as implemented in PSI-3D is depicted on Fig. 3.7. The inductance value of interest is measured at 13.5 MHz, while the resonance frequency point is expected to happen at around 90 MHz. Table 3.7 summarizes the parameters obtained from our PSI-3D simulation against the simulated parameters reported in [Eroglu-11]. As it is observed in Table 3.7, both numerical results are very similar. In our case the inductance measured at 13.5 MHz is off by 2 nH and there is a small difference of almost 3 MHz in the resonance frequency, with respect to Sonnet's simulation results. This slight discrepancy in the results can be attributed to the nature of the simulators employed. In our case, we used a zero-order model from a 3D FEM solver, while [Eroglu-11] employs Sonnet, a 2.5D tool that uses the MoM.

TABLE 3.7. SONNET *VS.* PSI-3D RESUTLS

| Simulator | $L$ (nH) @ 13.5MHz | $F_r$ (MHz) |
|---|---|---|
| Sonnet [5] | 132.78 | 92.5 |
| PSI-3D | 130.5 | 89.12 |

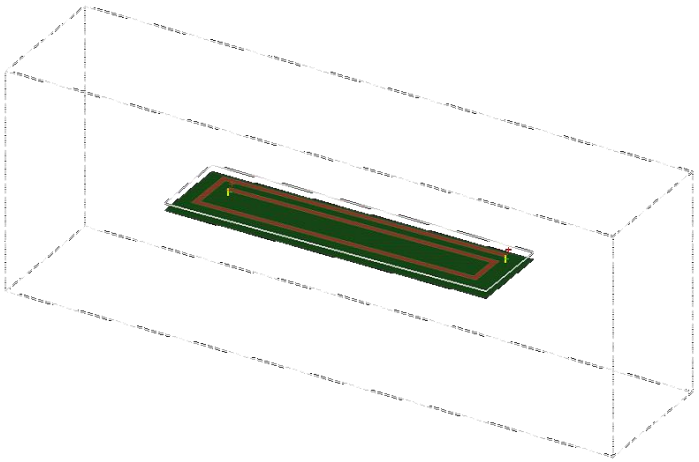

Fig. 3.7 Implementation of the 1.5 turns spiral inductor (fine model) in PSI-3D.

[4] PowerSI 3D-EM v17.0.0.12061.80497, Cadence Design Systems, Inc., San José, CA, 2016.

## 3.8. Power Inductor Coarse Model Implementation in APLAC

In our case, the coarse model is created in APLAC[5], a high-frequency circuit simulator. It is clear, that this optimization algorithm requires efficient drivers for both the coarse and fine model. In our case, the coarse model (APLAC) is directly driven from Matlab, while the fine model (PSI-3D) is driven from Matlab as well, using the proposed driver without utilizing the graphical user interface (GUI).

The coarse model implemented in APLAC is shown in Fig. 3.8. One simulation of this inductor in APLAC takes less than a second using a Xeon® computer server.

As mentioned before, the structure in PSI-3D is illustrated in Fig. 3.7. It is the same spiral inductor built in APLAC with all geometrical dimensions parameterized, such that they can be altered by the optimization algorithm implemented in Matlab. The inductor is contained inside a boundary box at least three times taller than the total height of the substrate plus the inductor and

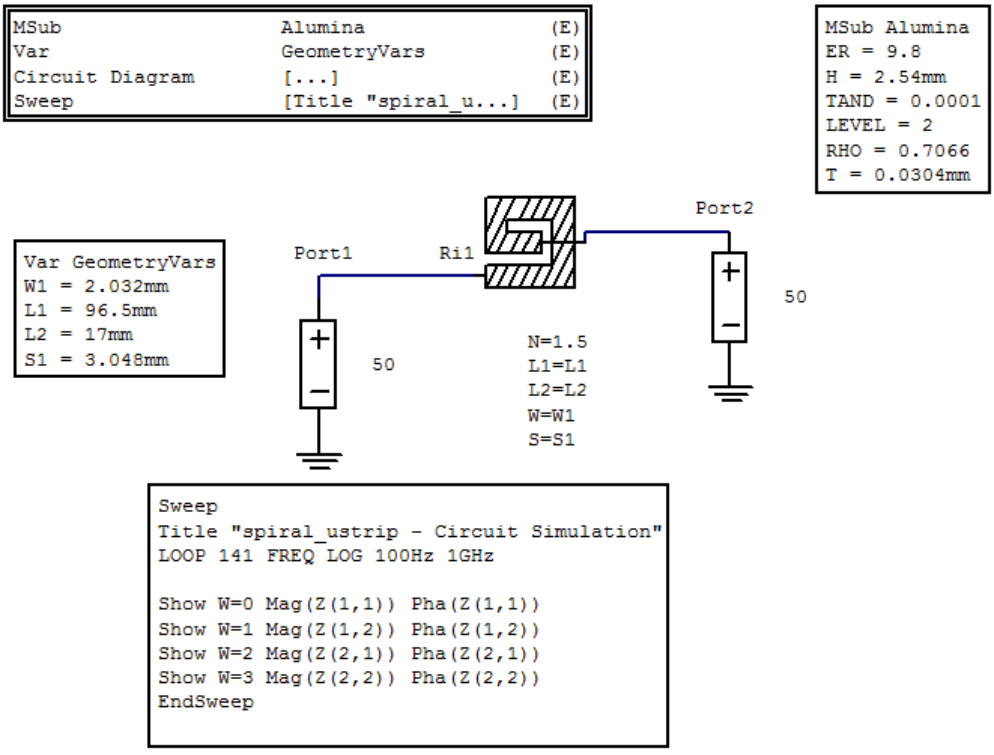


Fig. 3.8 Spiral inductor circuit as implemented in APLAC, taken here as the coarse model.

[5] APLAC, ver. 8.1, APLAC Solutions Corporation, Helsinki, Findland, 2005.

the reference plane and two times wider and larger than the spiral inductor structure, such that the electromagnetic fields in the structure do not interact with the enclosing box. Two 50 Ω lumped ports perpendicular to the input-output of the inductor are employed. One simulation (one frequency sweep from 100 Hz to 1 GHz with 141 frequency points) of this inductor in PSI-3D consumes 5 minutes and 47 seconds with the same server computer used for the coarse model, including the construction of the initial mesh, one adaptive iteration, with two minimum number of converged iterations per simulation.

One more benefit of non-GUI operation is the time saved by not having to load the project for graphical display, since, this operation can take long enough to impact the overall execution time.

## 3.9. Optimizing the Power Inductor with Space Mapping

To test our MATLAB-PSI-3D driver, the spiral inductor is optimized by implementing the ASM algorithm [Bandler-95], as depicted in Fig. 3.9 [Leal-Romo-17a]. This algorithm starts by

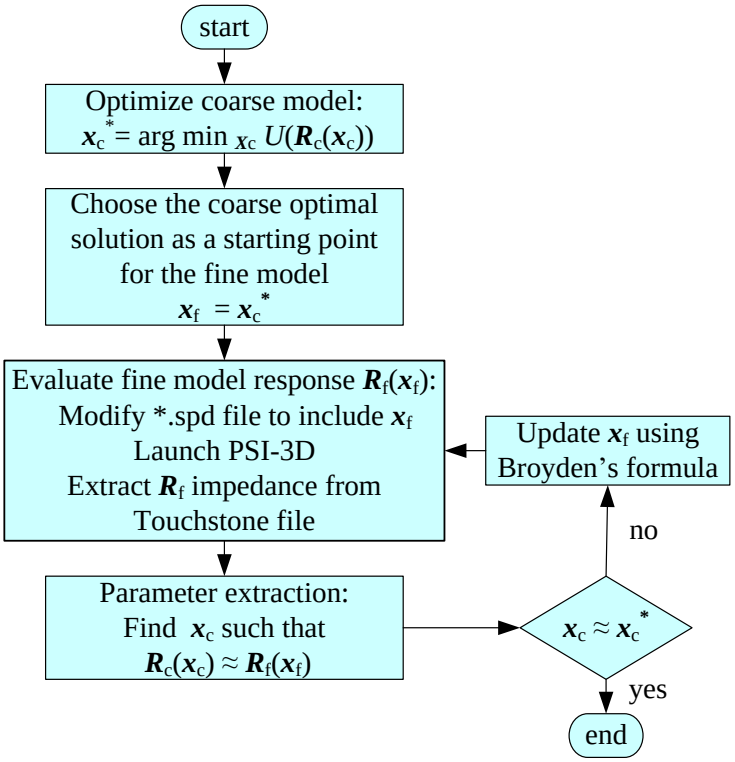


Fig. 3.9 Aggressive space mapping (ASM) algorithm as used with our MATLAB-PSI-3D driver. Taken from [Leal-Romo-17a].

optimizing a coarse model of the original structure, denoted as $\boldsymbol{R}_c(\boldsymbol{x}_c)$, to optimally satisfy some given specifications. The coarse model response is in $\boldsymbol{R}_c$, while the coarse model design parameters are in $\boldsymbol{x}_c$. Then, the optimal design of the coarse model, $\boldsymbol{x}_c^*$, is introduced as new geometrical parameters to PSI-3D, to run a simulation of the fine model $\boldsymbol{R}_f(\boldsymbol{x}_f)$. With this information, the algorithm reads the S-parameters from the fine model contained in vector $\boldsymbol{R}_f$ using our driver and converts them into Z-parameters. Next, coarse model design parameters are extracted and converted into Z-parameters to match the current fine model response. If the extracted parameters are sufficiently close to the optimal coarse model design, the algorithm ends, otherwise, it continues by updating the fine model design parameters using Broyden's formula [Broyden-65], simulating again the PSI-3D structure with the new geometrical parameters.

### 3.9.1 MATLAB Driver to Handle PSI-3D

As reviewed in Section 3.7, a selected spiral inductor for high-power applications was

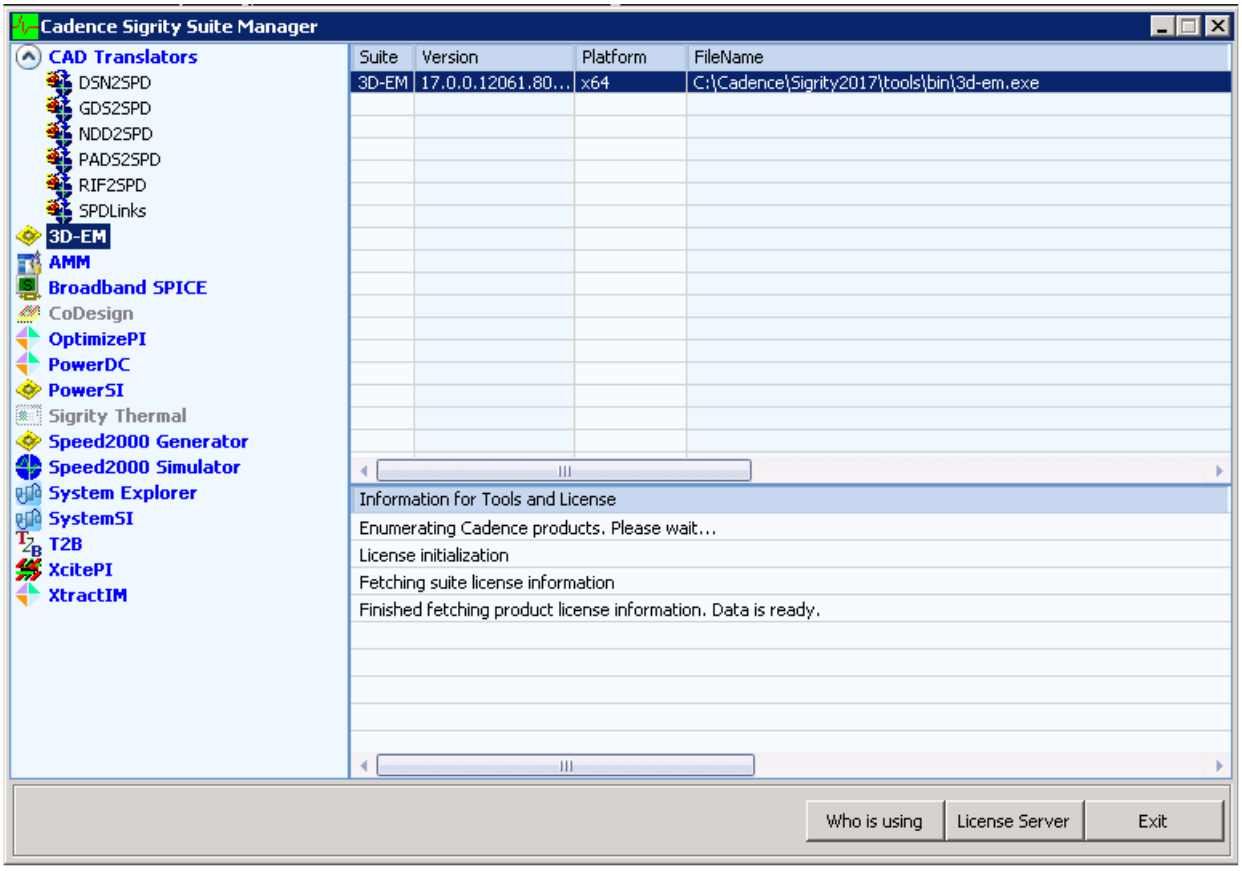


Fig. 3.10 Cadence's Sigrity Suite Manager active window to call PSI-3D in batch mode.

```
PSIexe = 'C:\Cadence\Sigrity2017\tools\bin\3D-EM.exe';
PSIProjectFileName = [out_Filename '.spd'];
system([PSIexe ' /b ' PSIProjectFileName]);
```

Fig. 3.11 MATLAB script to call PSI-3D from command window. First line indicates the path to 3D-EM.exe; second line defines the file name to simulate with ".spd" extension. Finally, the third line executes PSI-3D from command line under batch mode.

implemented in PSI-3D, showing good agreement against the results reported in [Eroglu-11]. In this section we cover the development of MATLAB's[6] driver to handle PSI-3D in batch mode.

#### *3.9.1.1 Executing PSI-3D in Batch Mode*

To execute PSI-3D in batch mode [Sigrity-11], first, it is needed to keep active Cadence's Sigrity Suite Manager window, illustrated in Fig. 3.10. As a second step, we open the command window introducing the path to the executable, followed by the indication of batch mode, and finally the name of the file with extension ".spd", as illustrated in Fig. 3.11.

#### *3.9.1.2 Generating MATLAB-PSI-3D File*

PSI-3D supports "tickle" (Tcl) programming language; hence it is relatively easy to change its scripts with any text editor. Since we already designed our PSI-3D structure, we can open the file "spiral.spd" with MATLAB's text editor. Basically, all the settings of the ports, material, and dielectric type, the order of the simulation to be performed, and the coordinates of the structure, are all indicated inside the script.

Since we want to manipulate the dimensions of the structure, we need to identify the ".Shape" instruction and the origin of the coordinates or center point. Then, it is needed to specify half of the dimensions to draw first the outer left section of the shape with the new coordinates, followed by other half of the dimensions with the new coordinates to draw the outer right section of the shape, and so on, to build the string of coordinates, as illustrated in Fig. 3.12.

Finally, the new Tcl sentence of the shape containing its string coordinates to draw the structure is inserted in PSI-3D's ".spd" file, as shown in Fig. 3.13.

[6] MATLAB, Version 8.5.0.197613, The MathWorks, Inc., 3 Apple Hill Drive, Natick MA 01760-2098, 2015.

```
%Xscale points
%Define the index of the moving vertex when scaled in X direction
X_R=[2,3,6,7,10,11];
X_L=[1,12,8,9,4,5];

Center_X=(Points(2,1)-Points(1,1))/2;
Center_Y=(Points(1,2)-Points(11,2))/2;

%move X external
Points(1,1)=Center_X-NewX_mm/2;
Points(12,1)=Center_X-NewX_mm/2;
Points(8,1)=Center_X-NewX_mm/2;
Points(9,1)=Center_X-NewX_mm/2;
.
.
.
    %%where we process the part of the shape
    if(strfind(newtline,'Polygon1'))
        %read two lines
        tline = fgets(fileID);
        tline = fgets(fileID);
        %write the new poly
        fprintf(OutfileID,'Polygon1::VCC+ %6.6fmm %6.6fmm %6.6fmm %6.6fmm %6.6fmm
%6.6fmm %6.6fmm %6.6fmm \n',Points(1,:),Points(2,:),Points(3,:),Points(4,:));
        fprintf(OutfileID,'+ %6.6fmm %6.6fmm %6.6fmm %6.6fmm %6.6fmm %6.6fmm %6.6fmm
%6.6fmm \n',Points(5,:),Points(6,:),Points(7,:),Points(8,:));
        fprintf(OutfileID,'+ %6.6fmm %6.6fmm %6.6fmm %6.6fmm %6.6fmm %6.6fmm %6.6fmm
%6.6fmm \n',Points(9,:),Points(10,:),Points(11,:),Points(12,:));
        continue
    end
.
.
.
    %write line from source
    fprintf(OutfileID,newtline);
    index=index+1
    if(index==368)
        a=1
    end
```

Fig. 3.12 Portion of MATLAB script to generate the string of coordinates to draw the shape of the spiral inductor with Tcl programming language. *Center_X* is the origin of the coordinates and *NewX_mm* represents one of the X axes variables to alter inductor's geometry on the left side and the right side.

#### *3.9.1.3 Reading Results from PSI-3D*

Once PSI-3D finished running the simulation, it generates a Touchstone file containing a matrix of S-parameters. In this case a ".s2p" file is generated. Next, we read the S-parameters in Matlab and convert them to impedance parameters (Z-parameters).

Finally, the port at the output of the inductor is open circuited to measure inductance and resistance parameters along the entire frequency range using the following equations:

```
.Shape Shape002
Polygon1::VCC+ 1.000000e+001mm 1.000000e+001mm 1.085320e+002mm 1.000000e+001mm
1.085320e+002mm 2.395200e+001mm 1.508000e+001mm 2.395200e+001mm
+            1.508000e+001mm 2.192000e+001mm 1.065000e+002mm 2.192000e+001mm
1.065000e+002mm 1.203200e+001mm 1.203200e+001mm 1.203200e+001mm
+            1.203200e+001mm 2.700000e+001mm 1.085320e+002mm 2.700000e+001mm
1.085320e+002mm 2.903200e+001mm 1.000000e+001mm 2.903200e+001mm
.EndShape
```

Fig. 3.13 Resulting Tcl code from MATLAB to draw the new shape of spiral inductor. String of coordinates to draw spiral inductor's structure.

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = [z] \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{3-12}$$

$$z_{in} = z_{11} = \left. \frac{V_1}{I_1} \right|_{I2=0} \tag{3-13}$$

where [***z***] represents the complex impedance matrix of the form $R + jX$; where $R$ is the real part or resistance and $X$ is the imaginary part or inductor's impedance, and $z_{11}$ is the input impedance when the output port is open.

#### *3.9.1.4 Design Specifications and Optimization Results*

To comply with our own power delivery application, the optimization problem was formulated to meet the following specifications [Leal-Romo-17a]:

$$L_{AC} \leq 115 \text{ nH for } 10 \text{ MHz} \leq f \leq 16 \text{ MHz} \tag{3-14}$$

$$R_{AC} \geq 90 \text{ m}\Omega \text{ for } 100 \text{ Hz} \leq f \leq 1 \text{ kHz} \tag{3-15}$$

The following parameters were used as optimization variables: $\boldsymbol{x} = [w \;\; L_1 \;\; L_2 \;\; s]^T$, keeping fixed the following preassigned parameters: $\boldsymbol{y} = [H \;\; t \;\; n \;\; \varepsilon_r \;\; \rho \;\; \sigma \;\; \tan\delta]^T$.

As a result of applying ASM, the structure was optimized with 181 APLAC runs and only 8 PSI-3D runs. Final dimensions of this structure are shown in Table 3.8, as well as the starting point for optimization ($\boldsymbol{x}_c^*$). During the execution of this optimization method, no GUI interface was required (except for the initial creation of the spiral inductor structure). The resulting $L_{AC}$ and $R_{AC}$ meet the desired behavior described by (3-14) and (3-15), as confirmed in Fig. 3.14.

TABLE 3.8. DESIGN PARAMETERS NUMBERS BEFORE AND AFTER OPTIMIZATION

| Variable Name and Units | Initial Values | Final Values |
|---|---|---|
| $L_1$ (mm) | 96.5 | 83.11 |
| $L_2$ (mm) | 17 | 16.22 |
| $S$ (mm) | 3.048 | 4.48 |
| $W$ (mm) | 2.032 | 1.659 |

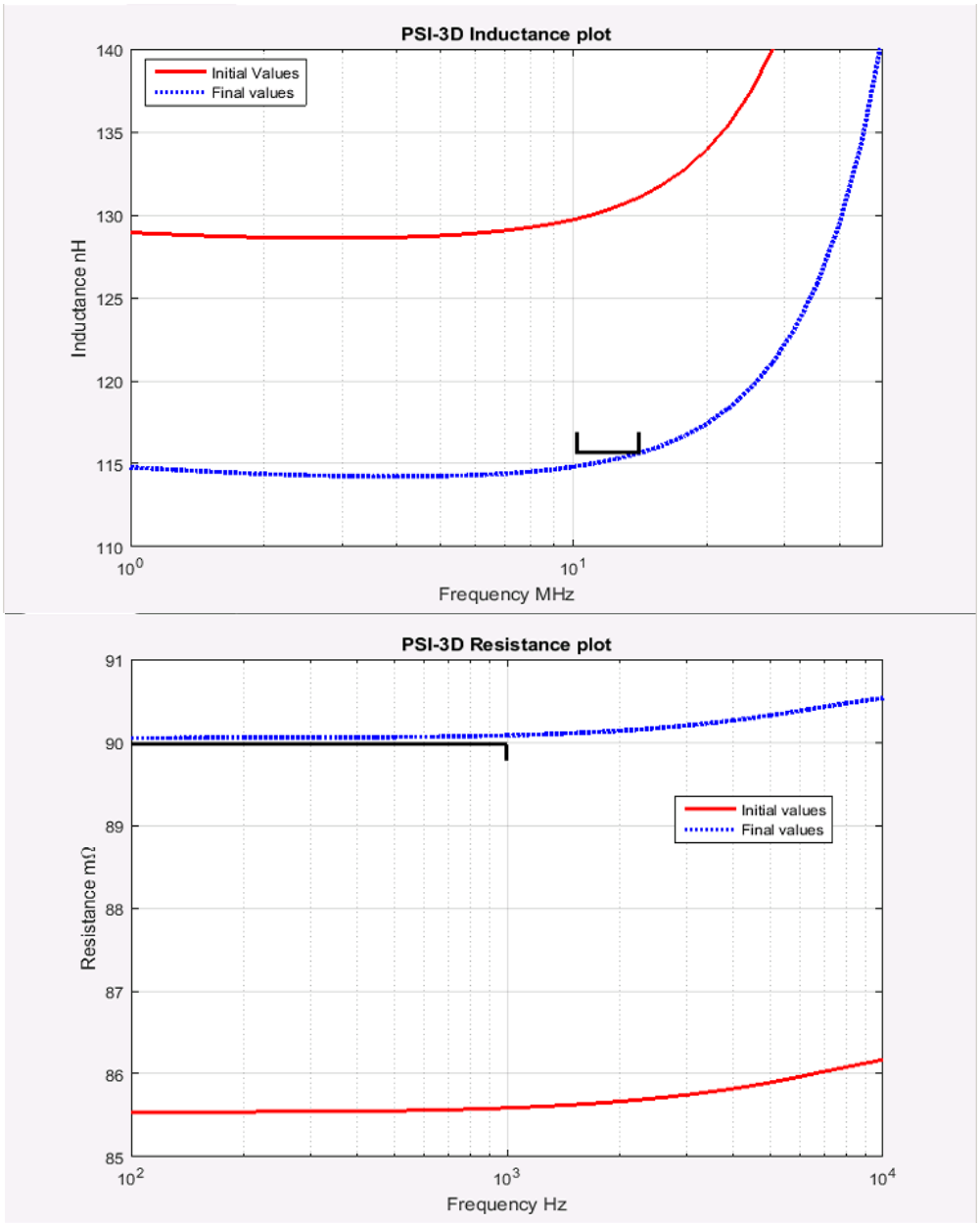


Fig. 3.14 Spiral inductor EM responses. $L_{AC}$ and $R_{AC}$ before (red) and after (dotted blue) optimization.

## 3.10. Conclusions

In this chapter, we applied a DoE-based methodology to analyze and optimize power delivery networks. DoE proved to be an effective technique to find the most significant factors for PD analysis and design, as well as to perform PDN optimization. Our simulations and physical laboratory measurements showed sufficiently good agreement for the optimized PDN. With this methodology, it is possible to reduce costs, since, from our physical platform implementation, it was possible to remove 29 % of the capacitors by finding a better VR's tuning recipe. As a future work, detailed DoE studies in the frequency domain would be desirable to ensure acceptable VR's stability criteria and bandwidth. Finally, more computationally efficient optimization techniques, such as those based on space mapping approaches, will be also addressed in future works to enhance our power delivery design process.

We also successfully tested our space mapping methodology by optimizing a spiral inductor structure in the 3D EM-FEM solver PowerSI®. To do that, we developed a driver to manipulate the 3D structure without the need of calling PowerSI® 3D GUI. Our optimization methodology was proved with the successful implementation of the aggressive space mapping method to fine tune the geometry of the spiral inductor structure using APLAC's equivalent circuit as our coarse model. The optimization achieved desired results for $L_{AC}$ and $R_{AC}$ in specific frequency ranges, with a few iterations of the fine model in PowerSI® 3D EM, while the coarse model required more than a hundred simulations to achieve the desired goal. As a future step, we will be looking for better matching of inductance and resistance along the whole frequency range by developing a surrogate spiral inductor-based model by means of neural networks or polynomial implementation.

# 4. Surrogate-based Analysis and Design Optimization of Power Delivery Networks

As microprocessor architectures continue to increase computing performance under low-energy consumption, the combination of SI, EMI, and PD is becoming crucial in the computer industry. In this context, power delivery engineers make use of complex and computationally expensive models that impose time-consuming industrial practices to reach an adequate power delivery design. In this chapter, we propose a general surrogate-based methodology for fast and reliable analysis and design optimization of PDNs. First, we formulate a generic surrogate model methodology exploiting passive lumped models optimized by parameter extraction to fit PDN impedance profiles. This PDN modeling formulation is illustrated with industrial laboratory measurements of a 4$^{th}$ generation server CPU motherboard. Next, we propose a black box PDN surrogate modeling methodology for efficient and reliable power delivery design optimization. To build our black box PDN surrogate, we compare four metamodeling techniques: support vector machines, polynomial surrogate modeling, generalized regression neural networks, and Kriging. The best resultant metamodel is then used to enable fast and accurate optimization of the PDN performance. Two examples validate our surrogate-based optimization approach: a voltage regulator with dual power rail remote sensing intended for communications and storage applications, by finding optimal sensing resistors and loading conditions; and a multiphase voltage regulator from a 6$^{th}$ generation Intel® server motherboard, by finding optimal compensation settings to reduce the number of bulk capacitors without losing CPU performance. This chapter revisits our work in [Leal-Romo-20].

## 4.1. An Introduction to Advanced Modeling and Optimization of Power Delivery Networks

As computer architectures continue to increase the number of cores while keeping frugal power consumption [Rupp-19], [Gonzalez-19], the combination of SI, EMI, and PD is becoming crucial in the industrial design of computer platforms to satisfy stringent performance requirements within time-to-market commitments. In this context, industry is paying more attention to PD by

emphasizing power integrity engineering to overcome cost and performance targets.

In a typical industrial PD analysis, a physical power delivery network is proposed for which a large and complex circuital model (SPICE-like network), including distributed passive components, is built. This circuital model is enabled to include detailed models for external decoupling capacitance aimed at compensating events of sudden change of load ($di/dt$), from the chip (CPU) up to the VR. These circuital models allow PI engineers to assess the performance of the PDN, for instance, by looking into the impedance profile [Swaminathan-04], [Altera-19], [Loo-06] for which specified target impedances are defined [Smith-99], [Kim-15]. In addition to the impedance profile, other performance metrics, such as voltage drop analyses, are needed to ensure the minimum voltage level of operation allowed by the VR and other components. Other metrics include simultaneous switching noise (SSN) [Ramdani-09], [Bharath-07], also known as ground bounce, voltage regulator's power losses [Kumar-15], [Tsygulev-17], plane current density for copper's reliability, etc.

PI engineers rely on several computer aided design (CAD) tools to design and characterize a PDN; they frequently employ 2.5-D and 3-D full-wave electromagnetic (EM) simulators to extract accurate circuital models able to emulate most intrinsic PDN parasitic effects. As mentioned before, these circuital models are typically implemented as large distributed SPICE networks representing the whole PDN [Bharath-07], [Goral-16], [Engin-07], [Zhao-18], whose simulation can last from a couple of minutes up to several hours or even days. To overcome this high computational cost, some approaches to speed up PDN network development and simulation have been proposed. Extraction of the PDN equivalent circuital model can be accelerated by using the partial element equivalent circuit (PEEC) method [Zhao-18], [Kim-14]. PDN metamodeling approaches for accurate package prediction of bump inductance is proposed in [Cao-19] by using design of experiments and machine learning techniques, *e.g.*, artificial neural networks (ANN), support vector machines (SVM), nonlinear regression, and combined ANN-piecewise-linear (PWL) modeling [Cao-19]. Efficient PDN Bayesian optimization is proposed in [Torun-18] to minimize clock skew and maximize voltage regulator's efficiency.

In this chapter, a general methodology for surrogate-based analysis and design optimization of power delivery networks is proposed. We first formulate a generic surrogate model methodology for accurate and fast prediction of PDN performance. Our modeling methodology exploits fast passive lumped models optimized by parameter extraction (PE) to fit PDN impedance

profile from industrial laboratory measurements. This is illustrated by modeling a PDN of a 4th generation Intel® Xeon® CPU server. Secondly, we propose a black box surrogate modeling approach for efficient and reliable PDN design optimization [Chavez-Hurtado-16], [Rangel-Patiño-17], [Koziel-13]. We compare several PDN metamodels, including support vector machines (SVM), polynomial surrogate modeling (PSM), generalized regression neural networks (GRNN), and Kriging. The end goal of these PDN metamodels is to enable accurate and fast optimization of PDN performance. We illustrate our metamodel-based design optimization approach by two examples: 1) a PDN with dual sensing voltage regulator for communications and storage applications, to find optimal sensing resistors and loading conditions; and 2) a PDN motherboard of a 6th generation Intel® Xeon® computer, to find optimal settings of a multiphase switching VR controller, reducing by 30 % the number of decoupling capacitors without losing CPU performance.

The rest of the chapter is organized as follows. Section 4.2 illustrates the development of PDN passive lumped models by fitting the impedance profile, intended to enable customers to efficiently build their customized PD board. Section 4.3 describes a generic formulation to develop PD black box surrogate models for enabling PDN performance assessment at a low computational cost. Section 4.4 illustrates an example to build a PD surrogate model of a dual sensing VR to come up with an optimized sense resistors' recipe and achieve the best power consumption without impacting silicon's threshold voltage. In Section 4.5, a second example is described by addressing components cost reduction of a 6th generation Intel® Xeon® CPU from motherboard and VR point of view. Finally, in Section 4.6, our conclusions are presented.

## 4.2. Surrogate Lumped Models by Parameter Extraction for Customized Analysis and Design

### 4.2.1 Custom PDN Design

Customers and vendors usually want to customize their own motherboard design to offer different CPU performance features or cheaper platform costs. CPU manufacturers can enable customers by providing a set of reference PD design guidelines, as well as coarse surrogate models to estimate impedance PDN. This is done with two goals: 1) to protect manufacturer's CPU and

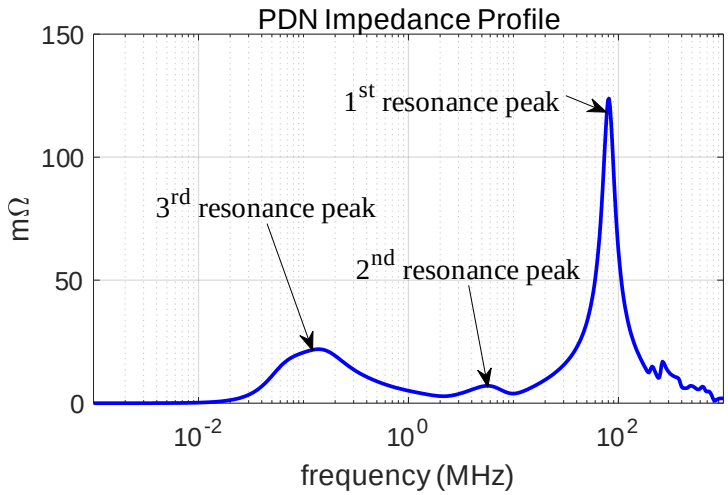


Fig. 4.1 Frequency domain analysis: a typical impedance profile showing PDN behavior from the VRM to the chip.

chipset intellectual property; and 2) to provide an easy way to simulate PD performance for further customers' analyses.

### 4.2.2 Surrogate Lumped Models for PDN Intellectual Property Protection

As mentioned before, the PDN impedance profile can be approximated by equivalent SPICE-like lumped models valid over a limited frequency band. A typical frequency response measured from a realistic PDN is illustrated in Fig. 4.1, where some frequency resonances caused by each decoupling state are shown.

A fast PDN lumped model can be implemented by a series of single-sided of resistor, inductor, and capacitor (RLC) sections with an ideal ground return path, as shown in Fig. 4.2. This lumped model approximation is built incrementally, where *N* corresponds to several RLC sections

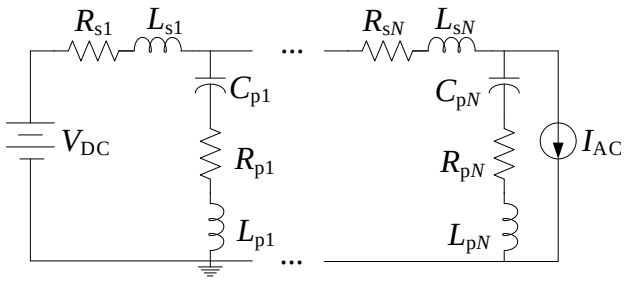


Fig. 4.2 Single-sided equivalent RLC lumped model with ideal ground connection to fit the impedance profile.

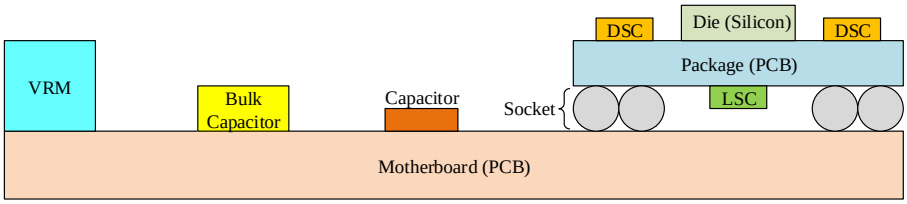


Fig. 4.3 Cross-sectional view of a PDN including different decoupling stages along the VR up to the die.

included, which mainly depends on the number of resonant points in the measured impedance profile. The series resistors ($R_{s1}$ … $R_{sN}$) account for the resistivity of copper from parallel power and ground layers. Series inductors ($L_{s1}$ … $L_{sN}$) are mainly associated to the vertical transitions of vias interconnecting layers as well as the distributed parasitic inductance of power and ground planes. Finally, parallel capacitances $C_{p1}$ … $C_{pN}$, along with their corresponding intrinsic parasitics $R_{p1}$ … $R_{pN}$ and $L_{p1}$ … $L_{pN}$, represent each capacitive decoupling stage placed along the entire PDN, from the VR to the chip (silicon). A simplified cross-sectional view of a typical PDN with different decoupling stages is shown in Fig. 4.3, where the path from the VRM to the chip is illustrated. As it is observed, the PDN is conformed of several components acting as decoupling stages to store energy until the VRM reacts. Some of the most decoupling stages are the die side capacitors (DSC), close to the chip for fast reaction. Next the land side capacitors (LSC), which act as a secondary reserve of energy, followed by the interconnection from the package to the motherboard with the socket, which typically is very resistive, and finally the last energy reserves implemented by decoupling and bulk capacitors.

### 4.2.3 Optimizing Surrogate Lumped Models by Parameter Extraction

Suitable parameter values for a given a number of RLC sections ($N$) in the proposed PDN lumped model (see Fig. 4.2) are determined by performing a curve fitting of the PDN impedance profile obtained from actual laboratory measurements. Laboratory measurements on the physical PDN were implemented with a voltage regulator test tool (VRTT) [Xu-13] and a frequency domain impedance measurement (FDIM) tool [Intel-19] that makes use of an interposer to emulate CPU loading conditions, as illustrated in Fig. 4.4. For the CPU, the PDN impedance profile was measured using an integrated power supply frequency domain impedance meter (iFDIM)

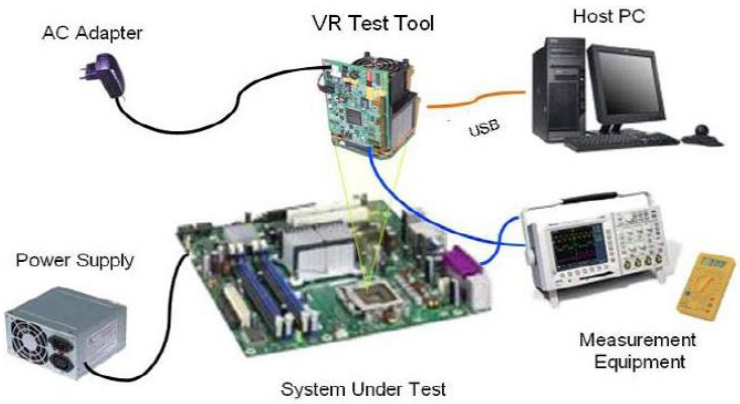


Fig. 4.4 Voltage regulator test tool (VRTT) to measure frequency and time-domain PDN and VR features. Taken from [Xu-13].

[Waizman-04]. After collecting the PDN impedance profile from the VRTT, we propose finding optimal surrogate lumped model parameter values by solving the following parameter extraction (PE) problem [Koziel-13]:

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} \left\| \boldsymbol{R}(\boldsymbol{x}) - \boldsymbol{R}^{\mathrm{t}} \right\|_2^2 \tag{4-1}$$

where optimization variables are $\boldsymbol{x} = [R_{\mathrm{s}1}\ \ L_{\mathrm{s}1}\ \ldots\ R_{\mathrm{s}N}\ \ L_{\mathrm{s}N}\ \ C_{\mathrm{p}1}\ \ R_{\mathrm{p}1}\ \ L_{\mathrm{p}1}\ \ldots\ C_{\mathrm{p}N}\ \ R_{\mathrm{p}N}\ \ L_{\mathrm{p}N}]^{\mathrm{T}} \in \Re^n$, with $n = 5N$, $\boldsymbol{x}^*$ contains the extracted optimal parameter values that make the lumped circuit response $\boldsymbol{R}(\boldsymbol{x}^*)$ as close as possible to the target response $\boldsymbol{R}^{\mathrm{t}} \in \Re^r$; in our case, $\boldsymbol{R}^{\mathrm{t}}$ contains the measured PDN impedance profile. Once $\boldsymbol{R}^{\mathrm{t}}$ is available, solving (4-1) is computationally very fast and can be repeated by gradually increasing $N$ until a good match is found at $\boldsymbol{x}^*$. To avoid being trapped in a weak local minimum after solving (4-1) [Bandler-99], [Rayas-Sánchez-16] for a given $N$, we select a physically meaningful starting point based on engineering expertise, and we perturb the starting point several times to make sure the PE solution is found.

### 4.2.4 PDN Lumped Model Parameters Extraction Example

To exemplify the usage of this technique, we measured the impedance profile of a 4th generation Intel® Xeon® CPU server. The SPICE lumped model uses the same topology as in Fig. 4.2, with $N = 8$ sections (a total of $n = 40$ optimization variables). The PDN impedance profile measured from 100 Hz to 7 MHz is shown in Fig. 4.5. This frequency range was selected considering the intended PDN application (motherboard). We solved (4-1) by using the trust-

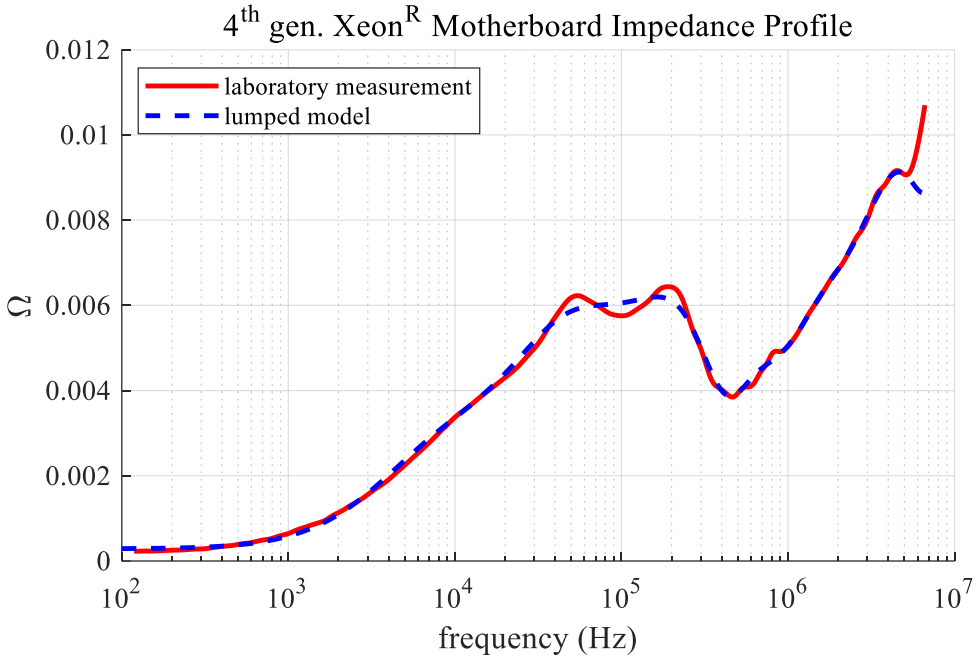


Fig. 4.5 Intel's 4th CPU generation motherboard's impedance profile comparison: equivalent lumped model (dashed line) *vs.* laboratory measurement (solid line).

region interior-point nonlinear optimization method available in MATLAB[7]. A comparison between the measured and surrogate lumped model impedance is also depicted in Fig. 4.5. It is observed that the lumped model closely follows the impedance profile up to 6 MHz, with a slight difference in the 30-200 kHz frequency range due to the circuit topology employed. The time to generate this optimized lumped model was 1 minute and 36 seconds on a laptop computer with 8 GB RAM and a 7th generation i5 processor.

## 4.3. A Methodology for Efficient and Accurate PDN Design Optimization

In contrast to using physics-based non-parameterized surrogate lumped models that emulate the PDN impedance profile for performance analysis, as described in the previous section, it is also possible to use PDN parameterized metamodels to optimize a PD design, as long as these metamodels have enough accuracy in the design region of interest. To obtain our PDN metamodels, we generate training and testing data within a desired design region and apply the

[7] MATLAB, Version R2010a, The MathWorks, Inc., 3 Apple Hill Drive, Natick MA 01760-2098, 2006.

corresponding metamodeling techniques. Then, we select the PDN metamodel with the best generalization performance and use it as a vehicle for direct PD design optimization. Our end goal is to accelerate the PD design process, by reducing the time that engineers spend on assessing several tradeoff scenarios during the PD design flow.

### 4.3.1 High Fidelity Simulation of Power Delivery Networks

Since most of the PDN building blocks are based on physical structures, engineers use CAD tools to predict the PD performance for specific power domains. Most of these CAD tools are either full wave EM simulators or quasi-static simulation tools. Some of the commercial tools most widely used in this area include ADS[8] (Momentum, Power EM, etc.), ANSYS[9] (HFSS, SIWave, etc.), Cadence[10] (PowerDC, PowerSI, etc.), CST[11], among others. They are in general, regarded as highly accurate, however, they are computational expensive given the complexity of the simulated structures. In this chapter, we will refer to them as fine models.

During the simulation stage, PD engineers typically assess the effects of changing, for instance, the voltage regulator bandwidth, the number of phases needed by the regulator, the copper thickness, etc., based on their expertise. Hence, these tradeoff scenarios imply a significant amount of time redoing fine model simulations, and therefore, there is a significant engineering cost to provide a robust PD solution.

### 4.3.2 PDN Surrogate Modeling Flow

We propose developing a computationally cheap but sufficiently accurate surrogate model of the PDN, which later can be used for fast parametric studies or for efficient direct design optimization. A simplified surrogate modelling flow is shown in Fig. 4.6. It essentially consists of the following steps:

1) Select a suitable PDN fine model (see Section 4.3.1), define the $n$ input design parameters ($\boldsymbol{x} \in \Re^n$) and the $r$ responses of interest ($\boldsymbol{R}_f \in \Re^r$).

[8] ADS – Advanced Design System, Keysight Technologies, Inc., 1400 Fountain Grove Pkwy, Santa Rosa, CA 95403-1738, USA, 2019.
[9] ANSYS Inc., Southpointe 2600 Ansys Dr., Canonsburg, PA 15317, USA, 2019.
[10] Cadence Design Systems, Inc., 2655 Seely Avenue, San Jose, CA 95134, USA, 2019.
[11] CST – Computer Simulation Technology AG, CST of America, LLC. Dassault Systemes, 175 Wyman St., Walman, MA 02451, USA., 2019.

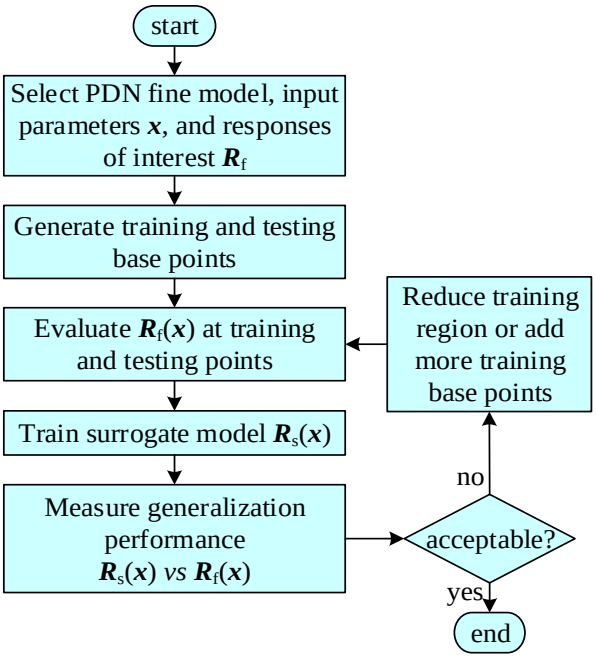


Fig. 4.6 Flow diagram to train a PDN surrogate model and test its generalization performance.

2) Generate training and testing data in the design space of interest. Given the high computational cost of each fine model simulation, frugal sets of data should be collected. We can exploit design of experiments techniques to improve coverage while keeping a small amount of fine model simulations. Among the most frugal distributions of points, the star and box distributions are preferred. The star distribution requires only $2n + 1$ training base points [Rayas-Sánchez-06], while the box distribution requires $2^n + 1$ training base points [Rayas-Sánchez-17]. Ideally, the star distribution should be used in all cases, however, in some cases the amount of learning data provided by the star distribution is not sufficient to develop a surrogate model with enough generalization accuracy in the region of interest, in which case a box distribution should be used. In cases where the computational cost of each high-fidelity simulation is not too high, a box distribution can be directly employed. Central composite design [Montgomery-12] can be exploited to define upper and lower limits, while the confusion technique with fractional factorial design [Montgomery-12] can further decrease the amount of training data in box distributions with high dimensionality. For testing, we use random points inside the training region, in the range of 20-25% of the total number of training data.

3) Train the PDN surrogate model $\boldsymbol{R}_s(\boldsymbol{x})$. Here we train several surrogate models with the available training data generated in the previous step. We use the following machine learning

approaches: support vector machines, polynomial surrogate modeling, generalized regression neural networks, and Kriging. These metamodeling techniques have the common characteristic of an easy regularization process, reducing the risks of over-training [Haykin-99]. They are briefly described in Section 4.3.3.

4) Test the PDN surrogate models. Here we test the generalization performance of the resultant surrogate models after training. This is done by measuring the relative error of each $\boldsymbol{R}_s(\boldsymbol{x})$ with respect to $\boldsymbol{R}_f(\boldsymbol{x})$ at all the random testing base points not seen during training.

5) Select the best PDN surrogate model. After measuring the testing errors of all the surrogate models trained, we select that one with the smallest maximum relative testing error. If the best generalization performance obtained is acceptable, we end the modeling flow. If not, we either reduce the region of interest and retrain the surrogate models or add more training data in the same region and retrain the surrogates (for cases where the training region size must be kept fixed).

Having available the best PDN surrogate model, with an acceptable generalization performance, we can optimize it to find the best PDN design, as described in Section 4.3.4.

### 4.3.3 Surrogate Modeling Techniques for Fast PDN Simulation

As mentioned before, we evaluated four different surrogate modeling techniques: polynomial surrogate modeling, generalized regression neural networks, support vector machines, and Kriging. A brief description of each technique follows.

Polynomial Surrogate Model (PSM). Polynomial functional surrogates have been efficiently exploited to approximate complex microwave structures [Rayas-Sánchez-10], even by enforcing low-order polynomials [Rayas-Sánchez-17]. Here we use the PSM formulation presented in [Chavez-Hurtado-16], where the multinomial theorem is exploited with automated regularization. It is in essence very similar to response surface models, although PSM is not limited to second order polynomials. The $m$-th order functional approximation used in scalar form (per frequency point) is

$$R_s^{(m)}(\boldsymbol{x}) = R_s^{(m-1)}(\boldsymbol{x}) + \boldsymbol{w}^{(m)\mathrm{T}}\boldsymbol{q}^{(m)}(\boldsymbol{x}) \tag{4-2}$$

where $R_s^{(m-1)}(\boldsymbol{x})$ is the previous $m-1$ order polynomial surrogate model function, $\boldsymbol{w}^{(m)}$ is the corresponding vector of weighting factors, and $\boldsymbol{q}^{(m)}(\boldsymbol{x}_f)$ contains the $m$-th order multinomial terms

[Chavez-Hurtado-16]. This technique exhibits good generalization performance when applied to relatively small training regions [Chavez-Hurtado-16].

Generalized Regression Neural Network (GRNN). GRNN is a special kind of ANN that does not require an iterative training procedure [Specht-91]. Its number of hidden neurons is equal to the amount of learning data [Specht-91]. As the number of learning samples becomes large, the GRNN exhibits a fast learning and convergence to the optimal regression surface [Panda-14]. GRNN uses a special type of radial basis functions as nonlinearity; for our purposes, we use GRNN default settings of the neural network toolbox available in MATLAB.

Support Vector Machines (SVM). While ANNs are trained using the empirical risk minimization principle, SVMs use the structural risk minimization, allowing them to obtain a good trade-off between model complexity and generalization performance [Tokan-08]. In order to find the optimal model parameters, the SVM technique solves a constrained quadratic optimization problem by exploiting the use of kernel functions [Xia-06], [Angiulli-07]. For our implementation, we use the SVM regression available in MATLAB with default linear kernel functions and sequential minimal optimization solver.

Kriging. Kriging is a type of kernel-based probabilistic model that is based on space-filling experiments aiming at covering the experimental area [Van-Beers-05]. Kriging minimizes the prediction variance by exploiting the best linear unbiased estimator (BLUE) of the output value for a given input [Van-Beers-05]. If there are not enough training samples, the predictions of the resultant Kriging models may become inaccurate [Van-Beers-05]. For our work, we use default settings of the algorithm as implemented in MATLAB by exploiting its Gaussian regression process.

Differences in generalization performance between the four previous surrogate modeling techniques mainly depend on the available learning base points, the size of the training region of interest, and the degree of nonlinearity of the approximated mapping. For a frugal amount of learning base points and a relatively small modeling region, PSM has proved to exhibit the best generalization performance [Chavez-Hurtado-16]. When enlarging the modeling region but keeping a frugal amount of learning base points, the best surrogate modeling technique varies depending on the response behavior for the system under study; if a large amount of learning base points are available, usually SVM, Kriging, and GRNN generalize better than PSM, regardless of the size of the modeling region [Chavez-Hurtado-16], [Rayas-Sánchez-10], [Panda-14]. In terms

of computational cost and algorithmic complexity, the four surrogate modeling approaches are very similar. We implement the four surrogate modeling techniques and select that one with the best generalization performance for each application.

All these metamodeling techniques suffer from a limited accuracy that essentially depends on the amount of data available within a given training region. The more training data is available in a broad region, the highest the accuracy (and complexity) of the resultant surrogate models (provided they are properly trained). However, the computational cost of the proposed methodology can be severely increased if too many training and testing samples are generated, mainly due to the high computational cost of each high-fidelity simulation, but also due to the increased training time of a more complex surrogate. That tradeoff motivates our aim of developing a computationally inexpensive but sufficiently accurate surrogate model of the PDN.

### 4.3.4 PDN Surrogate-Based Optimization

Once the metamodels are developed, the next step is to select the best one and use it for direct optimization to fulfill PDN performance specifications. A flow diagram showing the proposed optimization methodology is shown in Fig. 4.7, which essentially consists of the following steps:

1) Select the best PDN surrogate model according to their generalization performance.

2) Set PDN surrogate model input variables ($\boldsymbol{x}$) as well as its constant pre-assigned input parameters $\boldsymbol{z}$ and independent variables $\boldsymbol{\psi}$, if any.

3) Define PDN performance specifications. Regularly, the PDN specifications fall in the category of dc resistance ($R_{dc}$), also called as R-path, minimum functional threshold voltage ($V_{min}$), maximum voltage ($V_{max}$) allowed for functional reliability, target impedance ($Z_t$), peak to peak voltage noise ($V_{p2p}$), power consumption ($P_D$), power loss ($P_{loss}$), etc.

4) Set an initial design $\boldsymbol{x}^{(0)}$ to start the optimization algorithm. Usually, this seed is determined from PD engineer's expertise.

5) Formulate the objective function $U(\boldsymbol{x})$ to solve the following constrained minimax optimization problem:

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} U(\boldsymbol{x}) \tag{4-3}$$

$$U(\boldsymbol{x}) = \max\{\ldots e_k(\boldsymbol{x})\ldots\} \tag{4-4}$$

subject to

$$\boldsymbol{x}^{\text{lb}} \le \boldsymbol{x} \le \boldsymbol{x}^{\text{ub}} \tag{4-5}$$

where $\boldsymbol{x}^*$ is the optimal design found, $\boldsymbol{x}^{\text{lb}}$ and $\boldsymbol{x}^{\text{ub}}$ are the lower and upper limits of the input variables $\boldsymbol{x}$, respectively, and $e_k(\boldsymbol{x})$ is the $k$-th error function defined as:

$$e_k(\boldsymbol{x}) = \begin{cases} \dfrac{R_k(\boldsymbol{x})}{S_k^{\text{ub}}} - 1 & \text{for all } k \in I^{\text{ub}} \\ 1 - \dfrac{R_k(\boldsymbol{x})}{S_k^{\text{lb}}} & \text{for all } k \in I^{\text{lb}} \end{cases} \tag{4-6}$$

where $R_k(\boldsymbol{x})$ is the $k$-th model response at point $\boldsymbol{x}$, $S_k^{\text{ub}}$ and $S_k^{\text{lb}}$ are the upper and lower bound specifications ($\neq 0$), and $I^{\text{ub}}$ and $I^{\text{lb}}$ are the corresponding index sets.

6) Check if the optimum response $\boldsymbol{R}(\boldsymbol{x}^*)$ complies with the required performance specifications. For this assessment, two conditions can occur: a) $U(\boldsymbol{x}^*) < 0$, which implies the optimal solution found satisfies all the performance specifications, ending the algorithm; b) $U(\boldsymbol{x}^*) \ge 0$, which implies that at least one of the performance specifications is violated. If the second condition is found, it might be due to a local minimum, in which case we change the starting point and optimize again the surrogate model. If it is not a local minimum, then the PDN performance

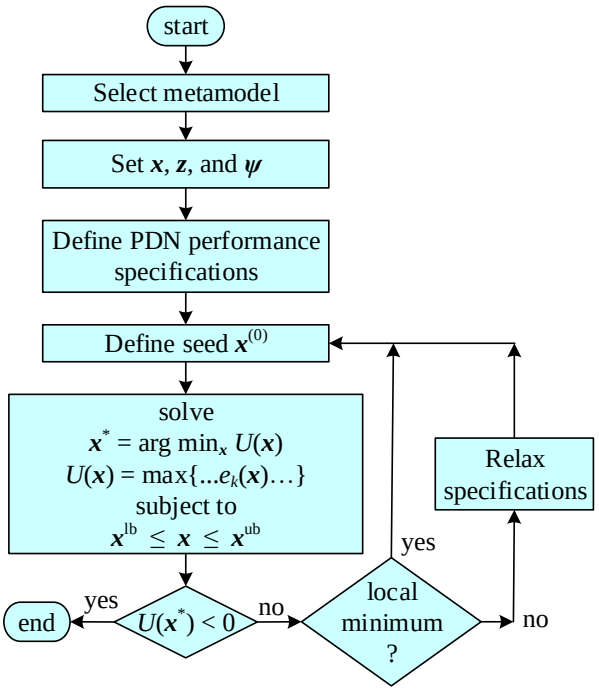


Fig. 4.7 Flow diagram for direct constrained design optimization of the PDN metamodel.

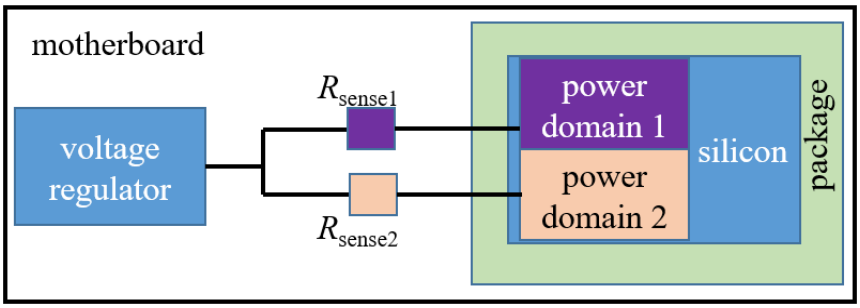


Fig. 4.8 PDN with a single voltage regulator and two remote sense resistors for two different power domains at silicon level. Taken from [Leal-Romo-18a].

specifications might be too demanding, in which case we relax them and re-optimize the surrogate (see Fig. 4.7).

## 4.4. Example I: PDN Optimization for Dual Sensing Voltage Regulator

Consider the monolithic CPU processor proposed in [Leal-Romo-18a], which consists of two power domains sharing a single VR using a dual sensing scheme, as shown in Fig. 4.8. Each power domain has its own individual minimum voltages (contained in vector $\boldsymbol{V}_{min} \in \Re^2$) and power consumptions ($\boldsymbol{P}_D \in \Re^2$) specifications. By varying the sense resistors ($\boldsymbol{R}_{sense} \in \Re^2$) and limiting the maximum current of each power domain ($\boldsymbol{I}_{max} \in \Re^2$), the purpose of the optimization problem is to ensure the best performance of the circuitry while reducing the power consumed from both power domains. Our PDN fine model was simulated with Synopsys®-HSPICE[12], where each simulation took an average of 5 minutes using a laptop computer with 8 GB RAM and a 7th generation i5 core processor. The design variables are $\boldsymbol{x} = [R_{sense1} \;\; R_{sense2} \;\; I_{max1} \;\; I_{max2}]^T \in \Re^4$ and the system responses are $\boldsymbol{R}(\boldsymbol{x}) = [P_{D1} \;\; P_{D2} \;\; V_{min1} \;\; V_{min2}]^T \in \Re^4$.

### 4.4.1 Training and Testing Data Generation

Training data was generated using a box distribution exploiting CCD and FFD techniques using 2 central points, resulting in 28 training base points. For generalization measurement, we

[12] Hspui for Windows, G-2012.06, Synopsys®, 690 East Middlefield Road, Mountain View, CA 94043.

simulated 6 random testing points within the design region of interest, which was delimited by the following lower and upper bounds: 15 Ω to 85 Ω for $R_{sense1}$ and $R_{sense2}$; 0.9 A to 2.2 A for $I_{max1}$; and 12 A to 28 A for $I_{max2}$. In addition, we normalized all the input data to train the surrogate models. The entire process of generating and collecting the training and testing data took 2.83 hours.

### 4.4.2 Surrogate Modeling

Four different surrogate modeling techniques were–implemented by using the above training data: PSM, Kriging, GRNN, and SVM. The corresponding training errors are shown in Table 4.1. By using the testing data, the corresponding generalization errors are shown in Table 4.2. From these results, it is observed that in this case the Kriging surrogate model exhibits the overall best training and generalization performance, selecting it to perform the direct optimization procedure.

### 4.4.3 Surrogate-based Optimization

After making a fast design space exploration with the available surrogate, as described in [Gonzalez-Soto-19], we use the following performance specifications:

a) Maximum transient power for $P_{D1}$, $P_{D1lim}$ = 2.86 W
b) Maximum transient power for $P_{D2}$, $P_{D2lim}$ = 36.45 W
c) Minimum transient voltage for $V_{min1}$, $V_{min1lim}$ = 0.71 V
d) Minimum transient voltage for $V_{min2}$, $V_{min2lim}$ = 0.70 V.

By using the Kriging surrogate model, we performed its direct optimization using a starting

TABLE 4.1. SUMMARY OF RELATIVE TRAINING ERRORS (%) USING DIFFERENT SURROGATE MODELS FOR TWO POWER DOMAINS

| Output | $E_{RGRNN}$ | $E_{RPSM}$ | $E_{RSVM}$ | $E_{RKriging}$ |
|---|---|---|---|---|
| $P_{D1}$ | 46.59 | 18.40 | 18.92 | 18.05 |
| $P_{D2}$ | 47.97 | 2.03 | 6.34 | 1.160 |
| $V_{min1}$ | 35.81 | 28.91 | 13.08 | 11.26 |
| $V_{min2}$ | 37.02 | 43.30 | 7.25 | 6.22 |

TABLE 4.2. SUMMARY OF RELATIVE TESTING ERRORS (%) USING DIFFERENT SURROGATE MODELS FOR TWO POWER DOMAINS

| Output | $E_{\text{RGRNN}}$ | $E_{\text{RPSM}}$ | $E_{\text{RSVM}}$ | $E_{\text{RKriging}}$ |
|---|---|---|---|---|
| $P_{\text{D1}}$ | 44.32 | 10.46 | 9.45 | 13.44 |
| $P_{\text{D2}}$ | 35.04 | 3.90 | 4.63 | 3.47 |
| $V_{\text{min1}}$ | 38.70 | 32.72 | 25.10 | 23.40 |
| $V_{\text{min2}}$ | 50.54 | 36.15 | 20.78 | 19.42 |

point $\boldsymbol{x}^{(0)} = [50 \quad 50 \quad 1.55 \quad 20]^{\text{T}}$. The corresponding initial system response is $\boldsymbol{R}_{\text{s}}(\boldsymbol{x}^{(0)}) = [1.6368 \quad 19.6409 \quad 0.710 \quad 0.691]^{\text{T}}$ which yields an objective function value $U(\boldsymbol{x}^{(0)}) = 0.0143$. By using the Nelder-Mead optimization algorithm available in MATLAB, the optimal design was found after 26 iterations and 136 surrogate model evaluations and corresponds to $\boldsymbol{x}^{*} = [50 \quad 49.97 \quad 0.8099 \quad 7.6522]^{\text{T}}$. The corresponding surrogate system response is $\boldsymbol{R}_{\text{s}}(\boldsymbol{x}^{*}) = [1.6168 \quad 19.9141 \quad 0.721 \quad 0.703]^{\text{T}}$, which leads to a surrogate objective function $U(\boldsymbol{R}_{\text{s}}(\boldsymbol{x}^{*})) = -0.0043$. The corresponding system fine response for the optimal metamodel design is $\boldsymbol{R}_{\text{f}}(\boldsymbol{x}^{*}) = [1.62 \quad 19.91 \quad 0.721 \quad 0.704]^{\text{T}}$ yielding a fine model objective function $U(\boldsymbol{R}_{\text{f}}(\boldsymbol{x}^{*})) = -0.0043$.

According to these results, the surrogate optimal designs resulted in a fine model that achieves the desired specifications. A total of 35 system simulations were required (34 for collecting training and testing data and one simulation to test the optimal design), instead of the hundreds of fine models system evaluations that a direct optimization methodology could require, speeding up the system design process.

## 4.5. Example II: Capacitors Reduction Adjusting Voltage Regulator's PID Compensation

Now consider a motherboard of a 6th generation Intel® Xeon® server. The compensation parameters of a multiphase VR controller are included in the design variables to optimize the motherboard performance, as discussed in [Xu-14] and [Singh-16]. The VR controller is simulated with SIMetrix/SIMPLIS[13], including the PDN parasitics and the VRTT interposer, as mentioned in [Xu-14] and illustrated in Fig. 4.9.

[13] SIMetrix/Simplis 7.20e (x64), Copyright © 2014 Simplis Technologies Ltd, 78 Chapel Street, Thatcham, Berkshire, RG18 4QN, UK, http://www.simetrix.co.uk/site/index.html

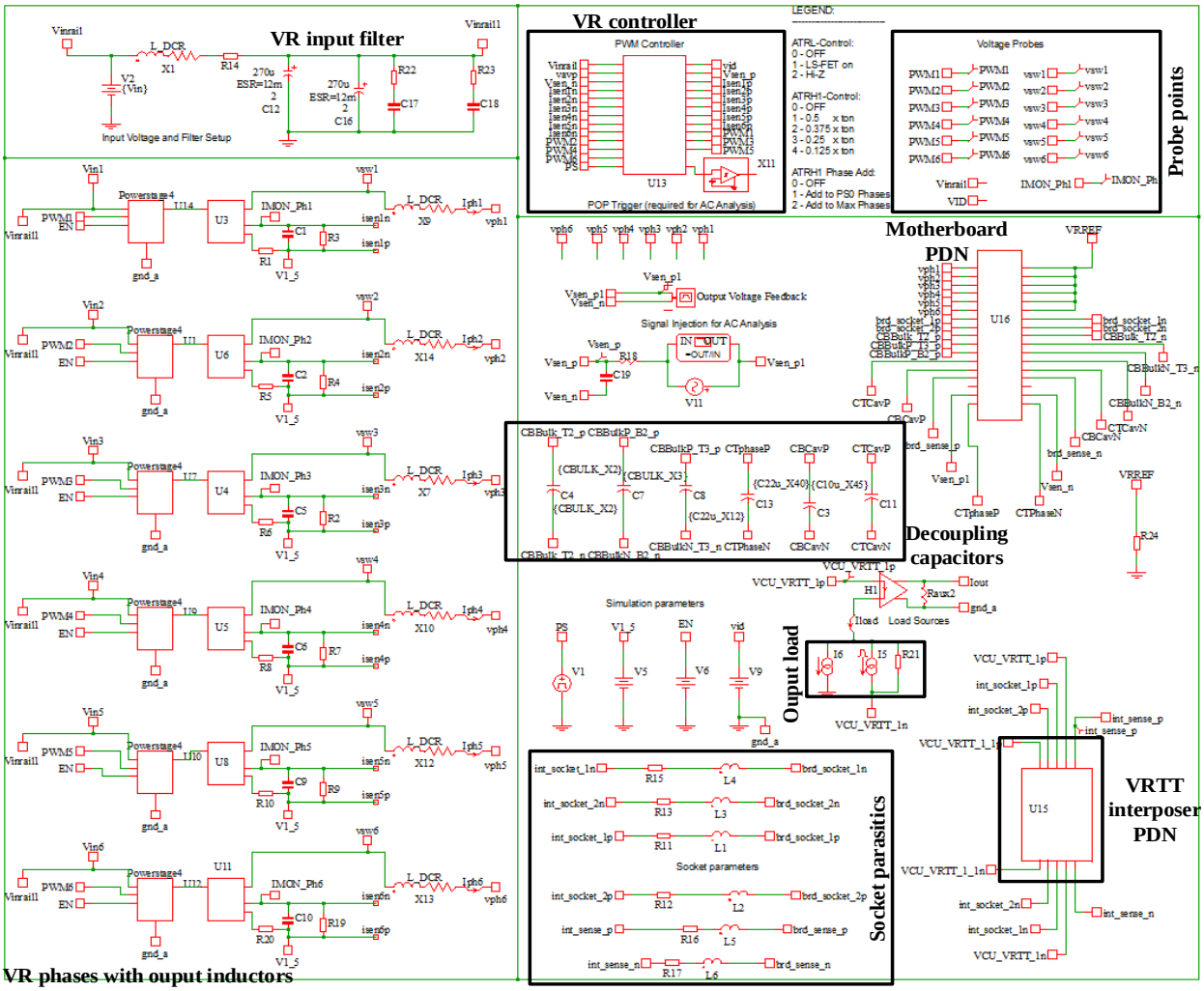


Fig. 4.9 SIMPLIS schematic of a multiphase VR controller including output inductors and all decoupling capacitors, as well as a 6th generation Xeon® CPU board and VRTT interposer parasites PD model.

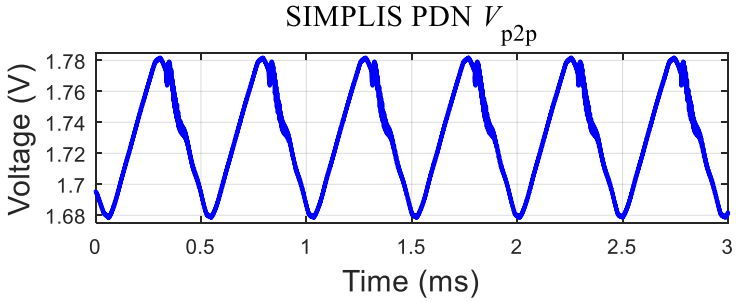


Fig. 4.10 SIMPLIS time domain simulation from 0 to 3 ms. In this case, $V_{max}$ = 1.78 V, $V_{min}$ = 1.68V, and peak to peak ripple noise is $V_{p2p}$ = 101.73 mV, measured under a specific slew rate scenario.

The VR controller with its PID compensation parameters ($k_p$, $k_d$, $k_i$) and the number of bulk

capacitors ($N_{Cblk}$) from the motherboard were selected as design variables, $\boldsymbol{x} = [k_d \;\; k_p \;\; k_i \;\; N_{Cblk}]^T \in \Re^4$. The responses of interest correspond to the maximum transient voltage $V_{max}$ and the minimum transient voltage $V_{min}$, represented as $\boldsymbol{R}(\boldsymbol{x}) = [V_{max} \;\; V_{min}]^T \in \Re^2$. Fig. 4.10 illustrates a typical transient waveform, where $V_{max}$ is measured as the maximum peak voltage and $V_{min}$ is measured as the lowest valley, both occurring during a 3 ms time window.

### 4.5.1 Training and Testing Data Generation

Training data was generated using a star distribution, resulting in 9 training points. For generalization measurement, 3 random testing points were generated. The design region was constrained by the following lower and upper bounds: 100 to 250 for $k_p$ and $k_i$; 250 to 450 for $k_d$; and 3 to 7 for $N_{Cblk}$. For training purposes, input data was normalized. Collecting this set of data from simulations took approximately 48 hours.

### 4.5.2 Surrogate Modeling

Once again, four different surrogate modeling techniques were implemented: PSM, Kriging, GRNN, and SVM. A summary of the resulting training and testing (generalization) errors are shown in Table 4.3 and Table 4.4, respectively. From these results, it is observed that the Kriging model exhibits the best generalization performance, selecting it as the PDN metamodel to perform direct optimization.

TABLE 4.3. SUMMARY OF RELATIVE TRAINING ERRORS (%) USING DIFFERENT SURROGATE MODELS FOR PDN

| Output | $E_{RGRNN}$ | $E_{RPSM}$ | $E_{RSVM}$ | $E_{RKriging}$ |
|---|---|---|---|---|
| $V_{max}$ | 0.81 | 8.21 | 0.88 | 0.66 |
| $V_{min}$ | 0.71 | 8.97 | 0.76 | 0.01 |

TABLE 4.4. SUMMARY OF RELATIVE TESTING ERRORS (%) USING DIFFERENT SURROGATE MODELS FOR PDN

| Output | $E_{RGRNN}$ | $E_{RPSM}$ | $E_{RSVM}$ | $E_{RKriging}$ |
|---|---|---|---|---|
| $V_{max}$ | 4.53 | 18.16 | 4.75 | 4.52 |
| $V_{min}$ | 4.12 | 17.86 | 4.27 | 3.96 |

### 4.5.3 Surrogate-based Optimization

The desired performance specifications are:

a) Lower bound for min. transient voltage, $V^{lb}_{min} = 1.65$ V
b) Upper bound for max. transient voltage, $V^{ub}_{max} = 1.85$ V
c) Peak to peak noise ripple, $V_{p2p} \leq 200$ mV.

For the surrogate-based optimization we used the initial design $\boldsymbol{x}^{(0)} = [175\ 350\ 175\ 5]^T$, which yields an initial surrogate system response $\boldsymbol{R}_s(\boldsymbol{x}^{(0)}) = [1.8270\ \ 1.6560]^T$ and an initial surrogate objective function value $U(\boldsymbol{R}_s(\boldsymbol{x}^{(0)})) = 0.0148$. By using the Nelder-Mead algorithm, the optimal design was found after 20 iterations and 105 surrogate model evaluations and corresponds to $\boldsymbol{x}^* = [162.7846\ \ 350.3494\ \ 189.9643\ \ 5]^T$. The optimal surrogate system response is $\boldsymbol{R}_s(\boldsymbol{x}^*) = [1.7810\ \ 1.6761]^T$ which leads to an optimal surrogate objective function $U(\boldsymbol{R}_s(\boldsymbol{x}^*)) = -0.01067$. The fine model system response at the optimal surrogate design is $\boldsymbol{R}_f(\boldsymbol{x}^*) = [1.782\ \ 1.678]^T$, yielding a fine model objective function $U(\boldsymbol{R}_f(\boldsymbol{x}^*)) = -0.0101$. These results confirm that the proposed methodology can be exploited to substantially speed up the design process by reducing the amount of fine model system simulations, finding an optimal design that achieves the performance specifications. The whole process required 13 system fine model simulations (12 for collecting training and testing data, plus one simulation to test the optimal design), instead of the hundreds of fine model evaluations that a direct optimization methodology could require. The engineer's expertise is used to define the metamodel design region as well as a suitable starting point. Once the metamodel is developed, the optimization process is conducted automatically with the proposed methodology, allowing engineers to focus their efforts on other aspects of the system design.

## 4.6. Conclusions

We described a general methodology for surrogate-based analysis and design optimization of power delivery networks. First, we proposed a formulation for accurate and fast prediction of PDN performance by exploiting passive lumped models optimized by parameter extraction to fit PDN impedance profiles obtained from industrial laboratory measurements. This formulation allows protecting chip makers intellectual property. Next, we proposed a metamodeling approach

for efficient and reliable PDN design optimization exploiting support vector machines, polynomial surrogate modeling, generalized regression neural networks, and Kriging. Our methodology allows accurate and fast optimization of PDN performance. Realistic industrial cases illustrate our general PDN analysis and design optimization methodology.

# General Conclusions

Cloud data center owners are very interested in pushing for higher CPU's operational frequency, while at the same time, there is not a significant increment of heat and power dissipation. Then, power delivery (PD) engineers need to focus on robust and cheaper power delivery designs in a very compressed time to market (TTM) product development schedule. Taking advantage of the design of experiments (DoE), surrogate-based modeling and optimization techniques, this doctoral dissertation proposed various methodologies to enhance power delivery designs in response to the data centers' demand.

As reviewed in Chapter 1, cloud computing nowadays is an attractive business model, enabling end-users with many opportunities, such as platform as a service (PaaS), software as a service (SaaS), etc. However, for the owners of the data centers, cloud computing becomes challenging in terms of the total operational cost and environmental impact, becoming crucial to decrease power consumption and minimize environmental carbon footprint contribution. For those reasons, data center owners are pushing very hard for robust CPU and platform power-thermal design solutions to find a sweet spot of power consumption vs. performance per watt. It is essential to highlight that as transistor technologies shrink and operational voltage goes lower, there is more leakage current dissipated by the transistors. Hence, it is more difficult to control power losses at the whole system level in modern nanometric semiconductor technologies.

In Chapter 2 of this dissertation, there is an overview of the most fundamental concepts and basic terminologies related to power integrity (PI) and power delivery (PD) design. Chapter 2 starts by describing a power delivery network (PDN), as a set of passive parasites that degrades the channel of the voltage traveling from the voltage regulator (VR) up to chip's buffers (die). Because of this voltage degradation in the PDN, some undesired effects in the performance might appear, such as jitter noise, reliability degradation of the chip, heat dissipation, electromigration, etc. It is essential to work over some power delivery performance metrics to ensure the chip's adequate performance, to avoid incurring in high-cost adders to the PDN, such as copper or decoupling capacitors. A target impedance defines a fundamental specification that is dependent on the maximum current supported by the power rail, the voltage at which the power rail operates, and the ripple supported by the voltage regulator. In consequence, the impedance profile should

be as flat as possible across a wide frequency range, from a few Hz to a few GHz. In addition to having an optimally flat impedance profile, another specification of performance to look at for PD engineers is in the time-domain space. PD engineers must check for voltage droops along the PDN due to a sudden CPU workload change event, to meet the minimum and maximum voltage specifications while achieving the highest efficiency of the voltage regulator to dissipate less heat.

Since power delivery is a tradeoff analysis process, its analysis is very dependent on the engineer's expertise, implying a significant effort to model the PDN aided by several CAD tools, such as 2.5-D and 3-D full-wave EM simulators to extract the parasites of the PDN. Later, these PDN parasites are incorporated into an equivalent distributed circuit model simulated in SPICE to assess the network's behavior. An important drawback of this type of assessment is that it usually consumes many computational resources and very long times due to several iterations to provide adequate design guidelines. Thus, in Chapter 3, it is exercised the usage of optimization techniques, including DoE approaches, on an Intel® Xeon® platform, using a screening technique to identify the main variables that have more contribution to the network. Once engineers identify variables with the highest weight, they use them for further cost reduction efforts by decreasing the number of decoupling capacitors utilizing an optimal VR compensation recipe. Additionally, Chapter 3 exemplifies the implementation of an aggressive space mapping (ASM) technique to optimize the dimensions of a spiral power inductor to meet desired resistive and inductive parasites. The end goal of this last optimization technique is to reduce as much as possible the use of the computationally expensive full-wave EM solver.

Finally, Chapter 4 focuses on the development and usage of surrogate modeling and surrogate-based optimization techniques to speed up PD analysis and design. The focus is to significantly reduce the time spent in performing typical tradeoff analyses, implementing a generic minimax formulation applied to several examples. The first example enabled data center customers to develop their motherboard through a PDN lumped model with a parameter extraction (PE) algorithm. The second example compared the performance of different surrogate-based modeling techniques to obtain the correct behavior of a dual sensing voltage regulator for a server communications application. Once the best surrogate model is identified, it is used as part of an optimization flow to get the best PDN recipe. To test a broader application of this technique, we approached a third example by minimizing the number of decoupling components while optimizing the VR compensation recipe for the same Xeon® platform evaluated in Chapter 2,

achieving similar results as those with the DoE technique previously implemented.

In summary, this doctoral dissertation contributed to the state or the art in this field by proposing a general methodology for surrogate-based analysis and design optimization of PDN. This contribution includes the proposal of a formulation for accurate and fast prediction of PDN performance by exploiting passive lumped models optimized by means of parameter extraction to fit PDN's impedance profile obtained from industrial laboratory measurements. Finally, it also contributed by a novel development of a surrogate-based approach for efficient and reliable PDN design optimization exploiting some surrogate-based techniques such as SVM, PSM, GRNN, and Kriging.

This doctoral dissertation puts into perspective more work left to do in the future. One field of future research would be to explore Bayesian and other similar optimization methods for PD's load balancing and VR tuning with different non-linear compensation parameters. Another relevant and interesting future research line consists of incorporating PDN multi-physics models and their interactions to consider power-thermal co-simulation optimization, as well as coupled thermo-mechanical and electromagnetic surrogate models as the basis for highly accurate PD design optimization. An additional future research line could be directed towards predictability of PD and VR laboratory measurements through surrogate-based models, especially for large regions in the parameter space. The end goal of these possible future research lines is to enhance the server's PD design for cloud computing applications and reduce the data center operational cost and its inherent environmental impact.

# Conclusiones Generales

Los propietarios de centros de datos de la nube están muy interesados en presionar por mayores frecuencias de operación en el CPU, mientras que, al mismo tiempo, no se dé un incremento significativo de disipación de calor y energía. Entonces, los ingenieros de entrega de potencia (EP) deben enfocarse en diseños de redes de distribución de potencia robustos y más baratos con tiempos de desarrollo de productos para su comercialización más acotados. Aprovechando el diseño de experimentos (DoE, por sus siglas en inglés), así como el modelado sustituto y algunas técnicas avanzadas de optimización, esta disertación doctoral propuso varias metodologías para mejorar los diseños de redes de distribución de potencia en respuesta a las demandas de los centros de datos anteriormente mencionadas.

Como se revisó en el Capítulo 1, el cómputo en la nube hoy en día es un modelo de negocio muy atractivo que brinda a los usuarios finales muchas oportunidades, como lo son los conceptos de plataforma como servicio, software como servicio, etc. Sin embargo, para los propietarios de los centros de datos, el cómputo en la nube se convierte en un desafío en términos del costo operativo total, así como del impacto ambiental, lo cual es crucial para disminuir el consumo de energía y minimizar la contribución de la huella de carbono al ambiente. Por estas razones, los propietarios de los centros de datos presionan mucho para que las soluciones de diseño térmico del CPU y de las plataformas de cómputo sean muy robustas para encontrar un punto óptimo en desempeño consumo de energía *vs*. rendimiento por watt. Es de importancia el resaltar que a medida que las tecnologías de transistores se reducen y el voltaje de operación disminuye, los transistores disipan más la corriente de fuga. Por lo tanto, es más difícil controlar las pérdidas de energía a nivel de todo el sistema para las tecnologías nanométricas de los actuales semiconductores.

En el Capítulo 2 de esta tesis, se hizo una descripción general de los conceptos más fundamentales y las terminologías básicas relacionadas con la integridad de potencia (PI, por sus siglas en inglés) y el diseño de la entrega de potencia (EP). El Capítulo 2 comienza describiendo una red de suministro o de distribución de potencia (PDN, por sus siglas en inglés), como un conjunto de múltiples parásitos pasivos que degradan el canal por el cual viaja el voltaje desde el regulador de voltaje (RV) hasta las compuertas del silicio (o dado). Debido a esta degradación del

voltaje en la red, pueden aparecer o exacerbarse algunos efectos no deseados en el desempeño, tales como el ruido de desplazamiento en tiempo (*jitter*), degradación de la confiabilidad del chip, disipación de calor, electromigración, etc. Por eso, es esencial trabajar sobre algunas métricas de rendimiento de entrega de potencia que aseguren el rendimiento adecuado del chip, evitando así el incurrir en adiciones de alto costo para la PDN, como son el uso adicional de cobre o de capacitores de desacoplamiento. El perfil de impedancia de una PDN se considera como una especificación fundamental que depende de la corriente máxima soportada por el riel de alimentación, el voltaje al que opera el riel de alimentación y el nivel de rizo soportado por el regulador de voltaje. En consecuencia, el perfil de impedancia debería ser lo más plano posible en un rango amplio de frecuencias, desde unos cuantos Hz hasta unos pocos GHz. Además de tener un perfil óptimo de impedancia, otra especificación de desempeño a tener en cuenta para los ingenieros de EP está en el dominio del tiempo en régimen transitorio. Los ingenieros de EP deben verificar si hay caídas de voltaje a lo largo del PDN debido a un evento repentino de cambio en la carga de trabajo del CPU, para cumplir con las especificaciones de voltaje mínimo y máximo mientras se logra la mayor eficiencia del regulador de voltaje para disipar menos calor.

Dado que la entrega de potencia es un proceso de análisis de decisión del desempeño *vs*. costo, su análisis depende mucho de la experiencia del ingeniero, lo que implica un esfuerzo significativo para modelar la PDN con la ayuda de varias herramientas de CAD, como lo son los simuladores 2.5-D y 3-D electromagnéticos de onda completa para extraer los componentes parásitos de la PDN. Posteriormente, estos parásitos de la PDN se incorporan a un circuito equivalente de parámetros distribuidos que se simula en SPICE para evaluar el comportamiento de la red. Un inconveniente importante de este tipo de evaluación es que generalmente consume muchos recursos computacionales y tiempos muy largos, debido a la necesidad de varias iteraciones para proporcionar pautas de diseño adecuadas. Por lo tanto, en el Capítulo 3, se usaron algunas técnicas de optimización, asistidas mediante el DoE, para una plataforma Intel® Xeon®, utilizando una técnica de detección para identificar las principales variables que tienen mayor contribución en la red de distribución de potencia. Una vez que los ingenieros identifican dichas las variables de alto impacto, las usan para reducir costos al disminuir la cantidad de capacitores de desacoplamiento mediante una receta de compensación del RV óptima. Además, el Capítulo 3 ejemplificó la implementación de una técnica de mapeo espacial agresivo (ASM, por sus siglas en inglés) que optimiza las dimensiones de un inductor espiral de potencia para cumplir con los

requerimientos de parásitos resistivos e inductivos deseados. El objetivo final de esta última técnica de optimización es reducir al máximo el uso del simulador EM de onda completa que es muy costoso computacionalmente hablando.

Finalmente, el Capítulo 4 se enfoca en el desarrollo y aplicación del modelado sustituto y de las técnicas de optimización basadas en modelo sustitutos para acelerar el análisis y diseño de las redes de distribución de potencia. El objetivo es reducir significativamente el tiempo empleado a realizar análisis de costo-beneficio típicos, implementando una formulación minimax genérica aplicada a varios ejemplos. El primer ejemplo permite a los clientes de centros de datos desarrollar su propia tarjeta madre a través de un modelo equivalente de parámetros concentrados de la PDN mediante un algoritmo de extracción de parámetros. El segundo ejemplo compara el rendimiento de diferentes técnicas de modelado sustituto para obtener el mejor comportamiento de un regulador de voltaje con doble sensor para una aplicación de servidor de comunicaciones. Una vez que se identifica el mejor modelo sustituto, se usa como parte de un flujo de optimización para obtener la mejor receta de la PDN. Para probar una aplicación más amplia de esta técnica, abordamos un tercer ejemplo minimizando el número de componentes de desacoplamiento mientras optimizamos la receta de compensación del RV para la misma plataforma Xeon® evaluada en el Capítulo 2, logrando resultados similares a aquellos con la técnica DoE previamente implementada.

En resumen, esta tesis doctoral contribuyó al estado del arte de este campo en particular proponiendo una metodología general para el análisis basado en modelos sustitutos para la optimización del diseño de PDNs. Esta contribución incluye la propuesta de una formulación para una predicción más precisa y rápida del desempeño de una PDN por medio de la explotación de modelos parámetros concentrados pasivos optimizados mediante la extracción de parámetros para ajustarse al perfil de impedancia de la PDN obtenidas de mediciones industriales en el laboratorio. Finalmente, este trabajo contribuyó al proponer un desarrollo novedoso mediante modelos sustitutos más eficientes y confiables para la optimización del diseño de PDNs aprovechando algunas técnicas de modelado sustituto como SVM, PSM, GRNN y Kriging.

Así mismo, en esta tesis doctoral se ponen en perspectiva más trabajos futuros por realizar. Un campo de investigación futura sería explorar el uso de métodos de optimización Bayesiana y otros métodos similares para equilibrio de cargas de EP y el ajuste del RV con distintos parámetros de compensación no lineal. Otra área de investigación a futuro de mucho interés y de relevancia consistiría en la incorporación de modelos multi-físicos de PDN con interacciones que consideren

la optimización de la co-simulación termoeléctrica, así como modelos sustitutos termomecánicos y electromagnéticos acoplados como la base para una optimización de diseño más precisa. Una línea de investigación adicional podría enfocarse hacia la predicción de las mediciones de laboratorio a través de modelos sustitutos de EP y RV, especialmente enfocados a grandes regiones de parámetros en el espacio de diseño. La finalidad de estas posibles líneas de investigación futuras sería mejorar el diseño de EP de los servidores para aplicaciones de cómputo en la nube y así reducir el costo operativo de los centros de datos y su inherente impacto al ambiente.

# Appendix

# A. LIST OF INTERNAL RESEARCH REPORTS

1) F. J. Leal-Romo, J. E. Rayas-Sánchez, and J. He, "An introduction to power delivery," Internal Report *PhDEngScITESO-15-02-R (CAECAS-15-02-R)*, ITESO, Tlaquepaque, Mexico, Feb. 2015.

2) F. J. Leal-Romo, J. E. Rayas-Sánchez, and J. He, "Power delivery design methodologies," Internal Report *PhDEngScITESO-15-03-R (CAECAS-15-04-R)*, ITESO, Tlaquepaque, Mexico, Apr. 2015.

3) F. J. Leal-Romo, J. E. Rayas-Sánchez, and J. He, "Power conversion in power delivery networks," Internal Report *PhDEngScITESO-15-09-R (CAECAS-15-11-R)*, ITESO, Tlaquepaque, Mexico, Aug. 2015.

4) F. J. Leal-Romo, J. E. Rayas-Sánchez, and J. He, "Power and thermal challenges for cloud computing applications," Internal Report *PhDEngScITESO-15-11-R (CAECAS-15-13-R)*, ITESO, Tlaquepaque, Mexico, Nov. 2015.

5) F. J. Leal-Romo, J. E. Rayas-Sánchez, and J. He, "Design of experiments implementation towards optimization of power distribution networks," Internal Report *PhDEngScITESO-16-12-R (CAECAS-16-09-R)*, ITESO, Tlaquepaque, Mexico, Nov. 2016.

6) F. J. Leal-Romo, M. Cabrera-Gómez, D. M. García-Mora, and J. E. Rayas-Sánchez, "Design optimization of a 3D spiral inductor using space mapping," Internal Report *PhDEngScITESO-17-06-R (CAECAS-17-05-R)*, ITESO, Tlaquepaque, Mexico, May 2017.

7) F. J. Leal-Romo and J. E. Rayas-Sánchez, "ADS-Matlab automation driver," Internal Report *PhDEngScITESO-17-31-R (CAECAS-17-14-R)*, ITESO, Tlaquepaque, Mexico, Nov. 2017.

8) F. J. Leal-Romo, J. L. Silva-Perales, C. López-Limón, and J. E. Rayas-Sánchez,

"Optimizing phase settings of high-frequency voltage regulators for power delivery applications," Internal Report *PhDEngScITESO-17-34-R (CAECAS-17-16-R)*, ITESO, Tlaquepaque, Mexico, Nov. 2017.

9) F. J. Leal-Romo, J. L. Chávez-Hurtado and J. E. Rayas-Sánchez, "Developing efficient surrogate based models to enhance power integrity analyses," Internal Report *PhDEngScITESO-18-28-R (CAECAS-18-11-R)*, ITESO, Tlaquepaque, Mexico, Nov. 2018.

10) A. E. Moreno-Mojica, F. J. Leal-Romo, and J. E. Rayas-Sánchez "Power delivery network impedance profile optimization," Internal Report *PhDEngScITESO-19-03-R (CAECAS-19-04-R)*, ITESO, Tlaquepaque, Mexico, May 2019.

11) F. J. Leal-Romo, J. E. Rayas-Sánchez, A. E. Moreno-Mojica, and J. L. Chávez-Hurtado, "A methodology for custom analysis and design of power delivery networks based on lumped model extraction," Internal Report *PhDEngScITESO-19-06-R (CAECAS-19-08-R)*, ITESO, Tlaquepaque, Mexico, Jun. 2019.

12) F. J. Leal-Romo, J. E. Rayas-Sánchez, and J. L. Chávez-Hurtado, "Optimization flow to enhance power delivery design by employing surrogate black box models," Internal Report *PhDEngScITESO-19-07-R (CAECAS-19-09-R)*, ITESO, Tlaquepaque, Mexico, Jun. 2019.

13) F. J. Leal-Romo, J. E. Rayas-Sánchez, and J. L. Chávez-Hurtado, "Finding a dual sensing voltage regulator recipe using PDN metamodeling optimization," Internal Report *PhDEngScITESO-19-08-R (CAECAS-19-10-R)*, ITESO, Tlaquepaque, Mexico, Jun. 2019.

14) F. J. Leal-Romo, J. E. Rayas-Sánchez, and J. L. Chávez-Hurtado, "Exploring platform PDN cost reduction opportunity using PDN metamodeling optimization," Internal Report *PhDEngScITESO-19-09-R (CAECAS-19-11-R)*, ITESO, Tlaquepaque, Mexico, Jun. 2019.

15) A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "Power delivery network impedance profile and voltage droop optimization," Internal Report *PhDEngScITESO-20-*

*07-R (CAECAS-20-03-R)*, ITESO, Tlaquepaque, Mexico, May 2020.

# B. LIST OF PUBLICATIONS

## B.1. Journal Papers

1) F. J. Leal-Romo, J. E. Rayas-Sánchez, and J. L. Chávez-Hurtado, "Surrogate-based analysis and design optimization of power delivery networks," *IEEE Trans. Electromagnetic Compatibility*, early access version (p-ISSN: 0018-9375; e-ISSN: 1558-187X; published online: 24 Mar. 2020; DOI: 10.1109/TEMC.2020.2973946)

## B.2. Conference Papers

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