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Especialidad en Diseño de Sistemas en Chip

Convertidor de Voltaje a Tiempo lineal CMOS de 0.18 um para un ADC SAR de baja potencia de 10 bits a 200kS/s con ciclo de conversión adaptable orientado a aplicaciones de audio

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TRABAJO RECEPCIONAL que para obtener el **GRADO** de
ESPECIALISTA EN DISEÑO DE SISTEMAS EN CHIP

Presenta: **FIGUEROA VÁZQUEZ, CRISTIAN F.**

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Tlaquepaque, Jalisco. agosto de 2020.

ITESO – The Jesuit University of Guadalajara

Department of Electronics, Systems, and Informatics

SPECIALIZATION PROGRAM IN SOC DESIGN

A 0.18um CMOS linear Voltage-to-Time Converter for a Low Power 10-bit 200kS/s SAR ADC with Adaptive Conversion Cycle Oriented to Audio Applications

Thesis/Project to achieve the university degree of

SOC DESIGN SPECIALIST

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Thesis Director: Cuauhtémoc R. Aguilera-Galicia, PhD

Tlaquepaque, Jalisco Mexico

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This work is dedicated to my family, my parents, and my wife, for their understanding, patience, and continuous support they gave me during all the time this important project lasted.

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List of acronyms and abbreviations

ADC	Analog to Digital Converter
VTC	Voltage to Time Converter
SAR	Successive Approximation Register
DC	Direct Current
DAC	Digital to Analog Converter
PVT	Process Variation Temperature

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Abstract

This document presents a 0.18 um CMOS process highly-linear Voltage-to-Time Converter (VTC) design that can operate at a low voltage of 1.8 V across PVT corners and with the power consumption of less than 13 uW and linearity error less than 1%.

The VTC was designed to work at a minimum of 1.68 V and accepts a maximum clock frequency of 900 MHz; to reduce non-linear behavior a symmetric load and current starved inverter configuration was proposed.

This circuit was designed using TSMC 0.18 um CMOS process technology.

Introduction

An ADC is a circuit that converts a continuous analog input voltage to a discrete binary word. ADCs are high in demand due to the increase of numerous mixed-signals systems. There are several conversion techniques in which analog-to-digital conversion can be done such as pipeline, delta-sigma, and flash. Nevertheless, Successive-Approximation technique is one of the most popular because of its accuracy, moderate conversion speed as well as low power consumption [1]. It is generally a feedback system that applies a trial-and-error algorithm to obtain a proportional digital word to an analog input voltage.

The SAR ADC

A SAR ADC (Figure 1) consists of the following design blocks:

i. Sample and Hold circuit
ii. Comparator
iii. N-bit SAR logic
iv. Digital-to-Analog Converter (DAC)

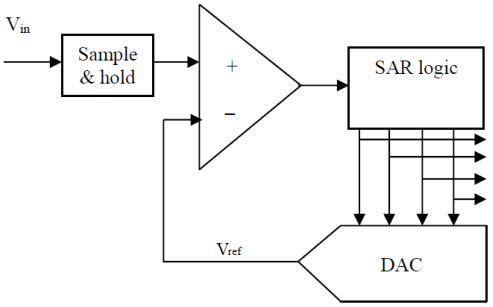

Figure 1. Block Diagram of Typical SAR-ADC

The conversion sequence of a SAR ADC is listed below:

i. The system samples the analog input V_{in} in a sample and hold circuit. Simultaneously, the SAR Logic resets the DAC.
ii. The MSB bit is set in the DAC by the SAR logic. The DAC output is known as Voltage Reference (V_{ref}).
iii. The V_{in} sampled and V_{ref} are compared by the comparator circuit. If $V_{in}$is greater than V_{ref} the Comparator output is '1' logic, else the output is '0'logic.
iv. The SAR logic saves the comparator output in the MSB position of the SAR output register and sets the bit MSB-1 and presents this partial conversion to the DAC input.
v. The conversion continues for MSB-1, MSB-2, and finishes on the LSB bit.

The Adaptive Conversion SAR ADC Proposal

Our proposal is a modification of the conventional SAR-ADC algorithm (Figure 2) to perform a conversion in fewer clock cycles. This is possible by a prediction of the consecutive 1's or 0's in the conversion result. Such prediction is based on the difference between V_{in} and V_{ref} signals. Our proposal is capable of predict 1 bit or 3 to 9 consecutive equal bits on a single clock cycle.

The conversion sequence of the proposed system is listed below:

i. The system samples the analog input V_{in} in a sample and hold circuit
ii. V_{in} and V_{ref} are converted to a time-domain signal via the VTC
iii. The time-amplifier (TA) extends the time difference between these two signals and distributes them to the arbiter and the counter.
iv. The arbiter decides which signal came in the first place.
v. The SAR Logic uses the information from the arbiter and the counter to predict equal-consecutive bits and to adapt the conversion cycles

This will improve overall conversion time and power dissipation per conversion.

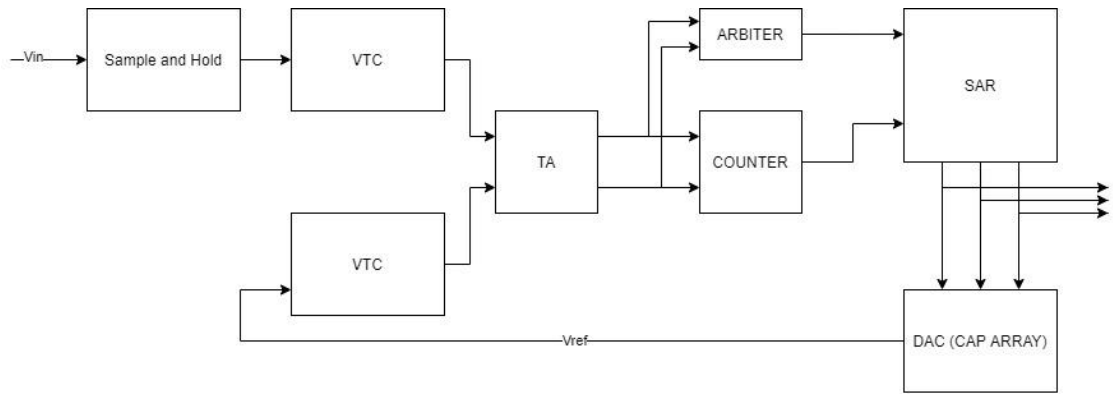

Figure 2. SAR-ADC Proposal

Section 1. Background for VTC

1.1 VTC circuit description

The purpose of the VTC is to generate a time delay proportional to a DC voltage input (provided by the sample and hold stage). The module VTC helps to the SAR logic block to determine how many conversion steps can be omitted and be able to optimize conversion-processing time, as well as reduce the power consumption of the ADC

Several VTC circuits have been introduced in the literature over the years [2], [3], [4], and [5]. The core of most of these circuits is based on the simple current-starved inverter which is shown in Figure 3. In this figure, the input voltage, V_{in}, controls the delay of the falling edge of the signal V_{clkb}, through the inverter (Transistors M2 and M3 node) by controlling the discharging current of transistor M1.

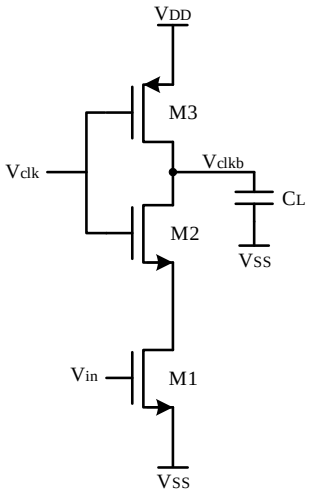

Figure 3. Current-starved inverter

After analysis of some of these architectures, we have noticed that these previously published VTC are not sufficiently linear and their voltage to time conversion sensitivity is not high enough to be used in high speed, low power, and high-resolution time-based ADCs. To surmount some of the limitations of traditional VTC architectures, we propose a variation of VTC circuit; based on the current-starved inverter architecture, to accomplish the requirements of the present project, i.e. a low power adaptive SAR-ADC.

Section 2. VTC Circuit Design

2.1 Architecture description

Using two complementary current starved inverters and a current discharge circuit causes time varies depending on the capacitor C_L (Figure 3). This creates a pulse width change based on a DC input voltage through V_{in} input, as is shown in Figure 4.

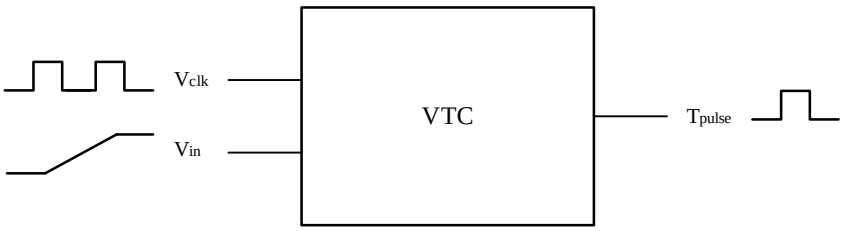

Figure 4. VTC black box

The first proposed VTC architecture is shown in Figure 5. The synchronizing clock signal, clk, controls the high-side charging and low-side discharging paths. The analog input voltage V_{in} tunes a variable resistor that modulates the discharging rate and provides different desirable delays. When the clk signal is low, the capacitor C is pre-charged to V_{DD}, at the same time, the node at the drain of M4 is discharged to avoid a residual voltage of the previous conversion. Simultaneously T_{pulse} node is pulled down to V_{SS}.

When clk goes high, T_{pulse} goes to a voltage close to $\frac{V_{DD}}{2}$ and with the help of an additional buffer, it reaches V_{DD}; at the same time C is being linearly discharged by a current defined by resistor R_D and its voltage, the discharging current is proportional to the input voltage V_{in}. During the discharging of C, when the voltage V_{clkb} reaches the threshold point of M5, T_{pulse} toggles indicating the final of the pulse that represents V_{in}.

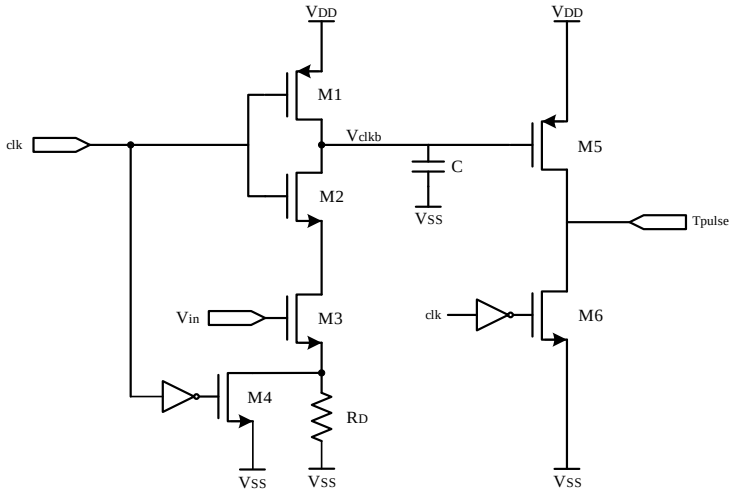

Figure 5. VTC design proposed by Zarate [6]

2.2 Dynamic range and linearization

The transistor-level characteristics of Zarate´s VTC approach were simulated using TSMC-0.18 µm process parameters with a 1.8 V power supply. To measure the linearity of this VTC, the input V_{in} is swept from 0 V up to 1.8 V. Figure 6 shows that the functional range is between 0.4 V and 0.5 V as well as the relationship between V_{in} and T_{pulse} is not linear.

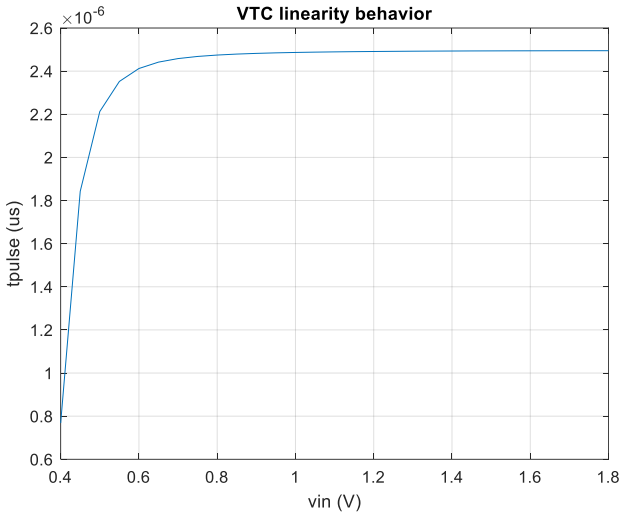

Figure 6. VTC linearity behavior with the Zarate's design

Unfortunately, this nonlinearity cannot be compensated in the SAR control logic and interfere with our proposed function as deciding how many conversions steps the SAR can skip. The cause of this behavior is due to the equivalent resistor value of M3 saturates when V_{gs3} is high enough, showing poor linearity. To minimize the source of nonlinearity, the M3 variable resistor in the triode region should be linearized.

A solution is to implement a symmetric load (for instance the Maneatis cell) [7], which brings high linearity to the design (Figure 7). The M4 diode-connected transistor lowers down the overall resistance when M3 is close to saturation. Also, after exhaustive analysis through simulations, we have removed the resistor R_D and transistor M4, because we noticed with this change the linearity range of VTC was increased.

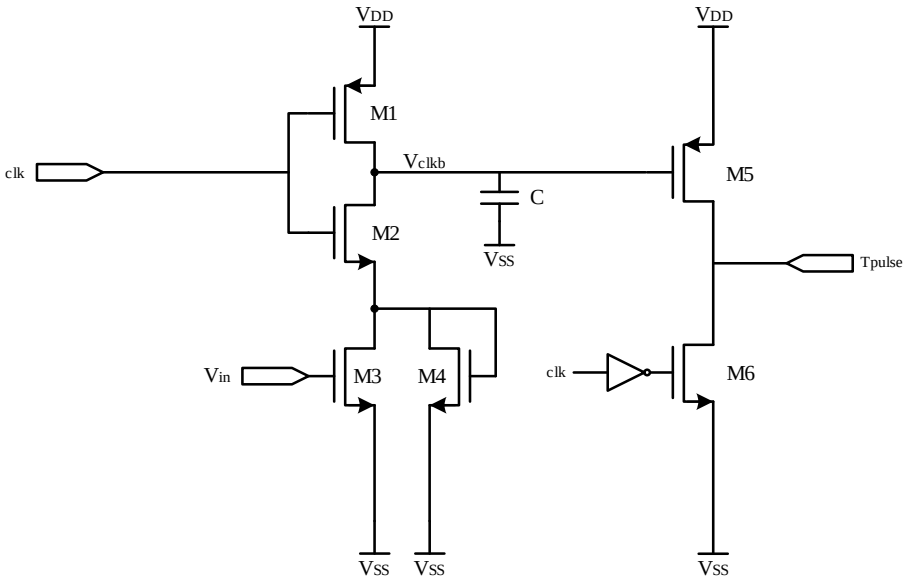

Figure 7. Proposed VTC circuit with Maneatis cell

Figure 8 shows that with the changes performed in Zarate's VTC circuit, the functional range is between 0.75 V and 1 V. This presents high linearity in the V_{in} - T_{pulse} relationship.

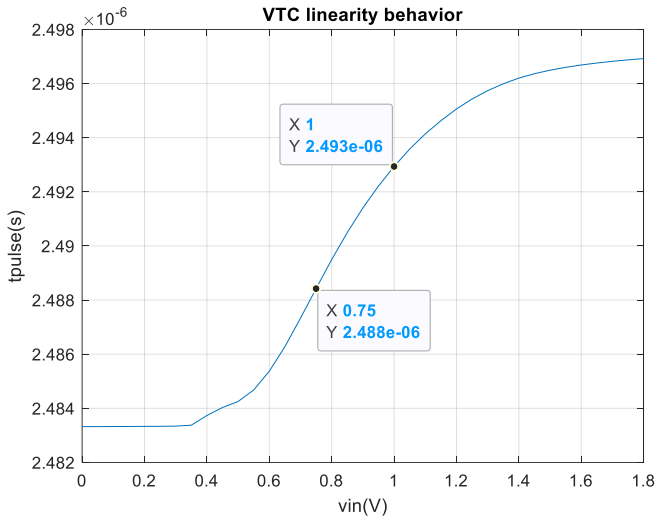

Figure 8. Proposed VTC circuit linearity behavior

2.3 Transistor sizing

Identifying the Pull-up network (PUN) and Pull-down network (PUN) in Figure 7 and using the sizing transistor methodology proposed in [8], the transistor sizes of the proposed VTC are calculated. The technology minimum channel length size is $180\ nm$, due to the etching effect in the manufacturing process, it is proposed to work with a minimum length size of $200\ nm$. The scaling factor is still $180\ nm$. Table 1 shows the size for each transistor in the VTC circuit.

Table 1. Transistor sizes for VTC circuit

Transistor	**Size (W/L)**
M1	3.24/0.2
M2	1.08/0.2
M3	1.08/0.2
M4	1.08/0.2
M5	3.24/0.2
M6	1.08/0.2
M7	3.24/0.2
M8	1.08/0.2

Section 3. VTC pre-layout verification

3.1 VTC schematic level simulation

Figure 9 shows the proposed VTC schematic with every transistor sized matching Table 1.

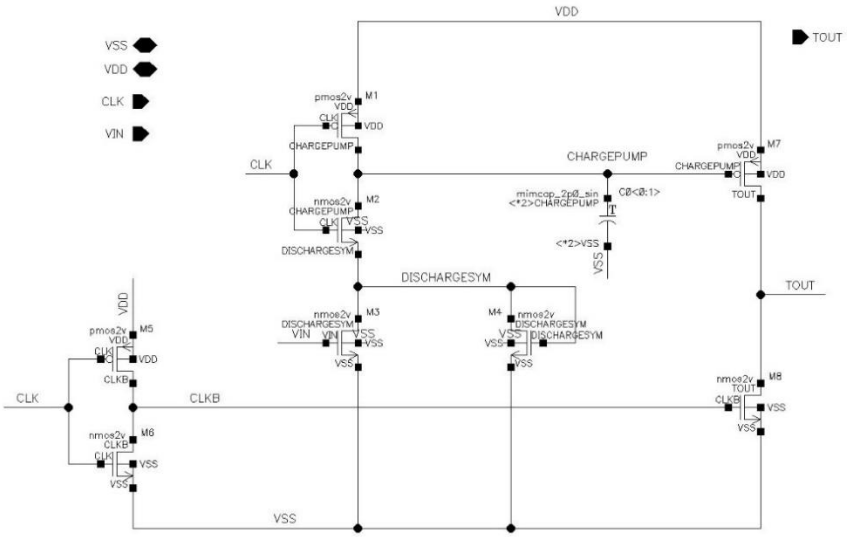

Figure 9. VTC schematic (transistors sizes are hidden for simplicity)

Having the VTC test bench that is shown in Figure 10, we can obtain the results of transient response (Figures 11-13). As can be noticed, the VTC is working as expected; first of all, giving a clk frequency of $200kHz$ (this is the ADC System frequency), and second of all, the waveforms show different time pulses to different input voltages.

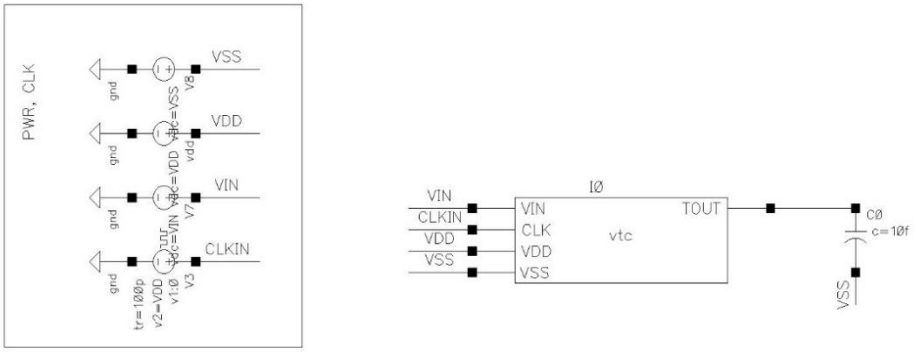

Figure 10. VTC schematic testbench

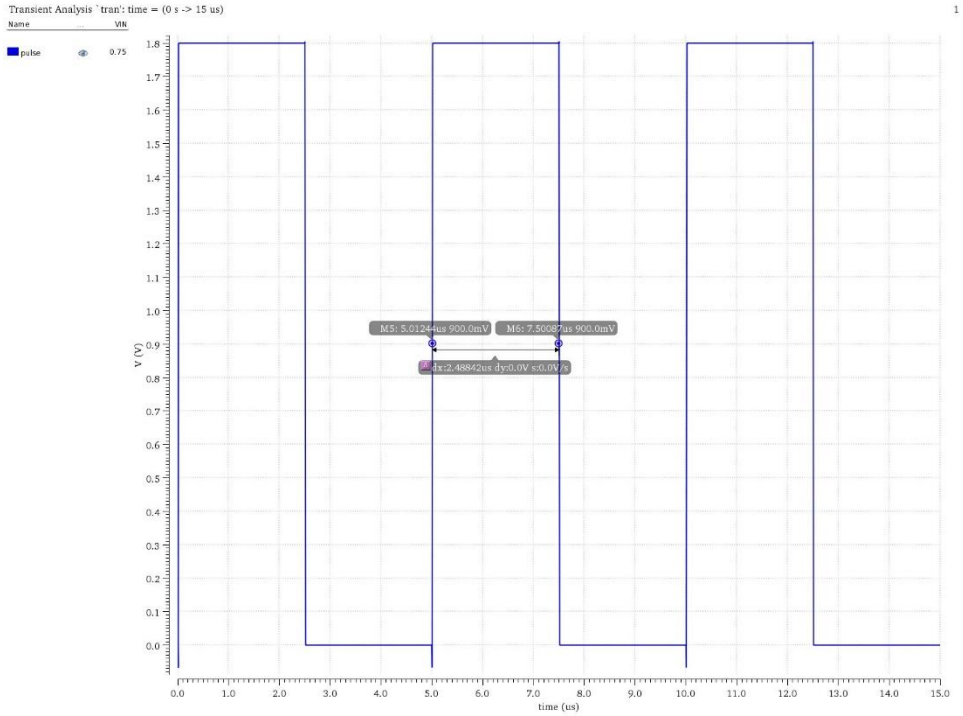

Figure 11. VTC Output Pulse = 2.4884 us, Vin = 0.75 V

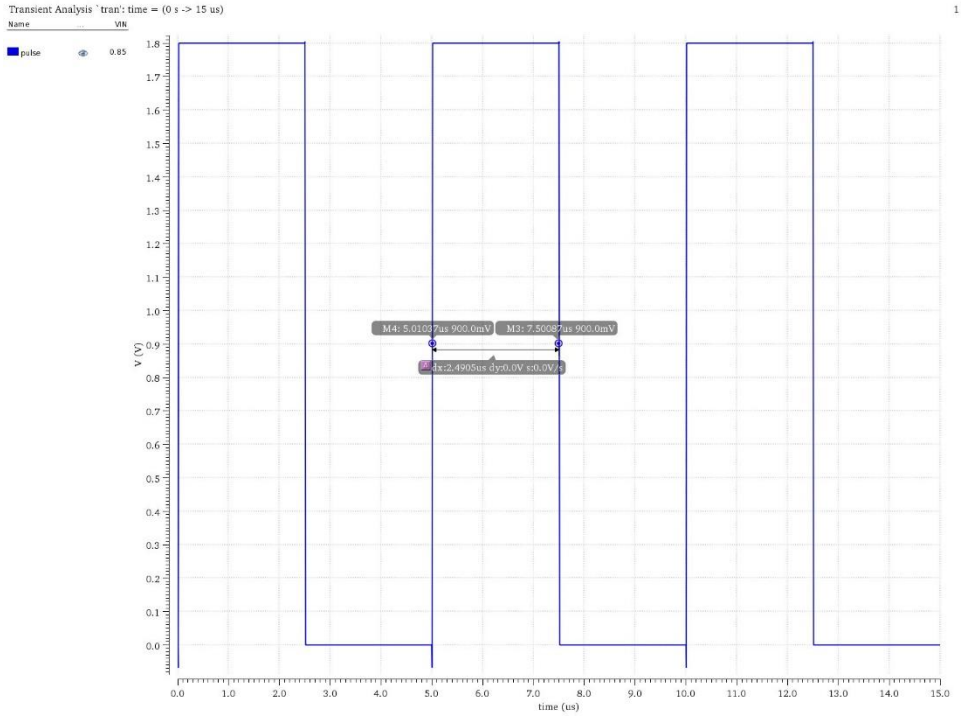

Figure 12. VTC Output Pulse = 2.4904 us, Vin = 0.85 V

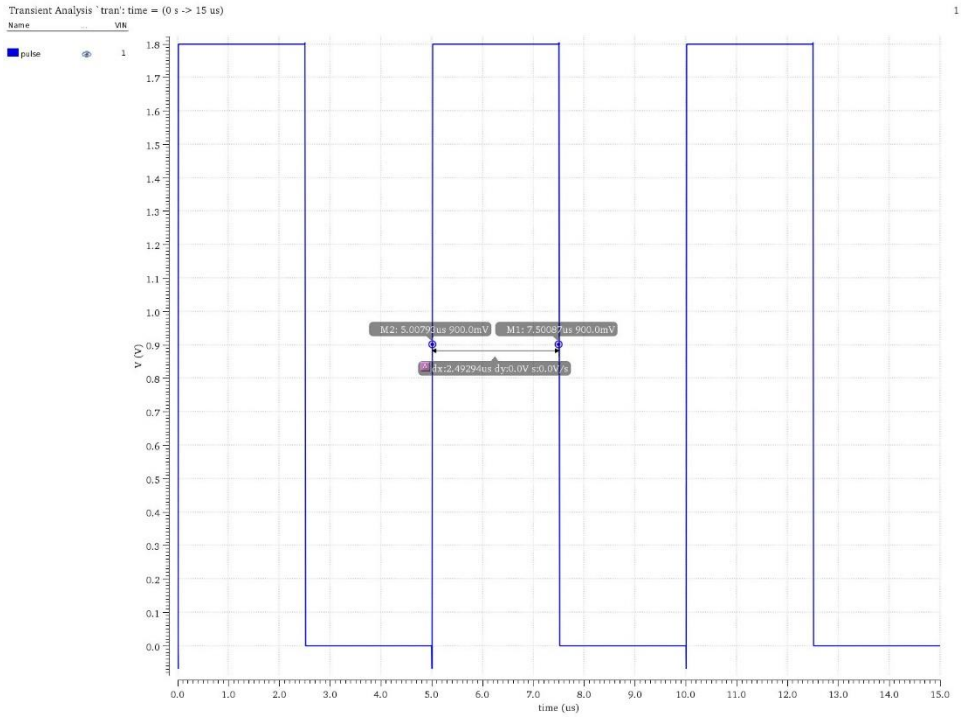

Figure 13. VTC Output Pulse = 2.4929 us, Vin = 1 V

3.2 VTC linearity error

Figure 14 shows the linear approximation for the linearity behavior. We can see the linearized line (red) is close to every calculated value (blue marks), this will help VTC resolution.

We can observe in Figure 15 the relative linearity error of the proposed VTC circuit in the functional range (0.75 V-1 V). This is less than 0.04% which will have a minimum impact on the design.

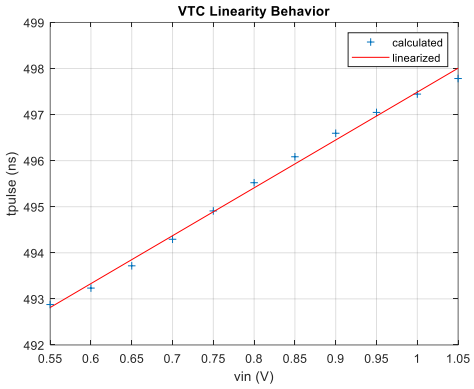

Figure 14. VTC linearity approximation

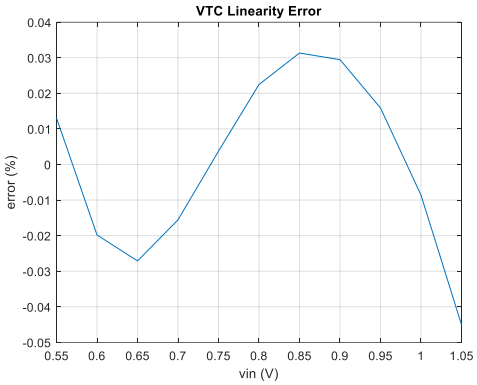

Figure 15. VTC linearity relative error

3.3 VTC PVT verification

Table 2 shows the selected PVT corners in which the circuit is simulated. Only corners TT/1.8 V/25 °C and FF/1.98 V/125 °C are required to pass criterion as the ASIC flow (RTL synthesis to GDS) is only performed under these conditions.

Table 2. VTC PVT Corners

PVT Corner	Model (V)	Voltage (V)	Temperature (°C)
tsmc018_tt_1p8V_25C	TT	1.8	25
tsmc018_ff_1p98V_125C	FF	1.98	125
tsmc018_ff_1p98V_m40C	FF	1.98	-40
tsmc018_ss_1p62V_125C	SS	1.62	125
tsmc018_ss_1p62V_m40C	SS	1.62	-40

We can see in Figures 16-18 the PVT simulation results. The VTC behavior over PVT corners, giving a clk frequency of $200kHz$, the waveforms show different time pulses to different input voltages.

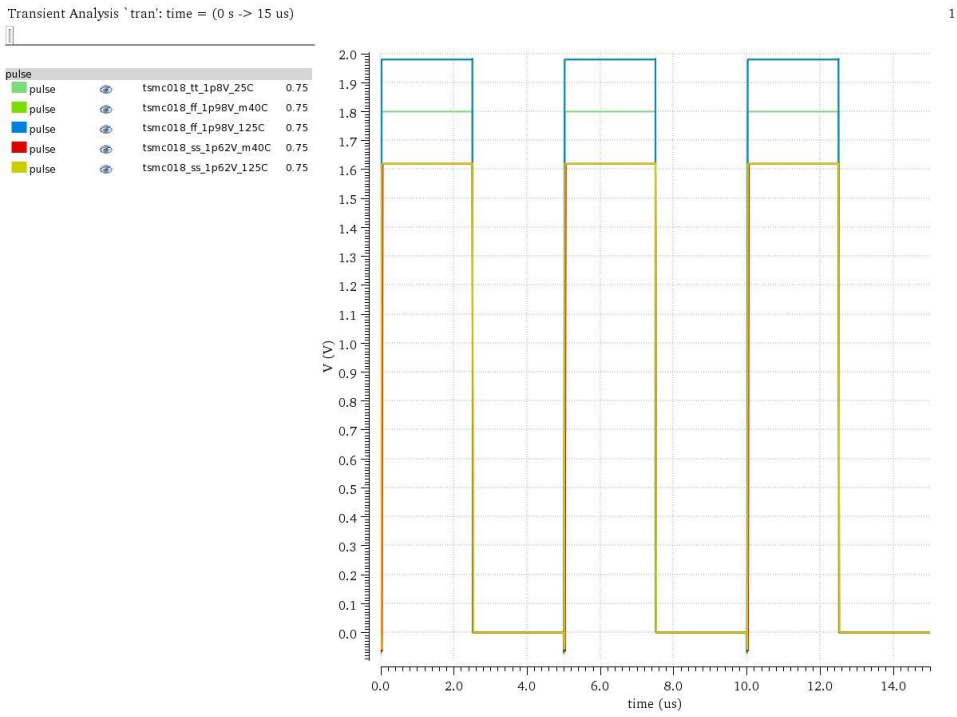

Figure 16. PVT simulation of VTC Output for Vin = 0.75V

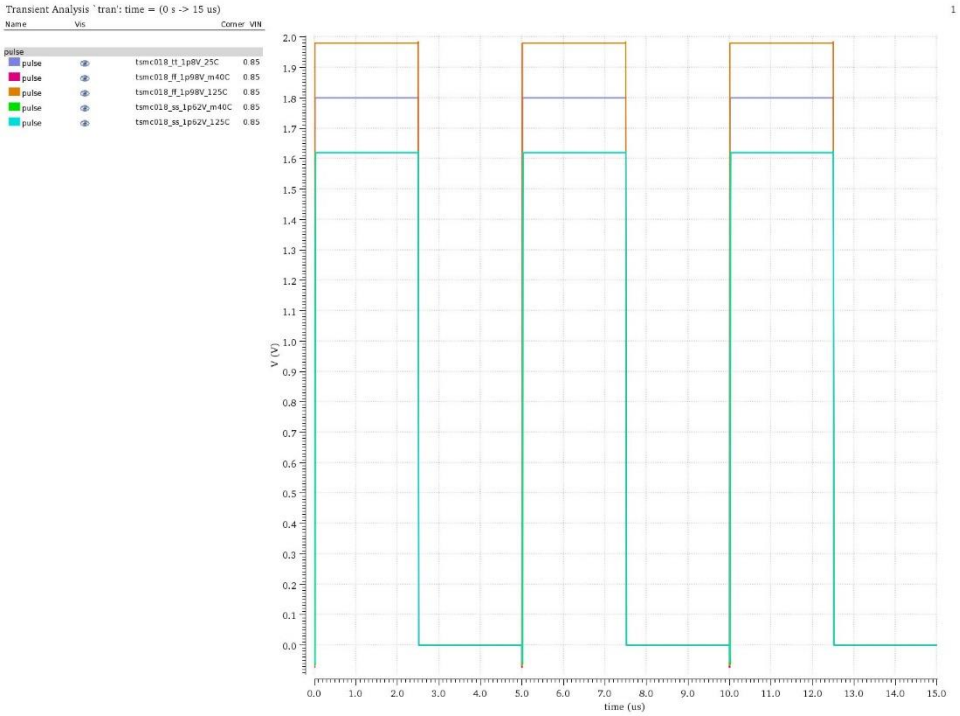

Figure 17. PVT simulation of VTC Output for Vin = 0.85V

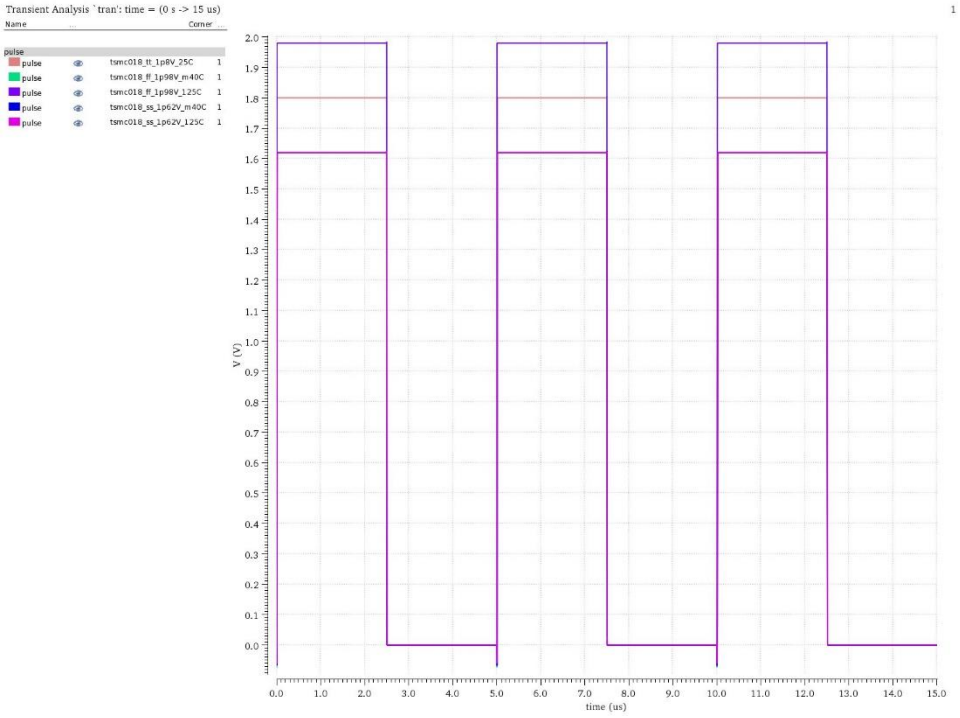

Figure 18. PVT simulation of VTC Output for Vin = 1V

Figures 19-23 show the linear approximation of the VTC behavior through PVT corners. We can see the linearized line (red curve) is close to every simulated value (blue curve), we observe that PVT corners are passing the requirement of less than 1% linearity error (Figures 24-29).

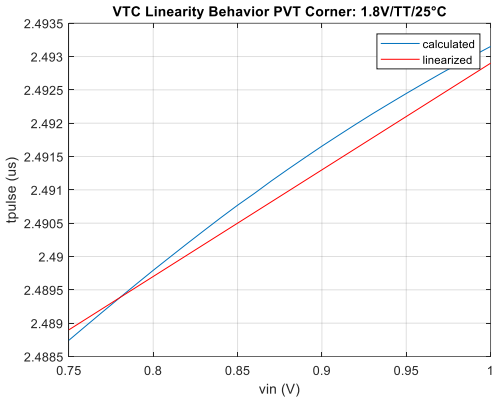

Figure 19. VTC linearity behavior for tsmc018_tt_1p8V_25C corner

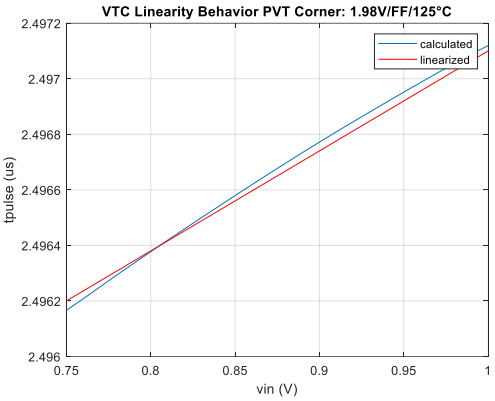

Figure 20. VTC linearity behavior for tsmc018_ff_1p98V_125C corner

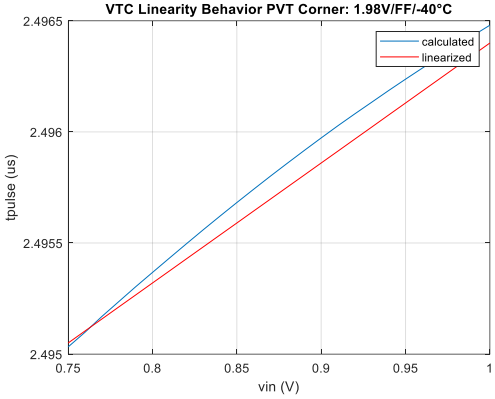

Figure 21. VTC linearity behavior for tsmc018_ff_1p98V_m40C corner

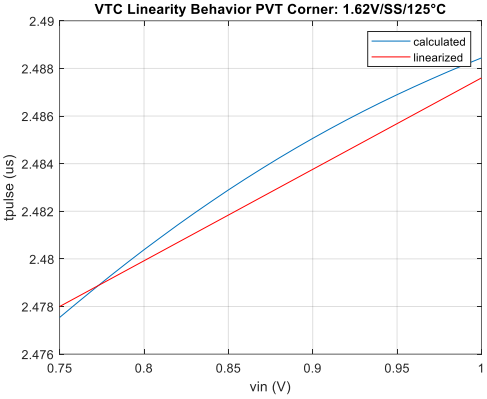

Figure 22. VTC linearity behavior for tsmc018_ss_1p62V_125C corner

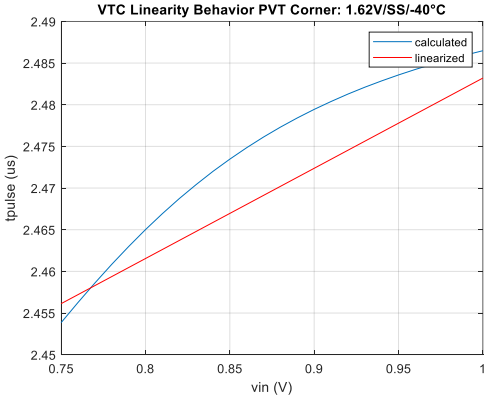

Figure 23. VTC linearity behavior for tsmc018_ss_1p62V_m40C corner

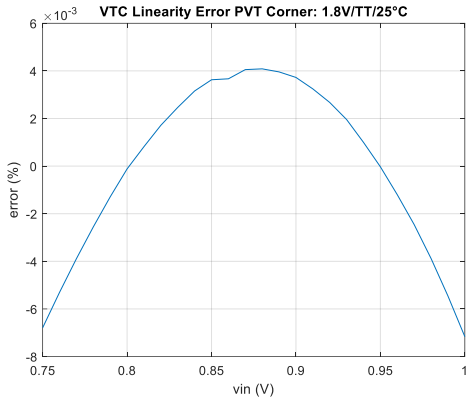

Figure 24. VTC linearity relative error for tsmc018_tt_1p8V_25C corner

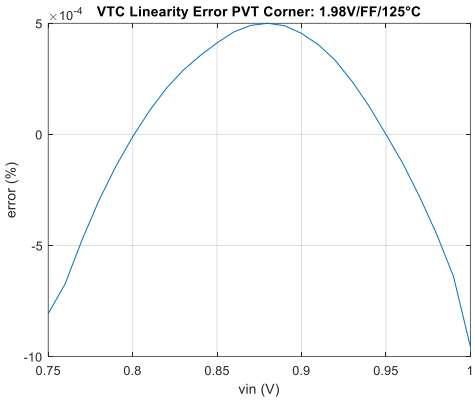

Figure 25. VTC linearity relative error for tsmc018_ff_1p98V_125C corner

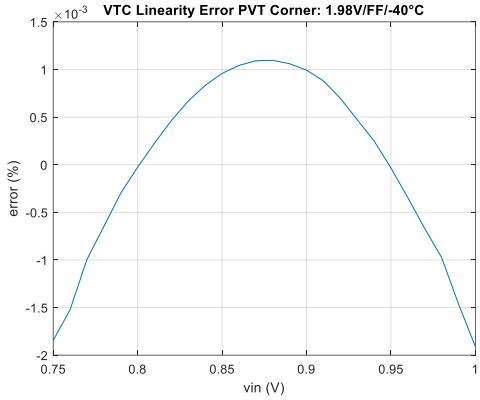

Figure 26. VTC linearity relative error for tsmc018_ff_1p98V_m40C corner

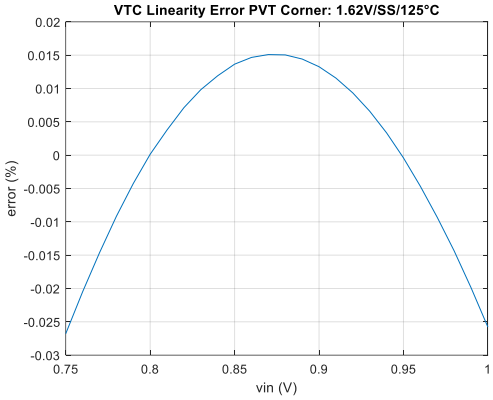

Figure 27. VTC linearity relative error for tsmc018_ss_1p62V_125C corner

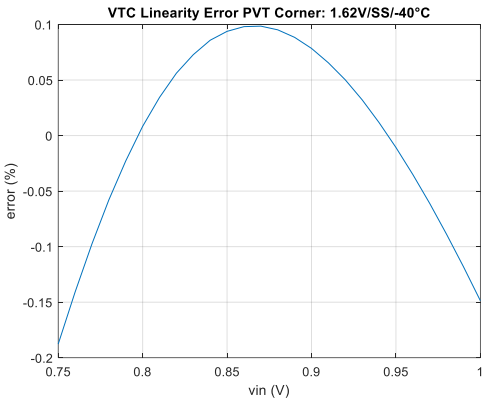

Figure 28. VTC linearity relative error for tsmc018_ss_1p62V_m40C corner

3.4 VTC pre-layout parameters

Table 3 shows the parameter characterization of the proposed VTC. These values are measured only for the typical corner, nominal power supply voltage, and room temperature.

Table 3. Pre-layout circuit characterization parameters

Parameter	**Value**
Dynamic Range Operation	[0.75- 1.00] V
Dynamic Power Dissipation per cycle	11.24 uW
Relative Linearity Error (Average)	0.04501%
Max Load Capacitance (CL)	250 fF
Charge Capacitance (Cp)	2 pF
Resolution	4.24 ps/count

Section 4. VTC Layout Design

4.1 VTC schematic level with dummies

Figure 29 shows the proposed VTC schematic with dummies required only for design layout purposes, this, to prevent etching effects. Figures 30 and 31 show the layout view of the VTC.

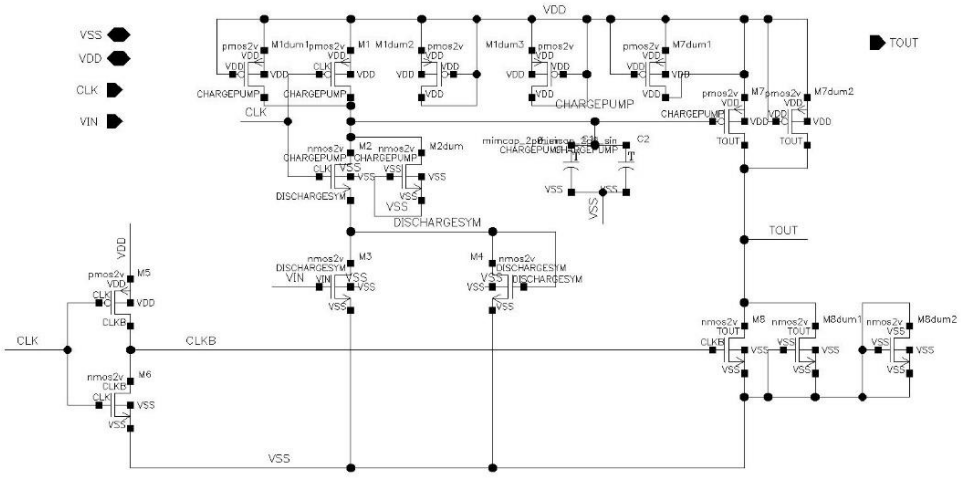

Figure 29. VTC schematic with dummies for layout

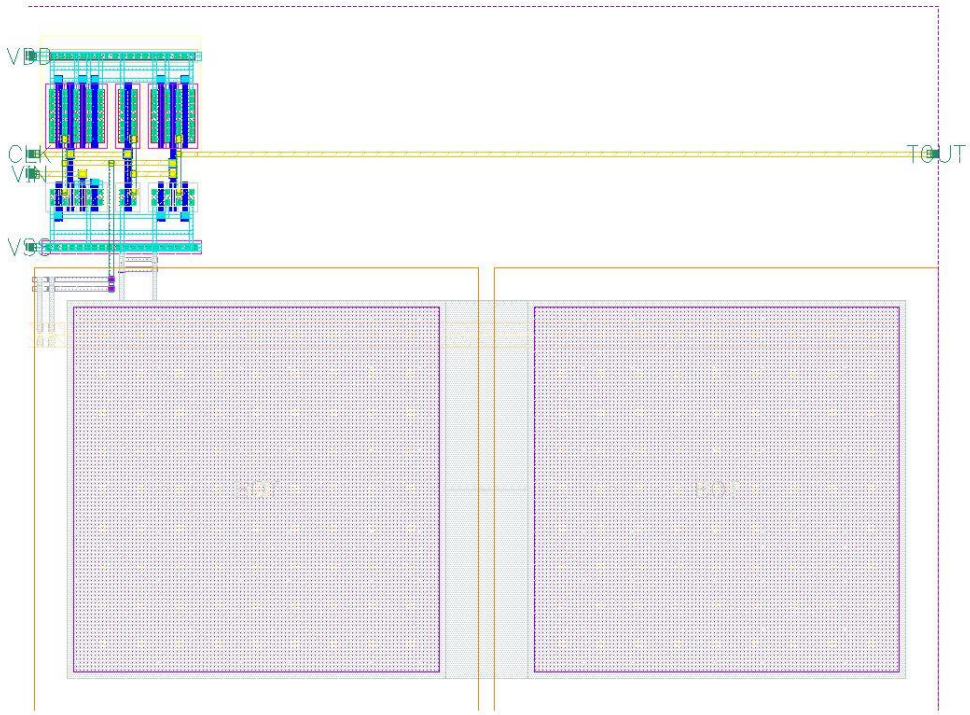

Figure 30: VTC Layout full view

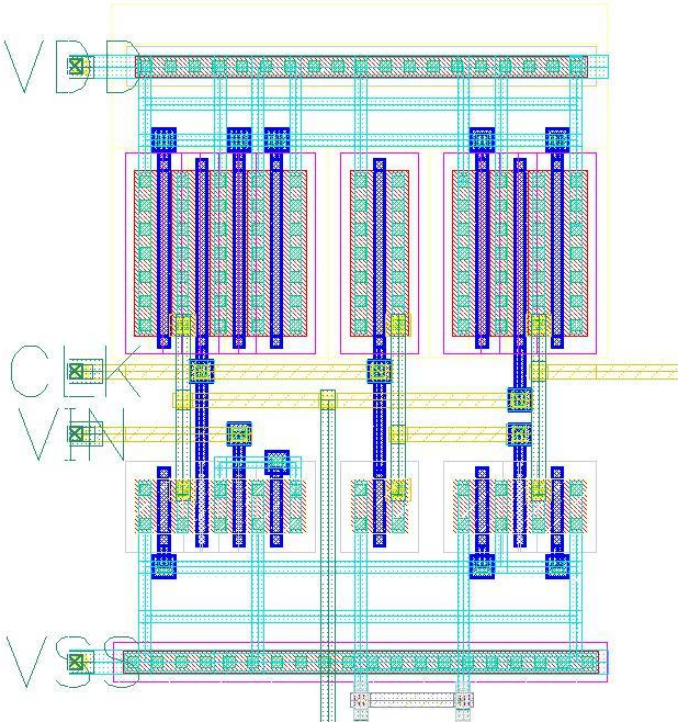

Figure 31: VTC layout device view

Section 5. VTC post-layout verification

5.1 VTC schematic level simulation

Figures 29-31 show the post-layout results of VTC transient response

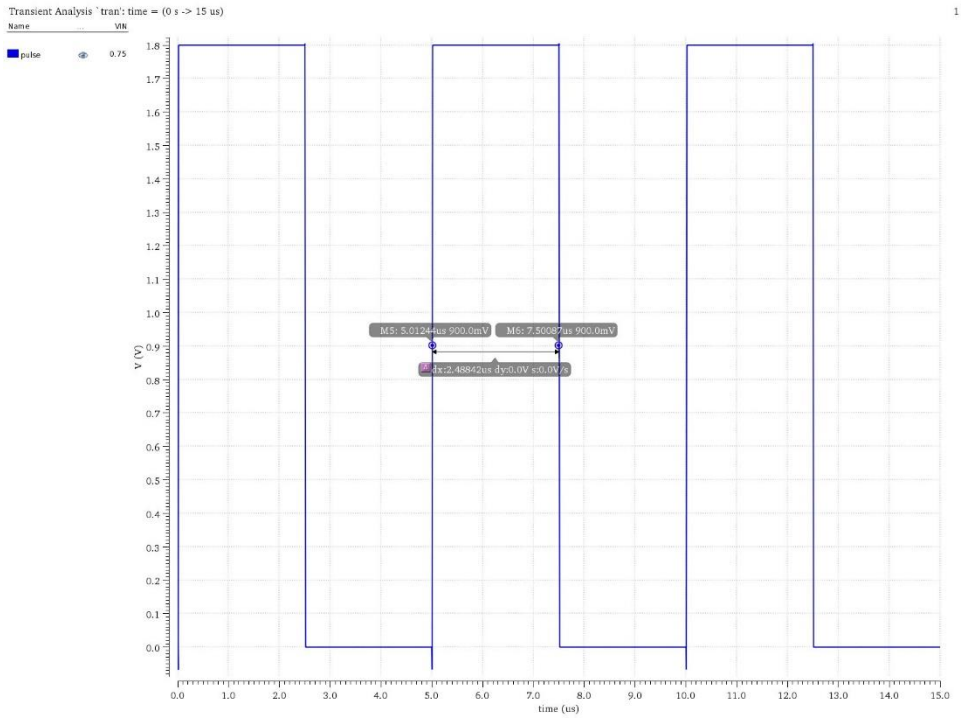

Figure 32. VTC Output Pulse = 2.48843 us, Vin = 0.75 V

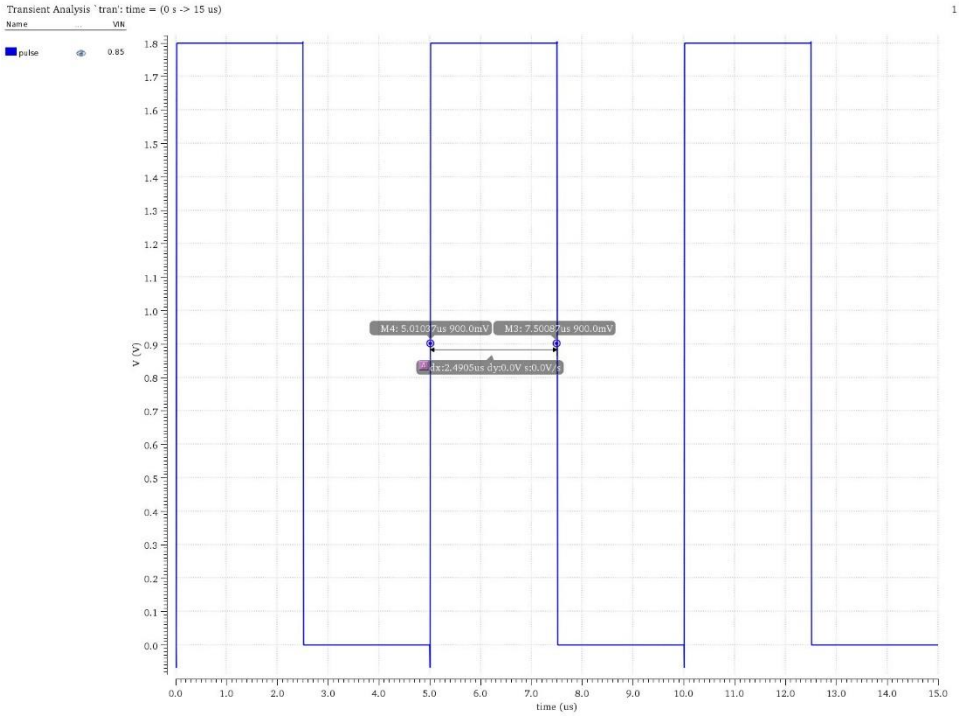

Figure 33. VTC Output Pulse = 2.49041 us, Vin = 0.85 V

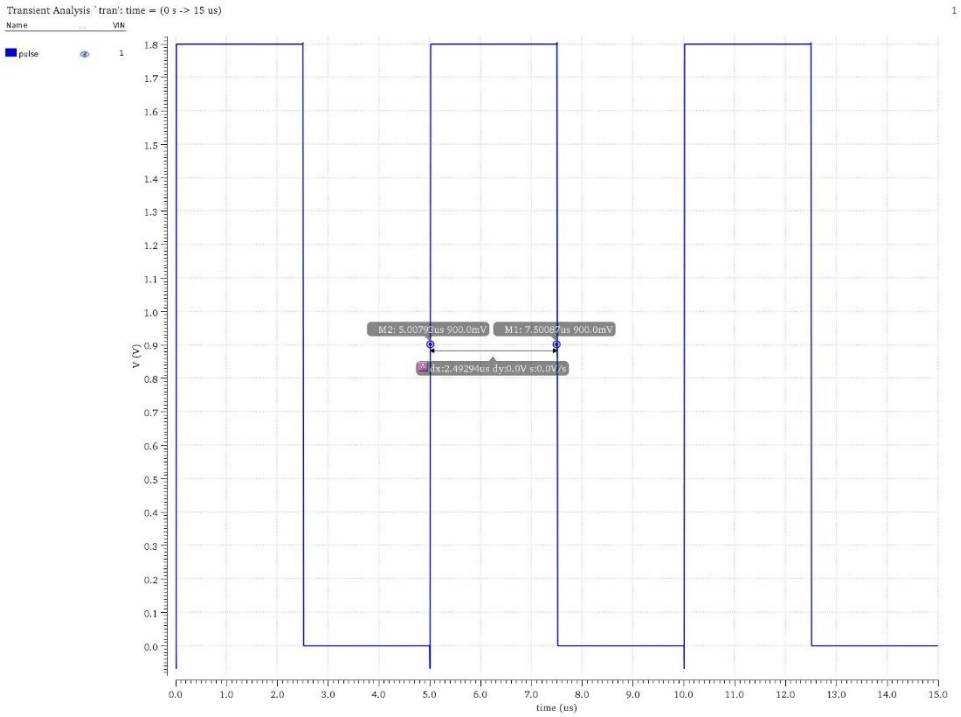

Figure 34. VTC Output Pulse = 2.49291 us, Vin = 1 V

5.2 VTC post-layout vs pre-layout linearity

Table 4 shows the VTC output differences for the input voltages 0.75 V, 0.85 V and 1 V between pre-layout design and post-layout design.

Table 4. Post-layout vs Pre-layout VTC output pulse comparison

Voltage	Pre-layout Output Pulse	Post-layout Output Pulse	% Error
Vin = 0.75 V	2.4884 us	2.48843 us	0.001206
Vin = 0.85 V	2.4904 us	2.49041 us	0.000402
Vin = 1 V	2.4929 us	2.49291 us	0.000401

5.3 VTC PVT post-layout verification

Figures 35-37 shown the results of PVT post-layout transient response. The VTC behavior over PVT corners is as expected, which indicates the implemented layout is correct; we can notice a clk frequency of $200kHz$ and the waveforms show different time pulses to different input voltages.

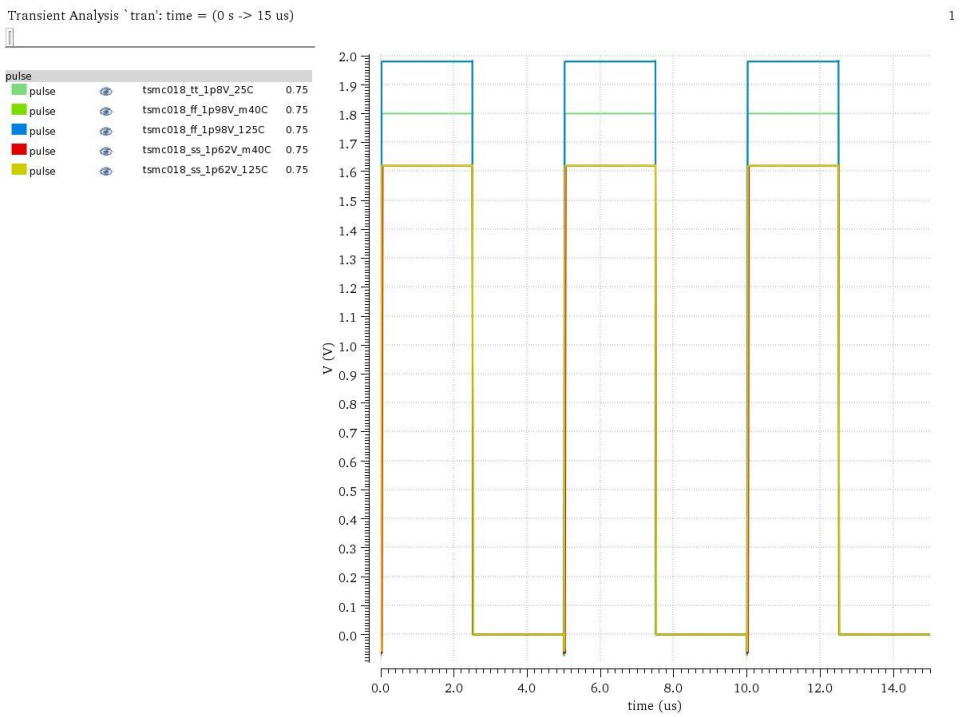

Figure 35. PVT VTC post-layout output with Vin = 0.75 V

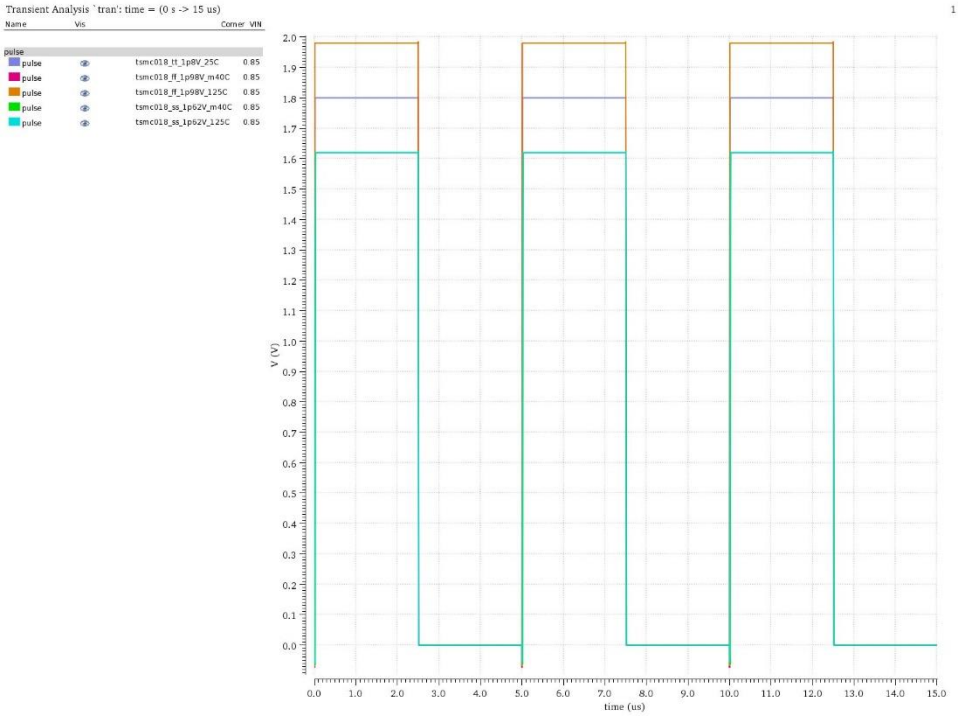

Figure 36. PVT VTC post-layout output with Vin = 0.85 V

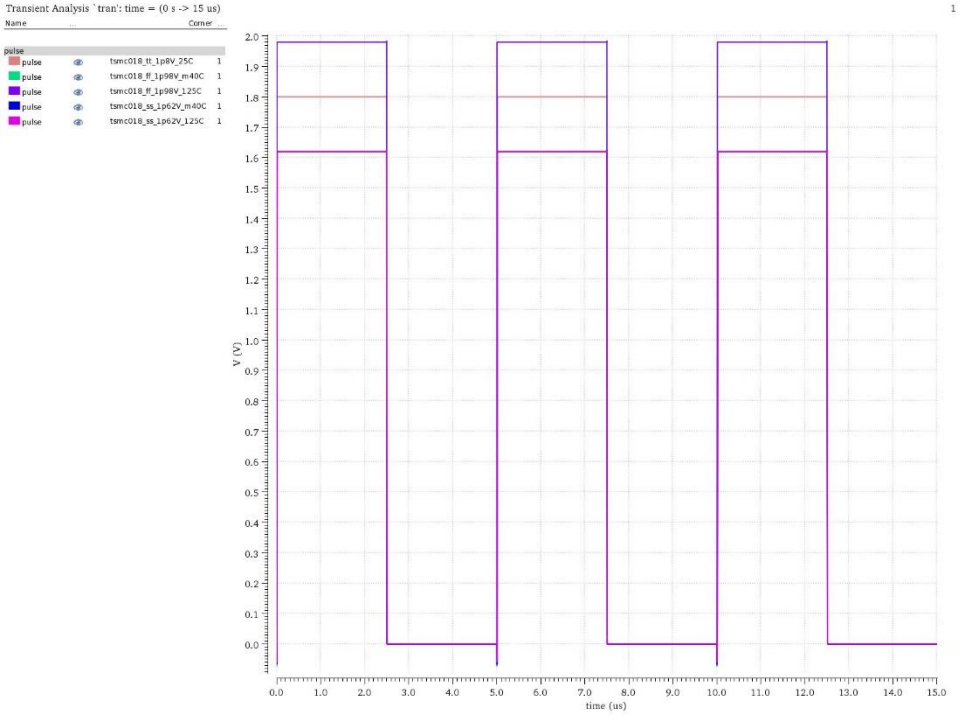

Figure 37. PVT VTC post-layout output with Vin = 1 V

Figures 38-42 show the linear approximation for the linearity behavior through PVT post-layout corners. We can see the linearized line (red curve) is close to every calculated value (blue curve), we observe that PVT corners are the requirement of less than 1% linearity error (Figures 45-47).

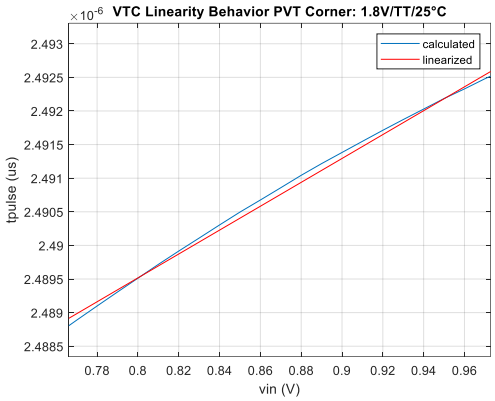

Figure 38. VTC linearity behavior for tsmc018_tt_1p8V_25C post-layout corner

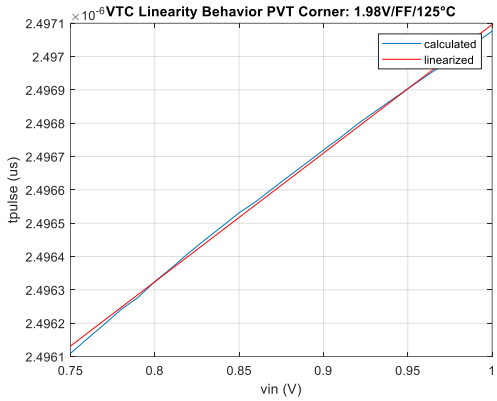

Figure 39. VTC linearity behavior for tsmc018_ff_1p98V_125C post-layout corner

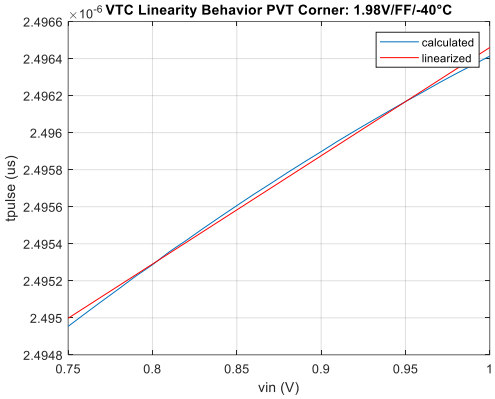

Figure 40. VTC linearity behavior for tsmc018_ff_1p98V_m40C post-layout corner

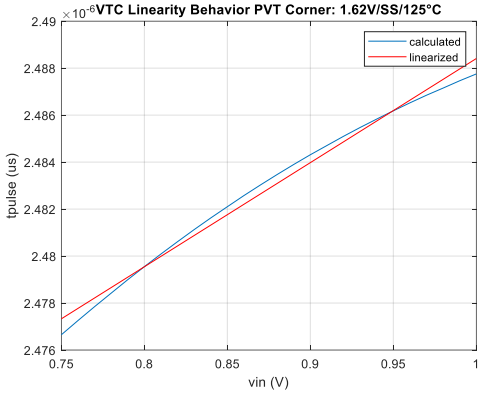

Figure 41. VTC linearity behavior for tsmc018_ss_1p62V_125C post-layout corner

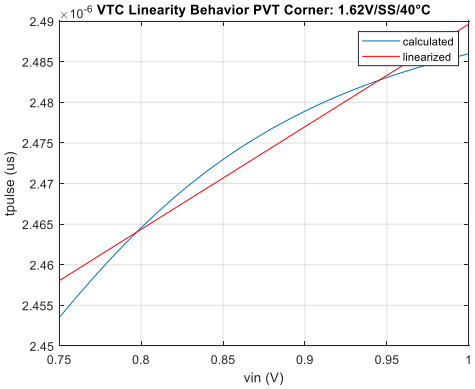

Figure 42. VTC linearity behavior for tsmc018_ss_1p62V_m40C post-layout corner

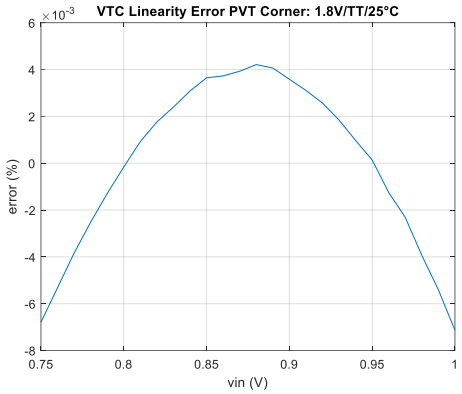

Figure 43. VTC linearity relative error for tsmc018_tt_1p8V_25C post-layout corner

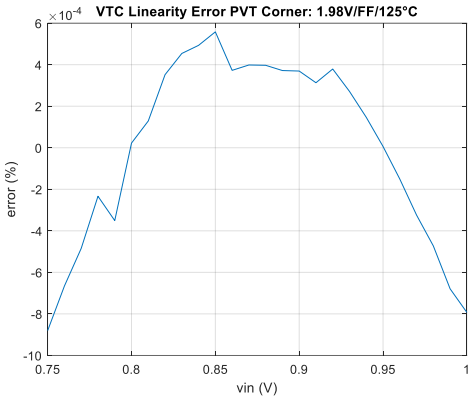

Figure 44. VTC linearity relative error for tsmc018_ff_1p98V_125C post-layout corner

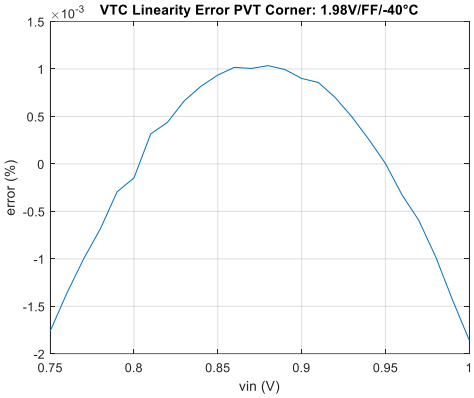

Figure 45. VTC linearity relative error for tsmc018_ff_1p98V_m40C post-layout corner

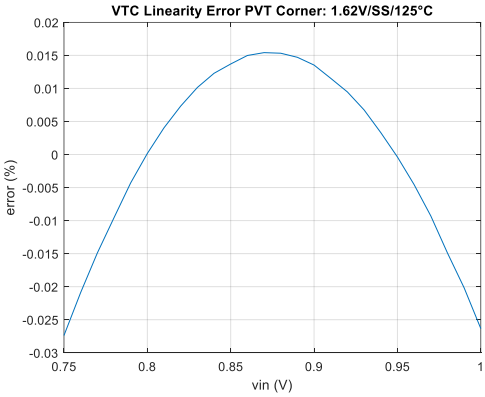

Figure 46. VTC linearity relative error for tsmc018_ss_1p62V_125C post-layout corner

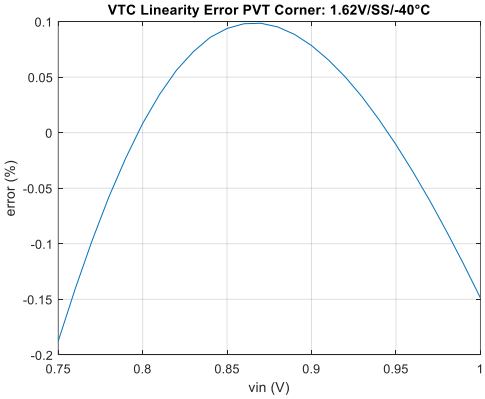

Figure 47. VTC linearity relative error for tsmc018_ss_1p62V_m40C post-layout corner

5.4 VTC post-layout parameters

Table 5 shows the parameter characterization of the proposed VTC post-layout. The values are measured only for the typical corner, nominal power supply voltage, and room temperature.

Table 5. Circuit Characterization Parameters Post-layout

Parameter	**Value**
Dynamic Range Operation	[0.75- 1.00] V
Dynamic Power Dissipation per cycle	12.73uW
Relative Linearity Error (Average)	0.07881%
Max Load Capacitance (CL)	250fF
Charge Capacitance (Cp)	2pF
Resolution	5.3ps/count

Conclusions

A novel VTC circuit is proposed which achieves a highly linear behavior and a large dynamic input range, from 0.75 V to 1 V. The proposed VTC circuit provides a pulse width which is proportional to the analog input voltage represented in the following equation $t_{pulse} = 2 * 10^{-8} * V_{in} + 2 * 10^{-6}$.

The proposed VTC works with a maximum operating frequency of 900 MHz, it consumes less than 13 uW of power and has a linearity error of less than 1%. The proposed VTC can be used in a time-based SAR-ADC at a working frequency of 200kHz.

The proposed VTC design passed all the analog design process, from the schematic diagram to the physical layout. This design experience gave me more than enough knowledge to apply this to my present and future career

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