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Departamento de Electrónica, Sistemas e Informática

Especialidad en Diseño de Sistemas en Chip

Implementación de un circuito Amplificador de Tiempo para un ADC SAR de 10-bits 200kS/s de baja potencia con conversión de ciclo adaptativapara aplicaciones de audio de alta fidelidad en proceso de tecnología CMOS TSMC de 0.18um

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TRABAJO RECEPCIONAL que para obtener el **GRADO** de
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Presenta: **HERNANDEZ FLORES JAIME G..**

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ITESO – The Jesuit University of Guadalajara

Department of Electronics, Systems, and Informatics

SPECIALIZATION PROGRAM IN SOC DESIGN

Implementing Time Amplifier for a Low Power SAR-ADC with Adaptive Conversion Cycle for High Quality Audio Applications in 0.18um TSMC CMOS Technology

Thesis/Project to achieve the university degree of

SOC DESIGN SPECIALIST

Presents: Jaime Guadalupe Hernandez Flores

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This work is dedicated to my family, coworkers and friends for their unconditional support and support during the hard hours of work and dedication.

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List of acronyms and abbreviations

ADC	Analog to Digital Converter
TA	Time amplifier
SAR	Successive Approximation Register
DC	Direct Current
DAC	Digital to Analog Converter
IB1	High value current source
IB2	Low value current source
VTC	Voltage to time converter
OTA	Transconductance amplifier
SWNP	Switch active with two different logic signals
SWPP	Switch active with two high logic signals
SWNN	Switch active with two low logic signals
INP	Positive Terminal OTA
INM	Negative Terminal OTA
FF	Flip-Flop

Contents

Section 1. ADC in the domain of time with SAR

1.1 Abstract

This document presents the design of a time amplifier circuit in 0.18 μm CMOS process with a supply voltage of 1.8 V. Simulation results performed with typical process parameters, nominal supply voltage, room temperature and an operating frequency of 200 KHz, show a time gain of 200, with an error of less than 7%. The power consumption of the designed circuit is 26 μW. The circuit can receive signals with a time difference from 10 ps to 4.7 nS. The layout dimension is 149.985 μm x 168.536 μm, with an area of 25.3 nm^2.

1.2 Introduction

An ADC is a circuit that converts a continuous analog input voltage to a discrete binary word. ADCs are high in demand due to the increase of numerous mixed-signals systems. There are several conversion techniques in which analog-to-digital conversion can be done such as pipeline, delta-sigma, and flash. Nevertheless, Successive-Approximation technique is one of the most popular because of its accuracy, moderate conversion speed as well as low power consumption [1]. It is generally a feedback system that applies a trial-and-error algorithm to obtain a proportional digital word to an analog input voltage.

1.3 The SAR ADC

A SAR ADC (Fig. 1.1) consists of the following design blocks:

i. Sample and Hold circuit
ii. Comparator
iii. N-bit SAR logic
iv. Digital-to-Analog Converter (DAC)

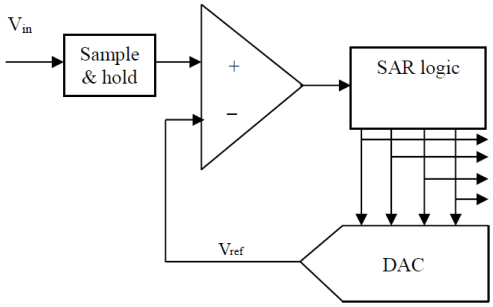

Fig.1.1: Block Diagram of Typical SAR ADC [1]

The conversion sequence of a SAR ADC is listed below [1]:

i. The system samples the analog input V_{in} in a sample and hold circuit. Simultaneously, the SAR Logic resets the DAC.
ii. The MSB bit is set in the DAC by the SAR logic. The DAC output is known as Voltage Reference (V_{ref}).
iii. The V_{in} sampled and V_{ref} are compared by the comparator circuit. If $V_{in}$is greater than V_{ref} the Comparator output is '1' logic, else the output is '0'logic.
iv. The SAR logic saves the comparator output in the MSB position of the SAR output register and sets the bit MSB-1 and presents this partial conversion to the DAC input.
v. The conversion continues for MSB-1, MSB-2, and finishes on the LSB bit.

1.4 The Adaptive Conversion SAR ADC Proposal

Our proposal is a modification of the conventional SAR-ADC algorithm (Fig. 1.2) to perform a conversion in fewer clock cycles. This is possible by a prediction of the consecutive 1's or 0's in the conversion result. Such prediction is based on the difference between V_{in} and V_{ref} signals. Our proposal is capable of predict 1 bit or 3 to 9 consecutive equal bits on a single clock cycle.

The conversion sequence of the proposed system is listed below:

i. The system samples the analog input V_{in} in a sample and hold circuit
ii. V_{in} and V_{ref} are converted to a time-domain signal via the VTC
iii. The time-amplifier (TA) extends the time difference between these two signals and distributes them to the arbiter and the counter.
iv. The arbiter decides which signal came in the first place.
v. The SAR Logic uses the information from the arbiter and the counter to predict equal-consecutive bits and to adapt the conversion cycles.

This will improve overall conversion time and power dissipation per conversion.

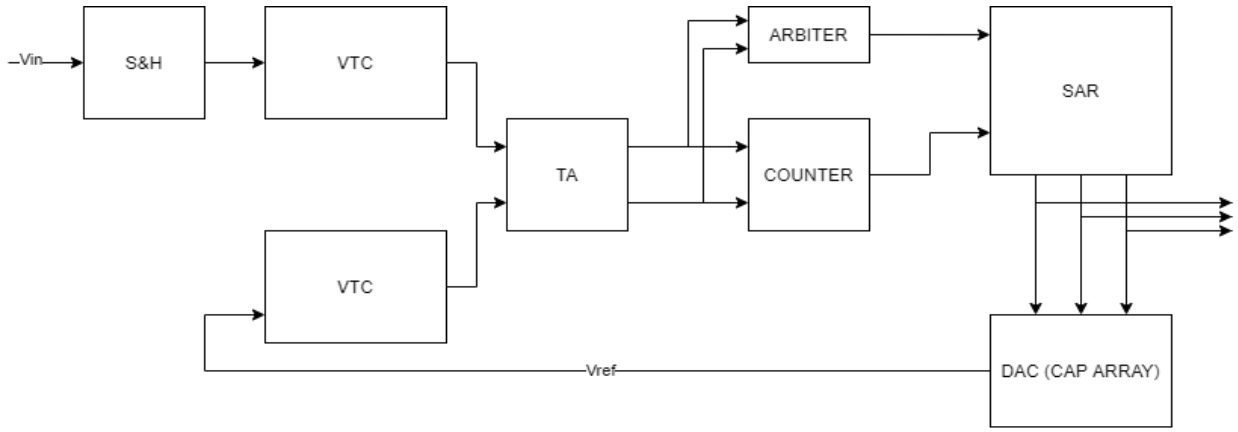

Fig. 1.2: SAR ADC System Proposal [2]

Section 2. The Time Amplifier Circuit

2.1 Circuit Description

A Time Amplifier (TA) is an electronic circuit that is used to increase the magnitude of the difference in time of two signals applied to its input. The purpose of the TA circuit is to amplify the difference between the two signals provided by the VTC blocks (see Fig. 1.2). The TA helps the SAR module to reduce the clock frequency of the Counter that determines a digital value proportional to the analog input voltage.

The block diagram of TA is presented in Fig. 2.1. Can be noted that at the input, the TA receives the two signals A and B with a time difference $of\ \Delta Tin$ and outputs VTC signals with an increased difference in time $\Delta Tout$.

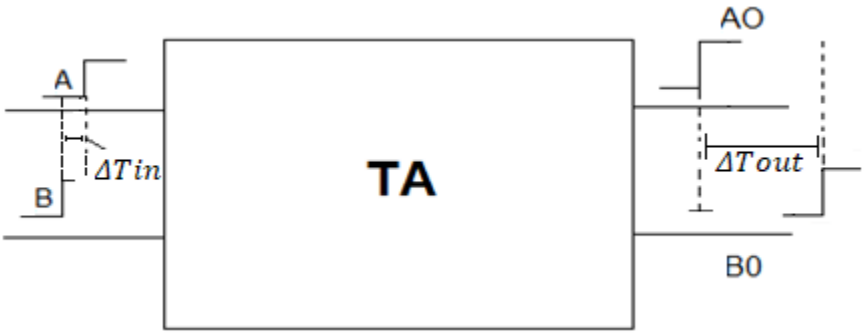

Fig. 2.1: Conceptual Diagram of Time Amplifier.

Several proposals of TA topologies have been published in the technical literature, [3] [4] [5] [6]. Time difference amplification can be achieved using either analog or digital circuitry.

Table 2.1 summarizes the performance of some architectures of TA.

Typology	SR latch based	Inverter based	DLL-like
Time Gain	20	2	4
Input Range	40 ps	100 ps	300 ps
Technology	90nm	0.180 µm	65 nm
Power	-	-	314 µA @5MHz

Table 2.1 Performance comparison of some digital TA architectures

The digital TA option is discarded for this SAR-ADC project due to its limited amplification and input range of time difference. Instead, propose an analog TA.

The analog TA approach that we propose in this work is adapted from [7] and it is shown in Fig. 2.2. This is composed of two symmetrical sections; the only difference between the two sections is that the control signals are inverted. This TA is an open-loop architecture. We have chosen this architecture for the SAR-ADC project because it promises to reach the highest gain and good linearity in a wide input time range.

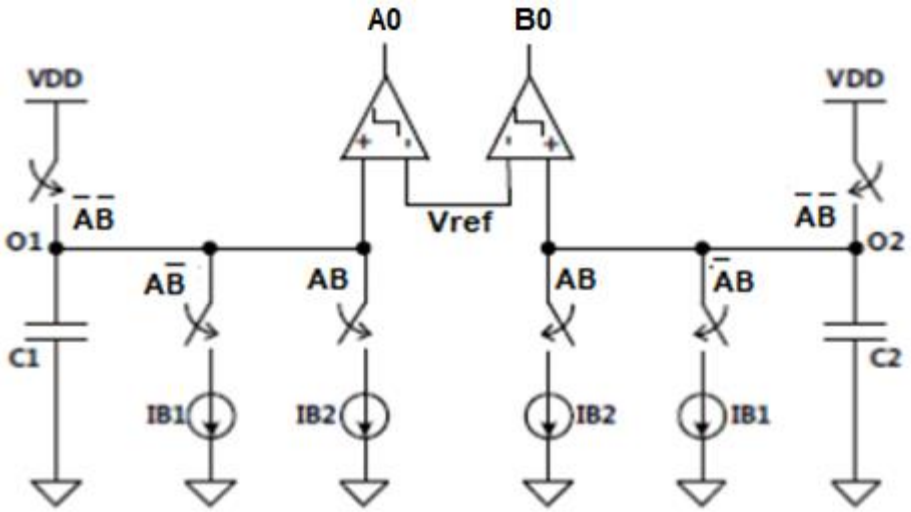

Fig. 2.2: Conceptual implementation of the analog TA circuit. [7]

The principle of this TA is as follows: the capacitors C1 and C2 are pre-charged to VDD when signal A provided by "VTC1" and signal B provided by "VTC2" are ‘0’. This sets both nodes O1 and O2 to VDD (see also the timing diagram in Fig. 2.3). When signals A and B are ‘1’ and ‘0’ respectively, the O1 node voltage ramps down linearly with time at a fast rate of SR1A, while the O2 voltage remains constant at VDD. When both signals A and B are at ‘1’, both voltage nodes O1 and O2 ramp down linearly with time at a slow rate of SR2A and SR1B respectively. In the time interval T2 – T3, SR2A, and SR1B are nominally the same. When either voltage nodes O1 or O2 voltage reaches Vref (where Vref is usually set to VDD/2), the comparator output changes from ‘0’ to ‘1’ if O2 > O1.

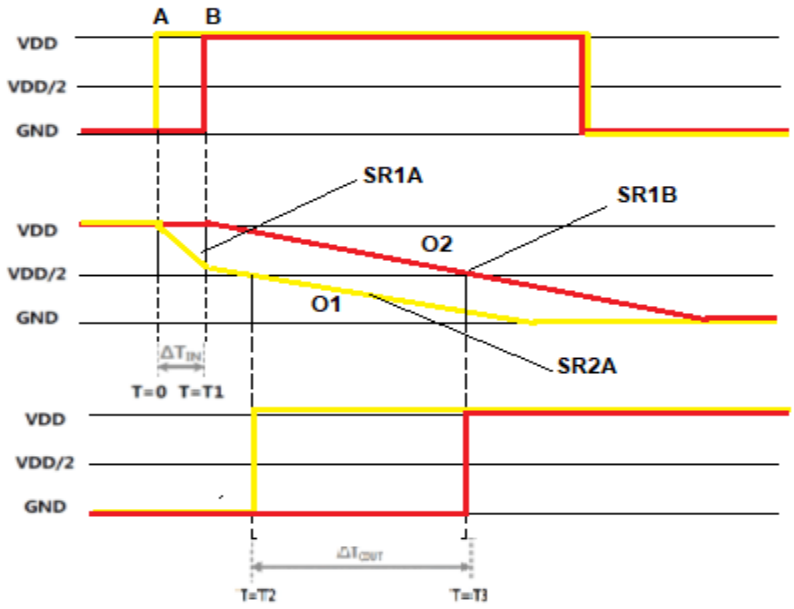

Fig. 2.3: The timing diagram of the analog TA: (a) A and B input signals, (b) discharge curves of capacitor and (c) outputs of comparator [7]

2.2 Mathematical model of TA

The first parameter to be analyzed is the voltage at nodes O1 and O2 as the case may be. To simplify the analysis, we will take the case of signal A ahead of signal B (See Fig. 2.4). We can deduce the charge and discharge equation as follows:

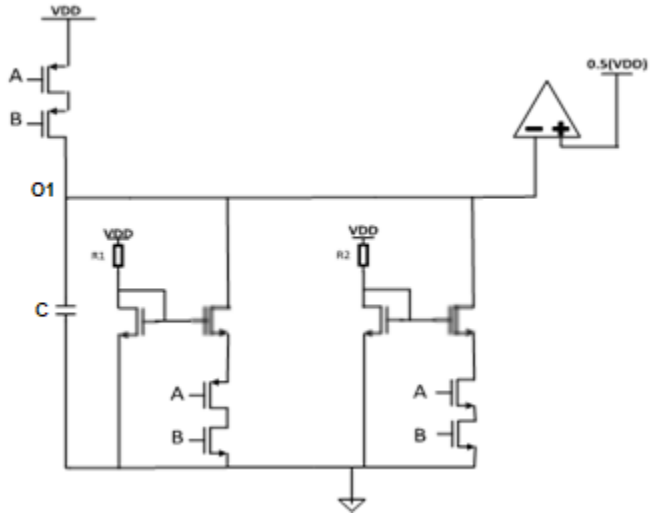

Fig. 2.4: The left section of the analog TA circuit.

At node O1 [7]:

$$IB1 * \Delta Tin + IB2 * (T2 - \Delta Tin) = 0.5VDD * C \quad (1)$$

Where, $\Delta Tin = A - B$

And at node O2:

$$IB2 * (T3 - \Delta Tin) = 0.5VDD * C \quad (2)$$

If we define T2 and T3 as the start times, we can combine (1) and (2) to determine $\Delta Tout$= T3-T1:

$$T2 = \Delta Tin * \left(1 - \frac{IB1}{IB2}\right) + \frac{VDD*C}{2*IB2} \quad (3)$$

$$T3 = \Delta Tin + \frac{VDD * C}{2 * IB2}$$

From (3) we calculate the transfer function $A_T = \frac{\Delta T_{out}}{\Delta T_{in}}$ as follows:

$$A_T = \frac{T3-T2}{\Delta Tin} = \frac{IB1}{IB2} \quad (4)$$

From (1) we can see the maximum differential input of the TA circuit is given by the discharge speed of the capacitor in O1, until it reaches a level below of VDD/2:

$$\frac{IB1}{C} * \Delta Tin \leq \frac{VDD}{2} \quad (5)$$

$$\Delta Tin \leq \frac{VDD * C}{2 * IB1}$$

And the maximum frequency is controlled by the discharge speed of the circuit at node O2 since the capacitor must be completely discharged before to start the next cycle and then the maximum frequency is given by (6):

$$Fmax = \frac{IB2}{C*VDD} \quad (6)$$

The Power consumption of this TA circuit is given by (7):

$$P = 2 * C * VDD^2 * F \quad (7)$$

Section 3. TA Circuit Design

3.1 Transistor Level Architecture of TA

Fig. 3.1 presents the transistor schematic of the TA circuit. The Comparators are implemented using OTAs, which design development is addressed in section 3.4. The two capacitors C of Fig. 3.1 are of MIMCAP_2Po_SIN type from the TSMC 0.18 μm process. The two current sources are implemented using simple current mirrors, and the three switches SWNN, SWPP, and SWNP are implemented using transmission gates topologies.

All switches are controlled by the signals coming of the VTC blocks (A and B).

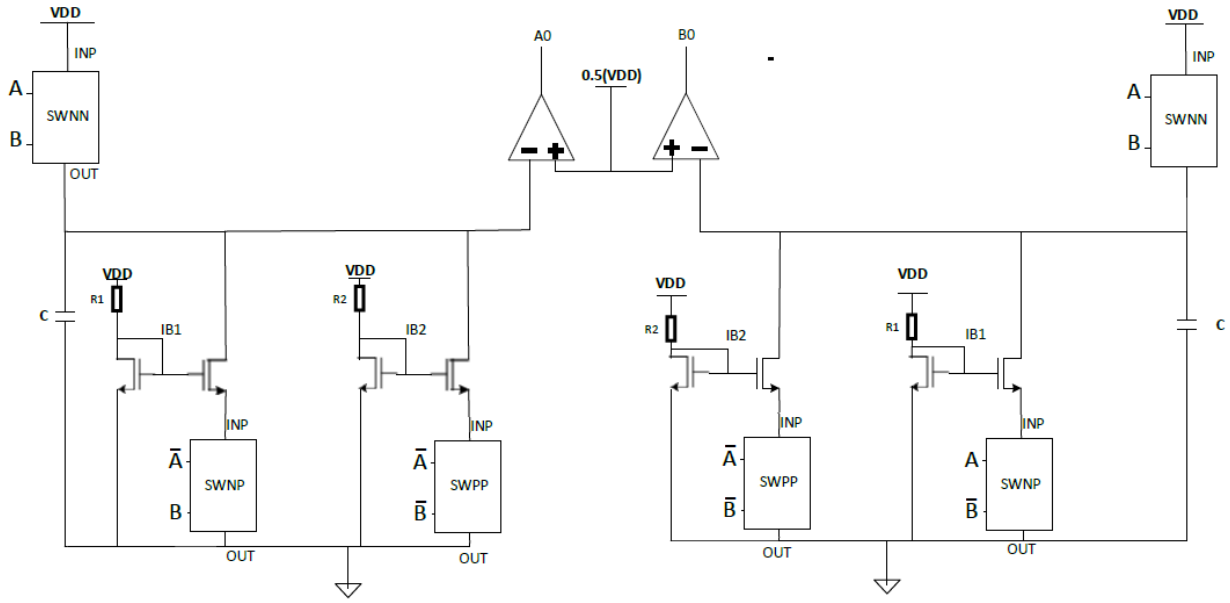

Fig. 3.1: Schematic Diagram of implemented TA circuit.

3.2 TA Design Characterization

The value of current sources IB1 and IB2 was defined in reason of the required time gain. We looked for the maximum gain and minimum error of TA in order to get the minimum operating frequency of SAR-ADC. Having the time-difference range of 10 pS <ΔTin <4.7 nS measured from the VTC blocks., The time gain is defined as A_T = 200. Then, using Ec. (4) IB1 = 1 mA and IB2 = 5 µA. Capacitors C values are defined in terms of the discharge rate which is controlled by the current sources IB1 andIB2; the value is 10 pF. The Transmission Gate (TG) topology for the three switches is chosen in reason of the lowest Ron in order to get the best speed performance; the current through the switch SWNN is 585 µA when it is turned on and the capacitor is fully discharged, then the current diminishes exponentially until the capacitor is charged to VDD. The leakage current is 10 pA in off state. The current through the switch SWNP is 200 µA when it is turned on and a minimum leakage current of 5 pA in off state. Finally, the current through the switch SWPP is 5 µA when it is turned on and a minimum leakage current of 3 pA in off state. The switches are activated with a combination of A and B signals, to do this, we have designed a logic-gate control circuit that is explained in detail in section 3.3. We use OTAs with buffer as comparators. Comparators are designed for a Vref of 900 mV; The propagation delay is 1.29 µS; the power consumption is $13\ \mu W$. The design specifications of the TA circuit are summarized in Table 3.1.

Parameter	**Value**
Time Gain	200
Input time range	10 pS-4.7 nS
Power	13 µA @200KHz
Max Error %	7%

Table 3.1: TA Design characterization.

3.3 Design of the switches

As mentioned above, the switches are activated by A and B signals provided each by VTC blocks. However, note that the switch SWNN is turned on with both A and B signals in the low state, the SWPP is activated with the two A and B signals in the high state while the SWNP is activated with A signal in the low state and B signal in the high state. To generate these A and B signals combination, we have added a logic control circuit to the switches. Each switch develops similar performance, however, its architecture and the dimensions are different.

To design the switches, we have considered that they must be as fast as possible in both transitions high to low and low to high. This requirement was achieved with the transmission gate topology. Another important requirement is the amount of current that flows through them, that in some cases it reaches up to 1 mA; this was achieved by proper sizing of transistors. Design specifications of switches are summarized in Table 3.2.

Parameter	**Specification**
Rise Time	4 pS
Fall Time	15 pS
Current level in the on state	1 mA
Current level in the off state (leakage current)	3 pA
Maximum Delay	40 pS

Table 3.2: TA Switches design specifications.

3.3.1 The switch SWNN.

The transistor schematic of the switch SWNN is shown in Fig. 3.2. As can see, the TG structure implemented with transistors M0 and M1. The logic control circuit is implemented with two inputs NAND gate (M4 – M7), and an inverter (M13, M12). The width and length of the transistors are summarized in Table 3.3. The transient response of the switch SWNN is presented in Fig. 3.3.

Transistor	W	L
M0	1u	200n
M1	1u	200n
M4	220n	200n
M5	800n	220n
M6	220n	220n
M7	220n	200n
M12	220n	200n
M13	220n	200n

Table 3.3: Transistors' widths and lengths of switch SWNN.

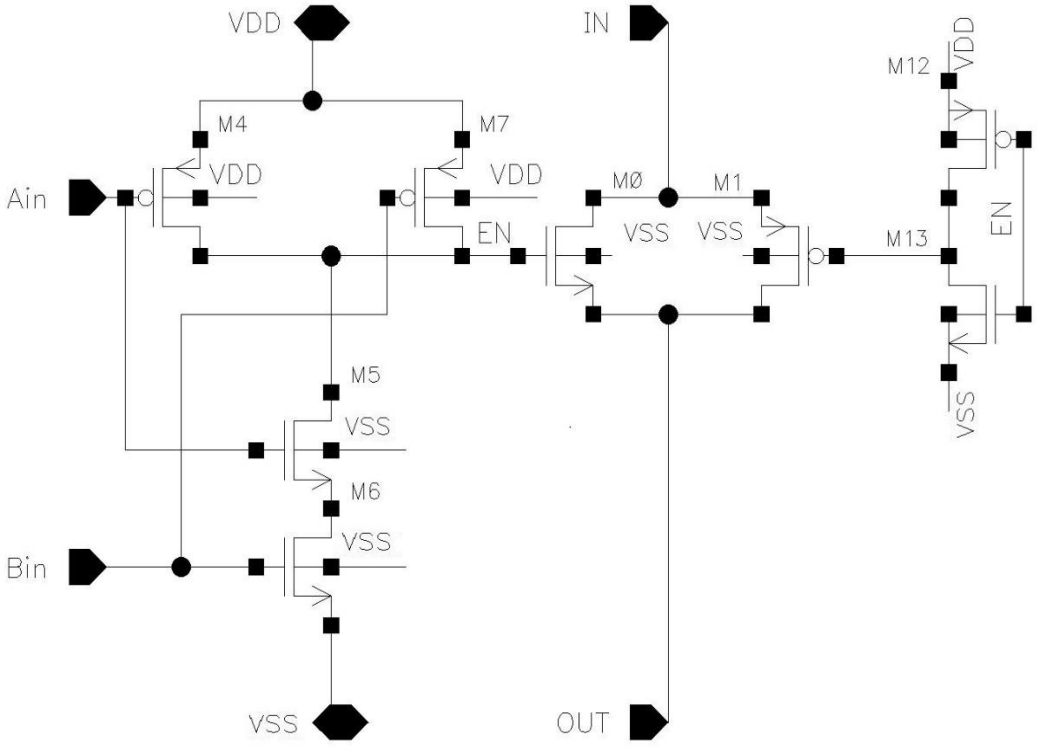

Fig. 3.2: Schematic diagram of switch SWNN.

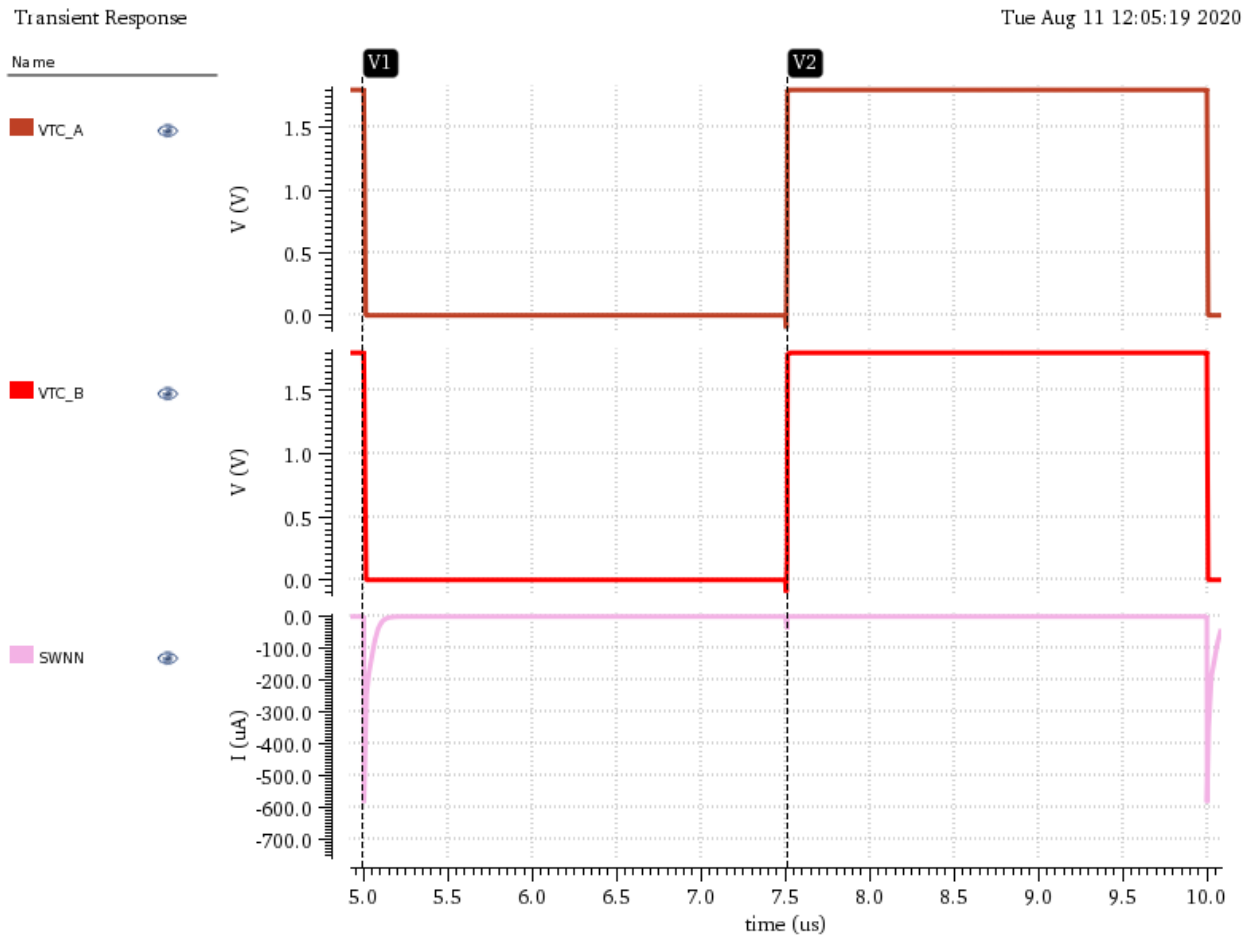

Fig. 3.3 Transient response of switch SWNN.

As can be see in Fig. 3.3, on the first negative edge of A and B signals, the current through the switch SWNN is about 550 µA, then it decreases exponentially with time until it reaches the leakage level.

3.3.2 The switch SWPP

Fig. 3.4 shows the transistor schematic of the switch SWPP. The TG switch is formed by transistors M0 and M1. The logic control circuit is implemented with two inputs NAND gate (M4 – M7), and two cascaded inverters (M3, M2, M8, M9). The width and length of transistor is summarized in Table 3.4. The transient response is presented in Fig. 3.5.

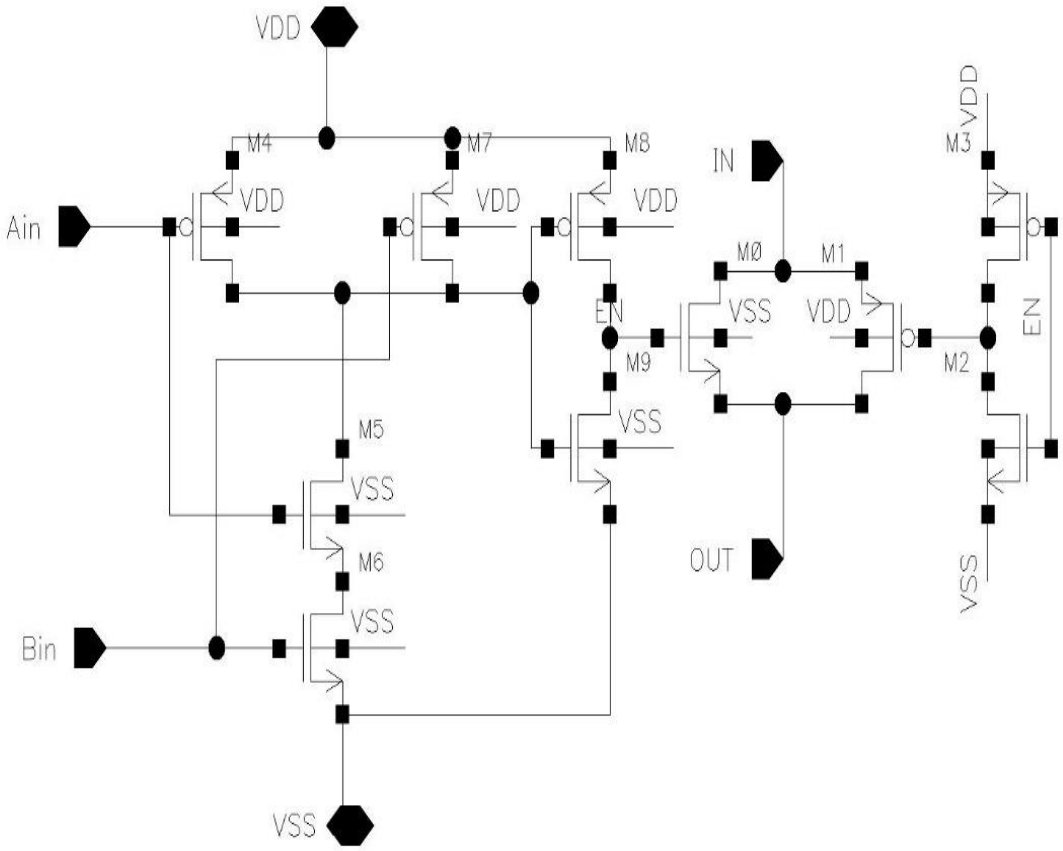

Fig. 3.4: Schematic of the switch SWPP.

Transistor	W	L
M0	300n	200n
M1	300n	200n
M2	220n	200n
M3	220n	200n
M4	220n	200n
M5	800n	220n
M6	220n	220n
M7	220n	200n
M8	220n	200n
M9	220n	200n

Table 3.4: Transistor sizes of the SWPP switch.

In this switch, unlike the SWNN, we can note a smaller dimension in M1 and M2, this is because in this switch flows a low value of current provided by the current source IB2. This switch is used to slow down the discharge rate of the capacitor C. Notice however, the sizing of transistors of this switch is critical for the operation of TA. The most important parameters are the speed and leakage current. We have noted if the switch has a high leakage current, the transistors of current mirror IB2 do not operate in the saturation region and then, the output current of IB2 current source is very different from the expected value. The delay of the logic control circuit is the other important factor for the fast response of this switch. We have sized the transistor of this switch taking into account the minimum delay possible and minimum leakage current.

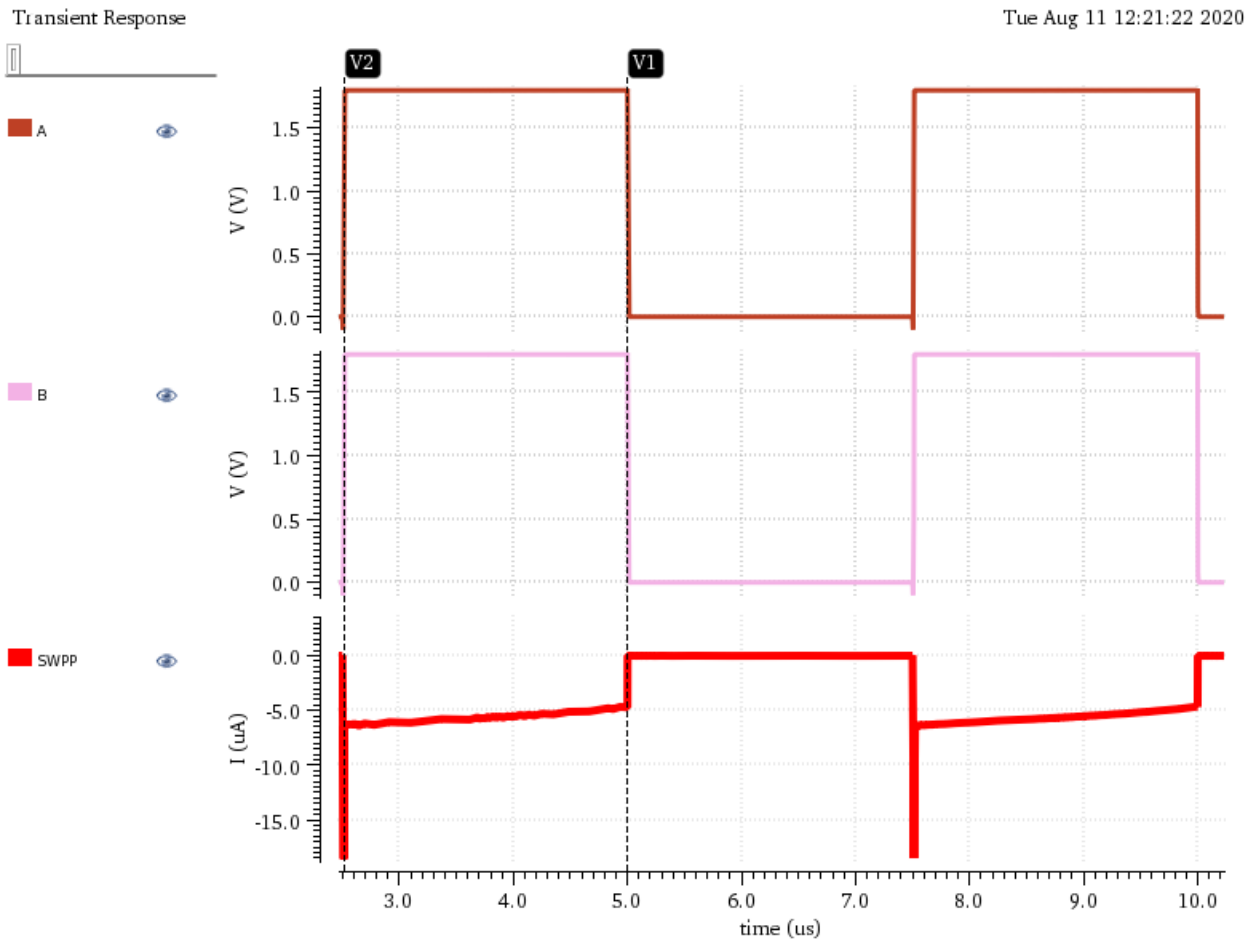

Fig. 3.5 Transient response of the switch SWPP

3.3.3 The switch SWPN

In Fig. 3.5, the transistor schematic of the switch SWPN is shown. The TG switch is formed by transistors M0 and M1. In this case, the logic control circuit is implemented with two inputs NAND gate (M14, M10,

M6, M7), and three cascaded inverters (M2, M3, M4, M5, M15, M11). The width and length of the transistors are summarized in Table 3.5. The transient response is presented in Fig. 3.7.

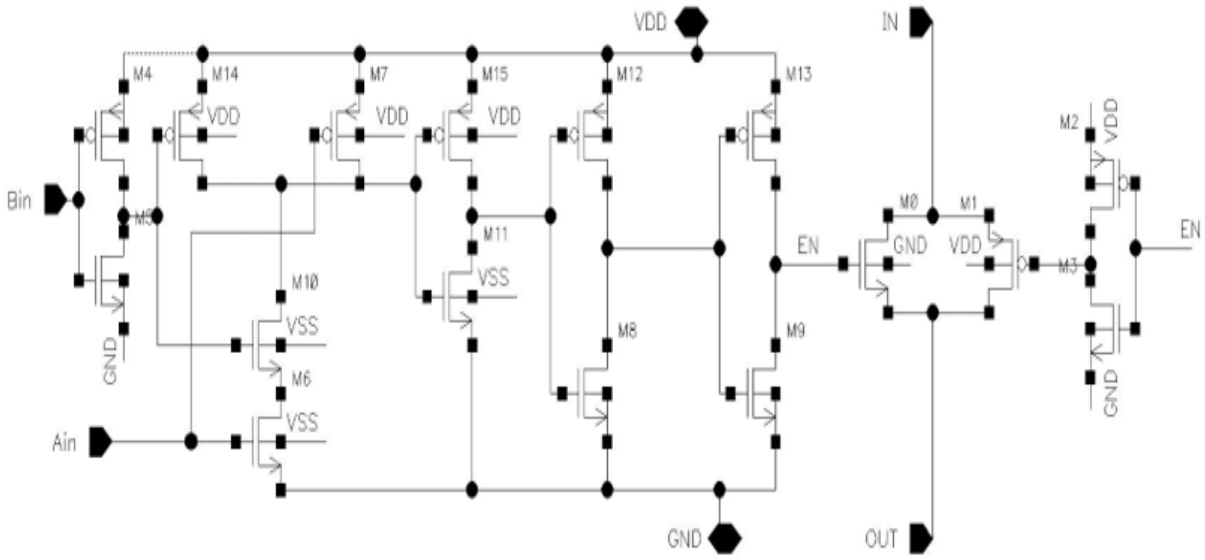

Fig. 3.6: Schematic of the switch SWPN.

Transistor	W	L
M0	3U	200n
M1	3U	200n
M2	220n	200n
M3	220n	200n
M4	220n	200n
M5	220n	200n
M6	220n	220n
M7	220n	200n
M8	540n	200n
M9	540n	200n
M10	220n	200n
M11	220n	200n
M12	1u	200n
M13	1u	200n
M14	220n	200n
M15	220n	200n

Table 3.5: Transistor sizes of the SWPN switch.

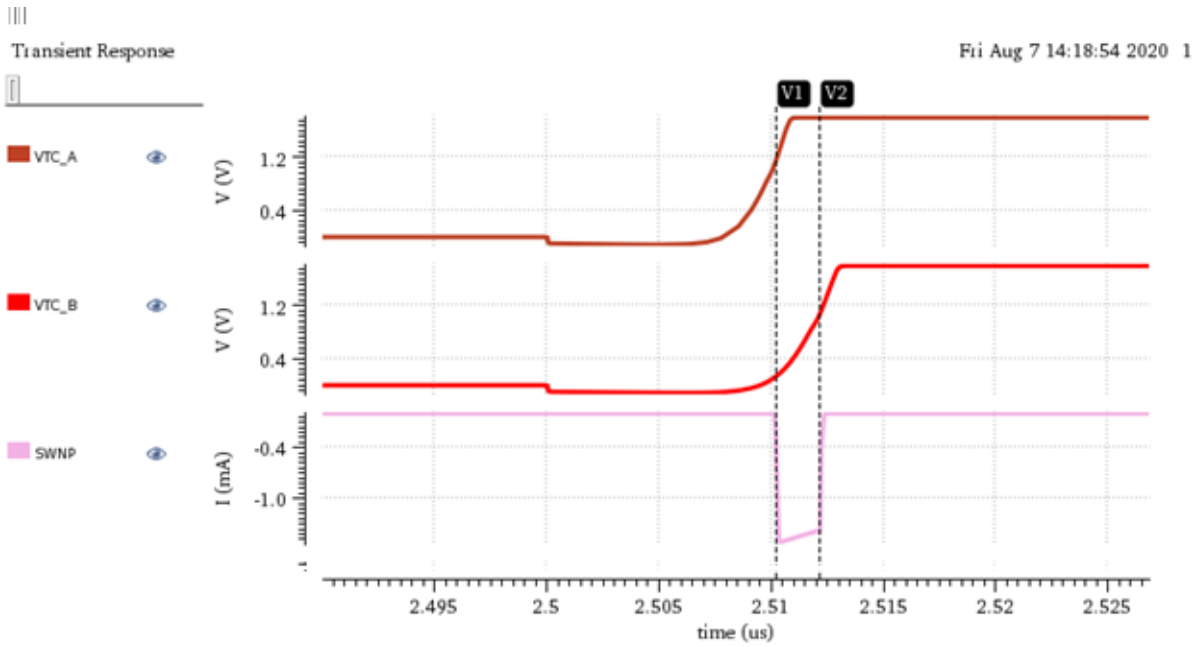

Fig. 3.7 Transient response of the switch SWPN

This switch, unlike the other two, must be the fastest one and with a power consumption not so great for the current mirror to work properly. The switch has a buffer to finely control the delay and then improve its speed. It should be noted that in this switch all the transistors of the three inverters have the minimum size in order to have a fast and balanced rise and fall times.

3.4 The Comparator Design.

The comparator used in the TA is based on an OTA with a buffer. The highest slew rate (19.775 uV/s) of the OTA is required for the proper operation of comparators. The capacitive load of this OTA is 20 fF, which is provides from the input capacitance of the Arbiter and the SAR blocks. The OTA schematic in Fig. 3.8 is a simple structure type (M0 – M3), biased by a cascode current mirror (M4-M7) and a pair of poly resistance as reference resistance. A digital buffer (M8 - M11) is added to enhance the output voltage level and to adjust the delay offset of the comparator. The widths and lengths of the comparator are summarized in Table 3.6.

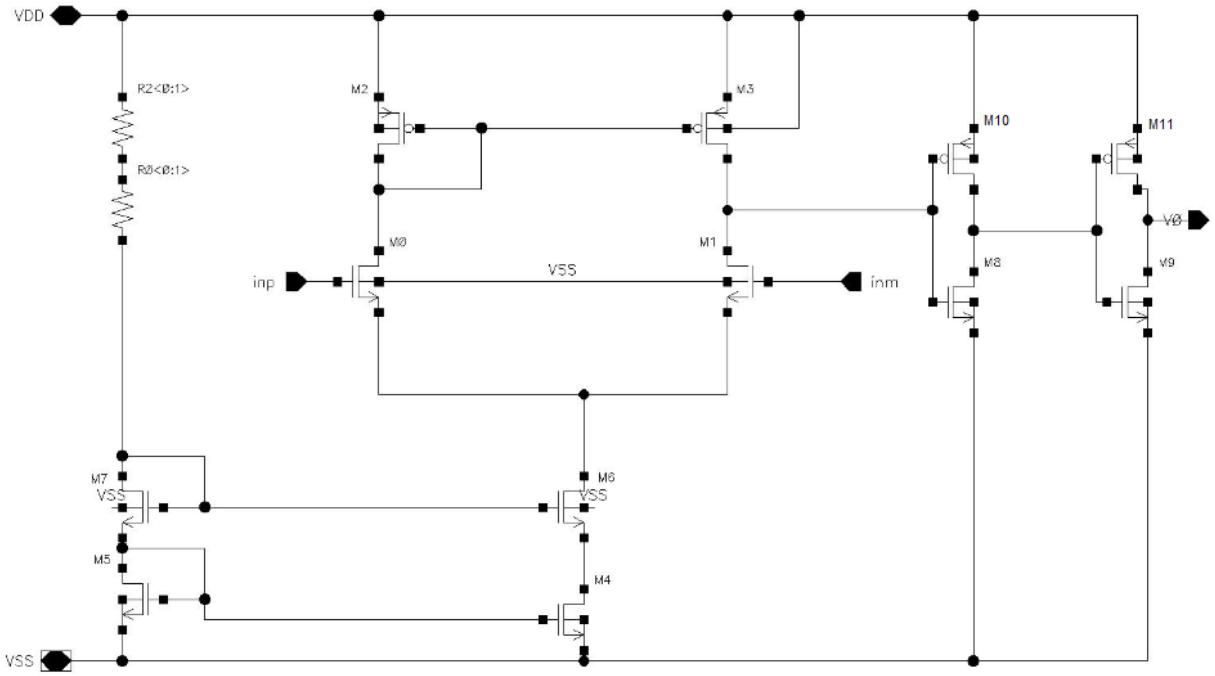

Fig. 3.8: Schematic of Comparator.

Transistor	W	L
M0	1.4u	700n
M1	1.4u	700n
M2	3.46u	720n
M3	3.46u	720n
M4	3u	200n
M5	3u	200n
M6	3u	220n
M7	3u	200n
M8	1.5u	200n
M9	1.5u	200n
M11	3.46u	200n
M12	3.46u	200n

Table 3.6: Transistor sizes of the Comparator.

Fig. 3.9 shows the Bode Diagram of the Comparator circuit. It can be see a DC gain of 10 dB and a bandwidth of 4GHz. The Bandwith is high enough for the present application.

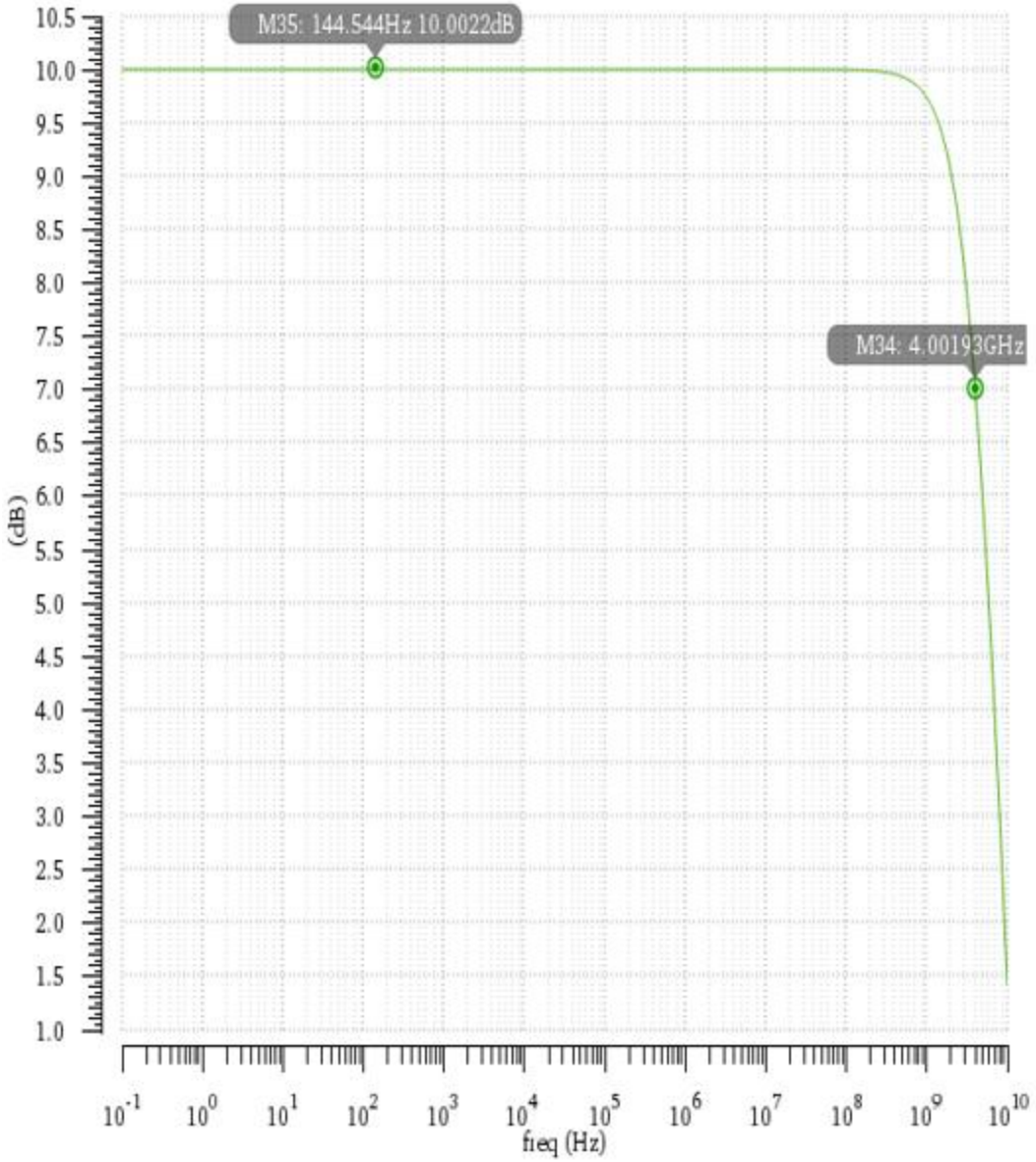

Fig. 3.9: OTA Frequency response.

3.5 Prelayout simulation results

The Fig. 3.10 shows the utilized schematic diagram to perform the pre-layout simulations. Simulations were done using typical process parameters, 1.8 V of supply voltage and room temperature. Signals A and B come each from the two VTC. This testbench is implemented to measure the time gain and the percentage of error. The Vref is implemented with a resistor divider, R4 and R5 in Fig 3.10.

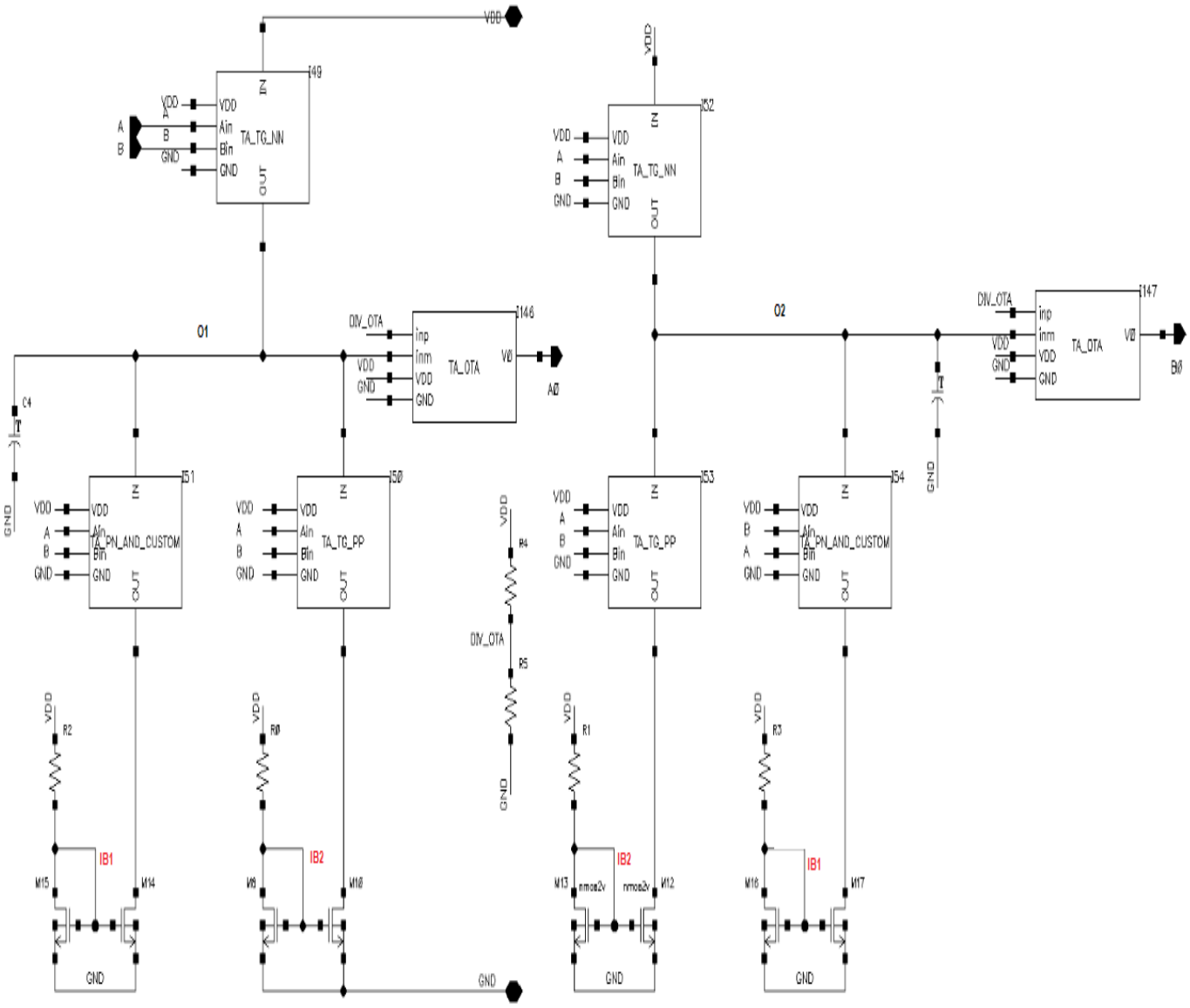

Fig. 3.10: Schematic of TA for simulation in Virtuoso-Cadence.

3.6.1 Transfer curve and gain error

Fig. 3.11 presents the transfer curve of TA when it was implemented with switches of a single transistor.

The percentage of error was calculated using the relationship

*(Measured Time Gain-Expected Time Gain)/Expected Time Gain)*100* (8)

Where the expected time gain is a linear variation from 0 to 200, and the Measured Time Gain is calculated as the ratio of Tout/Tin from collected data of simulations.

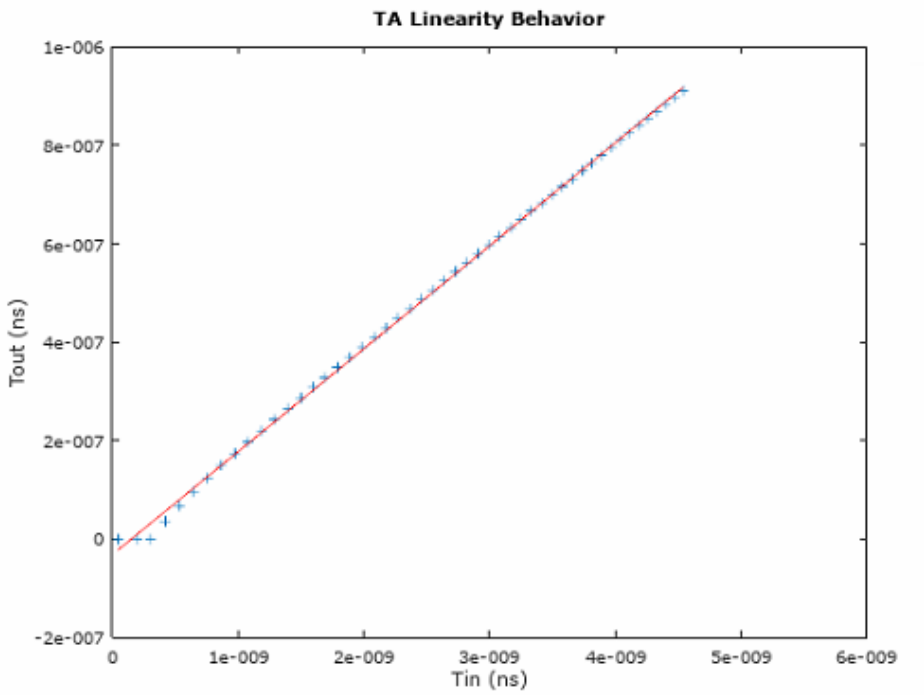

Fig. 3.11: Relationship between ΔTout and ΔTin when implemented with single transistor switches: simulated results (blue stars) and theoretical behavior (solid red line)

VIN	ΔTin	ΔTout	Time Gain	Expected Time Gain	%Error
7.50E-01	4.86E-11	3.83E-17	7.87E-07	0	0
7.55E-01	1.98E-10	3.78E-15	1.90813E-05	200	100.00%
7.60E-01	3.05E-10	2.78E-12	9.11E-03	200	100.00%
7.65E-01	4.21E-10	3.62E-08	85.98574822	200	57.01%
7.70E-01	5.36E-10	6.75E-08	126.0033601	200	37.00%
7.76E-01	6.48E-10	9.63E-08	148.5881808	200	25.71%
7.81E-01	7.59E-10	1.24E-07	163.4805537	200	18.26%
7.86E-01	8.67E-10	1.50E-07	172.9305972	200	13.53%
7.91E-01	9.75E-10	1.74E-07	178.4249385	200	10.79%
7.96E-01	1.08E-09	1.97E-07	182.2386679	200	8.88%
8.01E-01	1.19E-09	2.20E-07	185.3411963	200	7.33%

Table 3.7: TA Pre-layout first design simulation results of the time gain.

The calculated percentage of error from data presented in table 3.7 is shown in Fig. 3.13; to the value is 10% The percentage of error of TA was later reduced using transmission gates switches with the logic control circuit (Fig. 3.2, Fig. 3.4, and Fig 3.6).

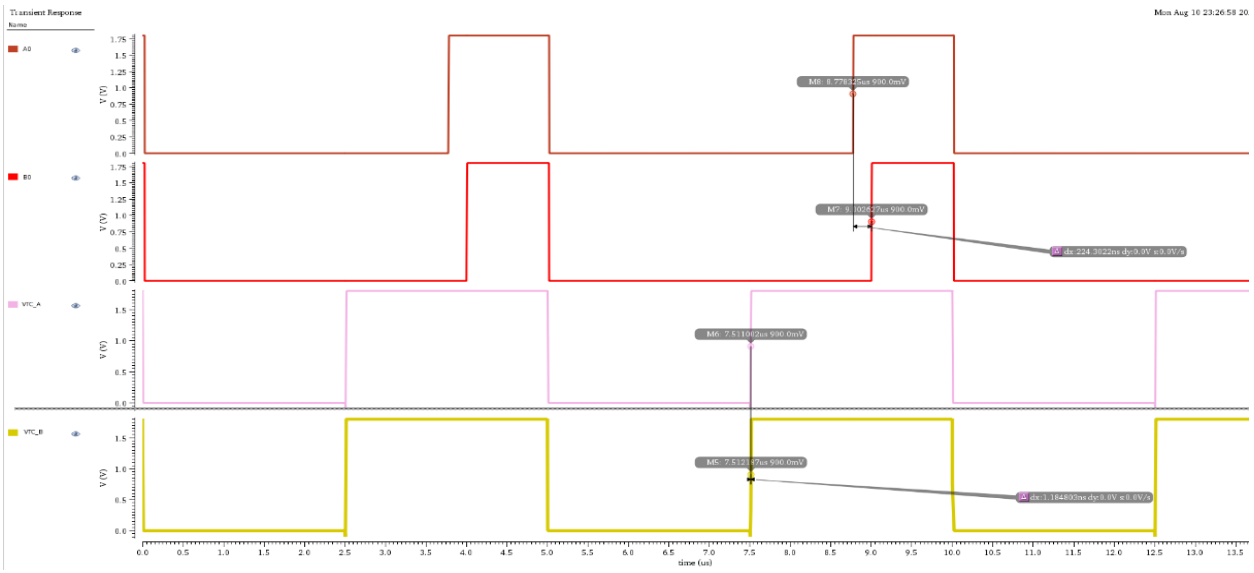

Fig. 3.12: Transient response of TA circuit with a Vref = 750mV, Vin =800 mV, and ΔTin = 1.1818 nS.

In this case, the measured ΔTout = 224.302 nS and the resulting Gain = 189.796919

In Fig. 3.13 we present the transfer curve of TA. The percentage of error was calculated using Ec 8 and the data presented in Table 3.7. The error is less than 7% and the time gain is about 200.

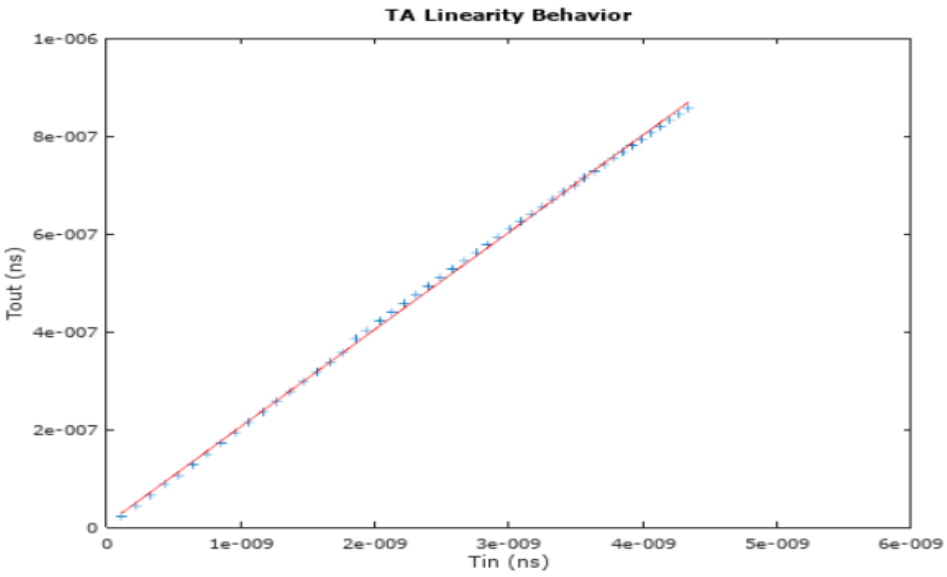

Fig. 3.13: Relationship between ΔTout and ΔTin of TA when implemented with transmission gate switches: simulated results (blue stars) and theoretical behavior (solid red line).

VIN	ΔTin	ΔTout	Time Gain	Expected Time Gain	%Error
7.50E-01	1.88E-19	-3.13E-12	-6.03E-08	0	0
7.55E-01	-2.19E-08	-1.12E-10	195.0044603	200	2.50%
7.60E-01	-4.42E-08	-2.22E-10	198.8748875	200	0.56%
7.65E-01	-6.54E-08	-3.30E-10	198.3030303	200	0.85%
7.70E-01	-8.86E-08	-4.34E-10	203.9834216	200	-1.99%
7.76E-01	-1.06E-07	-5.40E-10	195.7407407	200	2.13%
7.81E-01	-1.28E-07	-6.46E-10	198.3893449	200	0.81%
7.86E-01	-1.50E-07	-7.50E-10	199.786752	200	0.11%
7.91E-01	-1.72E-07	-8.57E-10	200.9105767	200	-0.46%
7.96E-01	-1.94E-07	-9.60E-10	201.5205166	200	-0.76%
8.01E-01	-2.15E-07	-1.06E-09	202.0696143	200	-1.03%

Table 3.8: TA Pre-layout simulation results of the time gain.

Section 4. TA Verification

4.1 System level simulation

To test the TA circuit and VTCs together we have implemented the testbench depicted in Fig. 4.1. In this figure can see two VTCs connected to a pair of buffers, this because it was detected that the TA capacitance affects the linear operation of the VTC. The output of the buffers is connected to the Vref and Vin inputs of TA and, the TA outputs are connected to a pair of load capacitors which simulate the loads to which it will be supported. The frequency of signals used to simulate this Testbench is 200 KHz and the VDD is 1.8 V.

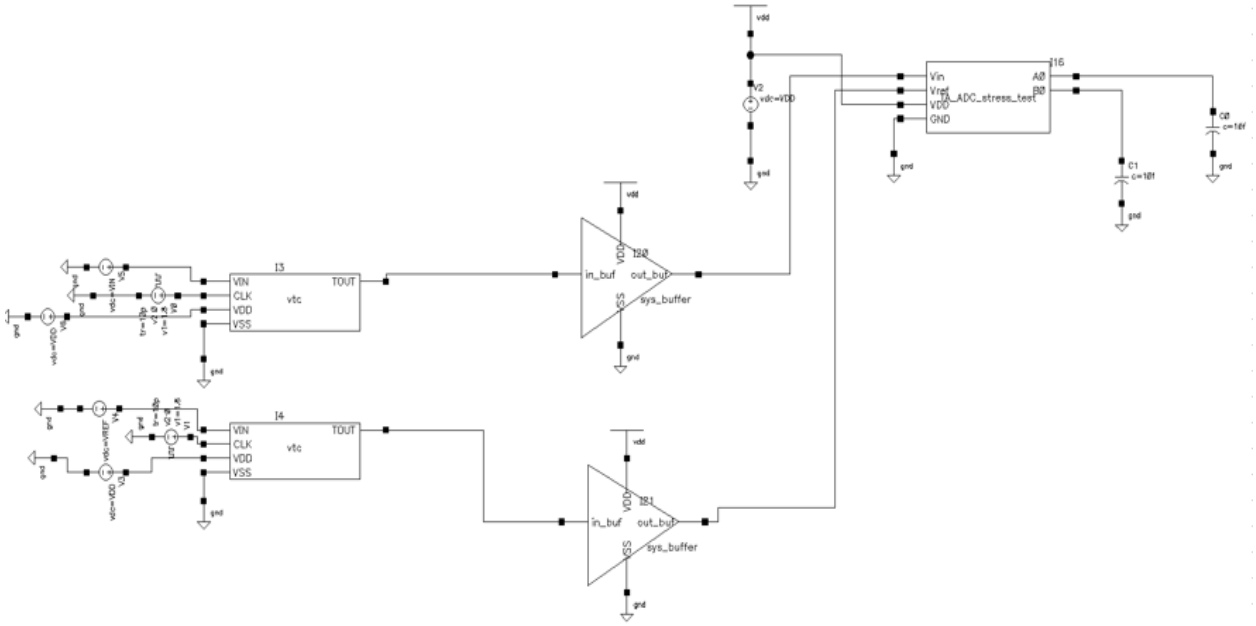

Fig. 4.1: Testbench Schematic to test the performance of TA circuit together the VTC.

In Figs. 4.2, to 4.4, the transient response of TA and VTC is shown. In this simulation we used three different Vin values in order to generate various input time differences between the VTC connected to Vref and Vin.

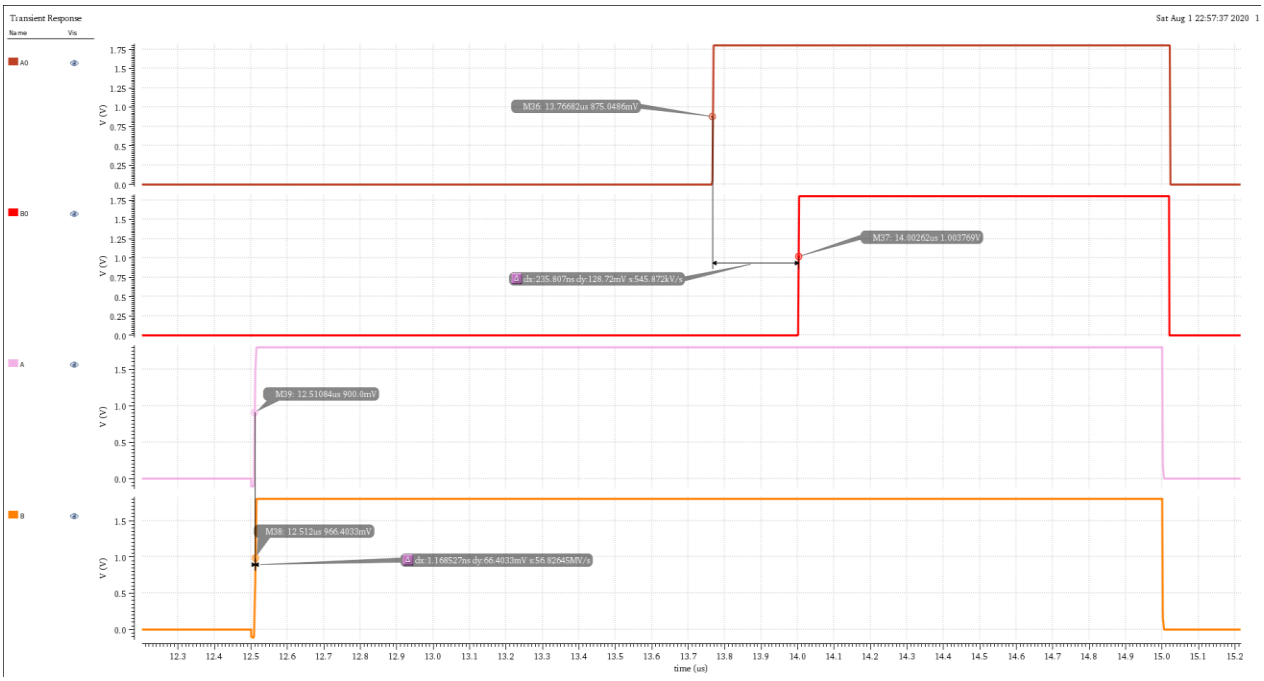

Fig. 4.2: Transient response of TA circuit with a Vref = 750 mV, Vin = 800 mV, and ΔTin = 1.168527 nS.

From results shown in Fig. 4.2, we have calculated a ΔTout = 235.807 nS, and then the is Gain = 201.7985.

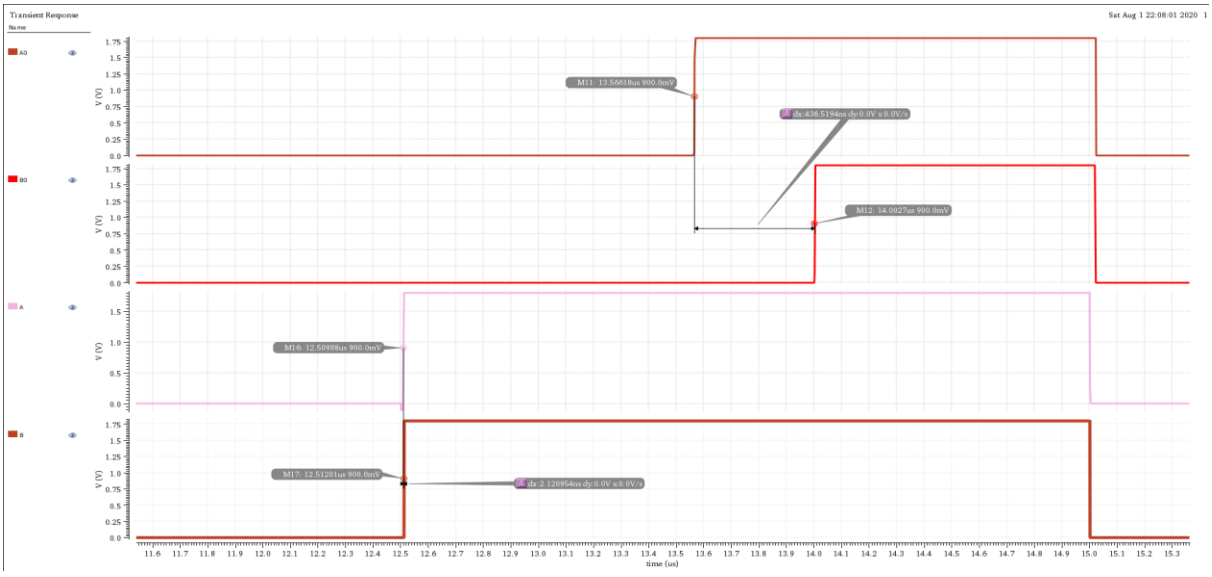

Fig. 4.3: Transient response of TA circuit with a Vref = 750 mV Vin = 850 mV, and ΔTin = 2.120954 nS.

In this case, the measured ΔTout = 436.5194 nS and the resulting Gain = 205.8131497.

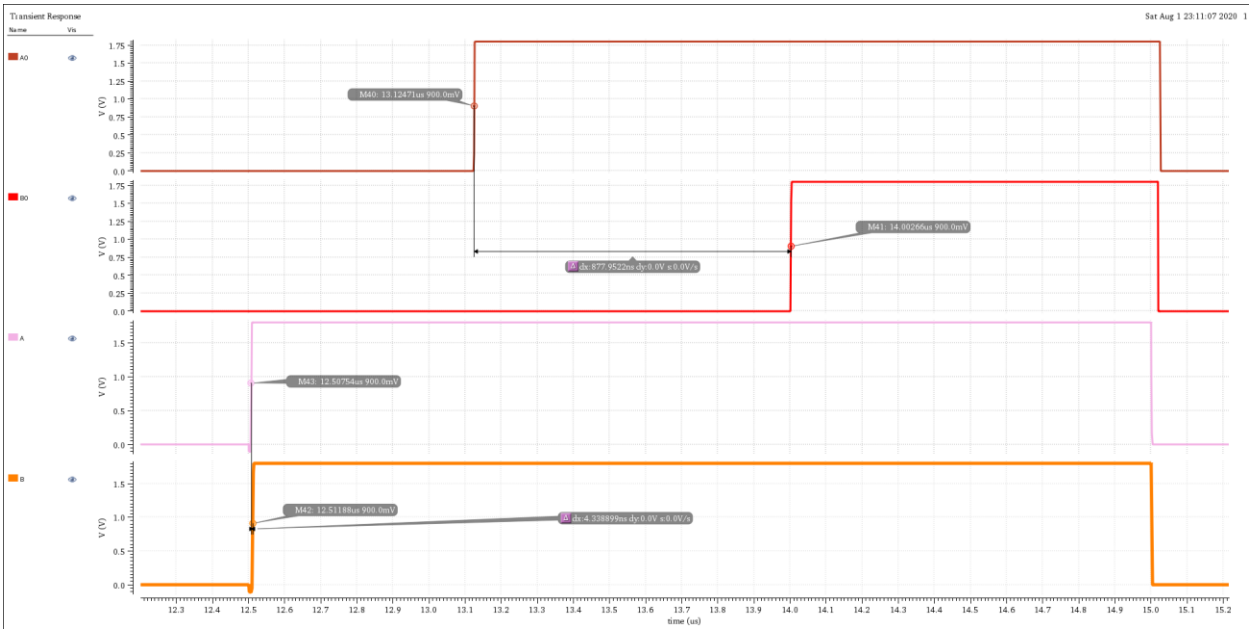

Fig. 4.4: Transient response of TA circuit with a Vref = 750 mV, Vin = 1 V, and ΔTin = 4.338899 nS.

The measured ΔTout = 877.9522 nS, and the resulting Gain = 202.34446572.

Section 5. TA Physical Design

5.1 Layout Design and Verification

The layout of the TA circuit, which is implemented using TSMC 0.18 μm CMOS technology, is designed using CADENCE tools. For illustration purposes, the design is presented first by cells separately, then, all cells of the TA circuit are assembled. The Layout XL tool from CADENCE provide the option to merge these cells together into one cell. Six interconnect layers were used in the layout design, namely, metal 1, metal 2, metal 3, metal 4, metal5, and metal 6. The widths of interconnect layers were defined according to DRC rules of TSMC 0.18 μm CMOS technology. We looked for shorter paths of interconnections in order to minimize parasitic effects in the post-layout response. The layout dimension of the TA is 149.985 μm x 168.536 μm, and area of 25.3 nm^2. The location of the pins was defined in terms of the assigned area and pins locations of other modules in the SAR-ADC floorplan.

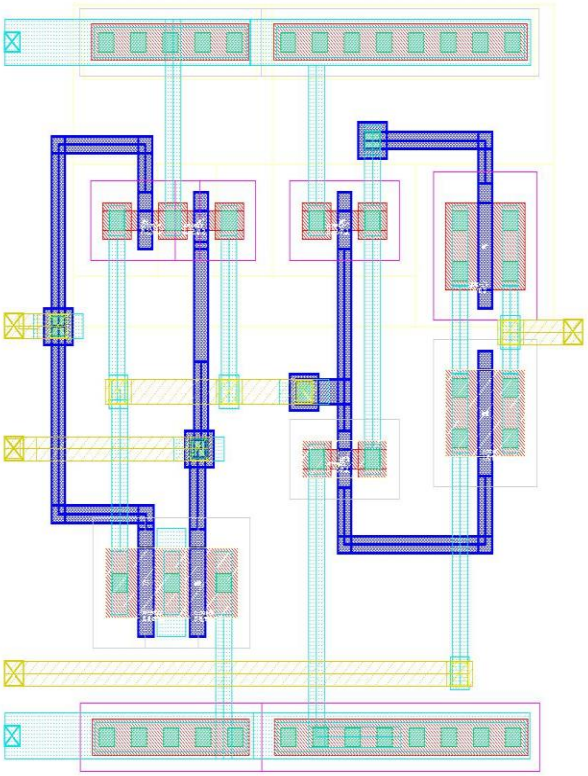

Fig. 5.1: Layout view of the SWNN switch.

Since this switch does not have to be used in other layouts, the dimension is fair and without extra spaces.

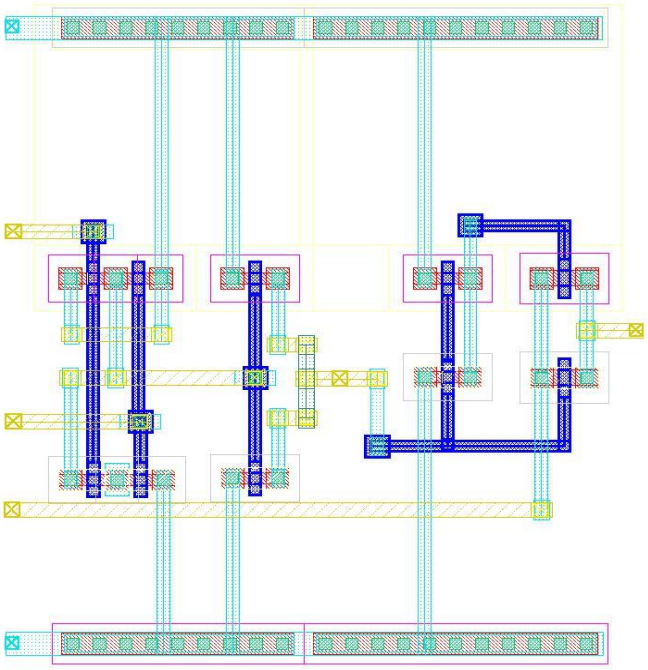

Fig. 5.2: Layout view of the SWPP switch.

The layout of this switch (Fig. 5.2) is seen with even more space at the top and bottom, these spaces are to have a similar height of other blocks in the assembled layout of the TA module.

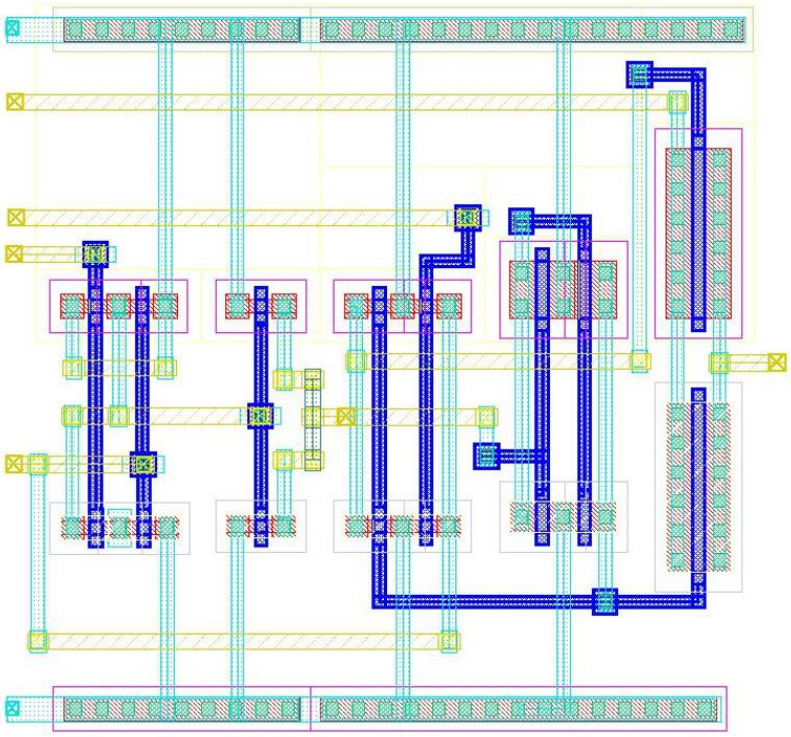

Fig. 5.3: Layout view of the SWPN switch.

This switch is the one with the largest layout of the three switches Fig. 5.3. The larger area is due to more complex logic control circuit.

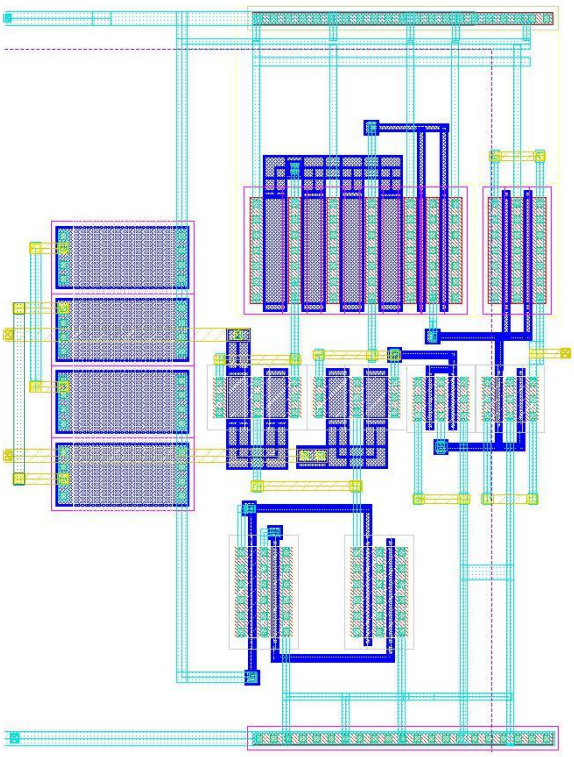

Fig. 5.4: Layout view of the OTA.

The layout of the OTA includes polysilicon resistors that have the same orientation of transistors in order to minimize temperature variations.

The layout of the TA circuit is shown in Fig. 5.5. In this, we note that the larger area is occupied by capacitors and the smallest area occupied by switches, logic control circuit, current mirrors, and comparators. The total layout dimension of the TA cell is 149.985 μm x 168.536 μm and area of 25.3 nm^2 which fulfills the area requirements of the SAR-ADC floorplan. All the cells passed the DRC rules checker and LVS rules checker using Assura tools. The results of these tests are presented in the Annex A, B and C.

Fig. 5.5: Layout view of the TA circuit.

For time limitations, the post layout analysis has to be done as future work.

Conclusions

We have performed the physical designed of an analog time amplifier for a based-time SAR ADC.

The TA presents a maximum-time gain of 200, with a maximum error of 7%. The maximum time-input range is limited to 4.7 nS. The gain can be increased more than 240, but the error is drastically increased.

The VTC, and TA limitations, impact some requirements of the SAR ADC such as higher clock frequency, and therefore, lower power consumption cannot be achieved.

The simulation results of the TA when it is assembled to the VTC and Arbiter modules show some changes in the gain error. However, this is corrected adding buffer between the TA and VTCs.

The physical design of the TA, successfully passed the DRC and LVS analysis, despite the fact that we combined several modules, and that we have used up to 6 level of metals.

References

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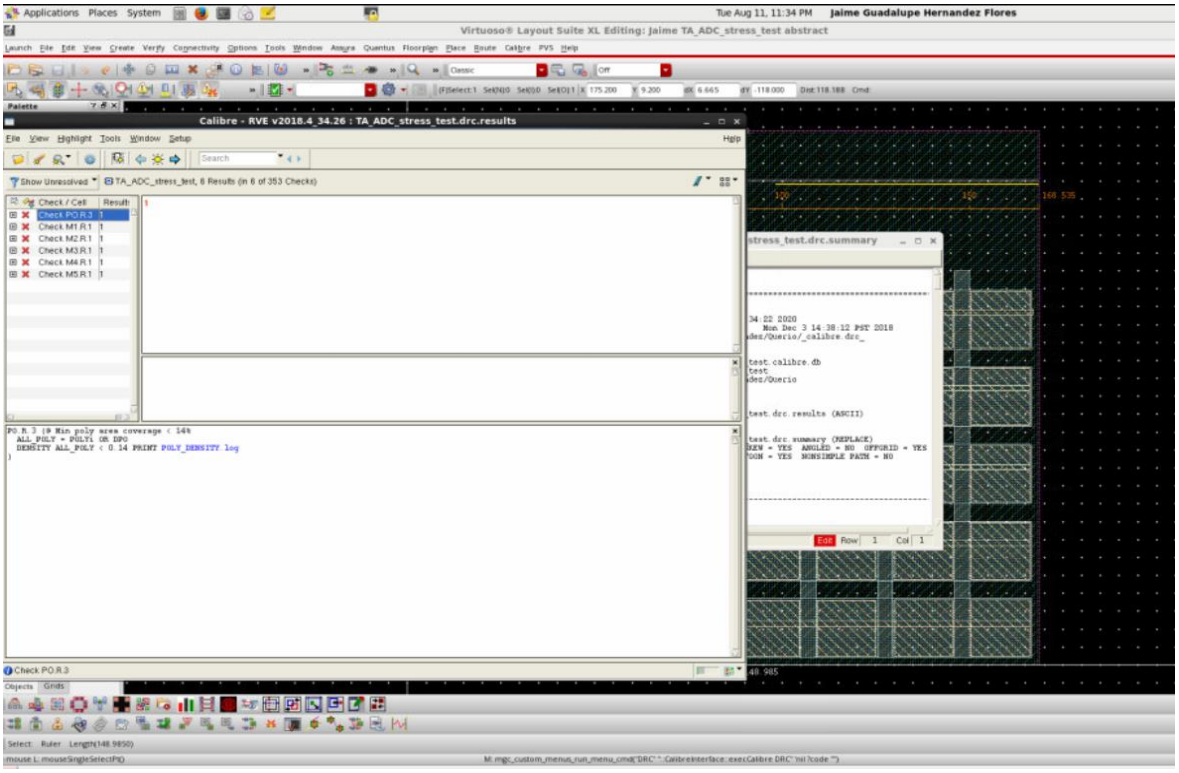
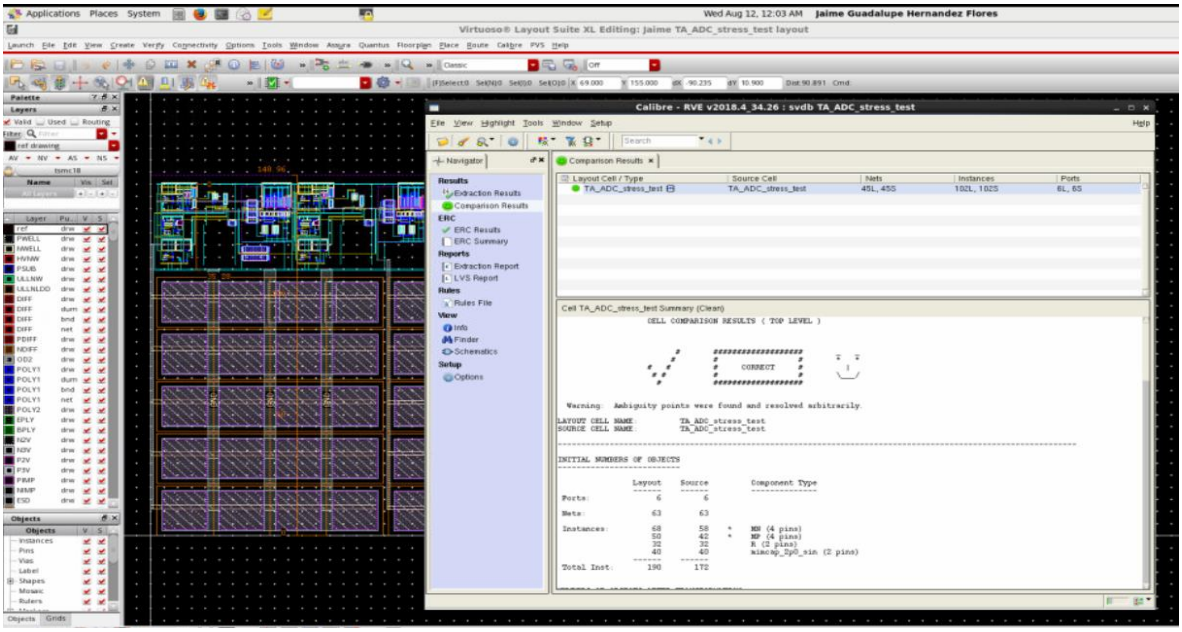
Annex:

A) DRC_CALIBRE:

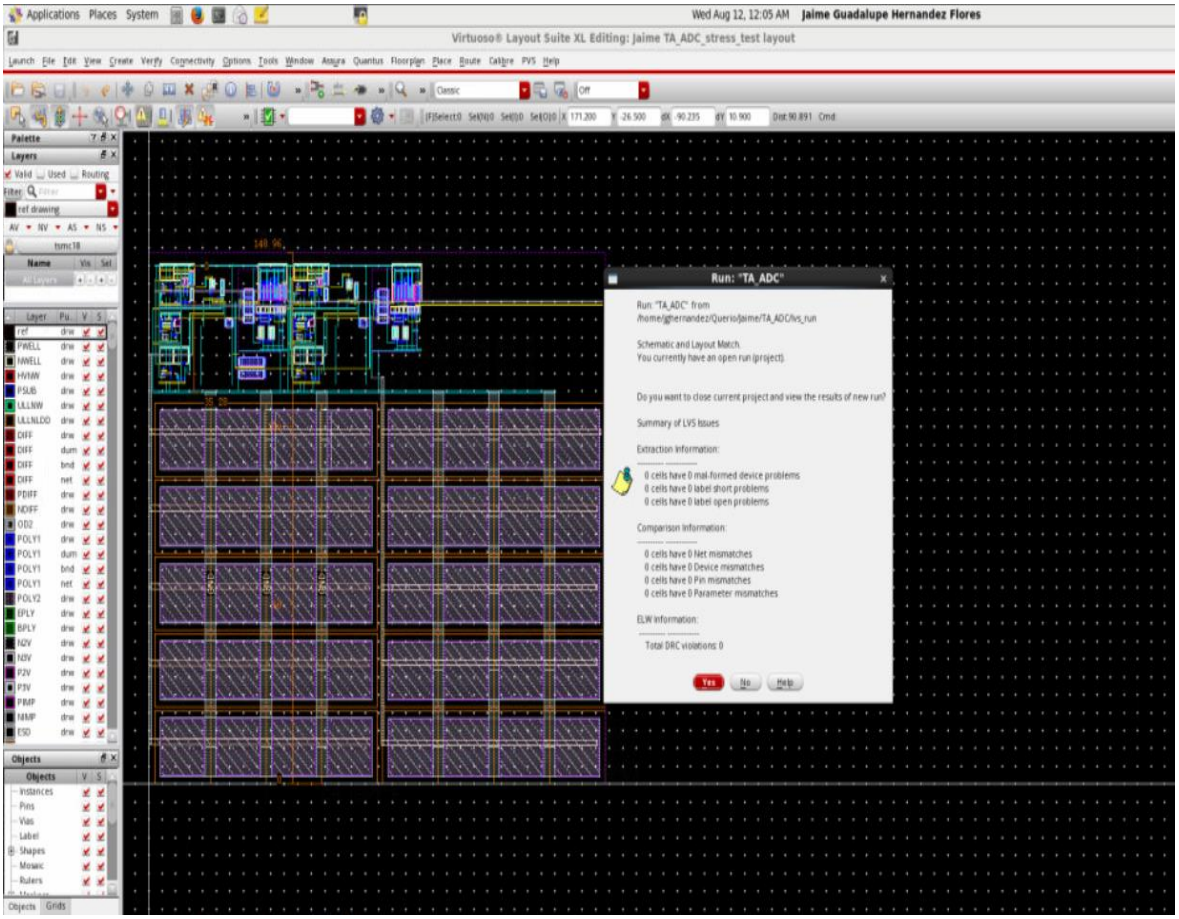


*density metal errors no considered

B) LVS_CALIBRE:



C) LVS_ASSURA:


Applications Places System
Wed Aug 12, 12:05 AM Jaime Guadalupe Hernandez Flores
Virtuoso® Layout Suite XL Editing: Jaime TA_ADC_stress_test layout
Run: "TA_ADC"
Run: "TA_ADC" from
/home/jghernandez/Queries/Jaime/TA_ADC/lvs_run
Schematic and Layout Match.
You currently have an open run (project).
Do you want to close current project and view the results of new run?
Summary of LVS Issues
Extraction Information:
0 cells have 0 mal-formed device problems
0 cells have 0 label short problems
0 cells have 0 label open problems
Comparison Information:
0 cells have 0 Net mismatches
0 cells have 0 Device mismatches
0 cells have 0 Pin mismatches
0 cells have 0 Parameter mismatches
ELW Information:
Total DRC violations: 0
Yes
No
Help