INSTITUTO TECNOLÓGICO
Y DE ESTUDIOS SUPERIORES DE OCCIDENTE

Reconocimiento de validez oficial de estudios de nivel superior según acuerdo secretarial 15018, publicado en el Diario Oficial de la Federación el 29 de noviembre de 1976.

Departamento de Electrónica, Sistemas e Informática

DOCTORADO EN CIENCIAS DE LA INGENIERÍA

METODOLOGÍAS DE OPTIMIZACIÓN DE CAPACITORES DE DESACOPLO PARA REDES DE SUMINISTRO DE POTENCIA EN PLATAFORMAS DE CÓMPUTO

Tesis que para obtener el grado de

DOCTOR EN CIENCIAS DE LA INGENIERÍA

presenta: Aurea Edna Moreno Mojica

Director de tesis: Dr. José Ernesto Rayas Sánchez

Tlaquepaque, Jalisco. Noviembre de 2022

DOCTOR EN CIENCIAS DE LA INGENIERÍA (2022) ITESO, Tlaquepaque, Jal., México

TÍTULO: **Metodologías de optimización de capacitores de desacoplo para redes de suministro de potencia en plataformas de cómputo**

AUTOR: Aurea Edna Moreno Mojica
Ingeniera Electrónica (ITESO, México)
Maestra en Diseño Electrónico (ITESO, México)

DIRECTOR DE TESIS: José Ernesto Rayas Sánchez
Profesor Numerario del Departamento de Electrónica, Sistemas e Informática, ITESO
Ingeniero en Electrónica (ITESO, México)
Maestro en Sistemas Electrónicos (ITESM Campus Monterrey, México)
Doctor en Ingeniería Eléctrica (Universidad McMaster, Canadá)
Senior, IEEE

NÚMERO DE PÁGINAS: xxix, 135

ITESO – The Jesuit University of Guadalajara

Department of Electronics, Systems, and Informatics

DOCTORAL PROGRAM IN ENGINEERING SCIENCES

DECOUPLING CAPACITORS OPTIMIZATION METHODOLOGIES FOR POWER DELIVERY NETWORKS IN COMPUTER PLATFORMS

Thesis to obtain the degree of

DOCTOR IN ENGINEERING SCIENCES

Presents: Aurea Edna Moreno-Mojica

Thesis Director: Dr. José Ernesto Rayas-Sánchez

Tlaquepaque, Jalisco, Mexico
November 2022

TITLE: **Decoupling Capacitors Optimization Methodologies for Power Delivery Networks in Computer Platforms**

AUTHOR: Aurea Edna Moreno-Mojica
Bachelor's degree in electronics engineering (ITESO, Mexico)
Master's degree in electronic design (ITESO, Mexico)

THESIS DIRECTOR: José Ernesto Rayas-Sánchez
Department of Electronics, Systems, and Informatics, ITESO
Bachelor's degree in electronics engineering (ITESO, México)
Master's degree in electrical engineering (ITESM, México)
Ph.D. degree in electrical engineering (McMaster University, Canada)
Senior, IEEE

NUMBER OF PAGES: xxix, 135

To my parents, Pablo and Edna.

To my brother, Pablo R.

For their unconditional support and words of encouragement

that made this achievement possible.

Resumen

Toda plataforma de cómputo requiere de una red de suministro de potencia (PDN, por sus siglas en inglés) para energizar sus dispositivos. Cuando la señales en los diferentes dispositivos de una PDN comienzan a conmutar, provocan picos de corriente que crean ruido de voltaje. El control de ruido fallido en la PDN puede deteriorar el desempeño y provocar fallas funcionales graves en la plataforma de cómputo. El nivel de voltaje requerido por los chips depende del espectro de frecuencia de la corriente que consumen; así un buen diseño de PDN debe tener un perfil de impedancia bajo. Esto se hace colocando varias etapas de capacitores de desacoplo para reducir la impedancia y proporcionar fuentes locales de carga. Estos arreglos de capacitores paralelos introducen frecuencias resonantes que pueden magnificar los problemas de ruido y que se traducen en el dominio del tiempo como caídas de voltaje. Esta tesis doctoral presenta un procedimiento numérico para encontrar las frecuencias resonantes paralelas de un arreglo paralelo de más de dos capacitores, así como ecuaciones analíticas para encontrar las frecuencias resonantes paralelas de un arreglo de tres capacitores, que también aproximan las frecuencias de resonancia de arreglos de más de tres capacitores. Luego presenta varias técnicas de optimización numérica para optimizar el número de capacitores de desacoplo en una PDN y los valores de los elementos de compensación de un regulador de voltaje que aseguran estabilidad, considerando los efectos en el dominio de la frecuencia y del tiempo. Además, esta tesis presenta un enfoque de optimización del rendimiento en el dominio de la frecuencia y del tiempo considerando el impacto de las tolerancias de capacitancia en los capacitores de desacoplo. Finalmente, la tesis proporciona los primeros pasos para obtener un circuito equivalente concentrado de planos discretizados de una PDN que permita colocar capacitores de desacoplo en cualquier lugar de la PDN. Cada metodología propuesta es debidamente validada por casos de prueba adecuados, demostrando la eficiencia de las técnicas propuestas. También se prevén algunas oportunidades de investigación futuras.

Summary

Every computer platform requires a power delivery network (PDN) to energize its devices. When the signals on the different devices of a PDN start switching, they cause current surges that create voltage noise. Unsuccessful noise control on the PDN can cause performance deterioration and severe functional failures on high-speed computer platforms. The acceptable voltage level required by the chips depends on the frequency spectrum of the current they draw, which implies that a good PDN design should have a low impedance profile. This is typically done by placing multiple stages of different decoupling capacitors to bring down the impedance profile and provide local sources of charge. These arrays of parallel capacitors introduce resonant frequencies that can magnify noise problems and are translated into the time domain as voltage droops. This doctoral dissertation first presents a numerical procedure to find the parallel resonant frequencies of an array of more than two decoupling capacitors connected in parallel, as well as an analytical set of equations to find the parallel resonant frequencies of an array of three capacitors connected in parallel, which can be used to approximate the parallel resonant frequencies of more than three decoupling capacitors connected in parallel. It next presents several numerical optimization techniques to tackle the issue of optimizing the number of decoupling capacitors in a PDN and the values of the compensation elements of a Buck voltage regulator that ensure stability, considering both frequency- and time-domain effects. Additionally, this doctoral dissertation presents a frequency- and time-domain yield optimization approach considering the impact of large tolerances in the capacitance of the decoupling capacitors. Finally, this Ph.D. thesis provides the first steps towards obtaining a lumped equivalent circuit of discretized PDN power-ground planes that allows the placement of decoupling capacitors anywhere on the PDN. Each methodology proposed is properly validated by suitable test cases, demonstrating the efficiency of the proposed techniques. Some future research opportunities are also envisioned.

Acknowledgements

The author wishes to express her sincere appreciation to Dr . José Ernesto Rayas-Sánchez, professor of the Department of Electronics, Systems, and Informatics at ITESO, and director of research in the Computer-Aided Engineering of Circuits and Systems (CAECAS) group at ITESO, for his encouragement, expert guidance and keen supervision as doctoral thesis director throughout the course of this work. The author thanks Dr. Zabdiel Brito-Brito, now at the Polytechnic University of Catalonia, Spain, for his feedback during the initial part of my PhD research. She also thanks Dr. Omar Humberto Longoria-Gándara, Dr. Esteban Martínez-Guerrero, Dr. José Luis Chávez-Hurtado, and Dr. Francisco Elías Rangel-Patiño, members of his Ph.D. Thesis Committee, for their interest, assessment, and suggestions.

Special thanks are due to Dr. Felipe de Jesús Leal-Romo, from Apple, for fruitful cooperation and helpful technical discussions.

It is the author's pleasure to acknowledge fruitful collaboration and stimulating discussions with her colleagues of CAECAS research group at ITESO – The Jesuit University of Guadalajara: Francisco Rangel-Patiño, José Luis Chávez-Hurtado, Felipe de Jesús Leal-Romo, Roberto Loera-Díaz and Enrique Raúl Villa-Loustaunau.

The author has greatly benefited from working with PathWave Advanced Design System (ADS) developed by Keysight. The author is grateful to Dr. James Rautio, President of Sonnet Software, for making the Sonnet Suites available for this work.

The author gratefully acknowledges the financial assistance through a scholarship granted by the *Consejo Nacional de Ciencia y Tecnología* (CONACYT), Mexican Government, as well as financial support provided by ITESO. She also thanks the IEEE Microwave Theory and Technology Society, for the Graduate Fellowship granted in 2020.

Finally, special thanks are due to my family: my parents, my brother, and my husband, for their understanding, patience, and continuous loving support.

Contenido

Resumen ……..……. vii

***Summary* …… ix**

Agradecimientos ……... xi

Contenido ……. xiii

***Contents* ……... xvii**

Lista de figuras …..…….. xxi

Lista de tablas …...…….. xxix

Introducción ……..…….. 1

1. Un estudio sobre las frecuencias resonantes de un arreglo de capacitores de desacoplo para aplicaciones de PDN ……..… 5

1.1 FRECUENCIA RESONANTE EN SERIE DE UN CAPACITOR DE DESACOPLO ……..... 6

1.2 CAPACITORES DE DESACOPLO IDÉNTICOS EN PARALELO …… 7

1.3 DOS CAPACITORES DE DESACOPLO DIFERENTES EN PARALELO …….. 8

1.4 MÁS DE DOS CAPACITORES DE DESACOPLO DE DIFERENTES VALORES EN PARALELO 9

1.5 INVESTIGANDO OTRAS RESPUESTAS CIRCUITALES DE TRES CAPACITORES ESPACIADOS UNA DÉCADA ……... 12

1.6 CALCULANDO LAS FRECUENCIAS DE RESONANCIA PARALELAS ……..……..……... 14

1.7 FÓRMULAS ANALÍTICAS PARA CAPACITORES DE DESACOPLO EN PARALELO …… 17

1.7.1 Un solo capacitor de desacoplo ……. 17

1.7.2 Dos capacitores de desacoplo en paralelo ……. 19

1.7.3 Tres capacitores de desacoplo en paralelo ……. 20

1.7.4 Mas de tres capacitores de desacoplo en paralelo ……. 23

1.8 FÓRMULAS ANALÍTICAS PARA CAPACITORES DE DESACOPLO EN PARALELO – CASOS DE ESTUDIO ……. 23

1.9 CONCLUSIONES ……... 27

2 Desempeño de la PDN en el dominio de la frecuencia y del tiempo …… 29

2.1 REPRESENTANDO LA ESTRUCTURA DE LA PDN 30
2.2 UN ESTUDIO SOBRE LOS EFECTOS DEL CAPACITOR EN LA PDN EN EL DOMINIO DE LA FRECUENCIA Y DEL TIEMPO 32
2.2.1 Experimento de cribado 33
2.3 CONCLUSIONES 39
3 Optimización del perfil de impedancia y caída de voltaje de la red de suministro de potencia 41
3.1 OPTIMIZACIÓN DE UNA PDN COMBINANDO EFECTOS EN EL DOMINIO DE LA FRECUENCIA Y DEL TIEMPO – PRIMER ENFOQUE 42
3.2 OPTIMIZACIÓN DE UNA PDN COMBINANDO EFECTOS EN EL DOMINIO DE LA FRECUENCIA Y DEL TIEMPO – SEGUNDO ENFOQUE 48
3.3 OPTIMIZACIÓN DE UNA PDN COMBINANDO EFECTOS EN EL DOMINIO DE LA FRECUENCIA Y DEL TIEMPO – TERCER ENFOQUE 51
3.4 CONCLUSIONES 53
4 Optimizando un regulador de voltaje tipo Buck y el número de capacitores de desacoplo para una aplicación de PDN 55
4.1 MODELANDO EL REGULADOR DE VOLTAJE 56
4.2 METODOLOGÍA PROPUESTA PARA OPTIMIZAR EL REGULADOR DE VOLTAJE Y LOS CAPACITORES DE DESACOPLO 57
4.2.1 Paso 1: Optimizar el número de capacitores en la PDN asumiendo un VR ideal 59
4.2.2 Paso 2: Optimizar la compensación de un regulador de voltaje tipo *state average* para la PDN 60
4.2.3 Paso 3: Optimizar el número de capacitores en la PDN usando el regulador de voltaje tipo *state average* 61
4.3 RESULTADOS Y DISCUSIÓN 61
4.4 CONCLUSIONES 65
5 Optimización en el dominio de la frecuencia y del tiempo de una red de suministro de potencia sujeta a tolerancias grandes de los capacitores de desacoplo 67

5.1 CAPACITORES DE DESACOPLO DE LA PDN 68
5.2 ANÁLISIS ESTADÍSTICO DE UNA RED DE SUMINISTRO DE POTENCIA 69
5.2.1 Estimando cuantas simulaciones son necesarias 71
5.2.2 Resultados del análisis estadístico 73
5.3 OPTIMIZACIÓN DEL RENDIMIENTO DE LA PDN 75
5.3.1 Formulación de la optimización del rendimiento 76
5.3.2 Resultados de la optimización del rendimiento 77
5.4 CONCLUSIONES 78
6 Modelo circuital equivalente concentrado para placas paralelas sin pérdidas basado en la física 81
6.1 SIMULACIONES ELECTROMAGNÉTICAS EN SONNET 82
6.1.1 Placas paralelas Caso 1 83
6.1.2 Placas paralelas Caso 2 85
6.2 MODELO EQUIVALENTE CONCENTRADO DE LAS PLACAS PARALELAS 88
6.2.1 Modelo equivalente concentrado implementado en ADS 92
6.3 MODELOS EQUIVALENTES FÍSICOS DE LAS PLACAS PARALELAS 92
6.3.1 Valores de los componentes concentrados usando subsecciones de placa paralela ideal (IPPS) 92
6.3.2 Valores de los componentes concentrados usando aproximación de microcinta ideal (IMLA) 93
6.3.3 Valores de los componentes concentrados usando las fórmulas de Walker (WF) 95
6.4 MODELO EQUIVALENTE CONCENTRADO VS. SIMULACIÓN ELECTROMAGNÉTICA DE LAS PLACAS PARALELAS 96
6.4.1 Caso 1 97
6.4.2 Caso 2a ..... .99
6.4.3 Caso 2b 100
6.4.4 Caso 2c 103
6.4.5 Caso 2d 105
6.4.6 Discusión 106
6.5 CONCLUSIONES 106

General Conclusiones **……. 109**

Conclusiones Generales ……. 113

Apéndice ……... 119

A. Lista de reportes internos de investigación …….. 121

B. Lista de publicaciones ……. 123

Bibliografía ……. 125

Índice de autores ……. 131

Índice de términos ……... 133

Contents

Resumen ..... **vii**

Summary ..... **ix**

Acknowledgements ..... **xi**

Contenido ..... **xiii**

Contents ..... **xvii**

List of Figures ..... **xxi**

List of Tables ..... **xxix**

Introduction **1**

1. A Study on the Resonant Frequencies of an Array of Decoupling Capacitors for PDN Applications **5**

1.1. SERIES RESONANT FREQUENCY OF A DECOUPLING CAPACITOR 5

1.2. IDENTICAL DECOUPLING CAPACITORS IN PARALLEL 6

1.3. TWO DIFFERENT DECOUPLING CAPACITORS IN PARALLEL 8

1.4. MORE THAN TWO DECOUPLING CAPACITORS OF DIFFERENT VALUES IN PARALLEL 9

1.5. INVESTIGATING OTHER CIRCUITAL RESPONSES WITH THREE CAPACITORS SPACED ONE DECADE APART 12

1.6. CALCULATING THE PARALLEL RESONANT FREQUENCIES 14

1.7. ANALYTICAL FORMULAS FOR PARALLEL DECOUPLING CAPACITORS 17

1.7.1 Single Decoupling Capacitor 17

1.7.2 Two Parallel Decoupling Capacitors 19

1.7.3 Three Parallel Decoupling Capacitors 20

1.7.4 More than Three Parallel Decoupling Capacitors 23

1.8. ANALYTICAL FORMULAS FOR PARALLEL DECOUPLING CAPACITORS – TEST CASES 23

1.9. CONCLUSIONS 27

2. PDN Frequency- and Time-Domain Performances 29

2.1. REPRESENTING THE PDN STRUCTURE..... 30

2.2. A STUDY ON CAPACITOR EFFECTS OF A PDN IN THE FREQUENCY- AND TIME-DOMAIN 32

2.2.1 Screening Experiment..... 33

2.3. CONCLUSIONS 39

3. Power Delivery Network Impedance Profile and Voltage Droop Optimization.....41

3.1. OPTIMIZATION OF A PDN COMBINING FREQUENCY- AND TIME-DOMAIN EFFECTS: FIRST APPROACH..... 42

3.2. OPTIMIZATION OF A PDN COMBINING FREQUENCY AND TIME DOMAIN EFFECTS – SECOND APPROACH..... 48

3.3. OPTIMIZATION OF A PDN COMBINING FREQUENCY AND TIME DOMAIN EFFECTS – THIRD APPROACH..... 51

3.4. CONCLUSIONS 53

4. Optimizing a Buck Voltage Regulator and the Number of Decoupling Capacitors for a PDN Application 55

4.1. MODELING THE VOLTAGE REGULATOR..... 56

4.2. PROPOSED METHODOLOGY FOR OPTIMIZING THE VOLTAGE REGULATOR AND THE DECOUPLING CAPACITORS 57

4.2.1 Step 1: Optimizing the Number of Capacitors in the PDN Assuming an Ideal VR 59

4.2.2 Step 2: Optimizing the Compensation of a State Average Buck VR for the PDN 60

4.2.3 Step 3: Optimizing the Number of Capacitors in the PDN using a State Average Buck VR..... 61

4.3. RESULTS AND DISCUSSION..... 61

4.4. CONCLUSIONS 65

5. Frequency- and Time-Domain Yield Optimization of a Power Delivery Network Subject to Large Decoupling Capacitor Tolerances.....67

5.1. PDN DECOUPLING CAPACITORS 68
5.2. STATISTICAL ANALYSIS OF A POWER DELIVERY NETWORK 69
5.2.1 Estimating the Number of Outcomes for Reliable Monte Carlo Analysis 71
5.2.2 Statistical Analysis Results 73
5.3. YIELD OPTIMIZATION OF THE PDN 75
5.3.1 Yield Optimization Formulation 76
5.3.2 Yield Optimization Results 77
5.4. CONCLUSIONS 78

6. Physics-Based Lumped Circuit Model for Lossless Parallel Plates 81

6.1. SONNET EM SIMULATIONS 82
6.1.1 Parallel Planes Case 1 83
6.1.2 Parallel Planes Case 2 85
6.2. PARALLEL PLANE EQUIVALENT LUMPED MODEL 88
6.2.1 Equivalent Lumped Circuit Model Implementation in ADS 92
6.3. PARALLEL PLANE EQUIVALENT PHYSICAL MODELS 92
6.3.1 Lumped Component Values Using Ideal Parallel Plate Subsections (IPPS) 92
6.3.2 Lumped Component Values using Ideal Microstrip Line Approximation (IMLA) 93
6.3.3 Lumped Component Values Using Walker's Formulas (WF) 95
6.4. LUMPED EQUIVALENT CIRCUIT VS FULL WAVE EM SIMULATION OF PARALLEL PLATES 96
6.4.1 Case 1 97
6.4.2 Case 2a 99
6.4.3 Case 2b 100
6.4.4 Case 2c 103
6.4.5 Case 2d 105
6.4.6 Discussion 106
6.5. CONCLUSIONS 106

General Conclusions 109

Conclusiones generales 113

Appendix **119**

A. List of Internal Research Reports 121

B. List of Publications 123

Bibliography **125**

Author Index **131**

Subject Index **133**

List of Figures

Fig. 1.1 One-stage model of a realistic decoupling capacitor and its behavior. 6

Fig. 1.2 Impedance profile of identical decoupling capacitors in parallel. $Z_p(1)$ is the impedance of a single capacitor, $Z_p(2)$ is the impedance of two capacitors in parallel, and $Z_p(3)$ is the impedance of three capacitors in parallel. It is confirmed that the equivalent series resonant frequency remains the same. 7

Fig. 1.3 Impedance profile of two individual capacitors (self-impedance, Z_s) showing the individual series resonant frequencies and the frequency where the two impedance profiles cross. 8

Fig. 1.4 Impedance profile of two capacitors in parallel of different value showing the impedance peak at the parallel resonant frequency. 9

Fig. 1.5 Impedance profile of three capacitors in parallel of different value showing the impedance peaks and the analytical PRFs calculated with (1-5). 10

Fig. 1.6 Impedance profile of three individual capacitors showing the individual SRFs and the frequency where the adjacent impedance profiles cross. 10

Fig. 1.7 Impedance profile of three individual capacitors of different value spaced one decade apart showing the individual SRFs and the frequency where the adjacent impedance profiles cross. 11

Fig. 1.8 Impedance profile of three capacitors in parallel of different value spaced one decade apart showing the impedance peaks and the analytical PRFs calculated with (1-5) 11

Fig. 1.9 Imaginary part of the impedance of three capacitors in parallel of different value spaced one decade apart (thick green trace) and the impedance profile of the capacitors in parallel (thin blue trace). 12

Fig. 1.10 Zoom-in on the low PRF of Fig. 1.9. 13

Fig. 1.11 Zoom-in on the high PRF of Fig. 1.9. 13

Fig. 1.12 Calculation in wxMaxima of the parallel impedance of three capacitors and its imaginary part. 14

Fig. 1.13 Test 1: Impedance profile of three capacitors in parallel of different value showing the analytical PRFs calculated with (1-5) and the numerical PRFs found matching the actual PRFs. 15

Fig. 1.14 Test 2: Impedance profile of three capacitors in parallel of different value showing the analytical PRFs calculated with (1-5) and the numerical PRFs found matching the actual PRFs. 15

Fig. 1.15 Test 3: Impedance profile of three capacitors in parallel of different value showing the analytical PRFs calculated with (1-5) and the numerical PRFs found matching the actual PRFs. 16

Fig. 1.16 Test 4: Impedance profile of three capacitors in parallel of different value showing the analytical PRFs calculated with (1-5) and the numerical PRFs found matching the actual PRFs. 16

Fig. 1.17 Test 4: Impedance profile of three capacitors in parallel of different value showing the analytical PRFs calculated with (1-5) and the numerical PRFs found matching the actual PRFs. 17

Fig. 1.18 Parallel resonant frequencies for an array of three parallel decoupling capacitors. These frequencies can be calculated in an exact manner using formulas (1-25)-(1-29). 21

Fig. 1.19 Applying formulas (1-25)-(1-29) to approximate the PRFs for cases with more than three decoupling capacitors in parallel: a) the case of 4 capacitors, b) the case of 5 capacitors. 22

Fig. 1.20 Series resonant frequencies of four decoupling capacitors in parallel: a) complete impedance profile; zoom-ins to compare the calculated SRF using (1-8) versus the actual SRF in red for b) capacitor 4, c) capacitor 3, d) capacitor 2, e) capacitor 1. It is confirmed that the equivalent SRFs can be estimated accurately enough with (1-8), no matter how many capacitors are placed in parallel. 27

Fig. 2.1 Typical relationship between the PDN frequency-domain impedance profile and transient-domain voltage droop [Leal-Romo-20], [Zheng-03]. 30

Fig. 2.2 Power delivery network layout of an Intel® Xeon® platform (courtesy of Intel®). 31

Fig. 2.3 Circuit describing the on-die capacitance and package inductance viewed from two different perspectives: a) from the board; b) from the die. 32

Fig. 2.4 Lumped equivalent circuit of the power delivery layout schematic of Intel® Xeon® platform. 33

Fig. 2.5 Transient voltage response for all nine runs of the screening experiment in Table 2.1, using a current step with a rise time of 50 ns. 34

Fig. 2.6 Impedance profile for all nine runs of the screening experiment in Table 2.1. 35

Fig. 2.7 Normal plot showing the significant and not significant effects for the current step analysis, using a current step with a rise time of 50 ns and all capacitor types have a minimum of 1 capacitor. 35

Fig. 2.8 Normal plot of the significant and not significant effects for the impedance profile, all capacitor types have a minimum of 1 capacitor. 36

Fig. 2.9 Transient voltage response for all nine runs of the screening experiment in Table 2.1, using a current step with a rise time of 10 μs. 37

Fig. 2.10 Normal plot showing the significant and not significant effects for the current step analysis, using a current step with a rise time of 10 μs and all capacitor types have a minimum of 1 capacitor as shown in Table 2.1. 37

Fig. 2.11 Transient voltage response for all nine runs of the screening experiment in Table 2.2 using a current step with a rise time of 10 μs. 38

Fig. 2.12 Normal plot showing the significant and not significant effects for the current step analysis, using a current step with a rise time of 10 μs and all capacitor types have different minimum of capacitors as shown in Table 2.2. 38

Fig. 3.1 Results for seed 1 before optimization: a) impedance profile; b) time-domain voltage pulse; c) seed values used for the optimization. 43

Fig. 3.2 Results for seed 2 before optimization: a) impedance profile; b) time-domain voltage pulse; c) seed values used for the optimization. 43

Fig. 3.3 Results for seed 3 before optimization: a) impedance profile; b) time-domain voltage pulse; c) seed values used for the optimization. 44

Fig. 3.4 Results for seed 4 before optimization: a) impedance profile; b) time-domain voltage pulse; c) seed values used for the optimization. 44

Fig. 3.5 Results for seed 5 before optimization: a) impedance profile; b) time-domain voltage pulse; c) seed values used for the optimization. 45

Fig. 3.6 Results for seed 1 approach 1 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors. 45

Fig. 3.7 Results for seed 2 approach 1 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors. 46

Fig. 3.8 Results for seed 3 approach 1 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors. 46

Fig. 3.9 Results for seed 4 approach 1 after optimization: a) evolution of objective function; b) seed values used and optimal values found for the number of capacitors. In this case, a negative value of capacitors was obtained. 47

Fig. 3.10 Results for seed 5 approach 1 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors. 47

Fig. 3.11 Results for seed 1 approach 2 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors. 48

Fig. 3.12 Results for seed 2 approach 2 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors. 49

Fig. 3.13 Results for seed 3 approach 2 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors..... 49

Fig. 3.14 Results for seed 4 approach 2 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors..... 50

Fig. 3.15 Results for seed 5 approach 2 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors..... 50

Fig. 3.16 Results for seed 1 approach 3 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors..... 51

Fig. 3.17 Results for seed 2 approach 3 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors..... 52

Fig. 3.18 Results for seed 3 approach 3 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors..... 52

Fig. 4.1 Averaged equivalent circuit of a Buck regulator. 56

Fig. 4.2 Simulation circuit to obtain Bode plots of the voltage regulator connected to the power delivery network. 57

Fig. 4.3 Flow diagram of proposed methodology. 58

Fig. 4.4 Results for Step 1 before (dashed line) and after (solid line) optimization: a) transient analysis; b) impedance profile; c) objective function evolution and its final value; d) initial and final values for the optimization variables. 62

Fig. 4.5 Results for Step 2 before (dashed line) and after (solid line) optimization: a) open loop VR gain magnitude; b) open loop VR gain phase; c) transient analysis; d) impedance profile; e) objective function evolution and its final value; f) initial and final values of the optimization variables. 63

Fig. 4.6 Results for Step 3 before (dashed line) and after (solid line) optimization: a) transient analysis; b) impedance profile; c) open loop VR gain magnitude; d) open loop VR gain phase; e) objective function evolution and its final value; f) initial and final values for optimization variables..... 64

Fig. 4.7 Results for Step 4 before (dashed line) and after (solid line) optimization: a) open loop VR gain magnitude; b) open loop VR gain phase; c) transient analysis; d) impedance profile; e) objective function evolution and its final value; f) initial and final values of the optimization variables. 65

Fig. 5.1 Open loop VR gain magnitude showing crossover frequency between fL and fH. 70

Fig. 5.2 Preliminary yield analysis for the PDN impedance profile, with only 500 outcomes, to estimate expected yield. 73
Fig. 5.3 Yield analysis for the PDN impedance profile using 9220 outcomes. 74
Fig. 5.4 Yield analysis for the voltage regulator stability of the PDN using 9220 outcomes. 74
Fig. 5.5 Yield analysis for the PDN transient voltage droop using 9220 outcomes. 74
Fig. 5.6 PDN responses of interest for the 500 random outcomes around the nominally optimized PDN design using ±20% variation in decoupling capacitance values: a) impedance profile; b) open loop VR gain; and c) transient voltage droop. 75
Fig. 5.7 Yield analysis with 9,220 outcomes at the PDN optimal yield design: a) impedance profile; b) VR stability; c) transient voltage droop. 78
Fig. 5.8 Evolution of the objective function used in (1) during yield optimization. 78
Fig. 6.1 3D planar structure and shielding box in Sonnet. 82
Fig. 6.2 Simplified power delivery network as two parallel metal planes. 83
Fig. 6.3 Parallel planes Case 1, where the upper plane left edge touches the shielding box and the excitation port is at the middle of the left plane edge: a) 3D view; b) top view. 84
Fig. 6.4 Impedance profile ($|Z_{11}|$ in dB) of the parallel planes for Case 1. 84
Fig. 6.5 Current distributions for Case 1 in A/m: a) 10 MHz; b) 5.025 GHz; c) 9.45 GHz; d) 30 GHz. 85
Fig. 6.6 Parallel planes Case 2a, where the upper left plane edge does not touch the shielding box and the excitation port is on a feeding short microstrip line at the middle of the plane: a) 3D view; b) top view. 85
Fig. 6.7 Impedance profile ($|Z_{11}|$ in dB) of the parallel planes for Case 2a. 86
Fig. 6.8 Current distributions for Case 2a in A/m: a) 10 MHz; b) 3 GHz; c) 9.5 GHz; d) 30 GHz. 86
Fig. 6.9 Parallel planes Case 2b, where the upper left plane edge does not touch the shielding box and the excitation port is on a feeding short microstrip line at the top corner of the plane: a) 3D view; b) top view. 87
Fig. 6.10 Impedance profile ($|Z_{11}|$ in dB) of the parallel planes for Case 2b. 87
Fig. 6.11 Current distributions for Case 2b in A/m: a) 10 MHz; b) 2.4 GHz; c) 9.5 GHz; d) 30 GHz. 88
Fig. 6.12 Parallel planes Case 2c, where the upper left plane edge does not touch the shielding box, the excitation port is on a feeding short microstrip line at the center of the plane, and a capacitor is inserted at bottom edge to ground: a) top view; b) zoom-in of the capacitor. 89
Fig. 6.13 Impedance profile ($|Z_{11}|$ in dB) of parallel planes for Case 2b. 89

Fig. 6.14 Current distributions for Case 2c in A/m: a) 10 MHz; b) 0.7 GHz; c) 2 GHz; d) 3.7 GHz; e) 9.5 GHz; f) 30 GHz. 90

Fig. 6.15 Parallel metallic planes representing a simplified power delivery network: a) plane geometry; b) plane discretization into basic cells. 90

Fig. 6.16 Basic cell equivalent circuit T-model: a) current flows in the x direction; b) current flows in the y direction; c) complete T-model of the basic cell. 91

Fig. 6.17 Basic cell equivalent circuit T-model implemented in Keysight ADS. 92

Fig. 6.18 Equivalent lumped circuit implemented in Keysight ADS: a) basic cell subcircuit; b) example of a parallel plate circuit model by connecting 15 basic cells together in a 3 by 5 array. 93

Fig. 6.19 Parallel planes with W = 306.9 mils, L = 306.9 mils, EM model Case 1 in Sonnet (black solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 1, N = 3; c) M = 1, N = 5; d) M = 1, N = 7. As N increases, the accuracy of the equivalent lumped circuit models improves. 96

Fig. 6.20 Parallel planes with W = 306.9 mils, L = 306.9 mils, EM model Case 1 in Sonnet (black solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 3, N = 1; c) M = 5, N = 1; d) M = 7, N = 1. As M increases, the accuracy of the equivalent lumped circuit models deteriorates. 97

Fig. 6.21 Parallel planes with W = 306.9 mils, L = 306.9 mils, EM model Case 1 in Sonnet (black solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 3, N = 3; c) M = 5, N = 5; d) M = 7, N = 7; e) M = 13, N = 13; f) M = 25, N = 25. As both M and N increase the accuracy of the equivalent lumped circuit models deteriorates. 98

Fig. 6.22 Parallel planes with W = 306.9 mils, L = 306.9 mils, EM model Case 2a in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 1, N = 3; c) M = 1, N = 5; d) M = 1, N = 7. 99

Fig. 6.23 Parallel planes with W = 306.9 mils, L = 306.9 mils, EM model Case 2a in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 3, N = 1; c) M = 5, N = 1; d) M = 7, N = 1. 100

Fig. 6.24 Parallel planes with W = 306.9 mils, L = 306.9 mils, EM model Case 2a in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 3, N = 3; c) M = 5, N = 5; d) M = 7, N = 7; e) M = 13, N = 13; f) M = 25, N = 25. 101

Fig. 6.25 Parallel planes with W = 306.9 mils, L = 306.9 mils, EM model Case 2a with a 100-pF capacitor in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line):

a) M = 1, N = 1; b) M = 3, N = 3; c) M = 5, N = 5; d) M = 7, N = 7; e) M = 13, N = 13; f) M = 25, N = 25. 102

Fig. 6.26 Parallel planes with W = 306.9 mils, L = 306.9 mils, EM model Case 2b in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 3, N = 3; c) M = 5, N = 5; d) M = 7, N = 7; e) M = 13, N = 13; f) M = 25, N = 25. 103

Fig. 6.27 Parallel planes with W = 306.9 mils, L = 83.7 mils, EM model Case 2c in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 3, N = 5; c) M = 5, N = 5; d) M = 7, N = 5; e) M = 13, N = 5; f) M = 25, N = 5. 104

Fig. 6.28 Parallel planes with W = 83.7 mils, L = 306.9 mils, EM model Case 2d in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 5, N = 3; c) M = 5, N = 5; d) M = 5, N = 7; e) M = 5, N = 13; f) M = 5, N = 25. 105

List of Tables

Table 1.1. Analytical PRF vs. numerical PRF of different capacitors in parallel of different values 18
Table 1.2. Test cases for 3 parallel decoupling capacitors 24
Table 1.3. Numerical results for 3 parallel decoupling capacitors 24
Table 1.4. Test cases for 4 parallel decoupling capacitors 25
Table 1.5. Numerical results for 4 parallel decoupling capacitors 25
Table 1.6. Test cases for 5 paralle decoupling capacitors 26
Table 1.7. Numerical results for 5 parallel decoupling capacitors 26
Table 2.1. Screening experiment with all capacitor types having a minimum of one capacitor 33
Table 2.2. Screening experiment with all capacitor types having a different minimum number of capacitors 34
Table 5.1. Estimating the number of Monte Carlo outcomes using (5-14) 73
Table 5.2. Design parameters values before and after yield optimization 77

Introduction

The design of power delivery networks (PDN) for high-performance computer platforms was not a big issue in the past, however, it has become a growing challenge nowadays. In today's digital world, speed is the main factor that determines the performance of a computer platform. As data speeds increase, the degradation of the high-speed signals becomes more and more sensitive to power supply noise as a result of the closer spacing between signal traces on the PCB, the increase of layers in the stack-up, and the reduction of voltage levels for low power consumption.

A power delivery network consists of all the devices and interconnects that distribute the electrical power supply (biasing voltages) and return the electrical current throughout a board of an electronic system. The role of a PDN is to provide suitable voltage and enough current to the devices during different phases of operation [Goral-16].

When the signals at different on-board modules of a PDN start switching, they cause current surges that create voltage noise (fast time-varying voltage fluctuations) on the pads of the on-board modules, introducing high-frequency components. If this voltage noise is large enough, it can impact the switching frequency of the transistors in the devices, causing timing margin errors, as well as inducing a risk of transistor reliability issues [Chew-12]. Furthermore, unsuccessful noise control on the PDN will cause the amplitude of the eye diagram in the vertical direction to collapse due to the voltage noise. Additionally, the signal flowing to a reference plane will increase skin and proximity effects (due to the high-frequency components), increasing jitter due to dispersion and further reducing the eye opening. This leads to functional failures in the computer platform as internal core circuits suffer setup- and hold-time errors [Smith-17].

Power delivery networks consist of the following four main components: the voltage regulator (VR), active devices, the printed circuit board (PCB) parasitic impedance associated with the path from the VR to the active devices (including the package), and decoupling capacitors [Sjiariel-15].

The VR, usually a DC-DC converter, is the main power supply to the system and needs to provide a steady DC voltage level with an acceptable noise level or ripple to the various active devices. The acceptable voltage level required by the chips depends on the frequency spectrum of the current they draw. In designing the PDN, the worst-case current drawn by the chips must be

known. If the required voltage tolerance is also known, an impedance target can be determined that the PDN should meet in order to keep the voltage noise at an acceptable level. In this way, the impedance profile becomes a figure of merit of the acceptability of the PDN design [Smith-17]. The impedance profile of a PDN is the effective impedance magnitude for the whole range of frequency, from DC to the highest significant harmonic caused by the current transients feeding the devices. It is desirable to have a low impedance path from the VR to the devices [Chew-12].

The natural parasitic inductance of the planes in the PDN and the connections to the various on-board modules increase the impedance profile proportionally with frequency [Goral-16]. Voltage regulators are able to keep a low impedance profile from DC to several hundred kilohertz. However, even the most reliable VRs are too slow at higher frequencies and allow unacceptable voltage drops caused by the transient switching currents at the devices. These voltage drops can cause performance deterioration and severe functional failures on high-speed computer platforms. To minimize the dynamic voltage fluctuations, adding decoupling capacitors is a typical industrial practice in PDN design [Chew-12]. Decoupling capacitors are usually placed in multiple hierarchical parallel stages to ensure a small variation in the power supply voltage under a significant transient current load. This avoids using a single capacitor stage that would need a high capacitance and at the same time a low parasitic inductance to be effective at maintaining a low impedance at all frequencies [Paul-92]. Additionally, parallel decoupling capacitors provide local sources of charge to mitigate the current surges by quickly supplying current to loads and stabilizing voltage levels when the VR is not able to do so [Popovich-07]. The stages of decoupling capacitors include bulk capacitors, cavity or land side capacitors (LSC) and die side capacitors (DSC) on the package. Bulk capacitors provide low impedance up to around 1MHz. High frequency decoupling is provided by ceramic capacitors up to several hundred MHz [Roy-98].

Typically, many decoupling capacitors of different values are employed to maintain the impedance profile of the PDN within acceptable bounds. These arrays of parallel decoupling capacitors introduce parallel resonant frequencies (PRF) that can magnify noise problems when current transients contain considerable components at frequencies close to these resonant peaks [Zheng-03]. Furthermore, a large peak impedance from the parallel resonance of the effective output inductance of the VR and the bulk capacitance could potentially cause instability in the VR [Sotman-06].

Frequency-domain analysis of the PDN allows to understand all the resonances in the

system produced by the interaction of inductances and capacitances in the system, both inherent and purposely added. Frequency-domain analysis needs to ensure the target impedance is met by the PDN impedance profile over the required frequency range. Time domain analysis enables to evaluate the effects of switching currents in the PDN. It is desirable that the transient voltage droop is minimized and that the maximum voltage at the device pad will not cause reliability issues [Chew-12].

Most of the research work on decoupling capacitors optimization for PDN design includes manual trial-and-error optimization processes or has been developed either in frequency-domain or in time-domain exclusively. This doctoral dissertation presents several systematic numerical optimization techniques to tackle the issue of optimizing the decoupling capacitors in a PDN considering both the time- and frequency-domain effects. This dissertation is organized as follows.

Chapter 1 presents a numerical procedure to find the PRFs of an array of more than two decoupling capacitors connected in parallel, as well as an analytical set of equations to find the PRFs of an array of three capacitors connected in parallel, which can be used to approximate the PRFs of more than three decoupling capacitors connected in parallel.

Chapter 2 explores the performance of a PDN in the frequency- and time-domain. The effect of different stages of decoupling capacitors is analyzed in order to select the decoupling stages with the best impact on the PDN performance to limit the variables in subsequent optimization efforts.

Chapter 3 presents an optimization approach to determine the number of decoupling capacitors in a PDN, aiming at decreasing the amount of decoupling capacitors without violating the PDN design specifications, looking at both the impedance profile in the frequency domain and the resulting voltage droop in the transient time-domain.

Chapter 4 presents an optimization methodology to determine the best values of the compensation elements of a Buck voltage regulator as well as the optimal number of decoupling capacitors in a power delivery network application that meet some stability criteria and frequency-domain impedance profile specification as well as time-domain voltage droop requirements.

Chapter 5 provides a statistical analysis and yield estimation performed on a nominally optimized PDN considering capacitance fluctuations in the decoupling capacitors due to manufacturing variability. It also presents a frequency- and time-domain yield optimization approach suitable for power delivery networks considering the impact of large tolerances in the

decoupling capacitors.

Chapter 6 provides highly accurate full-wave electromagnetic (EM) simulations of parallel planes that are later used as reliable references to compare versus circuit-level simulations. It also presents a discretized lumped equivalent circuit of the parallel planes which allows to place ports anywhere on the equivalent circuit, enabling future research about the effects of placing decoupling capacitors at different locations on the planes while avoiding the high computational cost of the corresponding full-wave EM simulations.

In the General Conclusions, the most relevant remarks about this doctoral dissertation are summarized, discussing the results of the proposed optimization techniques and providing some opportunities for future research.

Finally, Appendix A shows the reference list of the thirteen internal research reports developed during these doctoral studies, and Appendix B shows the list of papers published during this same period.

1. A Study on the Resonant Frequencies of an Array of Decoupling Capacitors for PDN Applications

Decoupling capacitors are frequently used to mitigate many of the most typical problems in power delivery networks (PDN). These capacitors serve as local sources of charge and help to stabilize voltage levels as well as to reduce the inductive effect of the power distribution conductors. It is common practice to insert decoupling capacitors of different capacitance values to improve the PDN performance over a wide range of frequency [Paul-92]. These arrays of parallel decoupling capacitors introduce parallel resonant frequencies (PRF) that can magnify noise problems when current transients contain considerable components at frequencies close to these resonant peaks [Zheng-03]. The analytical calculation of these resonant frequencies becomes challenging in most practical cases when there are more than two capacitors connected in parallel.

Existing work on attempts to estimate the PRFs of more than two capacitors include empirical estimations using capacitor switching transient data, as in [Santoso-05] and [Hur-06]. Authors in [Paul-92] only focus on the behavior of two capacitors in parallel, one that is effective for lower frequencies and the second one effective at higher frequencies.

In this chapter, a numerical procedure to find the PRFs of an array of more than two decoupling capacitors connected in parallel is presented. The proposed numerical procedure starts from an analytical equation to calculate the PRFs of two capacitors. Such starting point is used to search for the zero crossing frequency points of the imaginary part of the parallel equivalent impedance, which correspond to the parallel resonances. Additionally, an analytical set of equations to find the PRFs of an array of three capacitors connected in parallel is presented. The proposed equations can be used to approximate the PRFs of more than three decoupling capacitors connected in parallel. This chapter is based on [Moreno-Mojica-19b] and [Moreno-Mojica-19c].

In the following sections, capacitors with arbitrary but typical parasitic values are considered to illustrate the impedance behavior of individual capacitors and capacitor arrays.

1.1. Series Resonant Frequency of a Decoupling Capacitor

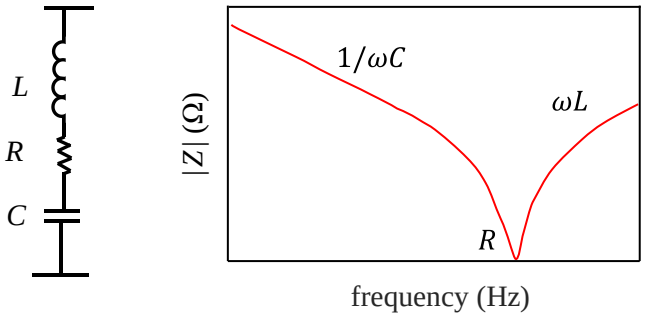


Fig. 1.1 One-stage model of a realistic decoupling capacitor and its behavior.

Physical or realistic capacitors have parasitic resistance and inductance. In the case of decoupling capacitors used for PDN applications, they are typically modeled by a series combination of ideal lumped resistance, inductance, and capacitance, whose impedance Z_c is given by

$$Z_c = R + j\omega L + \frac{1}{j\omega C} \tag{1-1}$$

where R is the equivalent series resistance (ESR), L is the equivalent series inductance (ESL), and C is the capacitance of the capacitor.

These parasitics prevent the decoupling capacitor from behaving as expected. The impedance of the decoupling capacitor is purely resistive before the series resonant frequency (SRF), which occurs where the inductive and capacitive reactances cancel each other (becoming Z_c purely resistive):

$$j\omega L = -\frac{1}{j\omega C} \tag{1-2}$$

The SRF is the obtained from (1-2):

$$SRF = \frac{1}{2\pi}\frac{1}{\sqrt{LC}} \tag{1-3}$$

The typical behavior of the impedance magnitude ($|Z|$) of a realistic decoupling capacitor is shown in Fig. 1.1. It is seen that below the SRF the impedance of the real capacitor is capacitive, and above the SRF the impedance becomes inductive, thus increasing the impedance and making the capacitor not as effective as desired [Pandit-11]. In attempting to overcome this effect, it is common practice to use parallel combinations of different capacitor values.

1.2. Identical Decoupling Capacitors in Parallel

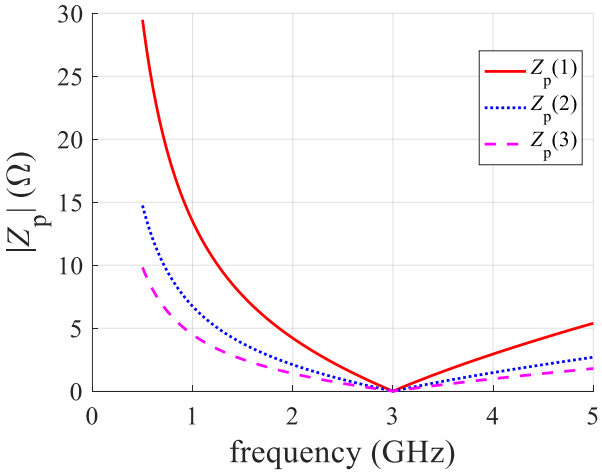


Fig. 1.2 Impedance profile of identical decoupling capacitors in parallel. $Z_p(1)$ is the impedance of a single capacitor, $Z_p(2)$ is the impedance of two capacitors in parallel, and $Z_p(3)$ is the impedance of three capacitors in parallel. It is confirmed that the equivalent series resonant frequency remains the same.

When identical decoupling capacitors are connected in parallel, the resulting behavior is similar in shape to that of a single decoupling capacitor, but the equivalent element values of the new impedance profile are different, as explained in [Smith-17]. At low frequency, the equivalent capacitance of *n* decoupling capacitors in parallel is equal to *n* times the capacitance of a single decoupling capacitor. At high frequency, the equivalent inductance of *n* parallel decoupling capacitors is equal to 1/*n* the inductance of each decoupling capacitor. In consequence, the equivalent SRF of multiple, identical decoupling capacitors in parallel does not change. At this frequency, the lowest impedance of the *n* elements in parallel is equal to 1/*n* the resistance of each element. This is important for PDN design, as adding identical capacitors results in an impedance performance of a single capacitor, but with more capacitance, less inductance, and less resistance.

To illustrate the above behavior, the impedance profile of a parallel array ($|Z_P|$) of 3 identical decoupling capacitors is shown in Fig. 1.2, where single decoupling capacitor uses R = 0.01 Ω, L = 0.2683 nH, and C = 10.4938 pF, yielding an SRF at 3 GHz.

However, when attempting to extend the frequency coverage of the impedance profile, it is common to use parallel combinations of different decoupling capacitors. In this resulting impedance profile, a new behavior emerges in the form of a parallel resonant peaks between the SRFs of the individual capacitors, as illustrated in the following sections.

1.3. Two Different Decoupling Capacitors in Parallel

As explained in [Smith-17], when two decoupling capacitors of different values are connected in parallel, a peak impedance occurs where the reactances of the impedances of these two capacitors are equal and cross (with opposite signs):

$$\omega L_1 - \frac{1}{\omega C_1} = -\omega L_2 + \frac{1}{\omega C_2} \tag{1-4}$$

The parallel resonant frequency is then calculated by solving (1-4) for ω:

$$PRF = \frac{1}{2\pi} \frac{1}{\sqrt{(L_1+L_2)\left(\frac{1}{\frac{1}{C_1}+\frac{1}{C_2}}\right)}} \tag{1-5}$$

Fig. 1.3 shows the impedance profile of two disconnected decoupling capacitors (self-impedance, Z_s) that use $R_1 = 0.01\ \Omega$, $L_1 = 1$ nH, and $C_1 = 10.49$ pF and $R_2 = 0.01\ \Omega$, $L_2 = 1$ nH, and $C_2 = 20.99$ pF, respectively. The individual SRFs are shown and comply with (1-3): $SRF_1 = 1.097$ GHz, $SRF_2 = 1.55$ GHz. It is seen in Fig. 1.3 that the two impedance magnitudes cross at 1.34 GHz, and a peak impedance profile of the parallel combination of these two decoupling capacitors is found precisely there, as shown in Fig. 1.4 and confirmed with (1-5).

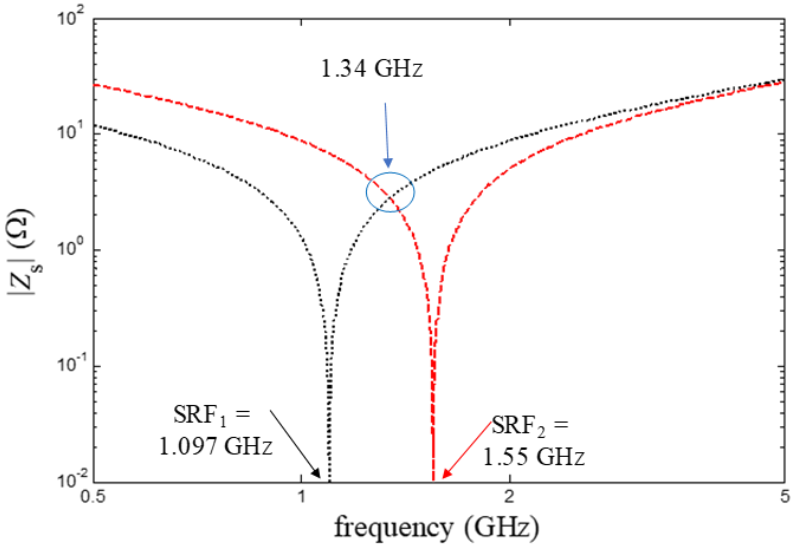


Fig. 1.3 Impedance profile of two individual capacitors (self-impedance, Z_s) showing the individual series resonant frequencies and the frequency where the two impedance profiles cross.

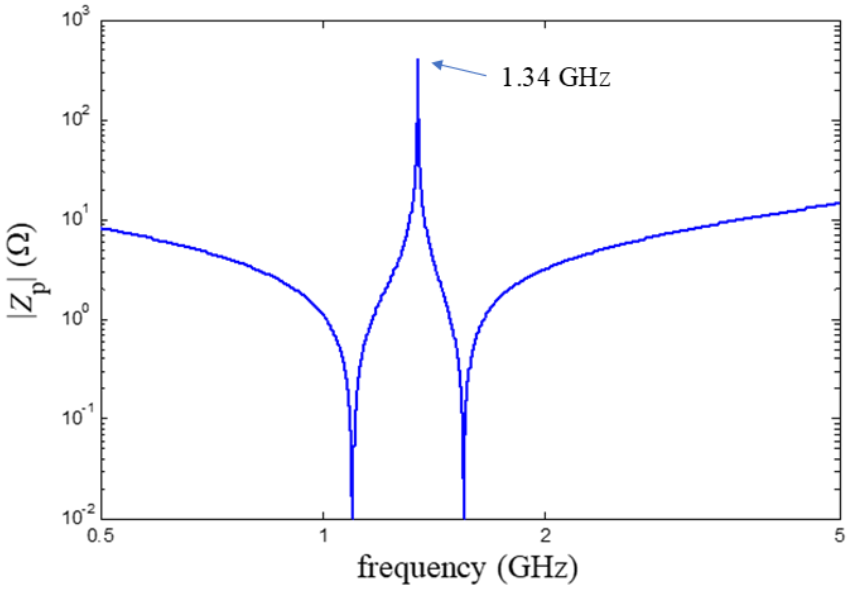


Fig. 1.4 Impedance profile of two capacitors in parallel of different value showing the impedance peak at the parallel resonant frequency.

1.4. More than Two Decoupling Capacitors of Different Values in Parallel

For more than two capacitors, generalizing (1-5) is not accurate since the behavior of the PRFs is more complex. Fig. 1.6 shows the individual impedance profile of the previous two capacitors plus a third one that uses $R_3 = 0.01\ \Omega$, $L_3 = 1$ nH, and $C_3 = 31.48$ pF. Generalizing (1-5), it is expected to see a peak impedance between the three SRFs at 1.0019 GHz and 1.34 GHz. However, the higher-frequency impedance peak is not where expected, as shown in Fig. 1.5. This suggests that the peak impedances in a parallel circuit of more than two capacitors depend not only on the two adjacent capacitors but are a result of a more complex combination of effects.

Another common practice is to use capacitors with SRFs spaced one decade apart. Fig. 1.7 shows the individual impedance profiles of such capacitors that use $R_1 = 0.01\ \Omega$, $L_1 = 1$ nH, $C_1 = 25.33$ pF and $R_2 = 0.01\ \Omega$, $L_2 = 1$ nH, and $C_2 = 2.533$ nF, and $R_3 = 0.01\ \Omega$, $L_3 = 1$ nH, and $C_3 = 0.2533$ μF with $SRF_1 = 1$ GHz, $SRF_2 = 0.1$ GHz and $SRF_3 = 0.01$ GHz. However, the same problem exists where the analytical PRFs are not the actual PRFs seen in the actual circuit response, as shown in Fig. 1.8.

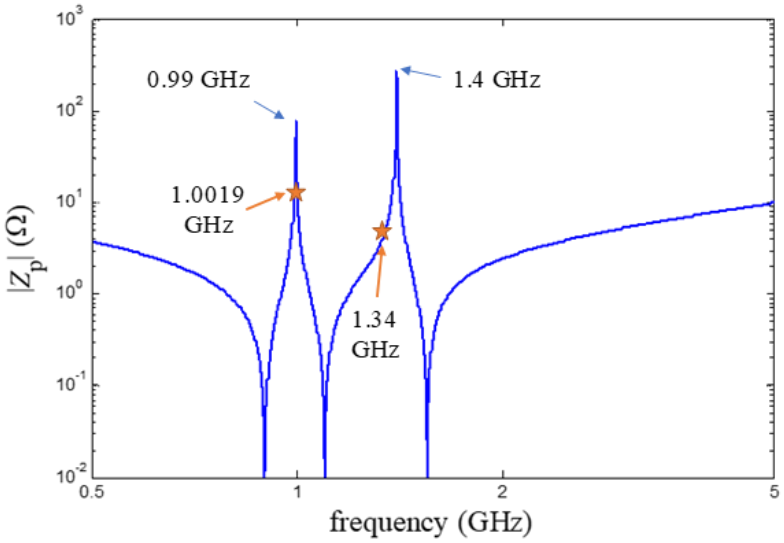


Fig. 1.5 Impedance profile of three capacitors in parallel of different value showing the impedance peaks and the analytical PRFs calculated with (1-5).

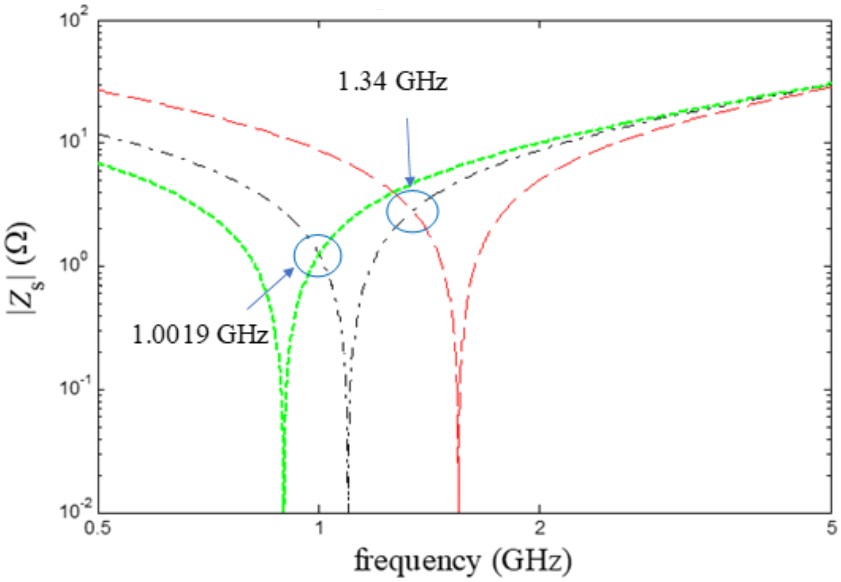


Fig. 1.6 Impedance profile of three individual capacitors showing the individual SRFs and the frequency where the adjacent impedance profiles cross.

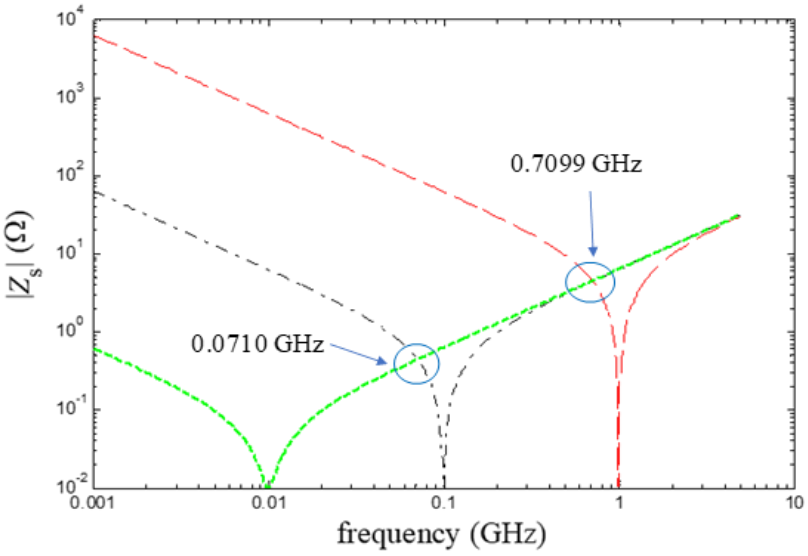


Fig. 1.7 Impedance profile of three individual capacitors of different value spaced one decade apart showing the individual SRFs and the frequency where the adjacent impedance profiles cross.

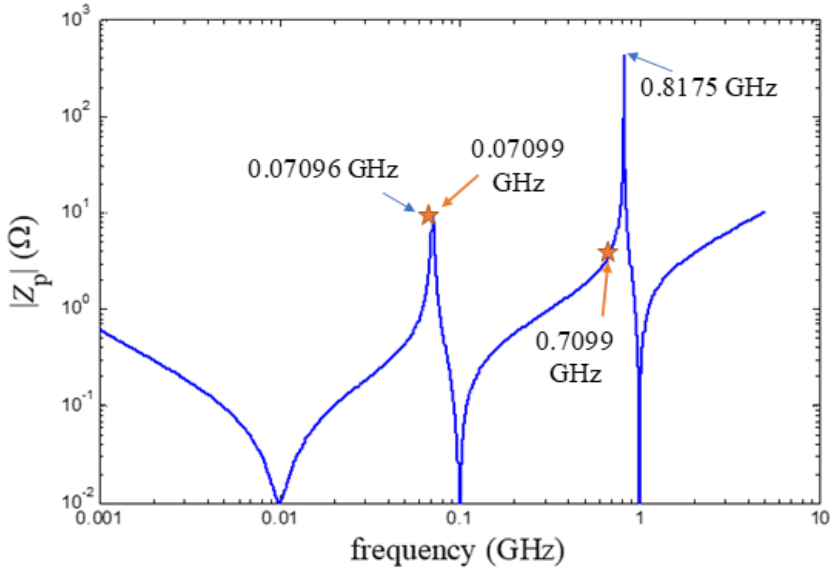


Fig. 1.8 Impedance profile of three capacitors in parallel of different value spaced one decade apart showing the impedance peaks and the analytical PRFs calculated with (1-5).

1.5. Investigating Other Circuital Responses with Three Capacitors Spaced One Decade Apart

Previous sections only considered the magnitude of the impedance of the capacitors, both individually and in parallel. In [Moreno-Mojica-19a] other circuital responses of the parallel array of capacitors were looked at. No further insight as to the locations of the peak impedances was found looking at the phases of the individual capacitors, the phase of capacitors C_1 and C_2 in parallel compared with the impedance profile of the three capacitors in parallel, the phase of capacitors C_2 and C_3 in parallel compared with the impedance profile of the three capacitors in parallel, the phase of capacitors C_1 and C_3 in parallel compared with the impedance profile of the three capacitors in parallel, the phase of the three capacitors in parallel compared with the impedance profile of the capacitors in parallel. Looking at the imaginary part of each individual capacitor compared with the impedance of the capacitors in parallel also did not provide any further information. The interesting point is seen in Fig. 1.9, which shows the imaginary part of he three capacitors in parallel and the impedance profile of the capacitors in parallel; Fig. 1.10 and Fig. 1.11 show a zoom-in around the PRFs. As it can be seen, the PRFs happen exactly when the imaginary part of the response of the capacitors in parallel cross zero, from positive to negative.

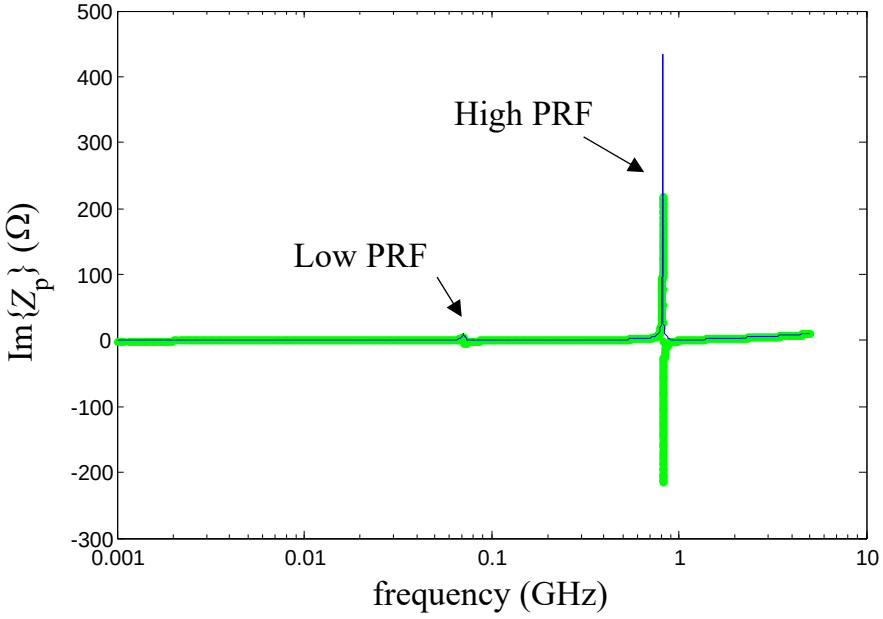


Fig. 1.9 Imaginary part of the impedance of three capacitors in parallel of different value spaced one decade apart (thick green trace) and the impedance profile of the capacitors in parallel (thin blue trace).

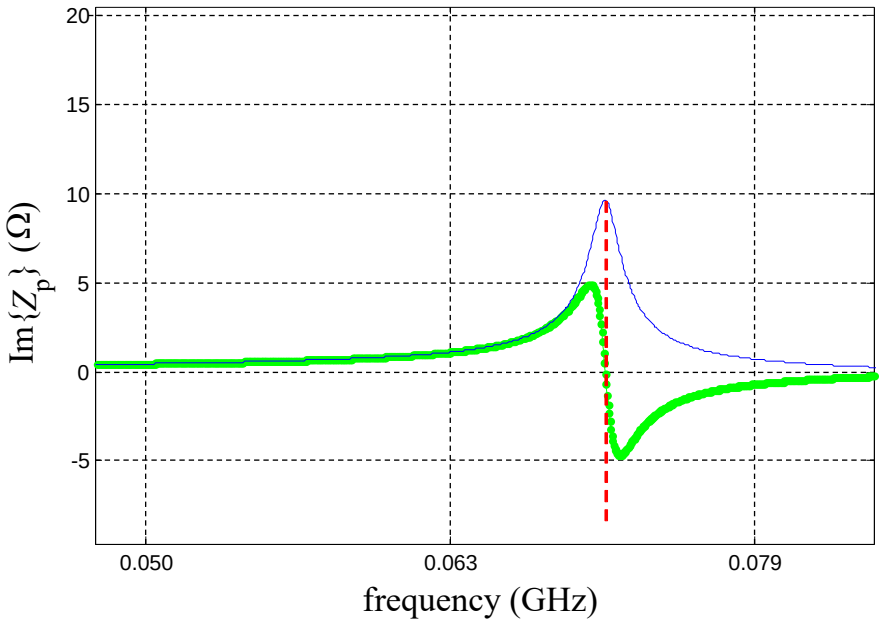


Fig. 1.10 Zoom-in on the low PRF of Fig. 1.9.

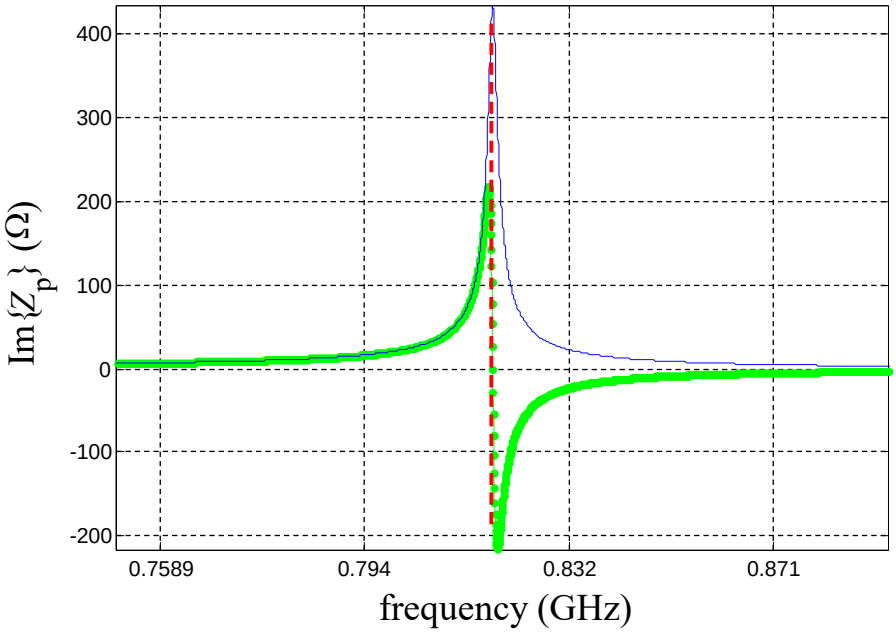


Fig. 1.11 Zoom-in on the high PRF of Fig. 1.9.

1.6. Calculating the Parallel Resonant Frequencies

Based on the experimental study realized in [Moreno-Mojica-19a] and summarized in Section 1.5, the imaginary part of the parallel impedance of the three capacitors is now calculated symbolically using wxMaxima[1], as shown in Fig. 1.12. With the PRFs calculated with (1-5) as a starting point, Matlab[2]'s fzero function is used to find the zero-crossings of the imaginary part of the parallel impedance. This way, the actual PRFs of the circuit response are found without having to simulate or do a frequency sweep of the parallel impedance of the three capacitors.

To test this numerical method, five runs are presented with random values for the parameters of each realistic decoupling capacitor. Fig. 1.13 to Fig. 1.17 show the parameters of each realistic capacitor, the analytical vs. numerical PRFs found, and the impedance profile of the capacitors in parallel showing these different frequencies. In all cases, taking the analytical PRF calculated with (1-5) as a starting point allowed to numerically find the actual PRF of the parallel capacitors using the zero-crossing of the imaginary part of the impedance, as summarized in Table 1.1.

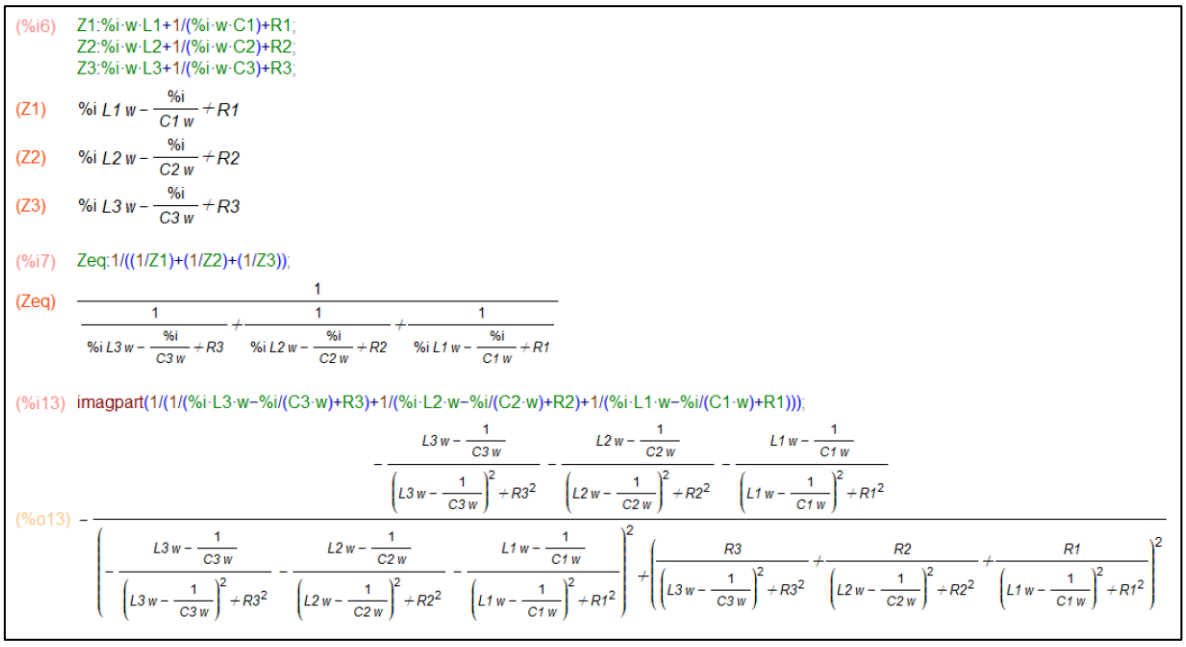
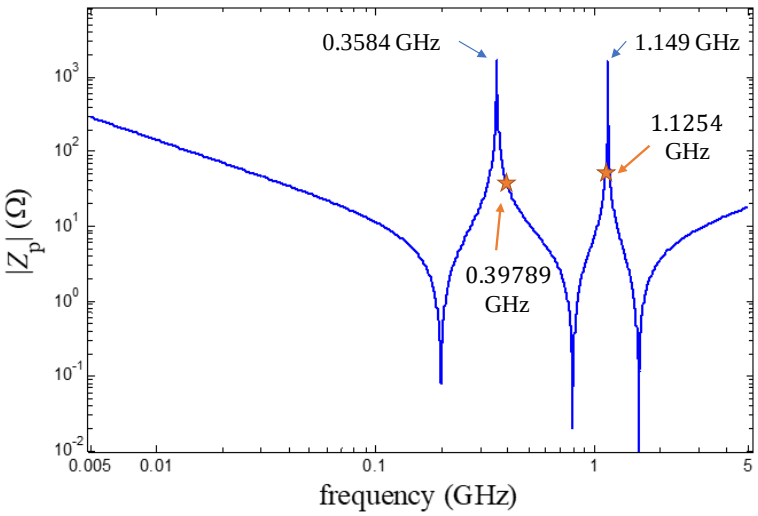


Fig. 1.12 Calculation in wxMaxima of the parallel impedance of three capacitors and its imaginary part.

[1] Maxima.sourceforge.net. Maxima, a Computer Algebra System. Version 5.34.1 (2014). http://maxima.sourceforge.net/

[2] MATLAB, Version 8.2.0.701 (R2013b), The MathWorks, Inc., 1 Apple Hill Drive, Natick MA 01760-2098, 2013.



$$Z_{c1} = 0.08 + 8 \times 10^{-9} j\omega + \frac{1}{80 \times 10^{-12} j\omega}$$

$$Z_{c2} = 0.02 + 2 \times 10^{-9} j\omega + \frac{1}{20 \times 10^{-12} j\omega}$$

$$Z_{c3} = 0.01 + 1 \times 10^{-9} j\omega + \frac{1}{10 \times 10^{-12} j\omega}$$

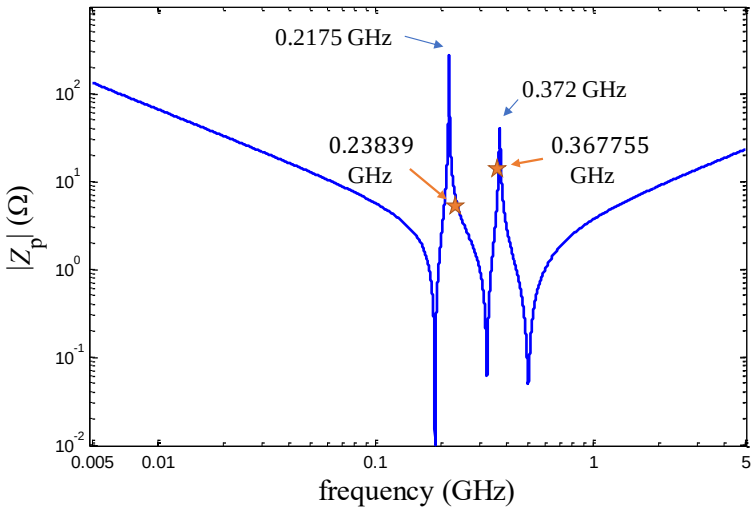
Analytical $PRF_{low} = 0.39789\ GHz$

Numerical $PRF_{low} = 0.3584\ GHz$

Analytical $PRF_{high} = 1.1254\ GHz$

Numerical $PRF_{high} = 1.1492\ GHz$

Fig. 1.13 Test 1: Impedance profile of three capacitors in parallel of different value showing the analytical PRFs calculated with (1-5) and the numerical PRFs found matching the actual PRFs.



$$Z_{c1} = 0.05 + 1 \times 10^{-9} j\omega + \frac{1}{100 \times 10^{-12} j\omega}$$

$$Z_{c2} = 0.06 + 4 \times 10^{-9} j\omega + \frac{1}{60 \times 10^{-12} j\omega}$$

$$Z_{c3} = 0.01 + 9 \times 10^{-9} j\omega + \frac{1}{80 \times 10^{-12} j\omega}$$

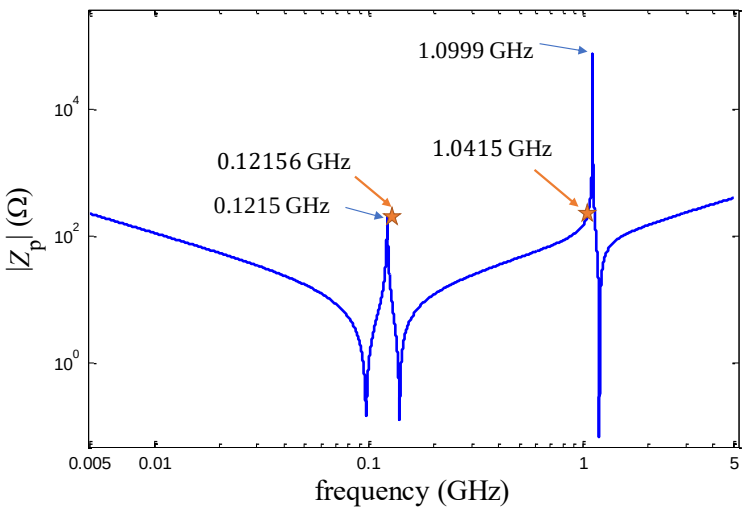
Analytical $PRF_{low} = 0.23839\ GHz$

Numerical $PRF_{low} = 0.2175\ GHz$

Analytical $PRF_{high} = 0.367755\ GHz$

Numerical $PRF_{high} = 0.3719\ GHz$

Fig. 1.14 Test 2: Impedance profile of three capacitors in parallel of different value showing the analytical PRFs calculated with (1-5) and the numerical PRFs found matching the actual PRFs.



$$Z_{c1} = 0.07 + 90 \times 10^{-9} j\omega + \frac{1}{0.2 \times 10^{-12} j\omega}$$

$$Z_{c2} = 0.15 + 27 \times 10^{-9} j\omega + \frac{1}{100 \times 10^{-12} j\omega}$$

$$Z_{c3} = 0.13 + 33 \times 10^{-9} j\omega + \frac{1}{40 \times 10^{-12} j\omega}$$

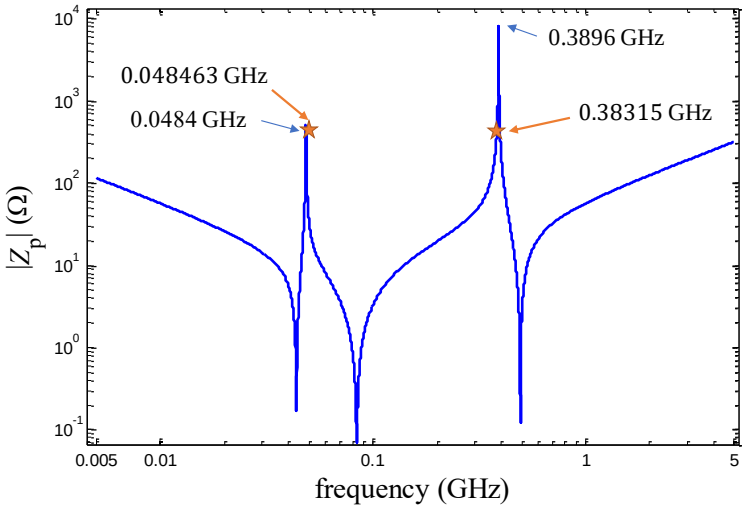
Analytical $PRF_{low} = 0.12156\ GHz$

Numerical $PRF_{low} = 0.1215\ GHz$

Analytical $PRF_{high} = 1.0415\ GHz$

Numerical $PRF_{high} = 1.0999\ GHz$

Fig. 1.15 Test 3: Impedance profile of three capacitors in parallel of different value showing the analytical PRFs calculated with (1-5) and the numerical PRFs found matching the actual PRFs.



$$Z_{c1} = 0.16 + 190 \times 10^{-9} j\omega + \frac{1}{70 \times 10^{-12} j\omega}$$

$$Z_{c2} = 0.07 + 18 \times 10^{-9} j\omega + \frac{1}{200 \times 10^{-12} j\omega}$$

$$Z_{c3} = 0.12 + 26 \times 10^{-9} j\omega + \frac{1}{4 \times 10^{-12} j\omega}$$

Analytical $PRF_{low} = 0.048463\ GHz$

Numerical $PRF_{low} = 0.0484\ GHz$

Analytical $PRF_{high} = 0.38315\ GHz$

Numerical $PRF_{high} = 0.3896\ GHz$

Fig. 1.16 Test 4: Impedance profile of three capacitors in parallel of different value showing the analytical PRFs calculated with (1-5) and the numerical PRFs found matching the actual PRFs.

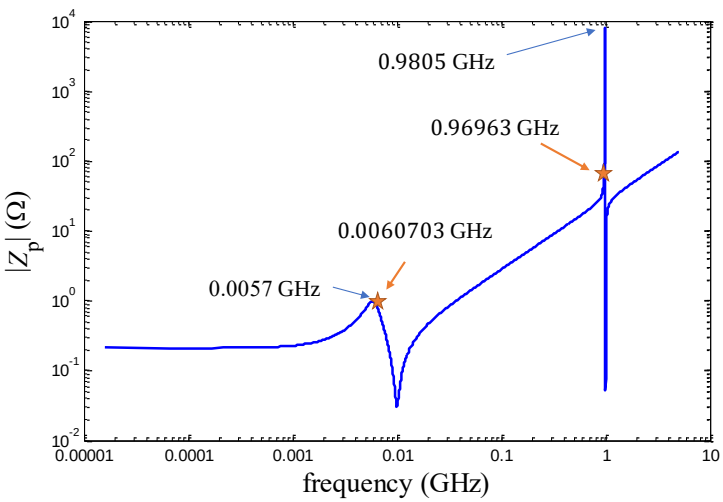


Fig. 1.17 Test 4: Impedance profile of three capacitors in parallel of different value showing the analytical PRFs calculated with (1-5) and the numerical PRFs found matching the actual PRFs.

1.7. Analytical Formulas for Parallel Decoupling Capacitors

1.7.1 Single Decoupling Capacitor

Considering the simplest case of a single decoupling capacitor with a nominal value C_1, and series parasitic inductance and resistance L_1 and R_1, respectively. Its equivalent impedance Z_{p1} is given by

$$Z_{\mathrm{p1}} = R_1 + jX_1 \tag{1-6}$$

where X_1 is the reactance given by

$$X_1 = \omega L_1 - 1/\omega C_1 \tag{1-7}$$

and ω is the angular frequency. The SRF of this decoupling capacitor occurs when $\mathrm{Im}\{Z_{\mathrm{p1}}\} = 0$, i. e., when $X_1 = 0$, which occurs at

$$\omega_{\mathrm{SRF1}} = 1/\sqrt{L_1 C_1} \tag{1-8}$$

Neglecting for a while the parasitic resistance in (1-6), the equivalent impedance Z_{p1}

becomes purely reactive, in which case ω_{SRF1} can also be calculated at the zero of Z_{p1}.

TABLE 1.1. ANALYTICAL PRF VS. NUMERICAL PRF OF DIFFERENT CAPACITORS IN PARALLEL OF DIFFERENT VALUES

	Realistic decoupling capacitors	Analytical PRF calculated with (5) (GHz)		Numerical PRF obtained from zero crossing points of Im{Z_c} (GHz)	
		Low	High	Low	High
Test 1	$Z_{c1} = 0.08 + 8 \times 10^{-9} j\omega + \frac{1}{80 \times 10^{-12} j\omega}$ $Z_{c2} = 0.02 + 2 \times 10^{-9} j\omega + \frac{1}{20 \times 10^{-12} j\omega}$ $Z_{c3} = 0.01 + 1 \times 10^{-9} j\omega + \frac{1}{10 \times 10^{-12} j\omega}$	0.39789	1.1254	0.3584	1.1492
Test 2	$Z_{c1} = 0.05 + 1 \times 10^{-9} j\omega + \frac{1}{100 \times 10^{-12} j\omega}$ $Z_{c2} = 0.06 + 4 \times 10^{-9} j\omega + \frac{1}{60 \times 10^{-12} j\omega}$ $Z_{c3} = 0.01 + 9 \times 10^{-9} j\omega + \frac{1}{80 \times 10^{-12} j\omega}$	0.23839	0.367755	0.2175	0.3719
Test 3	$Z_{c1} = 0.07 + 90 \times 10^{-9} j\omega + \frac{1}{0.2 \times 10^{-12} j\omega}$ $Z_{c2} = 0.15 + 27 \times 10^{-9} j\omega + \frac{1}{100 \times 10^{-12} j\omega}$ $Z_{c3} = 0.13 + 33 \times 10^{-9} j\omega + \frac{1}{40 \times 10^{-12} j\omega}$	0.12156	1.0415	0.1215	1.0999
Test 4	$Z_{c1} = 0.16 + 190 \times 10^{-9} j\omega + \frac{1}{70 \times 10^{-12} j\omega}$ $Z_{c2} = 0.07 + 18 \times 10^{-9} j\omega + \frac{1}{200 \times 10^{-12} j\omega}$ $Z_{c3} = 0.12 + 26 \times 10^{-9} j\omega + \frac{1}{4 \times 10^{-12} j\omega}$	0.048463	0.38315	0.0484	0.3896
Test 5	$Z_{c1} = 0.05 + 110 \times 10^{-9} j\omega + \frac{1}{0.2303 \times 10^{-12} j\omega}$ $Z_{c2} = 0.03 + 7 \times 10^{-9} j\omega + \frac{1}{36.1861 \times 10^{-9} j\omega}$ $Z_{c3} = 0.21 + 12 \times 10^{-9} j\omega + \frac{1}{211.0858 \times 10^{-6} j\omega}$	0.0060703	0.96963	0.0057	0.9805

1.7.2 Two Parallel Decoupling Capacitors

Considering two parallel decoupling capacitors of nominal values C_1 and C_2, with parasitic inductances L_1 and L_2, and parasitic resistances R_1 and R_2, respectively, the equivalent parallel impedance Z_{p2} is given by

$$Z_{\mathrm{p2}} = \frac{(R_1+jX_1)(R_2+jX_2)}{(R_1+jX_1)+(R_2+jX_2)} \tag{1-9}$$

where X_2 is the reactance of the second capacitor,

$$X_2 = \omega L_2 - 1/\omega C_2 \tag{1-10}$$

The series resonance frequency of each decoupling capacitor occurs when the corresponding reactance is zero, i. e. when $X_1 = 0$ and $X_2 = 0$, yielding

$$\omega_{\mathrm{SRF1}} = 1/\sqrt{L_1 C_1} \tag{1-11}$$

$$\omega_{\mathrm{SRF2}} = 1/\sqrt{L_2 C_2} \tag{1-12}$$

It is interesting to notice that the series resonant frequencies also occur when $\mathrm{Im}\{Z_{\mathrm{p2}}\} = 0$. For instance, if $X_1 = 0$ in (1-9), then

$$Z_{\mathrm{p2}}(\omega_{\mathrm{SRF1}}) = R_1 \frac{(R_2+jX_2)}{(R_1+R_2)+jX_2} \tag{1-13}$$

Since the parasitic resistances are generally small, $|X_2| \gg R_1, R_2$ at $\omega = \omega_{\mathrm{SRF1}}$, and from (1-8), $Z_{\mathrm{p2}}(\omega_{\mathrm{SRF1}}) = R_1$, that is, $\mathrm{Im}\{Z_{\mathrm{p2}}(\omega_{\mathrm{SRF1}})\} = 0$. Similarly, it can also be shown that $\mathrm{Im}\{Z_{\mathrm{p2}}(\omega_{\mathrm{SRF2}})\} = 0$.

Neglecting for a while the parasitic resistances in (1-9), the equivalent impedance Z_{p2} becomes purely reactive and given by

$$Z_{\mathrm{p2}} = \frac{jX_1X_2}{X_1+X_2} \tag{1-14}$$

It is seen from that ω_{SRF1} and ω_{SRF2} can also be calculated from the zeros of Z_{p2} in (1-14).

Regarding the parallel resonant frequency, it is also seen that it can be calculated from the poles of Z_{p2} in (1-14), i. e., from condition $X_1 = -X_2$. This is in consistency with [Smith-17], where authors indicate that a peak impedance occurs when the reactances of the impedances of these two capacitors are equal and with opposite signs, yielding:

$$\omega L_1 - \frac{1}{\omega C_1} = -\omega L_2 + \frac{1}{\omega C_2} \tag{1-15}$$

The corresponding parallel resonant frequency ω_{PRF} is then calculated by solving (1-15)

for ω:

$$\omega_{\mathrm{PRF}} = \frac{1}{\sqrt{(L_1+L_2)\left(\frac{1}{\frac{1}{C_1}+\frac{1}{C_2}}\right)}} \tag{1-16}$$

At the parallel resonant frequency ω_{PRF} condition $X_1 = -X_2$ holds. Applying this condition to (1-9) makes the equivalent parallel impedance at this frequency (including parasitic resistances) be given by

$$Z_{\mathrm{p2}}(\omega_{\mathrm{PRF}}) = \frac{(R_1R_2+X_1^2)+jX_1(R_2-R_1)}{(R_1+R_2)} \tag{1-17}$$

Since $|X_1| \gg R_1, R_2$ at ω_{PRF}, then the parallel impedance (1-17) can be simplified as

$$Z_{\mathrm{pPRF}} = \frac{X_1^2}{R_1+R_2} = \frac{X_2^2}{R_1+R_2} \tag{1-18}$$

which implies that $\mathrm{Im}\{Z_{\mathrm{p2}}(\omega_{\mathrm{PRF}})\} = 0$.

The above analysis suggests that all resonant frequencies of the parallel decoupling capacitors can be calculated by assuming that each decoupling capacitor is purely reactive (neglecting parasitic resistances). SRF are calculated from the zeros of the equivalent purely reactive impedance, while the PRF are calculated from its poles. Parasitic resistors are needed to calculate the magnitude of the resultant parallel impedance at each PRF.

1.7.3 Three Parallel Decoupling Capacitors

Consider now the case of three parallel decoupling capacitors of nominal values C_1, C_2, and C_3 with parasitic inductances L_1, L_2 and L_3, and parasitic resistances R_1, R_2 and R_3, respectively, with consecutive series resonant frequencies. Exploiting the previous simplification by using purely reactive impedances, the equivalent parallel impedance Z_{p3} is approximated by

$$Z_{p3} = \frac{jX_1X_2X_3}{X_1(X_2+X_3)+X_2X_3} \tag{1-19}$$

where X_3 is the reactance of the third capacitor,

$$X_3 = \omega L_3 - 1/\omega C_3 \tag{1-20}$$

The series resonant frequency of each capacitor can be found when the corresponding reactance is zero, i. e. $X_1 = 0$, $X_2 = 0$, and $X_3 = 0$, or equivalently, from the zeros of Z_{p3} in (1-19), yielding

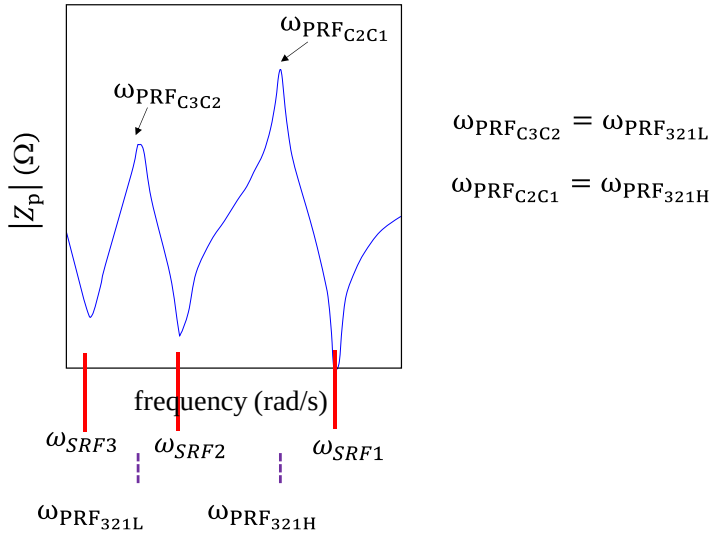


Fig. 1.18 Parallel resonant frequencies for an array of three parallel decoupling capacitors. These frequencies can be calculated in an exact manner using formulas (1-25)-(1-29).

$$\omega_{\mathrm{SRF1}} = 1/\sqrt{L_1 C_1} \tag{1-21}$$

$$\omega_{\mathrm{SRF2}} = 1/\sqrt{L_2 C_2} \tag{1-22}$$

$$\omega_{\mathrm{SRF3}} = 1/\sqrt{L_3 C_3} \tag{1-23}$$

The parallel resonant frequencies are then found at the poles of Z_{p3} in (1-19),

$$X_1(X_2 + X_3) + X_2 X_3 = 0 \tag{1-24}$$

and can be found by solving (1-24) for ω:

$$\omega_{\mathrm{PRF_H}} = \sqrt{\omega_{\mathrm{H}}},\ \omega_{\mathrm{PRF_L}} = \sqrt{\omega_{\mathrm{L}}} \tag{1-25}$$

where ω_H and ω_L are the positive roots of

$$a\omega^4 - b\omega^2 + c = 0 \tag{1-26}$$

where

$$a = L_1 L_2 + L_1 L_3 + L_2 L_3 \tag{1-27}$$

$$b = L_1\left(\frac{1}{C_2} + \frac{1}{C_3}\right) + \frac{1}{C_1}(L_2 + L_3) + \frac{L_2}{C_3} + \frac{L_3}{C_2} \tag{1-28}$$

$$c = \frac{1}{C_1 C_2} + \frac{1}{C_1 C_3} + \frac{1}{C_2 C_3} \tag{1-29}$$

Equations (1-25)-(1-29) yield two parallel-resonant frequencies, as illustrated in Fig. 1.18. The first one, $\omega_{\mathrm{PRF_H}}$, corresponds to the high PRF, while the second one, $\omega_{\mathrm{PRF_L}}$, corresponds to the low PRF. Notice that each of them depends on the three capacitors; for that reason, Fig. 1.18 uses the following notation: $\omega_{\mathrm{PRF_H}} = \omega_{\mathrm{PRF_{321H}}}$ and $\omega_{\mathrm{PRF_L}} = \omega_{\mathrm{PRF_{321L}}}$. In the terminology used

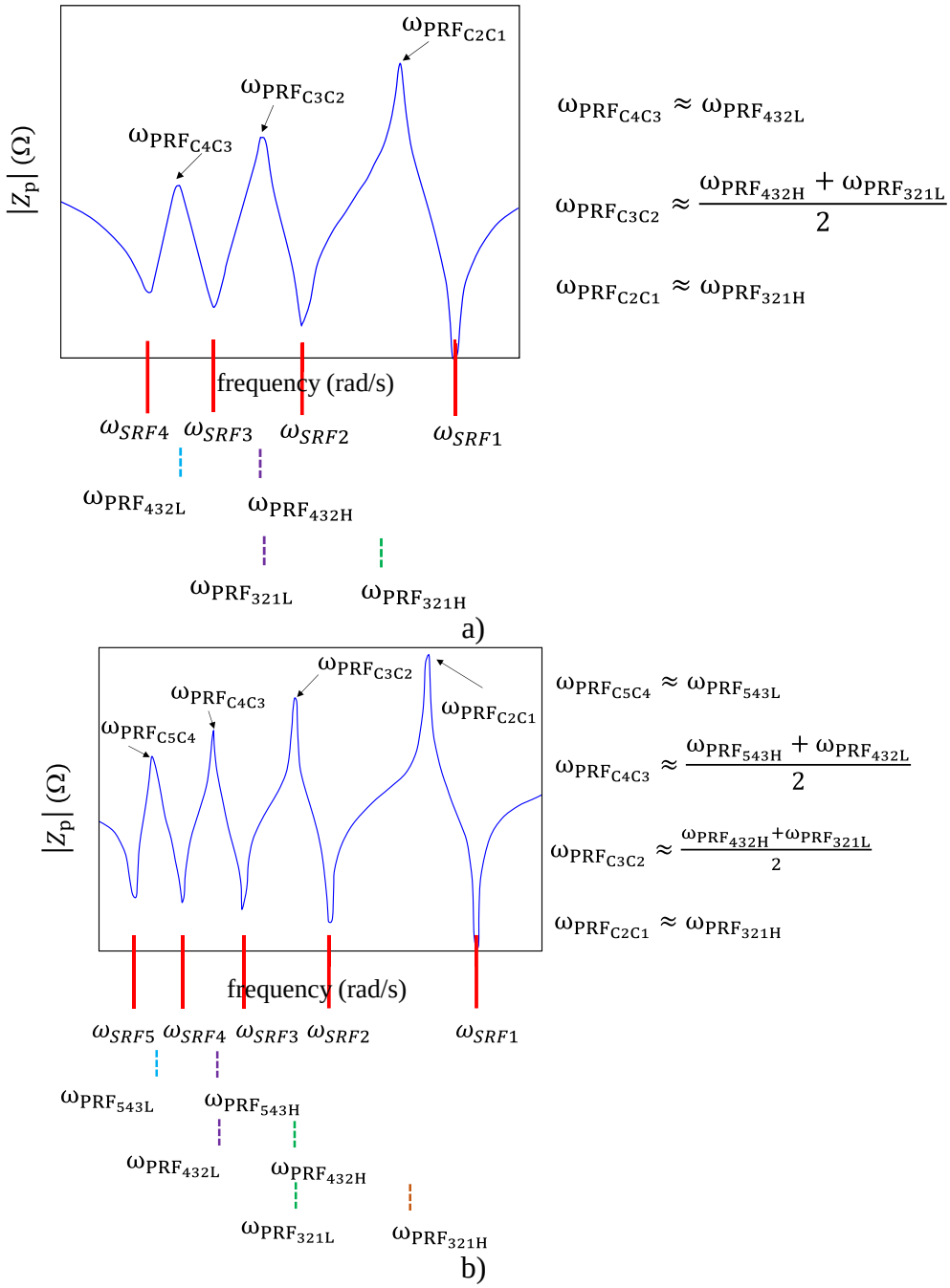


Fig. 1.19 Applying formulas (1-25)-(1-29) to approximate the PRFs for cases with more than three decoupling capacitors in parallel: a) the case of 4 capacitors, b) the case of 5 capacitors.

here, $\omega_{PRF_{C2C1}}$ corresponds to the PRF that lies between the series resonant frequencies of C_2 and C_1, that is, between ω_{SRF_2} and ω_{SRF_1}, which are the higher SRFs. Similarly, $\omega_{PRF_{C3C2}}$ corresponds to the PRF that lies between the series resonant frequencies of C_3 and C_2, that is, between ω_{SRF_3} and ω_{SRF_2}, which are the lower SRFs. Hence, $\omega_{PRF_{C3C2}} = \omega_{PRF_{321L}}$ and $\omega_{PRF_{C2C1}} = \omega_{PRF_{321H}}$.

1.7.4 More than Three Parallel Decoupling Capacitors

For cases with more than three capacitors, the same formulas can be used by considering three consecutive capacitors at a time and averaging the duplicated PRFs. To illustrate the proposed method, consider the case of four realistic capacitors with consecutive series resonant frequencies, with the following parameter values: C_1 = 10.5 pF, R_1 = 0.1 Ohms, L_1 = 0.26 nH; C_2 = 21 pF, R_2 = 0.2 Ohms, L_2 = 0.54 nH; C_3 = 31.5 pF, R_3 = 0.3 Ohms, L_3 = 0.8 nH; and C_4 = 42 pF, R_4 = 0.4 Ohms, L_4 = 1 nH.

Using the proposed method, equations (1-25)-(1-29) are first used with capacitors 4, 3 and 2 to calculate $\omega_{PRF_{432H}}$ and $\omega_{PRF_{432L}}$. Then capacitors 3, 2 and 1 are used to calculate $\omega_{PRF_{321H}}$ and $\omega_{PRF_{321L}}$. Referring to Fig. 1.19a, it is seen that the PRF between the SRFs of capacitors 4 and 3 can be approximated by $\omega_{PRF_{432L}}$, and similarly, the PRF between the SRFs of capacitors 2 and 1 can be approximated by $\omega_{PRF_{321H}}$. It is also seen from Fig. 1.19a that $\omega_{PRF_{432H}}$ and $\omega_{PRF_{321L}}$ approximate the same parallel-resonant frequency, that one between the SRFs of capacitors 3 and 2, so the average between $\omega_{PRF_{432H}}$ and $\omega_{PRF_{321L}}$is taken. In summary, $\omega_{\mathrm{PRF_{C4C3}}} \approx \omega_{\mathrm{PRF_{432L}}}$, $\omega_{\mathrm{PRF_{C2C1}}} \approx \omega_{\mathrm{PRF_{321H}}}$, and $\omega_{\mathrm{PRF_{C3C2}}} \approx (\omega_{\mathrm{PRF_{432H}}} + \omega_{\mathrm{PRF_{321L}}})/2$.

This same method is illustrated for the case of five capacitors in Fig. 1.19b.

1.8. Analytical Formulas for Parallel Decoupling Capacitors – Test Cases

Table 1.2 shows two test cases used for an array of three realistic capacitors in parallel. Table 1.3 shows the numerical results for these cases, comparing the calculated PRFs calculated with (1-16) and (1-25)-(1-29), and the actual PRFs for the different test cases. The proposed formulas in (1-25)-(1-29) give no error, as expected, while approximation (1-16) gives significantly more error.

Table 1.4 shows four test cases used for an array of four realistic capacitors in parallel. Table 1.5 shows the numerical results for these cases, comparing the PRFs estimated with (1-25)-

TABLE 1.2. TEST CASES FOR 3 PARALLEL DECOUPLING CAPACITORS

	test case 1			test case 2		
	C (pF)	*R* (Ω)	*L* (nH)	*C* (pF)	*R* (Ω)	*L* (nH)
Cap 1	10.4938	0.1	10.2683	10.4938	0.1	10.2683
Cap 2	20.9876	0.2	20.5366	209.876	0.2	205.366
Cap 3	31.4814	0.3	30.8049	220.3698	0.3	215.6343

(1-29) and (1-16) versus the actual PRFs. It is seen from Table 1.5 that approximations (1-25)-(1-29) give significantly much better results than approximation (1-16).

Finally, Table 1.6 shows four test cases used for an array of five realistic capacitors. Table 1.7 shows the same comparison for these cases, where it can be observed that approximations (1-25)-(1-29) again give overall better results than approximation (1-16).

Table 1.3, Table 1.5 and Table 1.7 demonstrate that using the classical "2-cap" formula, (1-16), may lead to very significant errors when considering more than 2 capacitors, depending on the actual capacitor values considered; they also indicate that the proposed "3-cap" formulas, (1-25)-(1-29), provide an overall much higher accuracy.

Fig. 1.20a shows the impedance profile of four realistic capacitors in parallel. Fig. 1.20b to Fig. 1.20e show zoom-ins to illustrate the difference between the calculated series resonant frequencies with (1-8) and the frequency points where the actual minima fall on the impedance profile. This comparison confirms that the SRFs of the decoupling capacitors in parallel can be calculated accurately enough using (1-8), no matter how many capacitors are placed in parallel. For this reason, only the parallel-resonant frequencies are compared in Table 1.2 to Table 1.7.

TABLE 1.3. NUMERICAL RESULTS FOR 3 PARALLEL DECOUPLING CAPACITORS
using 3-cap formulas (1-25)-(1-29) and 2-cap formulas (1-16)

	test case 1		test case 2		
	PRF1	PRF2	PRF1	PRF2	Units
3-cap formulas	0.1942	0.3650	0.0237	0.1463	GHz
2-cap formula	0.1979	0.3428	0.0237	0.1084	GHz
actual PRF	0.1942	0.3650	0.0237	0.1463	GHz
Error (3-cap formula)	0%	0%	0%	0%	-
Error (2-cap formula)	1.905%	6.082%	0%	25.906%	-

TABLE 1.4. TEST CASES FOR 4 PARALLEL DECOUPLING CAPACITORS

	test case 1			test case 2		
	C (pF)	*R* (Ω)	*L* (nH)	*C* (pF)	*R* (Ω)	*L* (nH)
Cap 1	10.4938	0.1	0.2683	0.7496	0.1	3.7562
Cap 2	20.9876	0.2	0.5366	5.2469	0.2	1.0732
Cap 3	31.4814	0.3	0.8049	3.9352	0.3	2.1464
Cap 4	41.9752	0.4	1.0732	3.8159	0.4	2.9513
	test case 3			test case 4		
	C (pF)	*R* (Ω)	*L* (nH)	*C* (pF)	*R* (Ω)	*L* (nH)
Cap 1	115.4318	0.1	112.9513	136.4194	0.1	133.4879
Cap 2	31.4814	0.2	30.8049	31.4814	0.2	30.8049
Cap 3	41.9752	0.3	41.0732	62.9628	0.3	61.6098
Cap 4	104.938	0.4	102.683	94.4442	0.4	92.4147

TABLE 1.5. NUMERICAL RESULTS FOR 4 PARALLEL DECOUPLING CAPACITORS
using 3-cap formulas (1-25)-(1-29) and 2-cap formulas (1-16)

	test case 1			test case 2			
	PRF1	PRF2	PRF3	PRF1	PRF2	PRF3	Units
With 3-cap formulas	0.8513	1.2352	2.2584	1.5791	1.8811	2.866	GHz
With 2-cap formula	0.8659	1.2245	2.1209	1.6015	1.8705	2.8278	GHz
Actual PRF	0.8487	1.246	2.334	1.578	1.892	2.883	GHz
Error (3-cap formula)	0.300%	0.867%	3.239%	0.070%	0.576%	0.590%	-
Error (2-cap formula)	2.021%	1.726%	9.130%	1.489%	1.136%	1.915%	-
	test case 3			test case 4			
	PRF1	PRF2	PRF3	PRF1	PRF2	PRF3	Units
With 3-cap formulas	0.0462	0.0782	0.1411	0.0437	0.0664	0.1217	GHz
With 2-cap formula	0.0767	0.14	0.0844	0.066	0.1143	0.0776	GHz
Actual PRF	0.0462	0.0792	0.1421	0.0433	0.0668	0.1254	GHz
Error (3-cap formula)	0%	1.263%	0.704%	0.9%	0.658%	2.951%	-
Error (2-cap formula)	66.020%	76.770%	40.600%	52.39%	71.005%	38.12%	-

TABLE 1.6. TEST CASES FOR 5 PARALLE DECOUPLING CAPACITORS

	test case 1			test case 2		
	C (pF)	*R* (Ω)	*L* (nH)	*C* (pF)	*R* (Ω)	*L* (nH)
Cap 1	10.4566	0.1	8.8781	10.4566	0.1	8.8781
Cap 2	8.9628	0.2	7.6098	1.4938	0.2	1.2683
Cap 3	11.9504	0.3	10.1464	11.9504	0.3	10.1464
Cap 4	13.4442	0.4	11.4147	7.469	0.4	6.3415
Cap 5	16.4318	0.5	13.9513	19.4194	0.5	16.4879
	test case 3			test case 4		
	C (pF)	*R* (Ω)	*L* (nH)	*C* (pF)	*R* (Ω)	*L* (nH)
Cap 1	20.9132	0.1	17.7562	73.4566	0.1	8.8781
Cap 2	13.4442	0.2	11.4147	62.9628	0.2	7.6098
Cap 3	5.9752	0.3	5.0732	115.4318	0.3	13.9513
Cap 4	7.4690	0.4	6.3415	52.469	0.4	6.3415
Cap 5	19.4194	0.5	16.4879	136.4194	0.5	16.4879

TABLE 1.7. NUMERICAL RESULTS FOR 5 PARALLEL DECOUPLING CAPACITORS
using 3-cap formulas (1-25)-(1-29) and 2-cap formulas (1-16)

	test case 1				test case 2				
	PRF1	PRF2	PRF3	PRF4	PRF1	PRF2	PRF3	PRF4	Units
With 3-cap formulas	0.3602	0.4305	0.489	0.5715	0.3374	0.4882	0.6287	1.9324	GHz
With 2-cap formula	0.3675	0.4309	0.4886	0.5642	0.3585	0.4886	0.6181	1.6352	GHz
Actual PRF	0.3548	0.4282	0.4919	0.5776	0.3289	0.4876	0.6471	2.220	GHz
Error (3-cap formula)	1.536%	0.537%	0.590%	1.056%	2.584%	0.133%	2.843%	12.855%	-
Error (2-cap formula)	3.594%	0.631%	0.671%	2.320%	9.00%	0.205%	4.482%	26.342%	-
	test case 3				test case 4				
	PRF1	PRF2	PRF3	PRF4	PRF1	PRF2	PRF3	PRF4	Units
With 3-cap formula	0.2706	0.3435	0.5426	0.8242	0.1147	0.1573	0.2123	0.2558	GHz
With 2-cap formula	0.271	0.338	0.5451	0.8176	0.1154	0.1572	0.2129	0.2519	GHz
Actual PRF	0.2704	0.346	0.5588	0.8312	0.114	0.1525	0.2125	0.2573	GHz
Error (3-cap formula)	0.074%	0.723%	2.899%	0.848%	0.614%	3.148%	0.094%	0.583%	-
Error (2-cap formula)	0.222%	2.312%	2.452%	1.642%	1.228%	3.082%	0.188%	2.099%	-

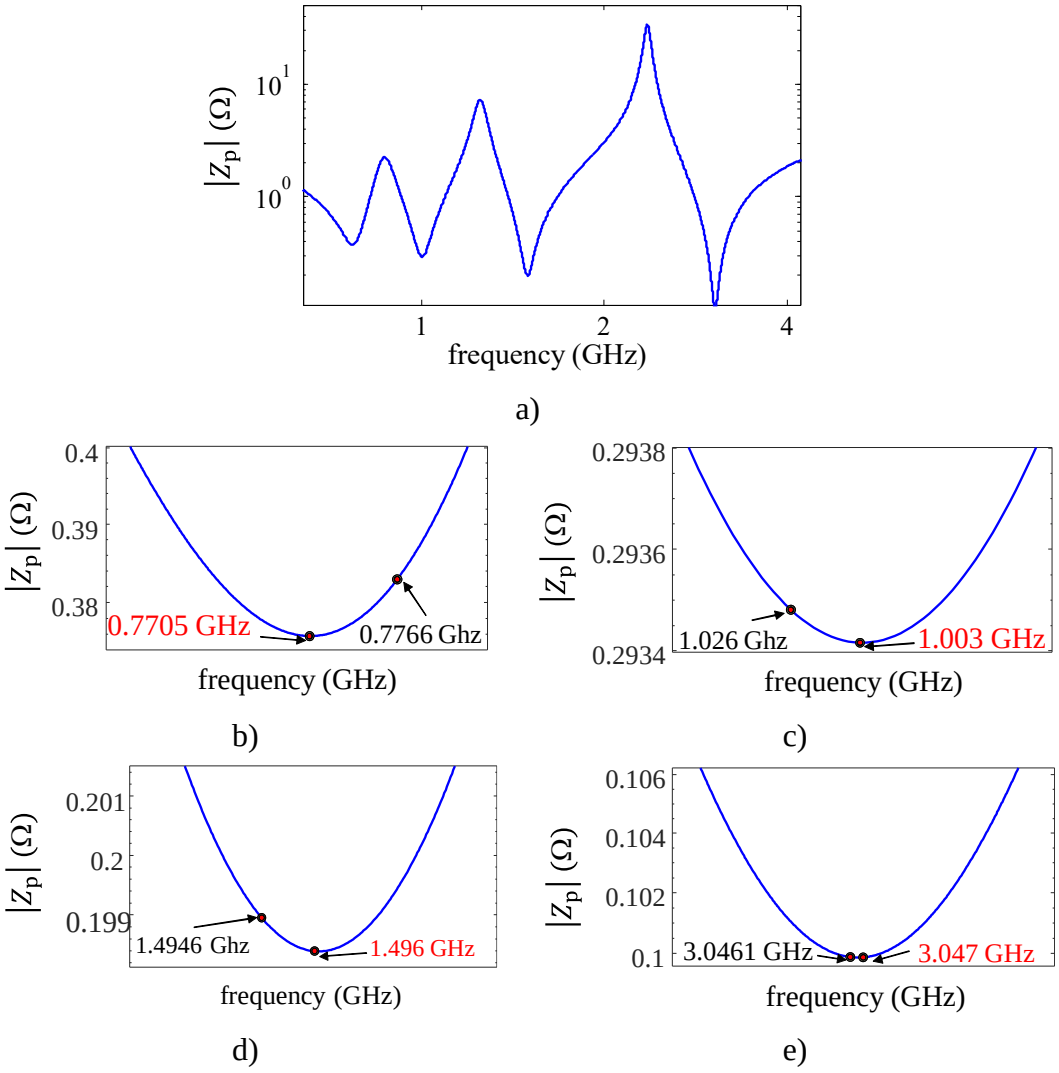


Fig. 1.20 Series resonant frequencies of four decoupling capacitors in parallel: a) complete impedance profile; zoom-ins to compare the calculated SRF using (1-8) versus the actual SRF in red for b) capacitor 4, c) capacitor 3, d) capacitor 2, e) capacitor 1. It is confirmed that the equivalent SRFs can be estimated accurately enough with (1-8), no matter how many capacitors are placed in parallel.

1.9. Conclusions

Decoupling capacitors are frequently used to mitigate many of the most typical problems in PDN. These arrays of parallel decoupling capacitors introduce parallel resonant frequencies whose analytical calculation becomes challenging in most practical cases when there are more than

two capacitors connected in parallel. A numerical procedure to find the parallel resonant frequencies of an array of more than two decoupling capacitors connected in parallel was presented in this chapter. The numerical procedure started from an analytical equation to calculate the parallel resonant frequencies of two capacitors. Such starting point was used to search for the zero crossing frequency points of the imaginary part of the parallel equivalent impedance, which correspond to the parallel resonances. Additionally, an analytical set of equations to find the parallel resonant frequencies of an array of three capacitors connected in parallel was presented. The proposed equations can be used to approximate the parallel resonant frequencies of more than three decoupling capacitors connected in parallel. The procedures described in this chapter confirm the high complexity involved in the analytical prediction of the impedance profile in practical PDN structures with many different decoupling capacitors. This complexity leads us to the systematic use of simulation-based numerical procedures, as described in the following chapters.

2. PDN Frequency- and Time-Domain Performances

A power delivery network (PDN) includes all the interconnects and devices on the power supply path of the computer platform, from the voltage regulator to the circuits on the active components. When these circuits start operating, they create current fluctuations through the PDN which can cause voltage noise. A suitable PDN design approach involves looking at the PDN in both the frequency- and time-domain to ensure acceptable noise levels.

Each component in the PDN has a different impedance associated with it, which causes voltage variations as the transient current passes through them. The PDN structure can be modeled in a limited frequency band by simple lumped RLC circuits [Klokotov-14]. To maintain the impedance profile within certain limits, different types of capacitors are placed throughout the PDN to lower the impedance at certain frequency ranges [Smith-99]. Fig. 2.1 is for illustrative purposes only, showing a typical PDN impedance profile, where some frequency resonances are normally present, with a large resonance at high frequency caused by the die and package parasitics (denoted as first-order effects). The impedance profile is normally obtained from $|Z_{11}|$ of the whole PDN measured at a given physical location. The ideal target impedance profile should be as low and flat as possible across all frequencies. However, designing a PDN that complies with such ideal target impedance can be too expensive given the high number of capacitors needed. Additionally, reducing the largest resonance at high frequencies would imply a redesign at the package and die levels, which can be extremely expensive.

Furthermore, multiple capacitors of different magnitude placed in parallel can result in sharp anti-resonant impedance peaks [Zheng-03]. These peaks can magnify noise problems when current transients contain considerable components at frequencies close to those resonant peaks. Frequency-domain effects will then translate into time-domain as voltage droops at different stages, potentially causing operational errors or failures [DiBene-14]. This relationship is also illustrated in Fig. 2.1. The first order voltage droop is typically driven by the on-die capacitance, on-die resistive parasitics, and the package connections. The second order droop is dominated by package capacitance and sometimes the connector pins. The third order droop is usually caused by the voltage regulator capacitance and the bulk capacitance nearby. The tolerance to the droop events depends on their magnitude and duration; as the droop events get larger and last a longer

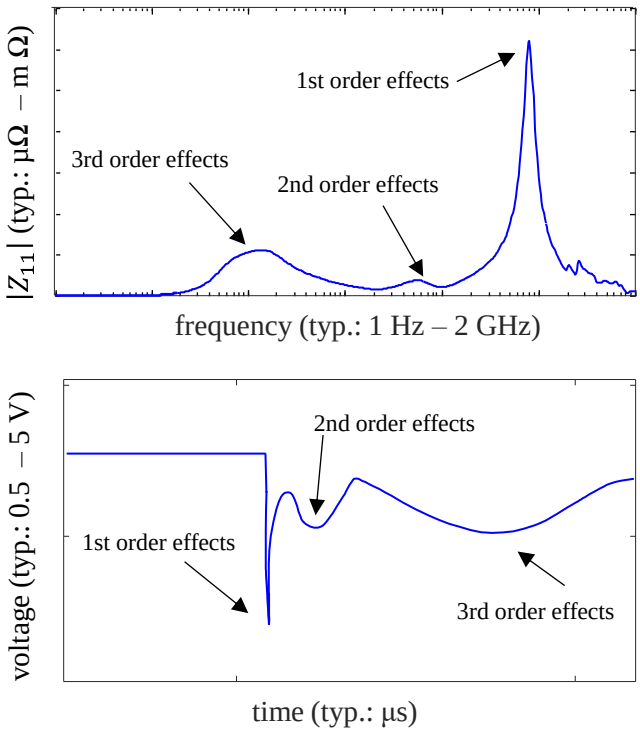


Fig. 2.1 Typical relationship between the PDN frequency-domain impedance profile and transient-domain voltage droop [Leal-Romo-20], [Zheng-03].

time, signal integrity becomes compromised, and thus the need for limiting the droop events.

This chapter explores the effect of the different stages of the decoupling capacitors on a PDN. The aim is to select the decoupling stages with the largest effect on the impedance profile to limit the variables in subsequent optimization efforts. This chapter is partly based on [Moreno-Mojica-19a] and is an abbreviated version of [Moreno-Mojica-20b].

2.1. Representing the PDN Structure

For argument's sake, the PDN of a CPU power net of an Intel® Xeon® server platform is considered. Fig. 2.2 shows a portion of the PDN platform layout. The yellow section is the PDN under study. Other colors represent signal networks.

Modeling the PDN structure in a limited frequency band as simple lumped RLC circuits [Klokotov-14] [Leal-Romo-20], a series LC circuit with a series resistance can be observed if the PDN is viewed from the board looking into the chip (see Fig. 2.3a). At high frequency an increase in impedance is seen due to the package lead inductance. This means only the low-impedance of

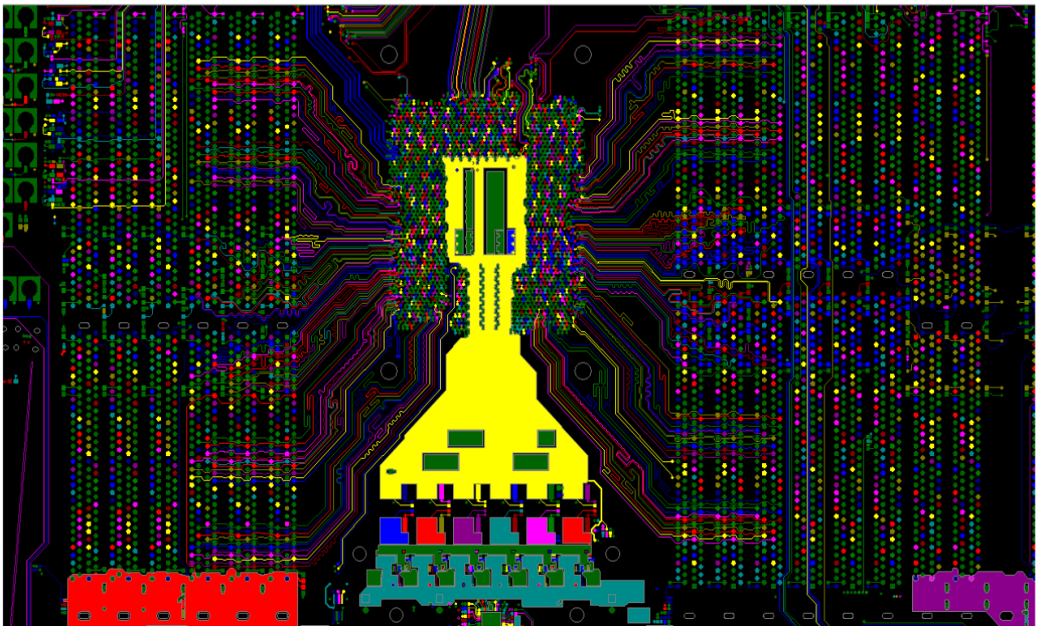


Fig. 2.2 Power delivery network layout of an Intel® Xeon® platform (courtesy of Intel®).

the on-die environment can be seen from the board, as the high-frequency properties of the die's PDN environment are blocked from view by the package lead inductance. Because of this, it is more useful to observe the PDN from the die's perspective. From here, the first thing seen is the on-die capacitance that consists of the on-die power rails and the transistor gates. To get from the die pads to the board, it is necessary to go through the die bumps, the power distribution in the package, and finally the balls and vias that connect the package to the board. This trajectory is very inductive, and it is seen as being in parallel with the on-die capacitance, as shown in Fig. 2.3b. This parallel circuit causes a resonant peak usually seen at high frequencies. At low frequencies the die sees its impedance shorted by the package lead inductance connected to the board, which in a good design is low impedance. The board-level impedance and the VRM have an impedance decreasing toward lower frequency.

Different types of capacitors are typically used in designing a PDN [Smith-99]. Bulk capacitors are the biggest in the PDN and are used to provide low impedance at the frequency at which the VRM is not able to do so. They are effective from 1 KHz to 1 MHz and typical values range from hundreds to thousands of µF. Cavity capacitors are located under the cavity of the package; they range from a few to tens of µF and are effective at higher frequencies, up to several MHz. Package capacitors are slightly smaller and are effective at even higher frequencies, up to several hundred MHz.

Fig. 2.4 shows the equivalent lumped model extracted from the PDN layout in Fig. 2.2. This lumped circuit is used in this work for subsequent optimization approaches.

2.2. A Study on Capacitor Effects of a PDN in the Frequency- and Time-Domain

Given that power delivery networks represent a quite complex system with many design factors involved, design of experiments (DoE) approaches are particularly amenable for PDN study and characterization. In addition, PDN noise and resonances in the frequency-domain translates into the time-domain as voltage drops in different stages and are affected by different components in the PDN [DiBene-14]. The on-die capacitance and package connections typically drive the first droop. This droop has a typical duration of tens of nanoseconds or less. The package capacitance and connector pins dominate the second droop. This droop has a typical duration of hundreds of nanoseconds to one microsecond. The third droop has a duration of tens of microseconds or longer. This droop is usually driven by the voltage regulator capacitance and the bulk capacitance.

The active factors in the PDN presented in Fig. 2.4 are explored by employing DoE techniques. Given that the design of a PDN is usually done at the board level, having already received a silicon die on its package, the work focuses on the third droop effects that can be dealt with at the board level. Screening experiments are done to explore the factor effects in the

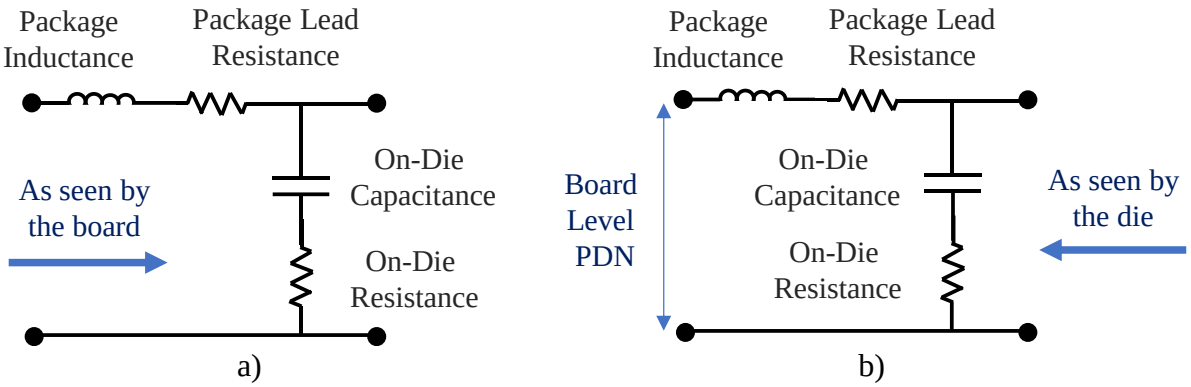


Fig. 2.3 Circuit describing the on-die capacitance and package inductance viewed from two different perspectives: a) from the board; b) from the die.

frequency-domain impedance profile and the time-domain current step transient analysis of the

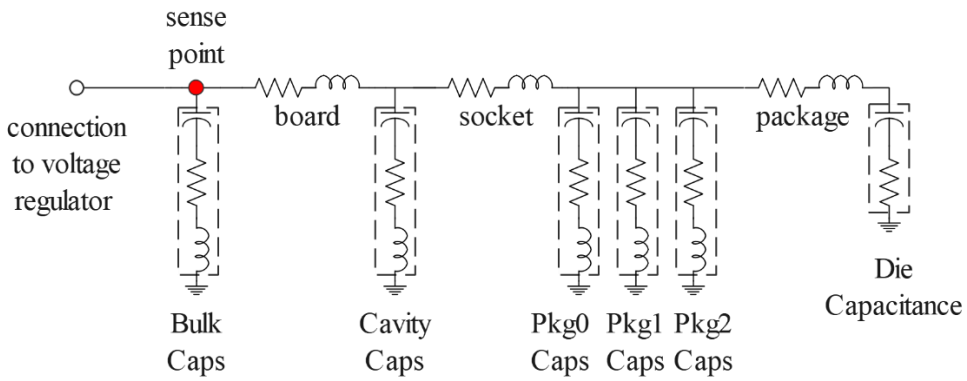


Fig. 2.4 Lumped equivalent circuit of the power delivery layout schematic of Intel® Xeon® platform.

PDN. The DoE design and analysis are done by using Minitab® Statistical Software[3], and the simulations are done by using SPICE and Matlab[4].

2.2.1 Screening Experiment

The design factors under consideration are decoupling capacitors placed in five different places on the PDN (see Fig. 2.4). Bulk capacitors are placed closest to the VR, cavity capacitors

TABLE 2.1. SCREENING EXPERIMENT WITH ALL CAPACITOR TYPES HAVING A MINIMUM OF ONE CAPACITOR

Run	Bulk Capacitors	Cavity Capacitors	Package 0 Capacitors
1	1	1	1
2	10	1	1
3	1	100	1
4	10	100	1
5	1	1	150
6	10	1	150
7	1	100	150
8	10	100	150
9	5.5	50.5	75.5

[3]MINITAB STATISTICAL SOFTWARE, Version 19.1, Minitab, LLC, Quality Plaza 1829 Pine Hal R, State College, PA 16801-3210, 2019.
[4]MATLAB, Version 8.2.0.701 (R2013b), The MathWorks, Inc., 1 Apple Hill Drive, Natick MA 01760-2098, 2013.

TABLE 2.2. SCREENING EXPERIMENT WITH ALL CAPACITOR TYPES HAVING A DIFFERENT MINIMUM NUMBER OF CAPACITORS

Run	Bulk Capacitors	Cavity Capacitors	Package 0 Capacitors
1	1	30	50
2	10	30	50
3	1	100	50
4	10	100	50
5	1	30	150
6	10	30	150
7	1	100	150
8	10	100	150
9	5.5	65	100

are placed beneath the package in the inner cavity of the socket, and package capacitors are placed in three different locations on the package; package 0 capacitors are farthest from the die, next are the package 1 capacitors, and package 2 capacitors are placed nearest the die.

For the screening experiment, a full two-level factorial is chosen since there are only three factors under study [Montgomery-05], giving eight runs for the experiment. However, a center run is added to the screening experiment to provide information about the curvature of the system [Box-05], resulting in a total of 9 runs required for a complete trial of the experiment.

The first study done uses a current step with a rise time of 50 ns for the transient analysis.

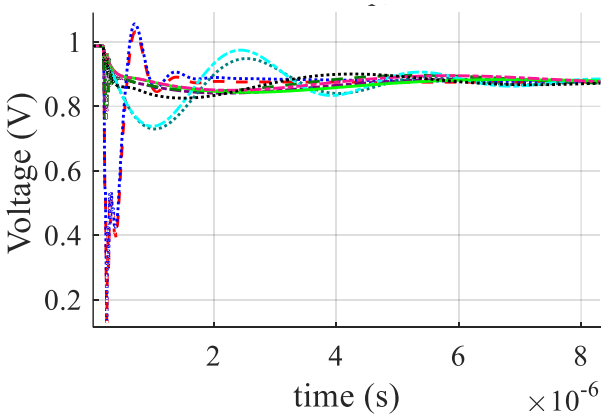


Fig. 2.5 Transient voltage response for all nine runs of the screening experiment in Table 2.1, using a current step with a rise time of 50 ns.

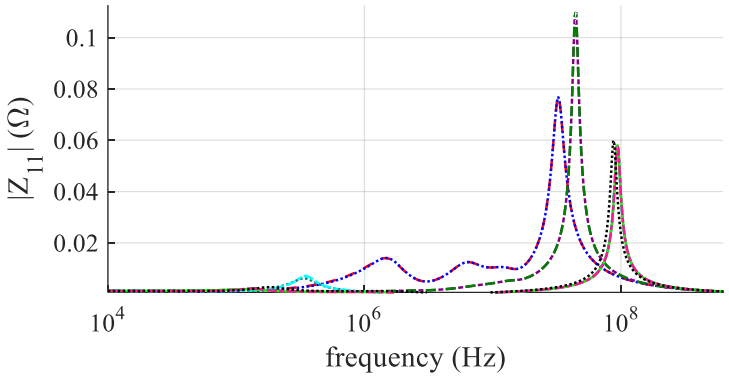


Fig. 2.6 Impedance profile for all nine runs of the screening experiment in Table 2.1.

A screening experiment was done with maximum 10 bulk capacitors, maximum 100 cavity capacitors, and maximum 150 package 0 capacitors. All capacitor types have a minimum of one capacitor. Table 2.1 shows the experiment. Fig. 2.5 shows the transient voltage response and Fig. 2.6 shows the impedance profile, which corresponds to the magnitude of the Z_{11} parameter, of all nine runs in this screening. Fig. 2.7 shows a normal plot of the factor effects for the current step analysis. A normal plot is a tool for analyzing the factor effects in DoE. It shows the standardized effects relative to a distribution fit line for the case when all effects are 0. Effects further from the fit line are more statistically significant [Minitab-22]. It can be seen that the cavity and the package 0 capacitors are active factors in this design for the current step analysis. Fig. 2.8 shows the normal

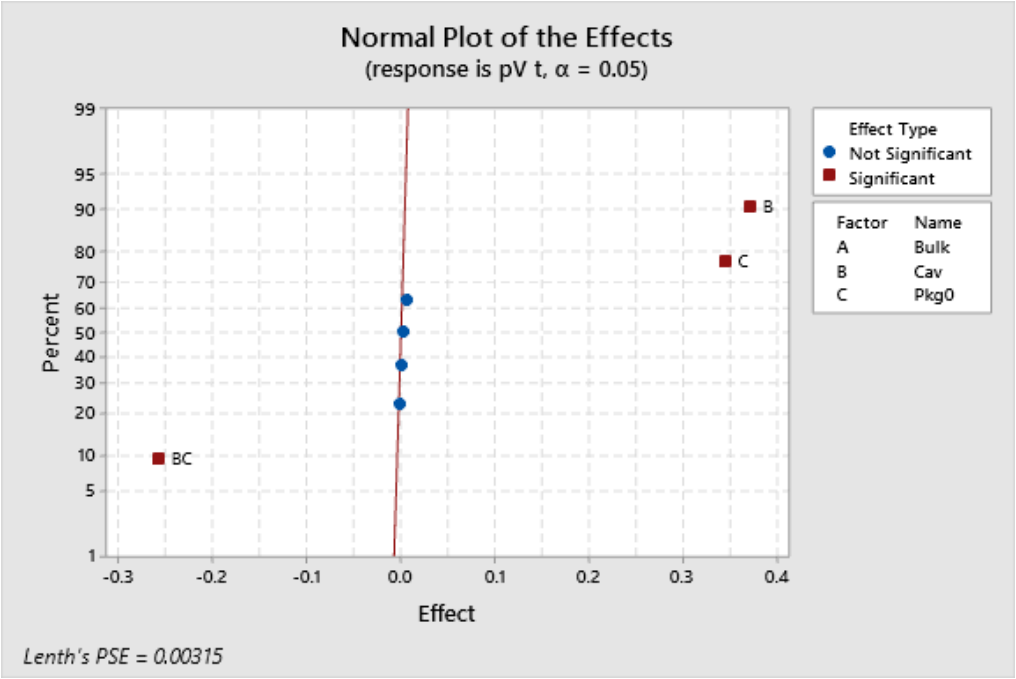


Fig. 2.7 Normal plot showing the significant and not significant effects for the current step analysis, using a current step with a rise time of 50 ns and all capacitor types have a minimum of 1 capacitor.

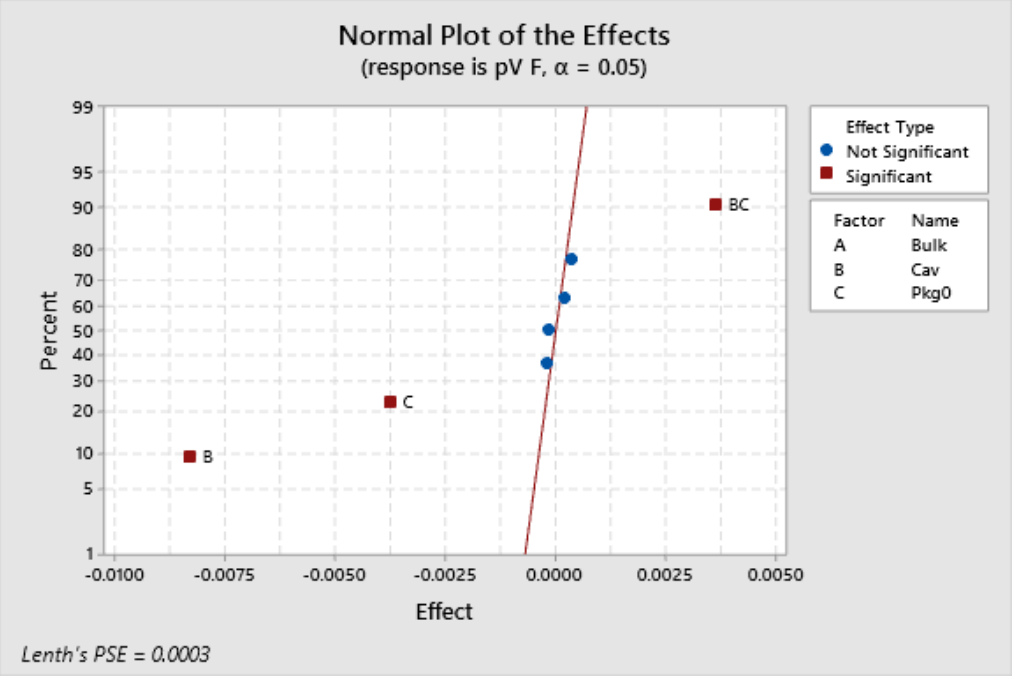


Fig. 2.8 Normal plot of the significant and not significant effects for the impedance profile, all capacitor types have a minimum of 1 capacitor.

plot of the factor effects for the impedance profile. This plot shows that the ca vity and package 0 capacitors are also active factors for the impedance profile. The work in [Moreno-Mojica-20b] also presents a second experiment using the same 50 ns current step, but now the minimum number of capacitors for all types is different, as shown in Table 2.2. The minimum for the bulk capacitors is 1, for the cavity capacitors is 30, and for the package 0 capacitors is 50. The maximum amount for each capacitor type remains the same. In this experiment only the cavity capacitors were seen to be active factors. The results for these two screening experiments show that a current step of 50 ns is too aggressive since the rise time is too fast and the effects on the third voltage droop cannot be observed.

Aiming to see the effects on the third voltage droop, a slow current step was used, with a rise time of 10 μs. Fig. 2.9 shows the voltage droop for this experiment with one minimum capacitor for all capacitor types. The effect of the third droop can be seen, and the bulk and cavity capacitors are active factors for the responses, as shown in the normal plot of Fig. 2.10. Fig. 2.11 shows all runs for the experiment when all types of capacitors have a different minimum. Once again, the bulk and cavity capacitors are active factors, as shown in Fig. 2.12.

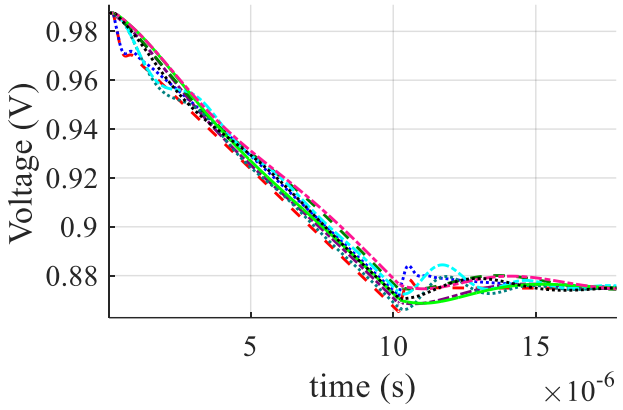


Fig. 2.9 Transient voltage response for all nine runs of the screening experiment in Table 2.1, using a current step with a rise time of 10 µs.

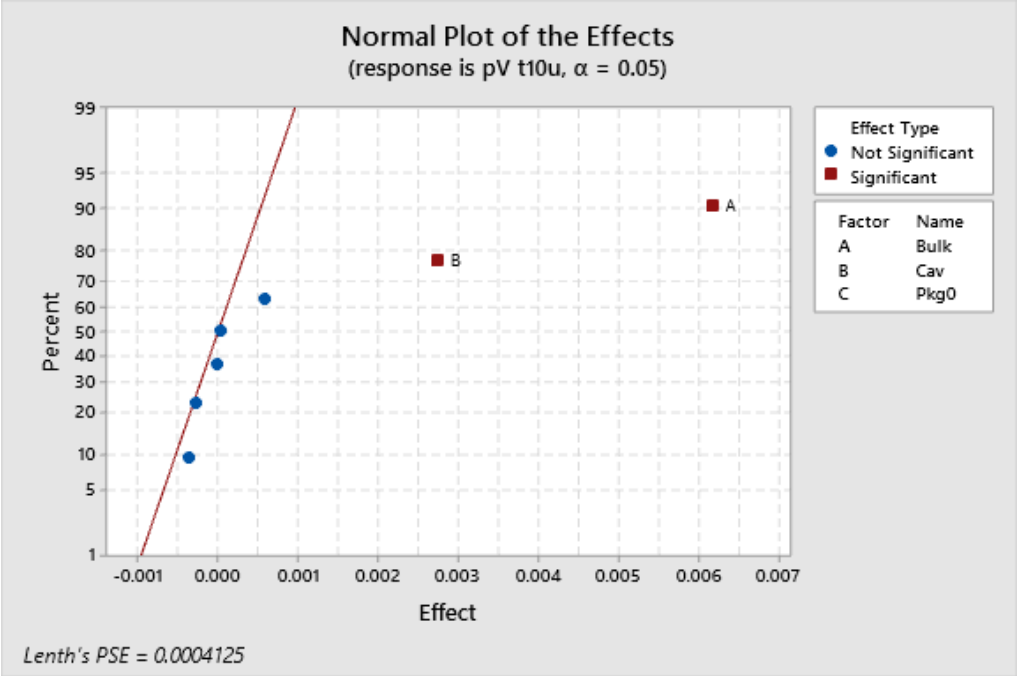


Fig. 2.10 Normal plot showing the significant and not significant effects for the current step analysis, using a current step with a rise time of 10 µs and all capacitor types have a minimum of 1 capacitor as shown in Table 2.1.

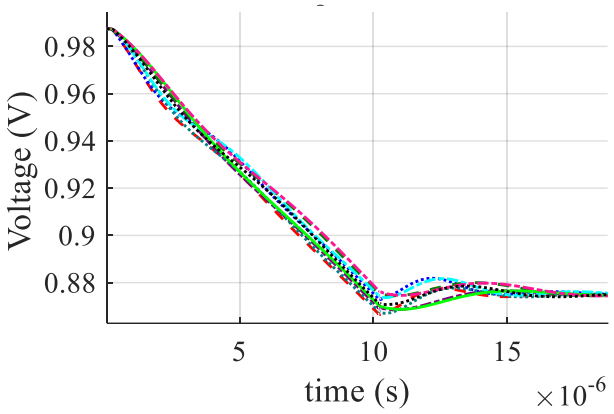


Fig. 2.11 Transient voltage response for all nine runs of the screening experiment in Table 2.2 using a current step with a rise time of 10 μs.

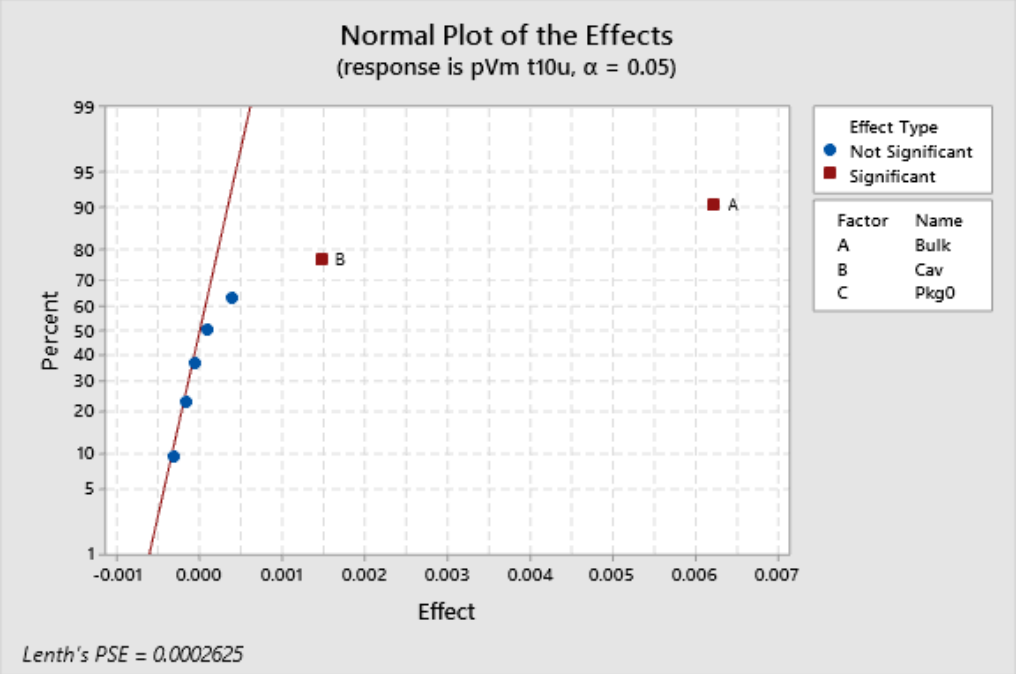


Fig. 2.12 Normal plot showing the significant and not significant effects for the current step analysis, using a current step with a rise time of 10 μs and all capacitor types have different minimum of capacitors as shown in Table 2.2.

2.3. Conclusions

In this chapter, both the frequency- and time-domain performances of a PDN were analyzed in terms of the effects of decoupling capacitors on the PDN to ensure acceptable noise levels when circuits start drawing current. The PDN structure was modeled by simple lumped RLC circuits in a limited frequency band. To maintain the impedance profile within certain limits, different types of capacitors were placed throughout the PDN. A statistical study was performed to find the active factors in the design. with a current step of 50 nanoseconds of rise time, the active factors in the design were the cavity and package 0 capacitors. In order to see the effects of the third voltage droop, a current step with a slower rise time was needed. With a rise time of 10 microseconds, the cavity capacitors were significant, and the bulk capacitors were significant in the time domain. The study was performed using an ideal voltage regulator with an infinite bandwidth, causing the bulk capacitors to not present as frequency-domain active factors affecting the impedance profile.

3. Power Delivery Network Impedance Profile and Voltage Droop Optimization

The design process of power delivery networks (PDN) in modern computer platforms is becoming more relevant and complex due to its relationship with high-frequency effects on signal integrity. When circuits start operating, the changing current flowing through the PDN produces fluctuations creating voltage noise. Unsuccessful noise control compromises data integrity as it will cause the amplitude of the eye diagram in the vertical direction to collapse due to the voltage noise, additionally, the time signal crossing a reference will spread out in the horizontal direction, causing jitter and reducing the eye opening [Smith-17].

In designing the PDN it is important to know the worst-case current drawn by the chips, since the acceptable voltage level required by the chips depends on the frequency spectrum of this current. The worst-case current spectrum and the voltage tolerance specifications of the design determines the impedance target that the PDN must meet to keep the voltage noise at acceptable levels for all chips. The impedance profile is then a figure of merit of the acceptability of the PDN design. Utilizing decoupling capacitors to reduce the impedance profile and reduce current surges is a viable PDN design strategy that ensures minimal change in the power supply under high transient current loads.

Most of the research work on decoupling capacitors optimization for PDN design has been developed either in frequency-domain or in time-domain and include manual trial-and-error optimization processes, as in [Yang-02] and [Chen-96]. Model order reduction (MOR) techniques have been employed to compute the impedance profile and search for optimal locations of the decoupling capacitors [Kamo-00]. Authors in [Hattori-02] obtain frequency dependent Poynting vectors and iteratively place decoupling capacitors at the port with maximum Poynting vector magnitude. The work done in [Zheng-03] models the inductive effect of packages and extracts a resistance-capacitance-susceptance model to build a macromodel using MOR techniques; then a simulated annealing algorithm is used to search for the optimal types of decoupling capacitors. Simulated annealing is used in [Chen-07] to minimize the total cost of decoupling capacitors under the constraints of a worst-case voltage noise bound instead of using impedance targets. Parameter extraction techniques to develop scalable lumped models and surrogate-based optimization

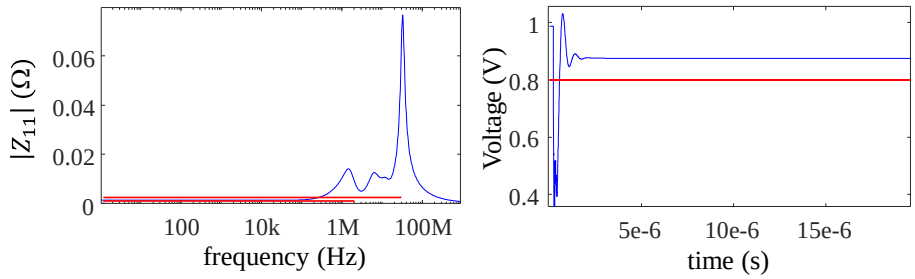
exploiting machine learning techniques are proposed in [Leal-Romo-20], exploiting the resultant metamodels to perform numerical PDN optimization exclusively in time-domain, or in the frequency domain as the work in [Moreno-Mojica-19a].

In this chapter, an optimization approach to determine the number of decoupling capacitors in the PDN described in Section 2.1 is presented, aiming at decreasing the amount of decoupling capacitors without violating the PDN design specifications, looking at both the impedance profile in the frequency domain and the resulting voltage droop in the transient time-domain. Several optimization experiments are conducted to reduce as much as possible the number of decoupling capacitors and in consequence, the overall PDN cost, without violating the PDN target impedance and transient voltage design specifications. The work is illustrated by optimizing the PDN of a CPU power network of an Intel® Xeon® server platform. This chapter consists of a more detailed version of the work in [Moreno-Mojica-20a] and [Moreno-Mojica-21a].

3.1. Optimization of a PDN Combining Frequency- and Time-Domain Effects: First Approach

Let $\boldsymbol{x} \in \Re^n$ represent the vector of n design parameters of the power delivery network, whose responses of interest are in vectors $\boldsymbol{R}_z(\boldsymbol{x}, f)$, and $\boldsymbol{R}_v(\boldsymbol{x}, t)$. In this formulation, $\boldsymbol{R}_z(\boldsymbol{x}, f)$ contains the PDN impedance profile response, i. e., the magnitude of the Z_{11} parameter at the frequency band of interest, and $\boldsymbol{R}_v(\boldsymbol{x}, t)$ contains the PDN voltage droop response, i. e., the amplitude of the transient voltage of the PDN. The design parameters are in vector $\boldsymbol{x}$, which contains the number of decoupling capacitors in the PDN to reduce the number of design optimization variables, only the number of bulk, cavity, and package 0 decoupling capacitors are optimized (see Fig. 2.4), since previous studies on the circuit provided the insight as to the capacitors with the largest effects on the circuit responses (see Section 2.2). Thus, the optimization variables are $\boldsymbol{x} = [N_{\text{BulkCap}} \;\; N_{\text{CavityCap}} \;\; N_{\text{Pkg0Cap}}]^{\text{T}}$. Package 1 and package 2 capacitors are left at the minimum of 1 for all starting points or seeds, excepting for seed 3, where the optimization with twenty package 1 capacitors is explored. All capacitors of the same type have the same capacitance and parasitics.

Error vector functions are used to measure the degree to which the responses satisfy or violate the performance specifications of a maximum target impedance of 2.24 mΩ for frequencies



a) b) c)

Fig. 3.1 Results for seed 1 before optimization: a) impedance profile; b) time-domain voltage pulse; c) seed values used for the optimization.

lower than f_{H} = 28.8 MHz, a minimum target impedance of 1.02 mΩ for frequencies lower than f_{H2} = 2 MHz, and a minimum voltage specification of 0.8 V for the voltage transient pulse.

The optimization problem uses a minimax formulation as

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} \max\left\{\boldsymbol{e}_{\mathrm{Z}}^{\mathrm{T}}(\boldsymbol{x}, f)\ \boldsymbol{e}_{v}^{\mathrm{T}}(\boldsymbol{x}, t)\ \boldsymbol{e}_{\mathrm{B}}^{\mathrm{T}}(\boldsymbol{x})\right\} \tag{3-1}$$

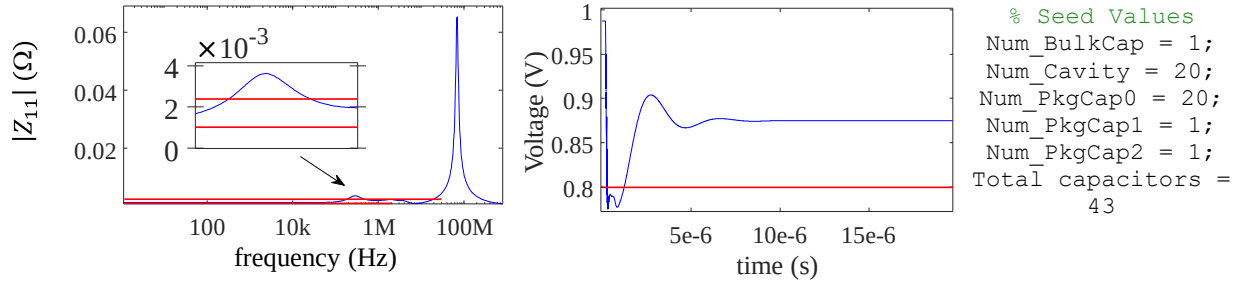
The error vector function $\boldsymbol{e}_{\mathrm{Z}}(\boldsymbol{x}, f)$ is used to ensure a desired maximum target impedance, where f is the simulated frequency, and is defined as

$$\boldsymbol{e}_{\mathrm{Z}}(\boldsymbol{x}, f) = \begin{cases} \dfrac{\boldsymbol{R}_{\mathrm{Z}}(\boldsymbol{x}, f)}{2.24\ \mathrm{m\Omega}} - 1 & \text{for } f \le f_H \\ 1 - \dfrac{\boldsymbol{R}_{\mathrm{Z}}(\boldsymbol{x}, f)}{1.02\ \mathrm{m\Omega}} & \text{for } f \le f_{H2} \end{cases} \tag{3-2}$$

The error vector function $\boldsymbol{e}_{v}(\boldsymbol{x}, t)$ is used to ensure a desired maximum transient voltage droop, where t is the simulated time,

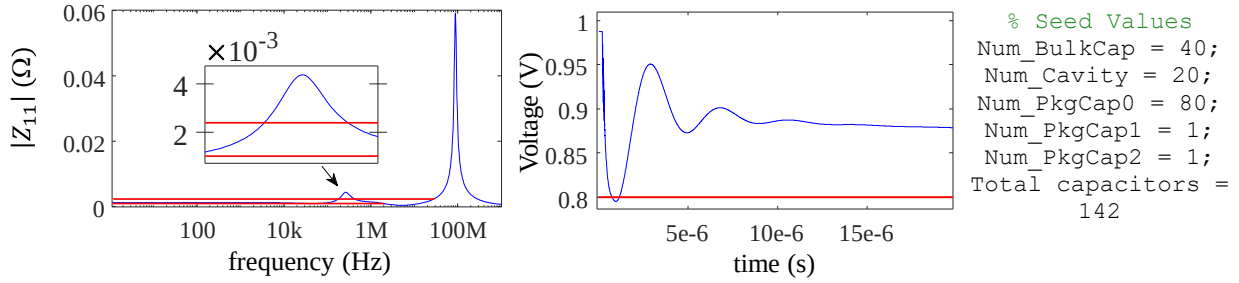
$$\boldsymbol{e}_{\mathrm{V}}(\boldsymbol{x}, t) = \left\{1 - \frac{\boldsymbol{R}_{v}(\boldsymbol{x}, t)}{0.8\ \mathrm{V}} \quad \text{for } 0 \le t \le t_{\mathrm{final}} \right. \tag{3-3}$$

The error function $\boldsymbol{e}_{\mathrm{B}}(\boldsymbol{x})$ is used to keep the optimization variables within feasible bounds and is defined as



a) b) c)

Fig. 3.2 Results for seed 2 before optimization: a) impedance profile; b) time-domain voltage pulse; c) seed values used for the optimization.



a) b) c)

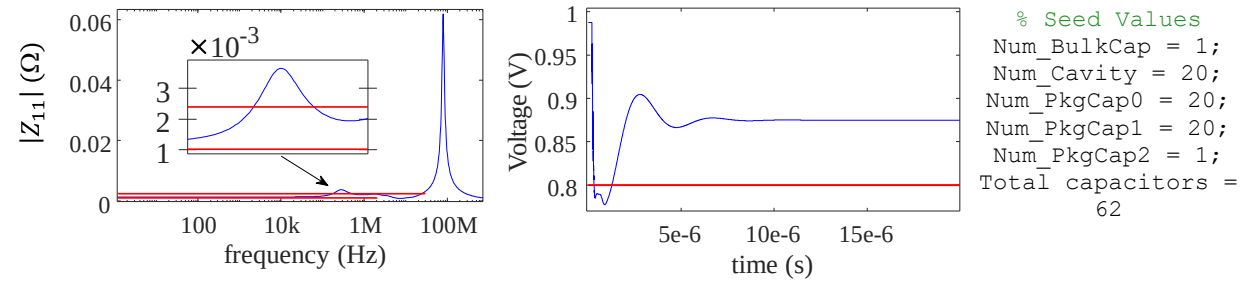
Fig. 3.3 Results for seed 3 before optimization: a) impedance profile; b) time-domain voltage pulse; c) seed values used for the optimization.

$$\boldsymbol{e}_{\mathrm{B}}(\boldsymbol{x}) = L_{\mathrm{B}} - \boldsymbol{x} \tag{3-4}$$

where L_{B} is the limiting lower bound for the optimization variables to ensure their values are positive and no less than 1. Here $L_{\mathrm{B}} = 1$. Notice that operations are element-wise.

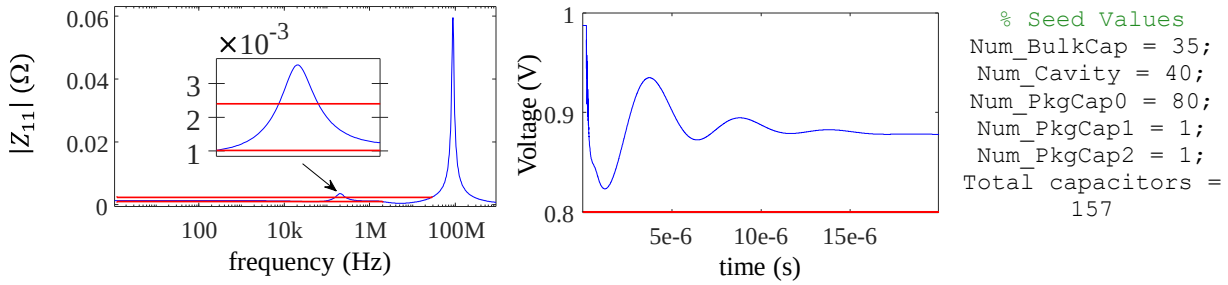
The number of decoupling capacitors, $\boldsymbol{x}$, is now optimized. The Nelder-Mead optimization algorithm is used to solve (3-1).

Fig. 3.1 to Fig. 3.5 show the PDN impedance profile and the resulting voltage pulse, before optimization, for different seed values that were used in the optimization efforts. Fig. 3.6- to Fig. 3.7 show the results after optimization for those seeds. When using seed 1 (Fig. 3.6) the optimization ended with a total of 233 capacitors and a low but not negative objective function value; the resulting voltage pulse meets the specification requirements, however the impedance profile does not meet the maximum impedance target for all frequencies. Using seed 2 (Fig. 3.7) the optimization ended with a total of 148 capacitors and a negative objective function value, meaning all requirements were met. Using seed 3 (Fig. 3.8) the optimization ended with 148 capacitors, and the minimum voltage and the maximum target impedance requirements were



a) b) c)

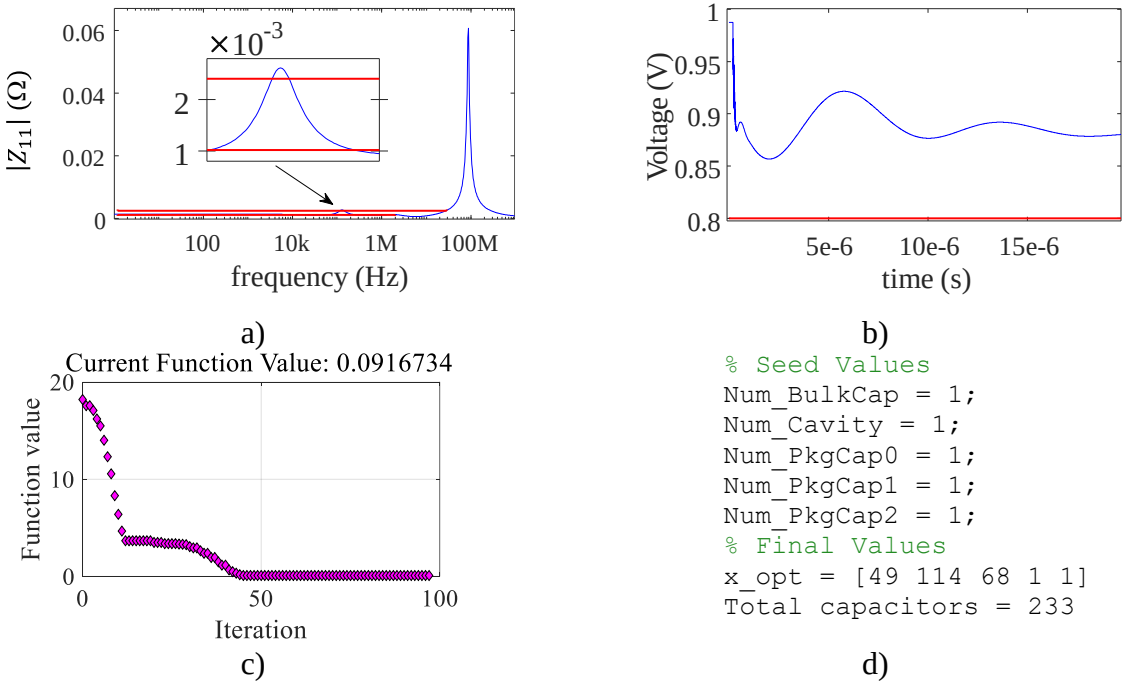
Fig. 3.4 Results for seed 4 before optimization: a) impedance profile; b) time-domain voltage pulse; c) seed values used for the optimization.



a) b) c)

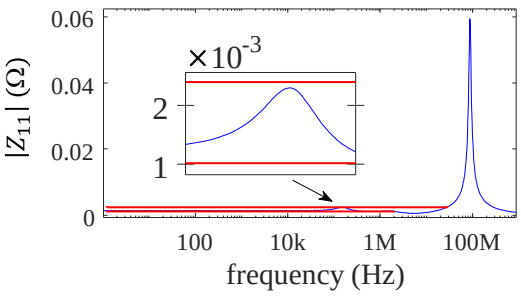
Fig. 3.5 Results for seed 5 before optimization: a) impedance profile; b) time-domain voltage pulse; c) seed values used for the optimization.

satisfied. When using seed 4 (Fig. 3.9) the optimization resulted in negative numbers of capacitors (for the pkg 0 capacitors); the algorithm was not able to correct course and the optimization ended by meeting the stopping criteria but not the requirements (since negative numbers of capacitors are not physically possible, the corresponding responses are not reported). Finally, when using seed 5 (Fig. 3.10) the optimization is successful with 149 capacitors, meeting both design requirements.

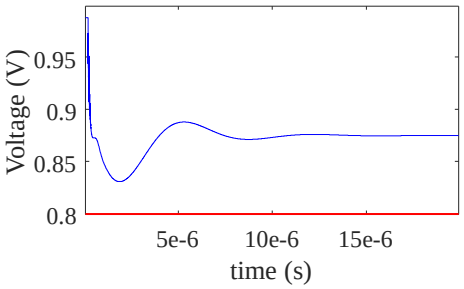


a) b) c) d)

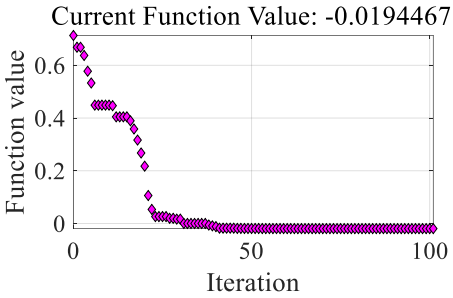
Fig. 3.6 Results for seed 1 approach 1 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors.



a)



b)

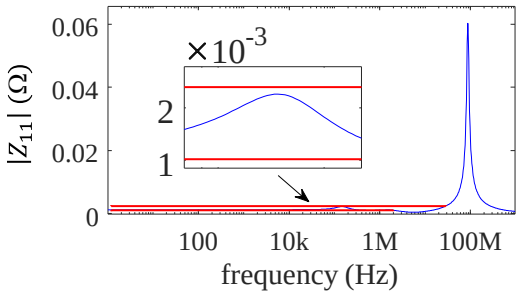


c)

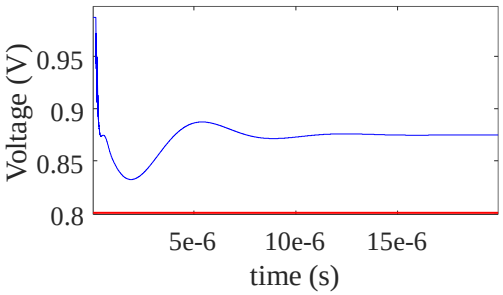
```
% Seed Values
Num_BulkCap = 1;
Num_Cavity = 20;
Num_PkgCap0 = 20;
Num_PkgCap1 = 1;
Num_PkgCap2 = 1;
% Final Values
x_opt = [1 68 77 1 1]
Total capacitors = 148
```

d)

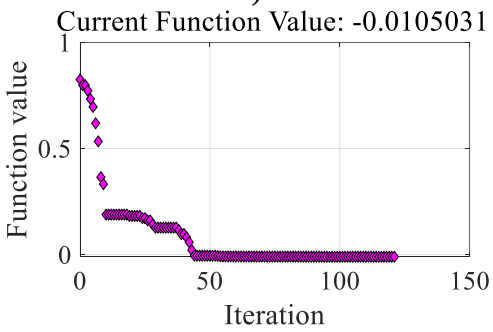
Fig. 3.7 Results for seed 2 approach 1 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors.



a)



b)

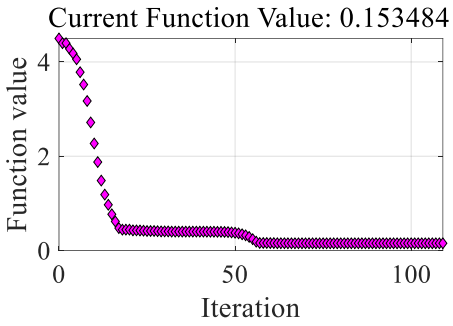


c)

```
% Seed Values
Num_BulkCap = 40;
Num_Cavity = 20;
Num_PkgCap0 = 80;
Num_PkgCap1 = 1;
Num_PkgCap2 = 1;
% Final Values
x_opt = [1 71 74 1 1]
Total capacitors = 148
```

d)

Fig. 3.8 Results for seed 3 approach 1 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors.

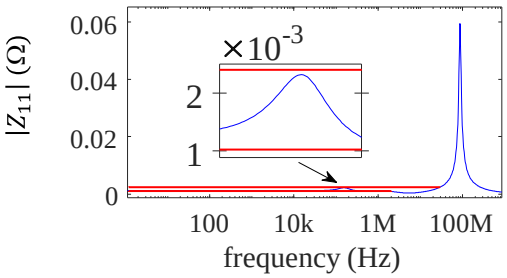


c)

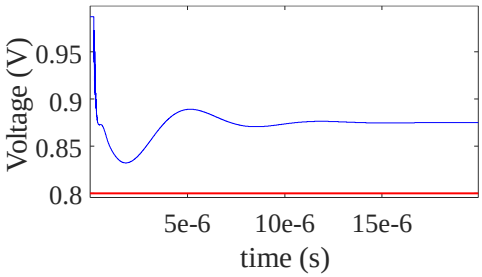
```
% Seed Values
Num_BulkCap = 1;
Num_Cavity = 20;
Num_PkgCap0 = 20;
Num_PkgCap1 = 20;
Num_PkgCap2 = 1;

% Final Values
x_opt = [125 47 -877 20 1]
Total capacitors = NA
```

d)

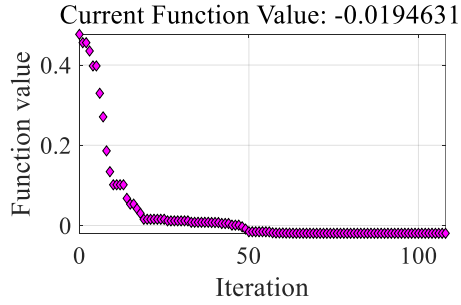
Fig. 3.9 Results for seed 4 approach 1 after optimization: a) evolution of objective function; b) seed values used and optimal values found for the number of capacitors. In this case, a negative value of capacitors was obtained.



a)



b)



c)

```
% Seed Values
Num_BulkCap = 35;
Num_Cavity = 40;
Num_PkgCap0 = 80;
Num_PkgCap1 = 1;
Num_PkgCap2 = 1;
% Final Values
x_opt = [2 68 77 1 1]
Total capacitors = 149
```

d)

Fig. 3.10 Results for seed 5 approach 1 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors.

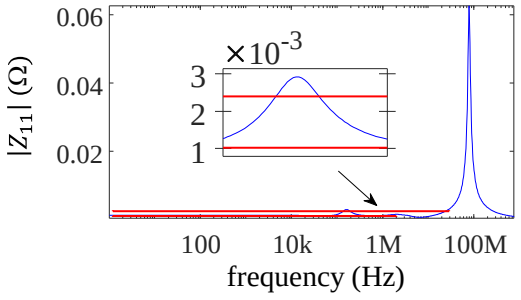
3.2. Optimization of a PDN Combining Frequency and Time Domain Effects – Second Approach

The error function in (3-4) was modified to add a constraint for the maximum number of capacitors allowed, by adding a scalar error defined as

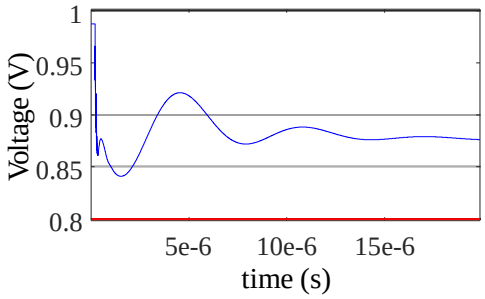
$$(N_{\text{BulkCap}} + N_{\text{CavityCap}} + N_{\text{Pkg0Cap}}) - U_{\text{B}} \tag{3-5}$$

For this new approach, an upper bound $U_{\text{B}} = 140$ is used (only considering the Bulk, Cavity, and Pkg 0 capacitors). The optimization was done with the same seed values as in Section 3.1.

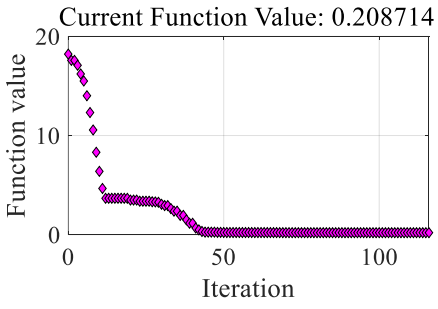
Fig. 3.11 to Fig. 3.15 show the results after optimization using different seeds for this second approach. When using seed 1 (Fig. 3.11) the optimization was not successful, meeting the voltage requirements but not being able to meet the maximum impedance target for all frequencies. Using seed 2 (Fig. 3.12) the optimization successfully meets the voltage and impedance requirements with 142 capacitors in total. Using seed 3 (Fig. 3.13) the optimization was successful in meeting all the requirements with 141 capacitors. Using seed 4 (Fig. 3.14) the optimization was successful in meeting all the requirements with 152 capacitors. Finally, using seed 5 (Fig. 3.15) the optimization was successful in meeting all requirements with only 138 capacitors, even though total number of capacitors used for the seed (157) was larger than the 140 allowed for the bulk,



a)



b)



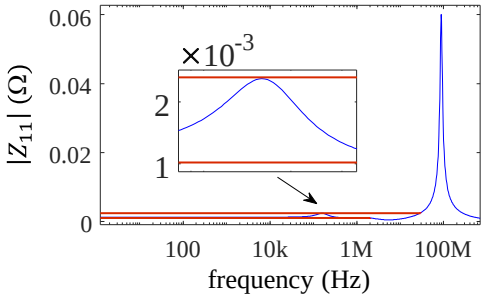
c)

```
% Seed Values
Num_BulkCap = 1;
Num_Cavity = 1;
Num_PkgCap0 = 1;
Num_PkgCap1 = 1;
Num_PkgCap2 = 1;
% Final Values
x_opt = [29 70 40 1 1]
Total capacitors = 140
```

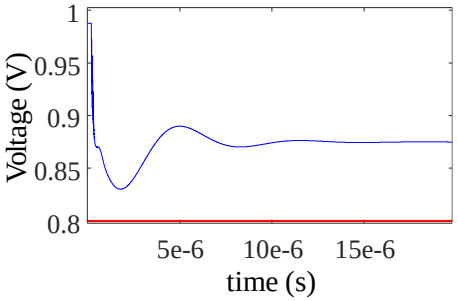
d)

Fig. 3.11 Results for seed 1 approach 2 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors.

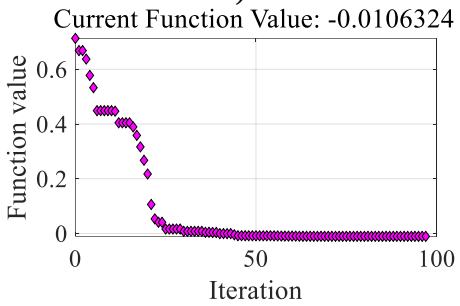
Cavity, and Pkg 0 capacitors.



a)



b)

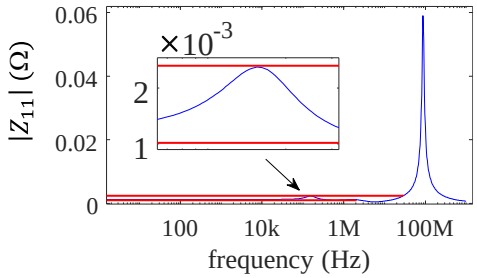


c)

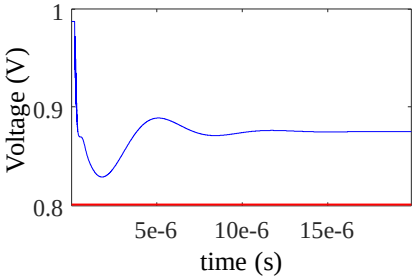
```
% Seed Values
Num_BulkCap = 1;
Num_Cavity = 20;
Num_PkgCap0 = 20;
Num_PkgCap1 = 1;
Num_PkgCap2 = 1;
% Final Values
x_opt = [2 64 74 1 1]
Total capacitors = 142
```

d)

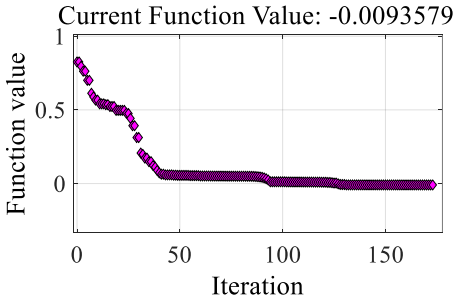
Fig. 3.12 Results for seed 2 approach 2 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors.



a)



b)

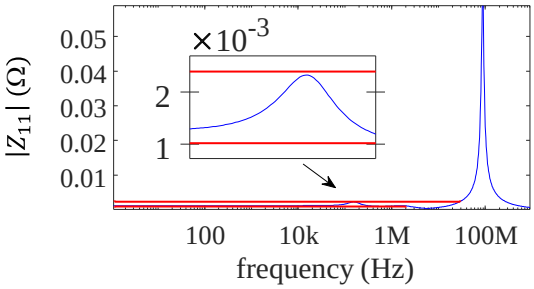


c)

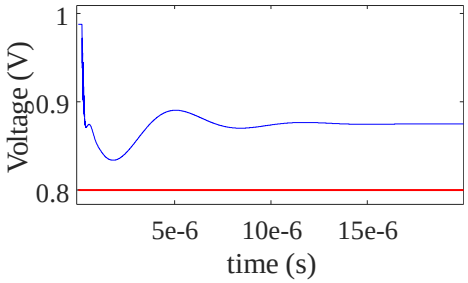
```
% Seed Values
Num_BulkCap = 40;
Num_Cavity = 20;
Num_PkgCap0 = 80;
Num_PkgCap1 = 1;
Num_PkgCap2 = 1;
% Final Values
x_opt = [1 63 75 1 1]
Total capacitors = 141
```

d)

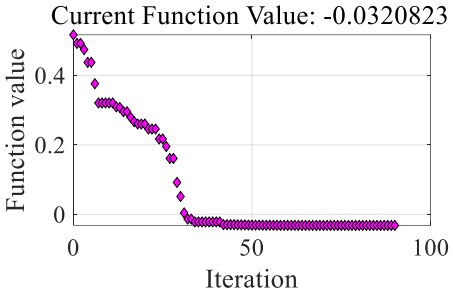
Fig. 3.13 Results for seed 3 approach 2 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors.



a)



b)

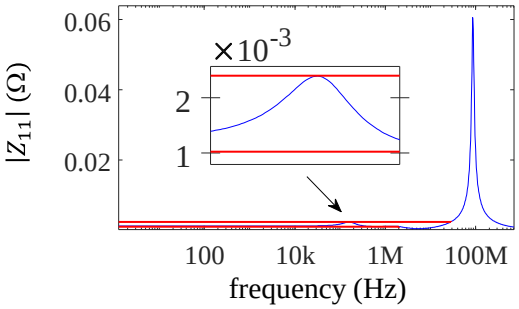


c)

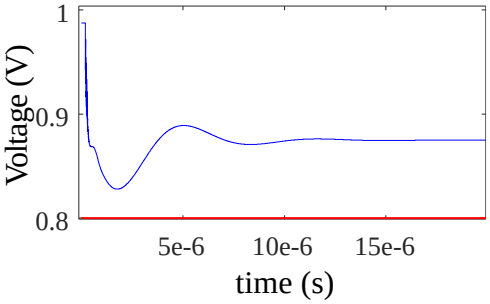
```
% Seed Values
Num_BulkCap = 1;
Num_Cavity = 20;
Num_PkgCap0 = 20;
Num_PkgCap1 = 20;
Num_PkgCap2 = 1;
% Final Values
x_opt = [3 70 58 20 1]
Total capacitors = 152
```

d)

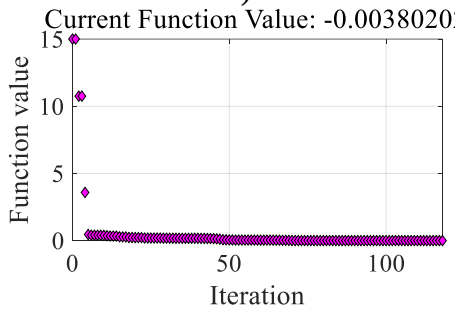
Fig. 3.14 Results for seed 4 approach 2 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors.



a)



b)



c)

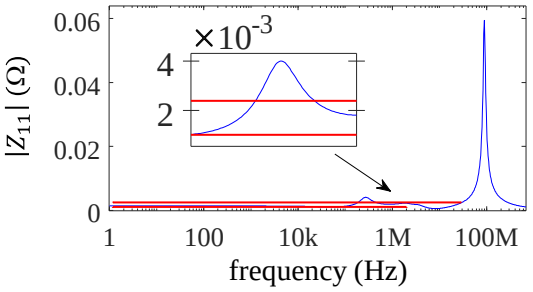
```
% Seed Values
Num_BulkCap = 35;
Num_Cavity = 40;
Num_PkgCap0 = 80;
Num_PkgCap1 = 1;
Num_PkgCap2 = 1;
% Final Values
x_opt = [1 62 73 1 1]
Total capacitors = 138
```

d)

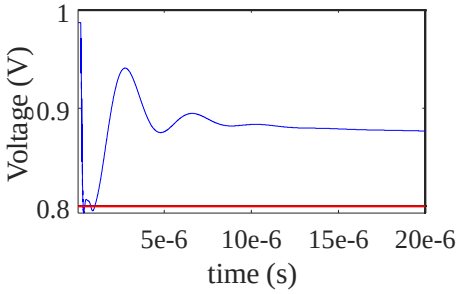
Fig. 3.15 Results for seed 5 approach 2 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors.

3.3. Optimization of a PDN Combining Frequency and Time Domain Effects – Third Approach

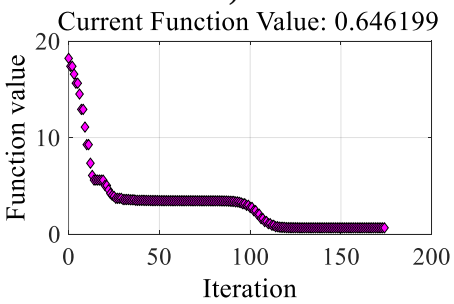
Now, the optimization variables are $\boldsymbol{x} = [N_{\text{BulkCap}}\ N_{\text{CavityCap}}\ N_{\text{Pkg0Cap}}\ N_{\text{Pkg1Cap}}]^{\text{T}}$. The error function in (3-5) now considers the bulk capacitors, cavity capacitors, the package 0 capacitors, and the package 1 capacitors. Fig. 3.16 to Fig. 3.18 show the results after optimization using different seeds for this third approach. Using seed 1 (Fig. 3.16) the optimization was not successful for the voltage requirements nor for the maximum impedance target. Using seed 2 (Fig. 3.17) the optimization was not successful in meeting the frequency-domain requirements. Using seed 3 (Fig. 3.18) the optimization did not meet the maximum impedance requirements. Other seeds were not tested since these results are already worse than using the error function with (3-5).



a)



b)

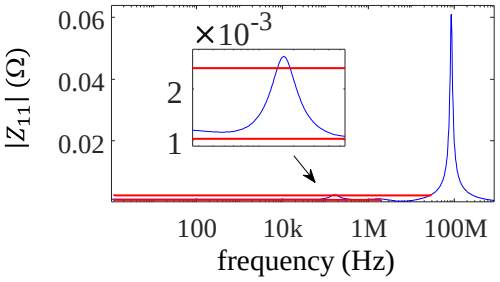


c)

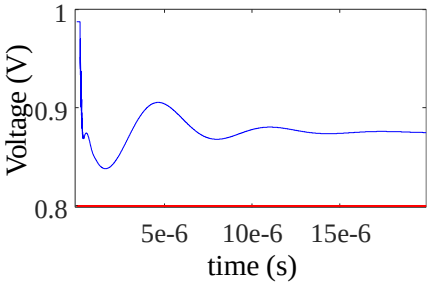
```
% Seed Values
Num_BulkCap = 1;
Num_Cavity = 1;
Num_PkgCap0 = 1;
Num_PkgCap1 = 1;
Num_PkgCap2 = 1;
% Final Values
x_opt = [31 23 1 84 1]
Total capacitors = 140
```

d)

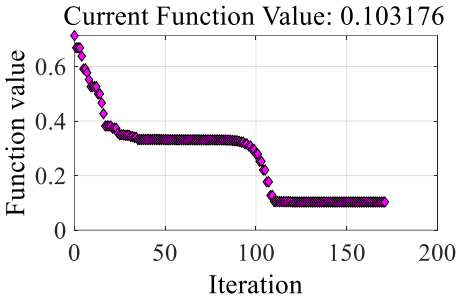
Fig. 3.16 Results for seed 1 approach 3 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors.



a)



b)

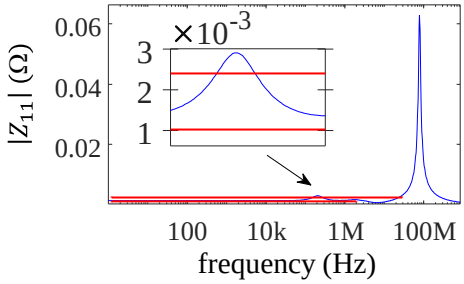


c)

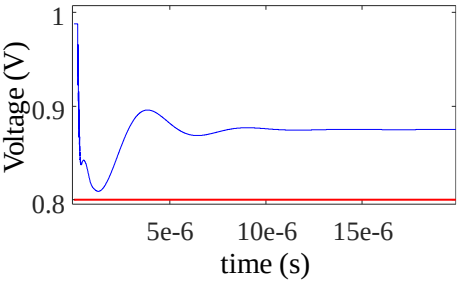
```
% Seed Values
Num_BulkCap = 1;
Num_Cavity = 20;
Num_PkgCap0 = 20;
Num_PkgCap1 = 1;
Num_PkgCap2 = 1;
% Final Values
x_opt = [12 69 57 1 1]
Total capacitors = 140
```

d)

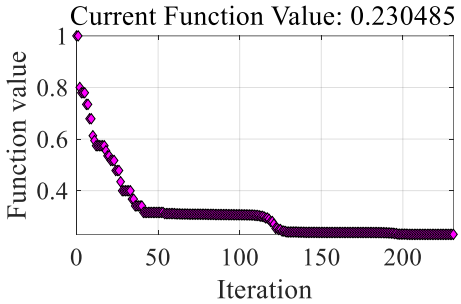
Fig. 3.17 Results for seed 2 approach 3 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors.



a)



b)



c)

```
% Seed Values
Num_BulkCap = 40;
Num_Cavity = 20;
Num_PkgCap0 = 80;
Num_PkgCap1 = 1;
Num_PkgCap2 = 1;
% Final Values
x_opt = [1 38 39 1 1]
Total capacitors = 80
```

d)

Fig. 3.18 Results for seed 3 approach 3 after optimization: a) impedance profile; b) time-domain voltage pulse; c) evolution of objective function; d) seed values used and optimal values found for the number of capacitors.

3.4. Conclusions

A numerical optimization approach to determine the number of decoupling capacitors in a PDN was presented in this chapter. Several optimization efforts were done to optimize the PDN, aiming at decreasing the number of decoupling capacitors without violating the PDN design specifications, looking at both the impedance profile in the frequency-domain and the resulting voltage droop in the transient time-domain. Better results were found by limiting the amount of design variables. Additionally, by limiting the maximum total number of capacitors allowed, a more robust formulation was obtained, capable of minimizing the number of capacitors to yield a PDN that satisfies the target impedance and minimum transient voltage supply specifications.

4. Optimizing a Buck Voltage Regulator and the Number of Decoupling Capacitors for a PDN Application

Voltage regulators (VR) distribute controlled voltage to the various active devices on a power delivery network (PDN), by providing a steady power supply at a desired DC voltage level with an acceptable noise level or ripple.

These VR transfer energy from one place to another, ideally with the highest possible efficiency [Erickson-96]. Substantial power loss dissipated as heat by the VR elements may lead to reduction in system reliability and could require a large and expensive cooling system.

High-efficiency voltage regulators have very little power loss, leading to smaller converter sizes and costs. Switched-mode semiconductor devices are preferred for VR since they are smaller and easier to incorporate into integrated circuits. The Buck converter is one of the most popular switching converters [DiBene-14]. This type of voltage regulator is simple, small, and efficient; it can also be controlled with relative ease.

Voltage regulators maintain a constant voltage regardless of changes in the input voltage or in the effective load resistance by means of a feedback loop [Erickson-96] that is the compensation portion of the VR. However, undesired output voltage ringing can occur if this feedback loop becomes unstable. Therefore, the compensation of the VR must be designed to ensure stability. The phase margin test is a special case of the Nyquist stability theorem and is typically considered to be sufficient for designing most voltage regulators. This test measures the difference between 180° and the actual phase when the gain reaches unity gain (at the crossover frequency). For a stable system the phase margin should be positive. It is typically recommended in the industry for the phase margin to be between 45° to 60° to avoid overshoots and ringing in the transient response [Mitchel-01].

In this chapter, an optimization methodology to determine the best values of the compensation elements of a Buck VR as well as the optimal number of decoupling capacitors in a power delivery network application is presented. Here, the PDN described in Section 2.1 is used. An averaged equivalent circuit model of the Buck converter is employed. Several optimization

efforts are made to optimize the VR compensation, aiming at a desired crossover frequency and phase margin that meets some stability criteria, as well as optimizing the number of decoupling capacitors in the PDN to meet a frequency-domain impedance profile specification and a time-domain voltage droop requirement. This chapter is based on [Moreno-Mojica-20c], [Moreno-Mojica-21b] and [Moreno-Mojica-21c] and consists of a more detailed version of the work in [Moreno-Mojica-21d].

4.1. Modeling the Voltage Regulator

For this work, an averaged model of a Buck converter was chosen. These models lend themselves nicely for small-signal responses to draw Bode or Nyquist plots to assess stability. Since there are no switching components, their simulation is much faster than the corresponding switching model [Sandler-06]. However, it is not possible to see ripple, spikes, gate charge, and instantaneous switching loss. Nevertheless, averaged modeling of voltage regulators is a mainstay of modern control theory, and under the small ripple approximation, they give a good representation of the main regulator characteristics [DiBene-14].

The equivalent circuit of the converter used in this work is shown in Fig. 4.1. The circuit consists of a single-ended input amplifier, a compensation amplifier, an output amplifier, and an output filter. The output amplifier is the power stage portion of the regulator. A simple output filter is connected to the power delivery network input. This filter consists of a resistor R_{VR}, an inductor L_{VR}, and the bulk capacitors that are part of the PDN (not shown in Fig. 4.1). The compensation

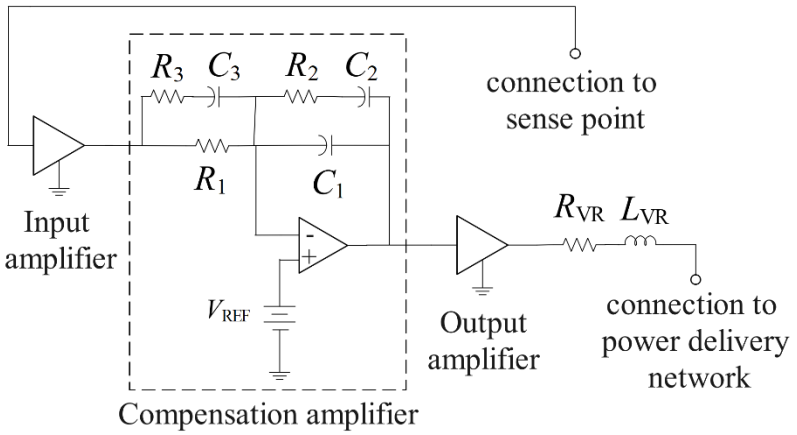


Fig. 4.1 Averaged equivalent circuit of a Buck regulator.

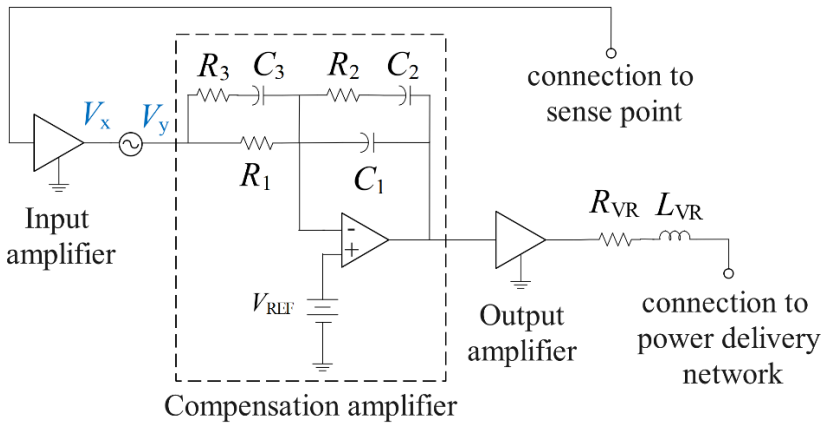


Fig. 4.2 Simulation circuit to obtain Bode plots of the voltage regulator connected to the power delivery network.

circuit amplifies the error between the reference voltage and the amplified feedback signal coming from a sense point on the PDN.

The simulation circuit is modified following [Basso-01] to obtain the open loop gain Bode plots, by adding a small-signal AC perturbation to open the loop. The resulting circuit is shown in Fig. 4.2. Probing V_x/V_y allows to plot the open loop gain magnitude and phase, which is where the stability criteria are assessed.

4.2. Proposed Methodology for Optimizing the Voltage Regulator and the Decoupling Capacitors

In previous studies it was attempted to optimize the decoupling capacitors in the PDN to meet a maximum impedance target and a minimum transient voltage, along with optimizing the compensation elements of the VR to meet a desired crossover frequency with acceptable phase margin for stability. It was not possible to obtain physically meaningful results with this method as the optimization algorithm went into negative numbers of capacitors or negative values for the compensation elements. Better results were obtained by breaking the problem into a several-step methodology. The flow diagram for the proposed methodology is shown in Fig. 4.3.

The first step is to find the optimal number of decoupling capacitors in the PDN, assuming an ideal VR, that meet a desired maximum impedance in the frequency domain and the target minimum transient voltage. The work done in [Moreno-Mojica-21a] found that when using an

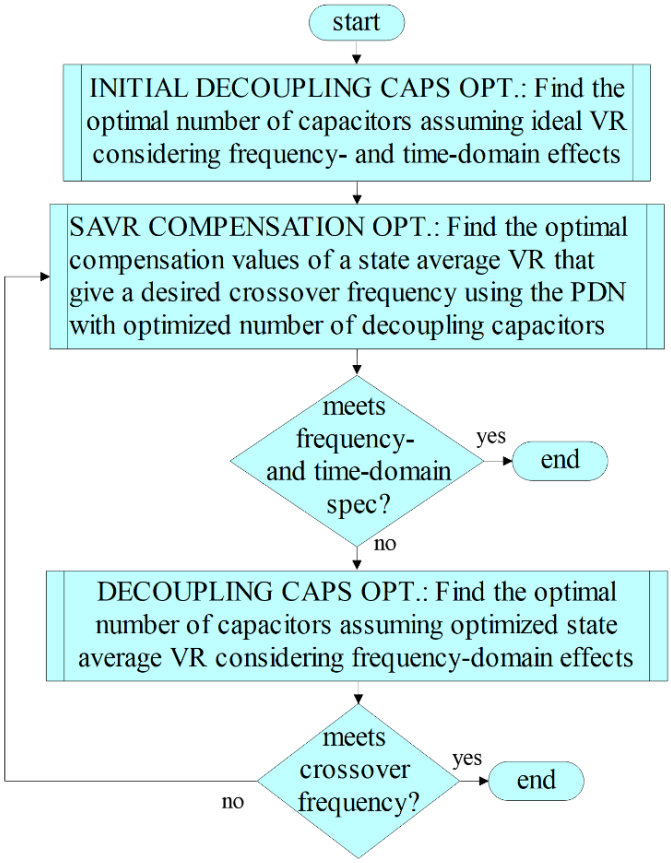


Fig. 4.3 Flow diagram of proposed methodology.

ideal voltage source as the voltage regulator, the bulk capacitors on the PDN do not have a significant effect on the circuit response. This allows to reduce the number of optimization variables and gives a good starting point for the next optimization events.

The second step is to find the optimal values of the components in the compensation of the practical VR connected to the PDN (see Fig. 4.1) with the optimized number of capacitors from the previous step. After finding the optimal compensation values that meets the required crossover frequency it is necessary to check if the entire circuit still meets the maximum impedance and minimum transient voltage.

If the design requirements are not met, the process goes to a third step to re-optimize the decoupling capacitors of the PDN but now using the optimized practical VR. In this step the bulk capacitors must be included in the optimization variables since a practical VR is used. After this optimization the compensation of the VR is checked to see if it meets the required crossover frequency; if not, the process goes back to step 2 until the design requirements are met.

In the next three steps the Nelder-Mead algorithm available in Matlab[5] is used to solve the corresponding optimization problem. SPICE is used for the circuit simulations in Step 1, and Keysight ADS[6] for the circuit simulations in Steps 2 and 3.

4.2.1 Step 1: Optimizing the Number of Capacitors in the PDN Assuming an Ideal VR

Let $\boldsymbol{x} \in \Re^n$ represent the vector of n design parameters of the power delivery network, whose responses of interest are in vectors $\boldsymbol{R}_{\mathrm{z}}(\boldsymbol{x}, f)$ and $\boldsymbol{R}_{v}(\boldsymbol{x}, t)$. The PDN impedance profile response, i. e., the magnitude of the Z_{11} parameter at the frequency band of interest is contained in $\boldsymbol{R}_{\mathrm{z}}(\boldsymbol{x}, f)$, and the PDN voltage droop response, i. e., the amplitude of the transient voltage of the PDN is contained in $\boldsymbol{R}_{v}(\boldsymbol{x}, t)$. The design parameters are in vector $\boldsymbol{x}$, which contains the number of decoupling capacitors in the PDN. The number of decoupling capacitors in the PDN is first optimized using an ideal voltage source of 1 V as the voltage regulator. Here only the number of cavity capacitors ($N_{\mathrm{CavityCap}}$) and the number of capacitors located at the package 0 location (N_{Pkg0Cap}) are optimized. The bulk capacitors and the capacitors located at package 1 and package 2 locations are left fixed. The optimization variables are $\boldsymbol{x} = [N_{\mathrm{CavityCap}} \;\; N_{\mathrm{Pkg0Cap}}]^{\mathrm{T}}$ (number of cavity and package 0 capacitors).

The design specifications are a maximum target impedance of 2.4 mΩ for frequencies lower than $f_{\mathrm{H1}} = 28.8$ MHz, a minimum target impedance of 0.52 mΩ for frequencies lower than $f_{\mathrm{H2}} = 400$ kHz, and a minimum transient voltage specification of 0.8 V.

The optimization problem uses a minimax formulation,

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} \max\{\boldsymbol{e}_{\mathrm{z}}^T(\boldsymbol{x}, f), \boldsymbol{e}_{v}^T(\boldsymbol{x}, t), \boldsymbol{e}_{\mathrm{B}}^T(\boldsymbol{x})\} \tag{4-1}$$

where the error vector function $\boldsymbol{e}_{\mathrm{z}}(\boldsymbol{x}, f)$ is used to ensure a desired maximum target impedance, where f is the simulated frequency, the error vector function $\boldsymbol{e}_{v}(\boldsymbol{x}, t)$ is used to ensure a desired maximum transient voltage droop, where t is the simulated time, and the error function $\boldsymbol{e}_{\mathrm{B}}(\boldsymbol{x})$ is used to keep the optimization variables within feasible bounds.

The error vector function $\boldsymbol{e}_{\mathrm{z}}(\boldsymbol{x}, f)$ is defined as

[5]MATLAB, Version 9.8.0.1359463 (R2020a), The MathWorks, Inc., 1 Apple Hill Drive, Natick MA 01760-2098, 2020.
[6]ADVANCED DESIGN SYSTEM (ADS), Version 512.update2.0, Keysight Technologies, 1400 Fountaingrove Pkwy, Santa Rosa CA 95403-1738, 1985-2020.

$$\boldsymbol{e}_{\mathrm{z}}(\boldsymbol{x},f)=\begin{cases}\frac{\boldsymbol{R}_{\mathrm{z}}(\boldsymbol{x},f)}{2.4\ \mathrm{m\Omega}}-1 & \text{for } f\le f_{\mathrm{H1}}\\ 1-\frac{\boldsymbol{R}_{\mathrm{z}}(\boldsymbol{x},f)}{1.02\ \mathrm{m\Omega}} & \text{for } f\le f_{\mathrm{H2}}\end{cases} \tag{4-2}$$

The error vector function $\boldsymbol{e}_{v}(\boldsymbol{x},t)$ is defined as

$$\boldsymbol{e}_{v}(\boldsymbol{x},t)=\left\{1-\frac{\boldsymbol{R}_{v}(\boldsymbol{x},t)}{0.8\ \mathrm{V}}\quad \text{for } 0\le t\le t_{\mathrm{final}}\right. \tag{4-3}$$

The error vector function $\boldsymbol{e}_{\mathrm{B}}(\boldsymbol{x})$ is defined as

$$\boldsymbol{e}_{\mathrm{B}}(\boldsymbol{x})=\begin{cases}L_{\mathrm{B}}-\boldsymbol{x}\\ \frac{(N_{\mathrm{CavityCap}}+N_{\mathrm{PkgoCap}})}{U_{\mathrm{B}}}-1\end{cases} \tag{4-4}$$

where L_{B} is the limiting lower bound for the optimization variables to ensure their values are positive and no less than 1, and U_{B} is the limiting upper bound for the optimization variables. Here $L_{\mathrm{B}}=1$ and $U_{\mathrm{B}}=140$. Notice operations are element-wise in the first part of (4-4).

4.2.2 Step 2: Optimizing the Compensation of a State Average Buck VR for the PDN

Now consider a response $\boldsymbol{R}_{\mathrm{VR}}(\boldsymbol{w},f)$ that contains the VR stability response, i. e., the frequency-domain open loop VR gain magnitude and phase. In this second step the compensation of the state average Buck regulator is optimized to now achieve a crossover frequency of 120 kHz with an acceptable phase margin. For this step, the optimized number of capacitors for the PDN found in step 1 are used. The optimization variables now are $\boldsymbol{w}$ = [R_2(Ω) R_3(mΩ) C_1(pF) C_2(nF) C_3(nF)]$^{\mathrm{T}}$ (see Fig. 4.1). To decrease the number of variables, R_1 was left at 10 kΩ and LVR at 300 nH.

From the work done in [Moreno-Mojica-20c] poor results were seen considering the converter's open loop gain phase in the objective function. For this reason, here only the converter's open loop gain magnitude is considered.

In this step the following minimax formulation is used:

$$\boldsymbol{w}^{*}=\arg\min_{\boldsymbol{w}}\max\{\boldsymbol{e}_{\mathrm{B}}^{T}(\boldsymbol{w}),\boldsymbol{e}_{\mathrm{VR}}^{T}(\boldsymbol{w},f)\} \tag{4-5}$$

where the error function $\boldsymbol{e}_{\mathrm{B}}(\boldsymbol{w})$ is used to keep the optimization variables within feasible bounds, and the error vector function $\boldsymbol{e}_{\mathrm{VR}}(\boldsymbol{w},f)$ is used to ensure the desired open loop frequency response.

The error vector function $\boldsymbol{e}_{\mathrm{B}}(\boldsymbol{w})$ is defined as

$$\boldsymbol{e}_{\mathrm{B}}(\boldsymbol{w}) = 1 - \frac{\boldsymbol{w}}{L_{\mathrm{B}}} \tag{4-6}$$

where L_{B} is the limiting lower bound for the optimization variables to ensure their values are positive; an element-wise subtraction is used in (4-6), with $L_{\mathrm{B}} = 1\times10^{-10}$.

The error vector function $\boldsymbol{e}_{\mathrm{VR}}(\boldsymbol{w}, f)$ in (4-5) is defined as

$$\boldsymbol{e}_{\mathrm{VR}}(\boldsymbol{w}, f) = \begin{cases} \frac{|\boldsymbol{R}_{\mathrm{VR}}(\boldsymbol{w},f)|}{0.8\ dB} - 1 & \text{for } f \geq f_{\mathrm{L}} \\ \frac{|\boldsymbol{R}_{\mathrm{VR}}(\boldsymbol{w},f)|}{-0.8\ dB} - 1 & \text{for } f \leq f_{\mathrm{H}} \end{cases} \tag{4-7}$$

where f_{H} is the upper frequency limit of interest, f_{L} is the lower frequency of interest. The error function (4-7) aims at making $|\boldsymbol{R}_{\mathrm{VR}}(\boldsymbol{w}, f)|$ as close as possible to 0 dB when the crossover frequency is between f_{L} and f_{H}. Here f_{L} = 118 kHz and f_{H} = 122 kHz are used.

4.2.3 Step 3: Optimizing the Number of Capacitors in the PDN using a State Average Buck VR

For this step, the optimization problem (4-1) is solved again, with some modifications. Now a state averaged Buck VR is used, so the bulk capacitors need to be considered. Thus, the optimization variables are now $\boldsymbol{x}$ = $[N_{\mathrm{BulkCap}}\ \ N_{\mathrm{CavityCap}}\ \ N_{\mathrm{Pkg0Caap}}\ ]^{\mathrm{T}}$. By obtaining a stable compensation in the VR it is not necessary to consider the error function $\boldsymbol{e}_v(\boldsymbol{x}, t)$ in (4-1), which helps reducing simulation time significantly; now $U_{\mathrm{B}} = 700$ is used and the error function (4-4) now considers the bulk capacitors,

$$\boldsymbol{e}_{\mathrm{B}} = \begin{cases} L_{\mathrm{B}} - \boldsymbol{x} \\ \frac{(N_{\mathrm{BulkCap}}+N_{\mathrm{CavityCap}}+N_{\mathrm{Pkg0Cap}})}{U_{\mathrm{B}}} - 1 \end{cases} \tag{4-8}$$

Notice operations are element-wise in the first part of (4-8).

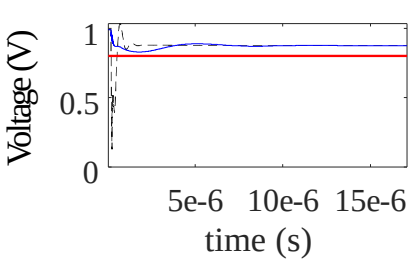
4.3. Results and Discussion

Fig. 4.4 shows the results for Step 1; it is seen that the impedance profile and voltage droop specifications are met after optimization. Fig. 4.5 shows the results for Step 2: the crossover frequency is achieved with a phase margin of 35.84°. When using the state averaged VR with the PDN circuit, the transient voltage droop and the impedance profile are affected. After the optimization in this step, the voltage droop meets the design specifications, however, the

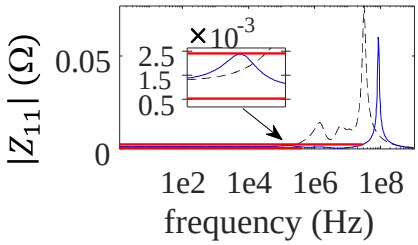
impedance profile has a violating impedance peak of around 5 mΩ. Fig. 4.6 shows the results for Step 3; the voltage droop and impedance profile meet the specifications, however, the VR compensation's crossover frequency moved to a lower frequency.

Following the proposed methodology (see Fig. 4.3), the procedure in Step 2 is repeated. Fig. 4.7 shows the results for this last step. The desired crossover frequency is obtained with a phase margin of 63.4°; the voltage droop and the impedance profile also meet the design specifications.

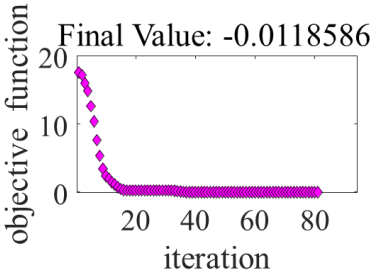
Good results are obtained by following the proposed methodology. The desired crossover frequency is achieved with a good phase margin to ensure stability, as confirmed in the decreased ringing in the transient analysis. The transient voltage noise meets the design specifications, and the impedance profile also meets the maximum target impedance at all frequencies.



a)



b)

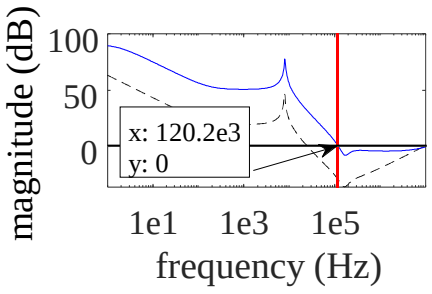


c)

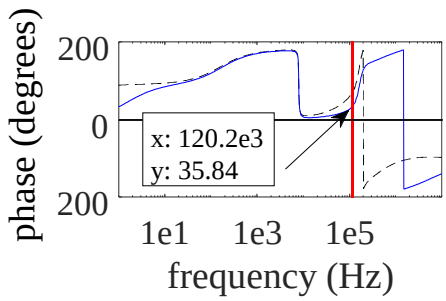
	Seed	Optimized
Bulk	1	1
Cavity	1	63
Pkg0	1	75
Pkg1	1	1
Pkg2	1	1
Total	5	141

d)

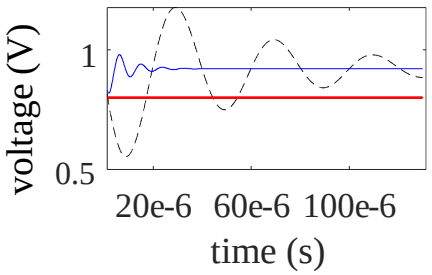
Fig. 4.4 Results for Step 1 before (dashed line) and after (solid line) optimization: a) transient analysis; b) impedance profile; c) objective function evolution and its final value; d) initial and final values for the optimization variables.



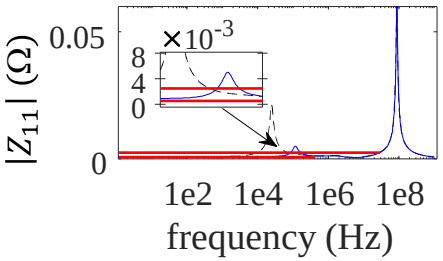
a)



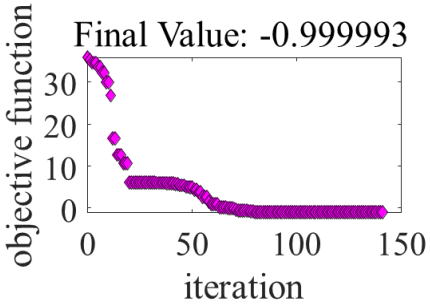
b)



c)



d)

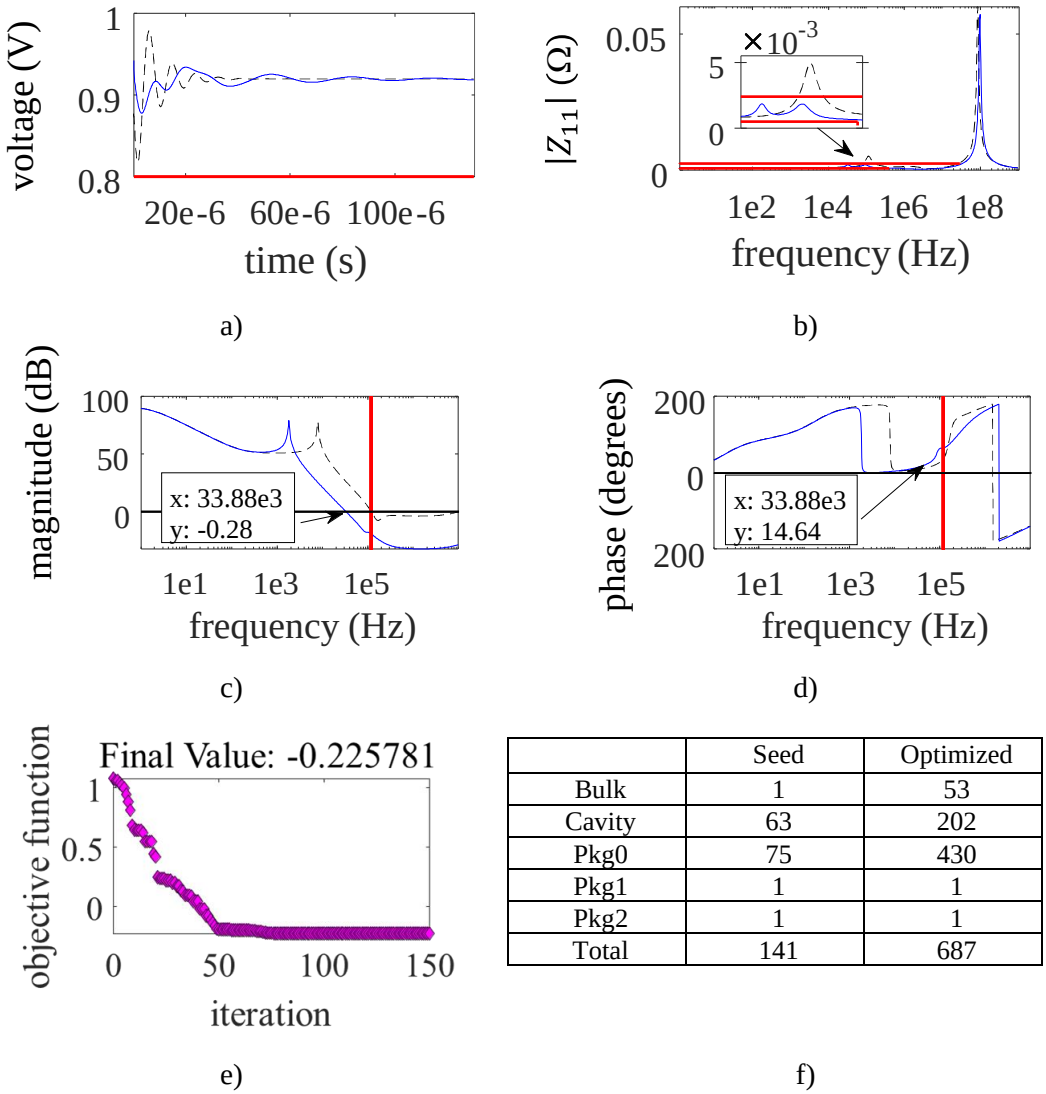


e)

	Seed	Optimized
R_1	10 kΩ	10 kΩ
R_2	10 Ω	8.112 Ω
R_3	100 mΩ	21.546 mΩ
C_1	100 pF	120.544 pF
C_2	100 nF	2.397 nF
C_3	100 nF	92.278 nF
L_{VR}	300 nH	300 nH

f)

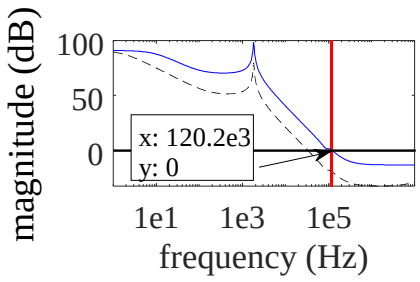
Fig. 4.5 Results for Step 2 before (dashed line) and after (solid line) optimization: a) open loop VR gain magnitude; b) open loop VR gain phase; c) transient analysis; d) impedance profile; e) objective function evolution and its final value; f) initial and final values of the optimization variables.



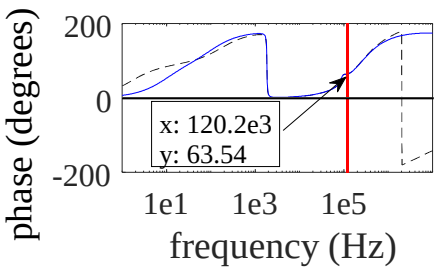
	Seed	Optimized
Bulk	1	53
Cavity	63	202
Pkg0	75	430
Pkg1	1	1
Pkg2	1	1
Total	141	687

f)

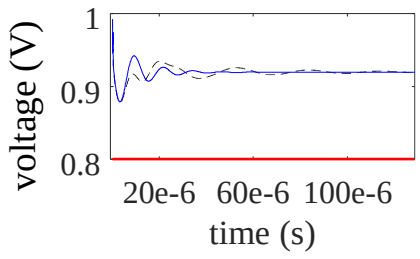
Fig. 4.6 Results for Step 3 before (dashed line) and after (solid line) optimization: a) transient analysis; b) impedance profile; c) open loop VR gain magnitude; d) open loop VR gain phase; e) objective function evolution and its final value; f) initial and final values for optimization variables.



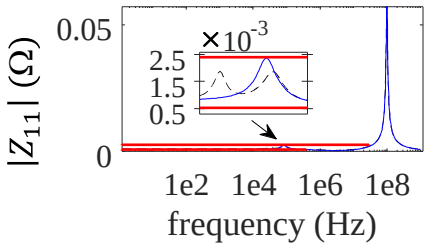
a)



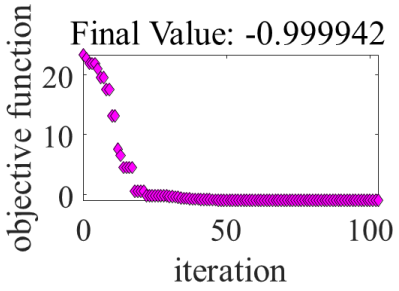
b)



c)



d)



e)

	Seed	Optimized
R_1	10 kΩ	10 kΩ
R_2	8.112 Ω	9.827 Ω
R_3	21.546 mΩ	22.374 mΩ
C_1	120.544 pF	131.170 pF
C_2	2.397 nF	0.340 nF
C_3	92.278 nF	149.765 nF
L_{VR}	300 nH	300 nH

f)

Fig. 4.7 Results for Step 4 before (dashed line) and after (solid line) optimization: a) open loop VR gain magnitude; b) open loop VR gain phase; c) transient analysis; d) impedance profile; e) objective function evolution and its final value; f) initial and final values of the optimization variables.

4.4. Conclusions

An optimization methodology was proposed in this chapter to gradually find the best compensation parameter values of a Buck VR to meet some stability criteria. Additionally, the number of parallel decoupling capacitors was optimized considering simultaneously frequency- and time-domain performance specifications. By using optimal VR compensation parameter values and a minimum number of decoupling capacitors, it was possible to meet the desired

crossover frequency with good phase margin, while the transient voltage and the impedance profile were able to meet the design specifications.

5. Frequency- and Time-Domain Yield Optimization of a Power Delivery Network Subject to Large Decoupling Capacitor Tolerances

Voltage regulators (VR) need to provide a steady power supply at a desired DC voltage level with an acceptable noise level or ripple to the active devices on a computer platform. However, VRs sometimes are too slow and allow unacceptable voltage drops caused by transient switching currents at the devices. These voltage drops can cause performance deterioration and severe functional failures on high-speed computer platforms. Decoupling capacitors are used to supply transient current to switching devices when the VRs are not able to do so, thus regulating the voltage transient droops. To ensure delivery of load voltages withing acceptable operating ranges, many decoupling capacitors are used to reduce power supply noise by lowering the PDN impedance profile.

The work in [Moreno-Mojica-21d] proposes a "single-point" nominal optimization methodology to find the best values of the compensation elements of a voltage regulator, as well as the optimal number of decoupling capacitors in a PDN. However, commercially available decoupling capacitors typically present large manufacturing variability.

In this chapter, a statistical analysis and yield estimation is performed on a nominally optimized PDN considering capacitance variations in the decoupling capacitors. The yield simulations are done in Keysight PathWave Advanced Design System (ADS[7]) through Matlab[8], following the procedure detailed in [Moreno-Mojica-21e], where the statistical capabilities of Keysight ADS are exploited to save simulation time and memory.

Additionally, this chapter proposes a frequency- and time-domain yield optimization approach suitable for power delivery networks considering the impact of large tolerances in the decoupling capacitors. As the responses of interest for yield calculations, the impedance profile magnitude, the transient voltage droop, and the voltage regulator stability are included. The numerical results obtained from the proposed optimization approach demonstrate its effectiveness

[7] ADVANCED DESIGN SYSTEM (ADS), Version 512.update2.0, Keysight Technologies, 1400 Fountaingrove Pkwy, Santa Rosa CA 95403-1738, 1985-2020.
[8] MATLAB, Version 8.2.0.701 (R2013b), The MathWorks, Inc., 1 Apple Hill Drive, Natick MA 01760-2098, 2013.

to assess and improve the PDN performance and reliability, confirmed by a significantly increased overall yield. This chapter is based on [Moreno-Mojica-21e], [Moreno-Mojica-21f], and [Moreno-Mojica-21g] and consists of a more detailed version of the work in [Moreno-Mojica-22a].

5.1. PDN Decoupling Capacitors

Voltage regulators must deliver the output voltage needed by the different chips on the computer platform. When the chips start operating, they create fluctuations in the load current and voltage. The VRs have a control loop that helps regulate these changes. However, the response time of the VR control loop can be slow, in the order of micro-seconds. As a result, temporary voltage fluctuations will be seen by the die before the VR can mitigate the changes. These fluctuations can jeopardize the performance and the reliability of the connect devices [Radhakrishnan-21]. A good PDN design is determined by its ability to keep the load voltage within an acceptable operating range even as the load current changes or the input voltage fluctuates. Keeping the impedance of the power delivery network low across a broad range of frequencies, from DC to several hundred MHz, helps to suppress power supply noise [Radhakrishnan-21]. Furthermore, an optimal PDN impedance profile reduces electromagnetic emissions, which contributes to pass the regulating agency's emission standards [Kim-04][Ichimura-14].

Several stages of decoupling capacitors are used to provide switching circuits with extra current when the VR is too slow to provide it. These capacitors also decrease the inductive effect in the loop current path, thus reducing the power supply noise [Kim-04].

Several types of decoupling capacitors are typically needed. The bulk capacitors are the biggest in the PDN. They act as charge reservoirs to transient currents and are placed on the motherboard at the output filter of the voltage regulator to provide large bulk storage [Analog Devices-09]. They provide a low impedance at low frequencies, below a few MHz.

Electrolytic capacitors are commonly used to provide the bulk output filter capacitance for the switching regulator on the platform. Aluminum electrolytic capacitors are commonly used on desktops and server platforms. Tantalum polymer capacitors are used on mobile platforms that have height constraints [Radhakrishnan-21].

Cavity capacitors, also known as land side capacitors, are located under the cavity of the

package and are effective at middle frequencies, up to several MHz. Package capacitors, or die side capacitors, are effective at higher frequencies, up to several hundred MHz. Despite being subject to significant variation in capacitance as a function of temperature and voltage bias, multi-layer ceramic capacitors (MLCC) are the most common in decoupling at middle and high frequencies due to their compact size, low loss, and low inductance [Radhakrishnan-21][Analog Devices-09].

In this chapter, the bulk capacitors are considered tantalum polymer capacitors with a form factor size code of 2917, the cavity capacitors are MLCC with a size code of 0805, and the package capacitors are also MLCC with size code 0201. The size code defines the capacitor package size in terms of width 0.0X inch and depth 0.0Y inch and is denoted as 0X0Y. These particular capacitors have a maximum tolerance of $\pm 20\%$ [Murata Manufacturing-21].

5.2. Statistical Analysis of a Power Delivery Network

Designing a robust PDN involves accounting for uncontrollable variations, such as the capacitance value fluctuations of the decoupling capacitors due to their tolerance associated to their manufacturing process. A robust design aims at selecting product design parameter values so that uncontrollable variations result in minimal deviation from the expected performance [Meehan-93]. Ideally, a robust PDN implies designing for high yield and reliability.

For yield analysis, circuit parameter values are randomly varied around a nominal reference design according to their manufacturing tolerances and their probability distribution functions. The corresponding simulated circuit responses are compared to specified performance criteria. The ratio of the number of circuits that pass the performance specifications to the total number of simulated circuits can be used to approximate the yield around the nominal reference design [Meehan-93][[Bandler-02][Rayas-Sánchez-06][Agilent Technologies-00].

Yield estimation is typically based on the Monte Carlo method. The accuracy of this method for yield estimation is independent of the number of statistical variables [Agilent Technologies-00] as long as the outcomes or system responses available have statistical significance. Typically, many simulations of the complete circuit (outcomes), are needed to achieve statistically significant results, which makes Monte Carlo in general a computationally intensive method for yield prediction.

Let $\boldsymbol{x} \in \Re^n$ represent the vector of n design parameters of the power delivery network, whose responses of interest are in vectors $\boldsymbol{R}_{\mathrm{z}}(\boldsymbol{x}, f)$, $\boldsymbol{R}_{\mathrm{VR}}(\boldsymbol{x}, f)$, and $\boldsymbol{R}_{v}(\boldsymbol{x}, t)$. In the proposed formulation, $\boldsymbol{R}_{\mathrm{z}}(\boldsymbol{x}, f)$ contains the PDN impedance profile response, i. e., the magnitude of the Z_{11} parameter at the frequency band of interest; $\boldsymbol{R}_{\mathrm{VR}}(\boldsymbol{x}, f)$ contains the VR stability response, i. e., the frequency-domain open loop VR gain magnitude and phase; and finally $\boldsymbol{R}_{v}(\boldsymbol{x}, t)$ contains the PDN voltage droop response, i. e., the amplitude of the transient voltage of the PDN. The design parameters are in vector $\boldsymbol{x}$, which contains the values of the decoupling capacitors in the PDN, $\boldsymbol{x} = [C_{\mathrm{Bulk}}\ \ C_{\mathrm{Cavity}}\ \ C_{\mathrm{Pkg0}}\ \ C_{\mathrm{Pkg1}}\ \ C_{\mathrm{Pkg2}}]^{\mathrm{T}}$ (bulk, cavity, and package capacitors, in pF).

Error vector functions are used to measure the degree to which the responses satisfy or violate the performance specifications. The error vector function $\boldsymbol{e}\mathrm{VR}(\boldsymbol{x}, f)$ is used for the desired open loop frequency response of the VR and is defined as

$$\boldsymbol{e}_{\mathrm{VR}}(\boldsymbol{x}, f) = \begin{cases} \frac{|\boldsymbol{R}_{\mathrm{VR}}(\boldsymbol{x}, f)|}{0.8\ dB} - 1 & \text{for } f \geq f_{\mathrm{L}} \\ \frac{|\boldsymbol{R}_{\mathrm{VR}}(\boldsymbol{x}, f)|}{-0.8\ dB} - 1 & \text{for } f \leq f_{\mathrm{H}} \end{cases} \tag{5-1}$$

$$U_{VR}(\boldsymbol{x}) = \max\left\{\boldsymbol{e}_{\mathrm{VR}}^{\mathrm{T}}(\boldsymbol{x}, f)\right\} \tag{5-2}$$

where f_{H} is the high frequency limit of interest, f_{L} is the low frequency limit of interest. Error function in (5-1) aims at making $|\boldsymbol{R}_{\mathrm{VR}}(\boldsymbol{x}, f)|$ as close as possible to 0 dB when the crossover frequency is between f_{L} and f_{H}. The effect of this formulation is illustrated in Fig. 5.1. Here $f_{\mathrm{L}} = 118$ kHz and $f_{\mathrm{H}} = 122$ kHz are used.

The error vector function $\boldsymbol{e}_{\mathrm{Z}}(\boldsymbol{x}, f)$ is used to ensure the desired maximum target impedance,

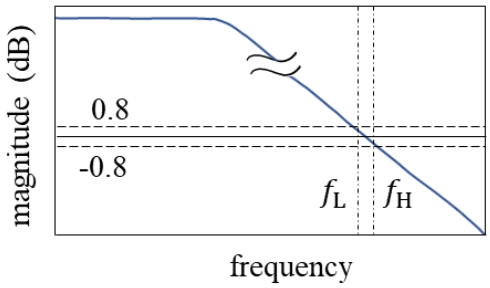


Fig. 5.1 Open loop VR gain magnitude showing crossover frequency between f_{L} and f_{H}.

$$\boldsymbol{e}_{\mathrm{Z}}(\boldsymbol{x},f)=\begin{cases}\frac{|\boldsymbol{R}_{\mathrm{Z}}(\boldsymbol{x},f)|}{2.4\ \mathrm{m\Omega}}-1 & \text{for } f\le f_{\mathrm{H1}}\\ 1-\frac{|\boldsymbol{R}_{\mathrm{Z}}(\boldsymbol{x},f)|}{0.52\ \mathrm{m\Omega}} & \text{for } f\le f_{\mathrm{H2}}\end{cases} \tag{5-3}$$

$$U_{\mathrm{Z}}(\boldsymbol{x})=\max\left\{\boldsymbol{e}_{\mathrm{Z}}^{\mathrm{T}}(\boldsymbol{x},f)\right\} \tag{5-4}$$

where f is the simulated frequency. Here $f_{\mathrm{H1}}=28.8$ GHz and $f_{\mathrm{H2}}=400$ kHz.

The error vector function $\boldsymbol{e}_v(\boldsymbol{x},t)$ is used to ensure a desired maximum transient voltage droop,

$$\boldsymbol{e}_v(\boldsymbol{x},t)=\left\{1-\frac{\boldsymbol{R}_v(\boldsymbol{x},t)}{0.8\ \mathrm{V}}\quad \text{for } 0\le t\le t_{\mathrm{final}}\right. \tag{5-5}$$

$$U_v(\boldsymbol{x})=\max\{\boldsymbol{e}_v^{\mathrm{T}}(\boldsymbol{x},t)\} \tag{5-6}$$

where t is the simulated time.

For the statistical yield analysis, the element values in the k-th vector of decoupling capacitors $\boldsymbol{x}^k$ are considered to spread around their nominal values in $\boldsymbol{x}$ according to their individual statistical distributions and tolerances. The k-th design parameters can be presented as

$$\boldsymbol{x}^k=\boldsymbol{x}+\Delta\boldsymbol{x}^k,\ k=1,2,\dots,N \tag{5-7}$$

where N is the number of simulations or outcomes and $\Delta\boldsymbol{x}^k$ is a k-th random perturbation.

Each outcome is associated with an acceptance index defined by

$$I_{VR}(\boldsymbol{x}^k)=\begin{cases}1, & \text{if } U_{\mathrm{VR}}(\boldsymbol{x}^k)\le 0\\ 0 & \text{if } U_{\mathrm{VR}}(\boldsymbol{x}^k)>0\end{cases} \tag{5-8}$$

$$I_{\mathrm{Z}}(\boldsymbol{x}^k)=\begin{cases}1, & \text{if } U_{\mathrm{Z}}(\boldsymbol{x}^k)\le 0\\ 0 & \text{if } U_{\mathrm{Z}}(\boldsymbol{x}^k)>0\end{cases} \tag{5-9}$$

$$I_v(\boldsymbol{x}^k)=\begin{cases}1, & \text{if } U_v(\boldsymbol{x}^k)\le 0\\ 0 & \text{if } U_v(\boldsymbol{x}^k)>0\end{cases} \tag{5-10}$$

If N is significantly large for statistical significance, following [Bandler-02] the yield Y can be approximated as the nominal design $\boldsymbol{x}$ for each type of performance by using

$$Y_{VR}(\boldsymbol{x})\approx\frac{1}{N}\sum_{k=1}^{N}I_{\mathrm{VR}}(\boldsymbol{x}^k) \tag{5-11}$$

$$Y_{\mathrm{Z}}(\boldsymbol{x})\approx\frac{1}{N}\sum_{k=1}^{N}I_{\mathrm{Z}}(\boldsymbol{x}^k) \tag{5-12}$$

$$Y_v(\boldsymbol{x})\approx\frac{1}{N}\sum_{k=1}^{N}I_v(\boldsymbol{x}^k) \tag{5-13}$$

5.2.1 Estimating the Number of Outcomes for Reliable Monte Carlo Analysis

In Monte Carlo yield estimation, the values for uncertain variables are replaced with functions that generate random samples from independent normal probability distributions [Agilent Technologies-00]. Many trials are run, each one using different random values for all uncertain variables.

To perform a reliable Monte Carlo yield estimation, it is necessary to approximate how many simulations are enough to obtain an reasonably accurate yield estimation. Too few runs and the yield will be inaccurate. As the number of simulations increases, the yield estimate approaches the true design yield [Agilent Technologies-00]. However, running too many simulations takes a long time and it might take even longer to analyze data afterwards.

Authors in [Meehan-93] propose a way to calculate the number of Monte Carlo trials or outcomes. This calculation assumes that all statistical system parameters follow a normal, or Gaussian, probability distribution function. The number of simulations N needed to have a certainty c when calculating the yield can be obtained from

$$N = round\left\{\frac{[t(c)]^2}{\varepsilon^2}(Y)(1-Y)\right\} \tag{5-14}$$

where Y is the expected yield ($0 < Y < 1$), ε is the error in the yield estimation, t is a statistical value with a probability c to happen (c is the area under the bell curve between $-t$ and $+t$). For sample sizes larger than 30, $t(c)$ is the Z-score value for the required confidence level [Sullivan-21].

To evaluate (5-14), the expected yield needs to be evaluated in advance. Fig. 5.2 shows a preliminary Monte Carlo yield estimation with only five hundred trials or outcomes, using a 20% tolerance in the capacitance of the decoupling capacitors of the PDN shown in Fig. 2.4. It can be see that the impedance profile yield starts stabilizing at around 60%. Using this value as the expected yield in (5-14), the number of required Monte Carlo trials is calculated for a 95% confidence and 1% error. The parameter values and results for these calculations are shown in Table 5.1. 9,220 Monte Carlo trials are needed to get a reliable yield estimation with 95% confidence and 1% error.

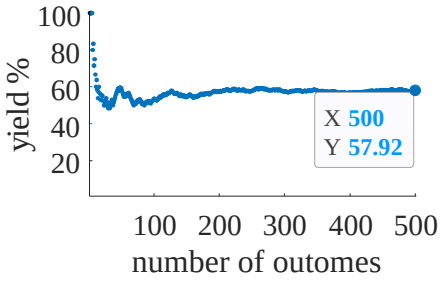


Fig. 5.2 Preliminary yield analysis for the PDN impedance profile, with only 500 outcomes, to estimate expected yield.

TABLE 5.1. ESTIMATING THE NUMBER OF MONTE CARLO OUTCOMES USING (5-14)

Parameter	Value
confidence	95%
$t(c)$	1.96 (Z-score)
ε	0.01
Y	0.60
number of trials	9220

5.2.2 Statistical Analysis Results

Here, yield estimation is done for the impedance profile and transient voltage droop of the PDN in [Moreno-Mojica-21d], as well as for the stability of the voltage regulator used in that PDN, as formulated in Section 5.2. 9,220 random outcomes are used for the three yield estimations. Fig. 5.3 shows the yield for the impedance profile; it stabilizes at around 57%. The yield for the stability of the voltage regulator is shown in Fig. 5.4, showing a yield of around 53%. Finally, a 100% yield is obtained for the transient voltage droop, as confirmed in Fig. 5.5, indicating that the minimum transient voltage droop is not sensitive to fluctuations in the capacitance of the decoupling capacitors. The transient voltage waveform does show different levels of voltage ripple for different values in the capacitance of the decoupling capacitors, however, the minimum voltage droop maintains a level above the specified performance.

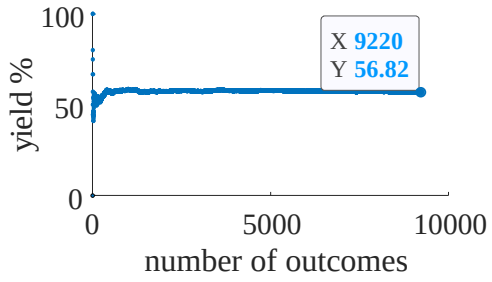


Fig. 5.3 Yield analysis for the PDN impedance profile using 9220 outcomes.

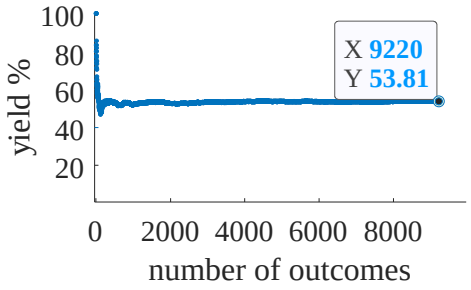


Fig. 5.4 Yield analysis for the voltage regulator stability of the PDN using 9220 outcomes.

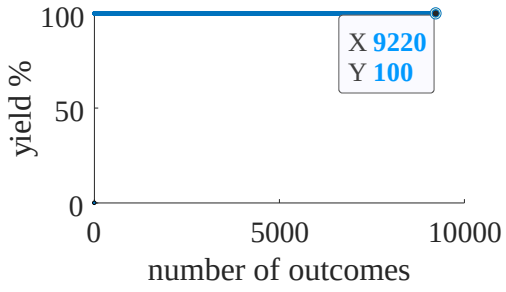


Fig. 5.5 Yield analysis for the PDN transient voltage droop using 9220 outcomes.

5.3. Yield Optimization of the PDN

It was found that considering 9,220 random outcomes, 95% confidence and 1% error, the yield for the impedance profile stabilizes at around 57%; the yield for the stability of the voltage regulator is around 53%; and a 100% yield is obtained for the transient voltage droop, indicating that the minimum transient voltage droop is not sensitive enough to fluctuations in the capacitance of the decoupling capacitors. The three PDN responses of interest for 500 random outcomes around the nominally optimized PDN design using ±20% variation in decoupling capacitance values are shown in Fig. 5.6. The transient voltage waveform does show different levels of voltage ripple for different values in these capacitances, however, the minimum voltage droop maintains a level above the specified performance, as confirmed in Fig. 5.6c.

The yield of the nominally optimized PDN obtained in [Moreno-Mojica-21d] is now optimized, subject to large decoupling capacitor tolerances, considering simultaneously the impedance profile and the VR stability design specifications. Since the minimum transient voltage droop is not sensitive enough to fluctuations in the capacitance of the decoupling capacitors, this is not considered in the yield optimization objective function to speed up the process. However,

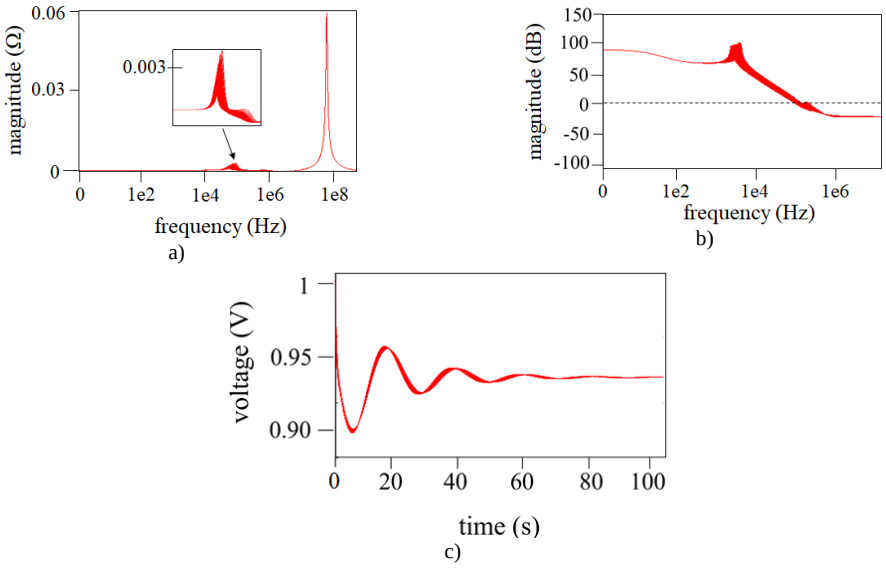


Fig. 5.6 PDN responses of interest for the 500 random outcomes around the nominally optimized PDN design using ±20% variation in decoupling capacitance values: a) impedance profile; b) open loop VR gain; and c) transient voltage droop.

the yield of the transient voltage droop is verified with the optimal yield component values.

5.3.1 Yield Optimization Formulation

The formulation in Section 5.2 is used to estimate the yield of the VR stability and impedance profile when the PDN is subject to variability in the capacitance of the decoupling capacitors.

The design parameters are in vector $\boldsymbol{s} \in \Re^{10}$, which contains the values of the VR compensation design parameters, $\boldsymbol{z} = [R_2(\Omega)\ \ R_3(\text{m}\Omega)\ \ C_1(\text{pF})\ \ C_2(\text{nF})\ \ C_3(\text{nF})]^{\text{T}}$, as well as the values of the capacitance of the decoupling capacitors, $\boldsymbol{w} = [C_{\text{Bulk}}(\mu\text{F})\ \ C_{\text{Cavity}}(\mu\text{F})\ \ C_{\text{Pkg0}}(\mu\text{F})\ C_{\text{Pkg1}}(\text{nF})\ \ C_{\text{Pkg2}}(\text{nF})]^{\text{T}}$; $\boldsymbol{s}^{\text{T}} = [\boldsymbol{z}^{\text{T}}\ \ \boldsymbol{w}^{\text{T}}]$.

The optimization problem considers simultaneously the yield of the VR stability and the yield of the impedance profile with a minimax formulation,

$$\boldsymbol{s}^{*} = \arg\min_{\boldsymbol{s}} \max\left\{e_{\text{YZ}}(\boldsymbol{s}), e_{\text{YVR}}(\boldsymbol{s}), \boldsymbol{e}_{\text{YB}}^{\text{T}}(\boldsymbol{s})\right\} \tag{5-15}$$

where $\boldsymbol{s}^{*}$ is the optimal yield design, $e_{\text{YZ}}(\boldsymbol{s})$ and $e_{\text{YVR}}(\boldsymbol{s})$ are the error scalar functions used to ensure the impedance profile yield and the VR stability yield are above their respective minimum requirements; and $\boldsymbol{e}_{\text{YB}}(\boldsymbol{s})$ is the error vector function used to keep the optimization variables within certain bounds.

Error scalar function $e_{\text{YZ}}(\boldsymbol{s})$ is defined as

$$e_{\text{YZ}}(\boldsymbol{s}) = 1 - \frac{Y_{\text{Z}}(\boldsymbol{s})}{Y_{\text{Zspec}}} \tag{5-16}$$

where Y_{Z} is the impedance profile yield and Y_{Zspec} is the required yield for the impedance profile. Here $Y_{\text{Zspec}} = 75\%$.

Error scalar function $e_{\text{YVR}}(\boldsymbol{s})$ is defined as

$$e_{\text{YVR}}(\boldsymbol{s}) = 1 - Y_{VR}(\boldsymbol{s})Y_{\text{VRspec}} \tag{5-17}$$

where Y_{VR} is the VR stability yield and Y_{VRspec} is the required yield for the VR stability. Here $Y_{\text{VRspec}} = 75\%$.

Error vector function $\boldsymbol{e}_{\text{YB}}(\boldsymbol{s})$ is defined as

$$\boldsymbol{e}_{\text{YB}}(\boldsymbol{s}) = \begin{cases} 1 - \dfrac{\boldsymbol{s}}{\boldsymbol{L}_{\text{B}}} \\ \dfrac{\boldsymbol{s}(6{:}10)}{\boldsymbol{U}_{\text{B}}} - 1 \end{cases} \tag{5-18}$$

TABLE 5.2. DESIGN PARAMETERS VALUES BEFORE AND AFTER YIELD OPTIMIZATION

Parameter	Initial Value	Final Value	Units
Bulk capacitance	418.71	732.85	μF
Cavity capacitance	12.7	17.62	μF
Pkg0 capacitance	1.14	0.9348	μF
Pkg1 capacitance	402.68	344.94	nF
Pkg2 capacitance	6.34	2.08	μF
R_2	9.827	9.5402	Ω
R_3	22.374	22.1182	mΩ
C_1	131.17	51.3604	pF
C_2	0.34	0.4096	nF
C_3	149.765	173.7384	nF

where $\boldsymbol{L}_B \in \Re^{10}$ is a vector of lower bounds; it contains an arbitrarily small number to ensure the VR compensation elements remain positive (1×10^{-10}), as well as the minimum commercial values of the capacitances. The lower bounds are 15 μF for the bulk capacitance, 1 pF for the cavity capacitance, and 0.1 pF for the package capacitances. $\boldsymbol{U}_B \in \Re^5$ is a vector of upper bounds; it only contains the maximum commercial values of the capacitances. The upper bounds are 100 μF for the cavity capacitance, 4.7 μF for the package capacitances, and 940 μF for the bulk capacitors (up to two 470-μF maximum commercial value). Notice that operations in (5-18) are element-wise.

Matlab's Nelder-Mead algorithm [Nelder-65] is used to solve the corresponding optimization problem, and Keysight ADS for the yield evaluations.

5.3.2 Yield Optimization Results

The design parameter values before and after yield optimization are shown in Table 5.2. The yield calculated with 9,220 random outcomes around the optimal yield design found, $\boldsymbol{s}^*$, for each PDN performance domain, are shown in Fig. 5.7. It is seen that a 92.8% yield is achieved for the PDN impedance profile (Fig. 5.7a) and a yield of 90.86 % for the VR stability (Fig. 5.7b). Both yields exceed the requirements and show a significant improvement, since they were 56.82% and 53.81%, respectively, before yield optimization. Fig. 5.7c verifies the yield of the transient voltage

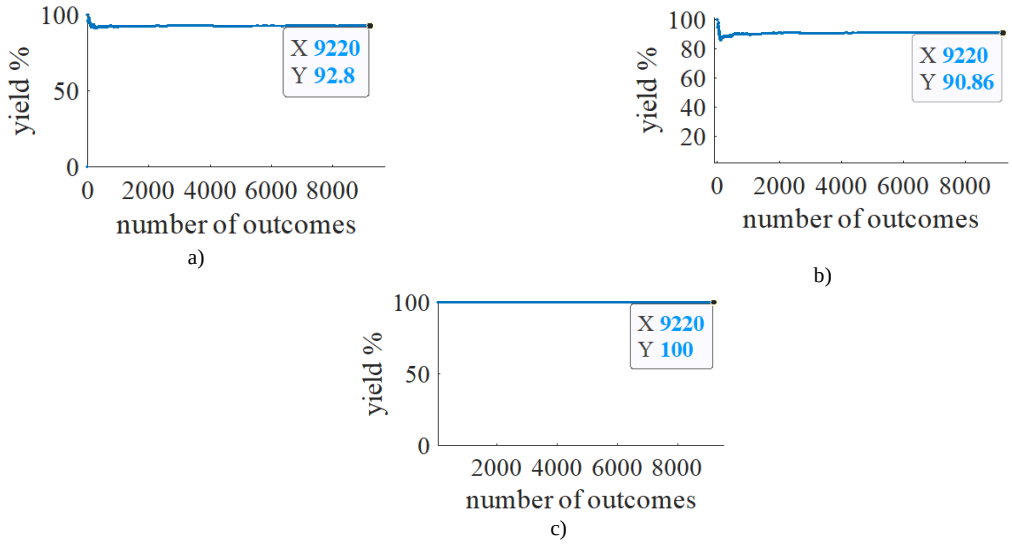


Fig. 5.7 Yield analysis with 9,220 outcomes at the PDN optimal yield design: a) impedance profile; b) VR stability; c) transient voltage droop.

droop is still 100% after the optimization. Fig. 5.8 shows the evolution of the objective function used in (5-15) during yield optimization.

5.4. Conclusions

A statistical analysis and yield prediction was performed in this chapter for a PDN impedance profile, transient voltage droop, and voltage regulator stability. A mathematical formulation to perform this yield estimation was proposed. Keysight ADS statistical capabilities

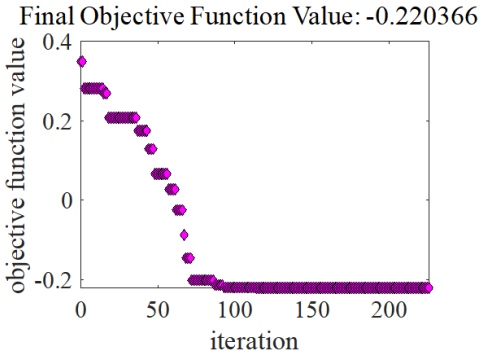


Fig. 5.8 Evolution of the objective function used in (1) during yield optimization.

were exploited to save simulation time and memory, while still allowing automated data processing through Matlab. It was found that the minimum transient voltage droop was not sensitive to fluctuations in the capacitance of the decoupling capacitors, so it maintained the correct performance from the nominal optimization showing a yield of 100%. The impedance profile had a yield of 57% and the stability of the voltage regulator had a yield of 53%. Then, a frequency- and time-domain yield optimization approach was proposed for nominally optimized power delivery networks considering the impact of large tolerances in the decoupling capacitors. After the optimization process, high yields were achieved on both the impedance profile and the VR stability (92.8% and 90.86%, respectively). The numerical results obtained from the proposed optimization approach demonstrated its effectiveness to assess and improve the PDN performance and reliability, confirmed by a significantly increased overall yield.

6. Physics-Based Lumped Circuit Model for Lossless Parallel Plates

A board power delivery network (PDN) consists of multiple couples of power and ground metallic planes with arbitrary shapes separated by thin dielectrics. These planes have a dominant capacitive behavior at low frequencies and an inductive behavior at very high frequencies. However, the inductance in the planes is much smaller than in other structures on the PDN. This makes the planes useful to supply biasing voltages from the decoupling capacitors mounted on the planes to devices switching at high frequencies and support return current of the signal lines [Swaminathan-07].

Optimal placement of decoupling capacitors on the PDN is of particular interest to power integrity designers, as the distance of the capacitor to the signal pad affects the capacitor's effectiveness [Erdin-18]. The distributed planar impedance of the PDN power-ground planes needs to be considered for the location of the decoupling capacitors [Erdin-21]. PDN metallic planes behave as spatially distributed systems and can create standing wave resonances along the *x* and *y* directions due to reflections from the open edges. These resonances can create signal and power integrity problems [Swaminathan-07]. Furthermore, the planes in a PDN can be of arbitrary shape, and under tight ball grid array pin fields they are actually very thin power transmission lines [Erdin-22]. Full-wave electromagnetic EM simulation provides high accuracy and a high degree of versatility in modeling PDN planes with arbitrary shapes; however, the simulation time can be prohibitive for efficient noise predictions [Roy-11].

Equivalent circuit models are computationally much more efficient. A popular approach to model a PDN is to derive an equivalent circuit model that matches the response of the actual structure, however, the equivalent circuit is accurate enough only up to a certain operating frequency [Leal-Romo-20]. Another widely used approach to represent a PDN is to use the partial element equivalent circuit (PEEC) method [Swaminathan-07]. This method essentially consists of a quasi-static EM representation of the physical structure by an equivalent distributed circuit, however, it also has a limited frequency range of validity.

In this chapter, a simplified PDN consisting of a single pair (power and ground) of lossless parallel rectangular planes is considered. Highly accurate full-wave EM simulations on the planes

are performed. The aim is to obtain reliable references to compare versus circuit-level simulations. The effects of different placements of the excitation port on these planes are also examined. Sonnet[9] is used to perform these highly accurate EM simulations. High-resolution discretization in Sonnet is used to observe the superficial current density distribution as well as the impedance profile of the planes. Additionally, the parallel planes are discretized into small cells connected to each other. Each cell is modeled with a basic lumped equivalent circuit. The resultant equivalent circuit for the complete parallel planes is validated versus the full-wave EM simulations implemented in Sonnet. Different physics-based models are evaluated to calculate the lumped elements values of the basic cell, varying the number of cells used. The discretization of the planes allows to place ports anywhere on the equivalent circuit, enabling future research about the effects of placing decoupling capacitors at different locations on the planes, avoiding the high computational cost of the corresponding full-wave electromagnetic (EM) simulation. This chapter corresponds to a slightly modified version of [Moreno-Mojica-22b] and [Moreno-Mojica-22c].

6.1. Sonnet EM Simulations

Sonnet performs full-wave electromagnetic analysis for arbitrary 3D mostly planar structures inside a shielding box, as shown in Fig. 6.1. The sidewalls of the box are made of lossless metal and the top and bottom of the box can be assigned any metal type. The top box surface can also be defined as “free-space”. Port connections are usually made at the sidewalls, though

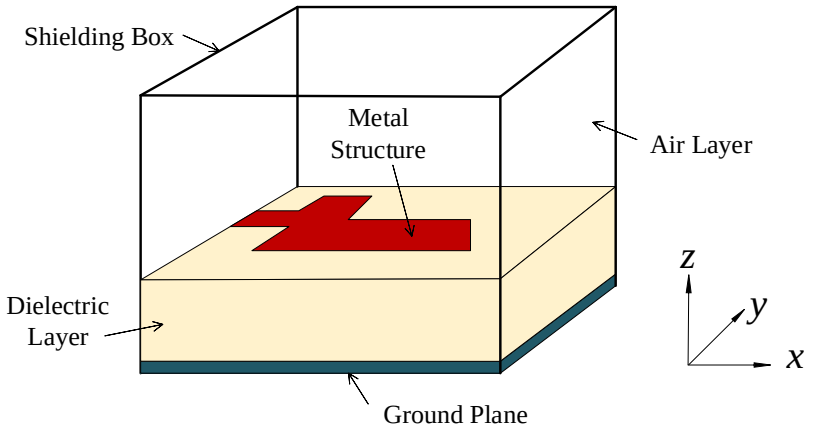


Fig. 6.1 3D planar structure and shielding box in Sonnet.

[9] Sonnet v18.52, Sonnet Software Inc., North Syracuse, NY, 2022, https://www.sonnetsoftware.com/.

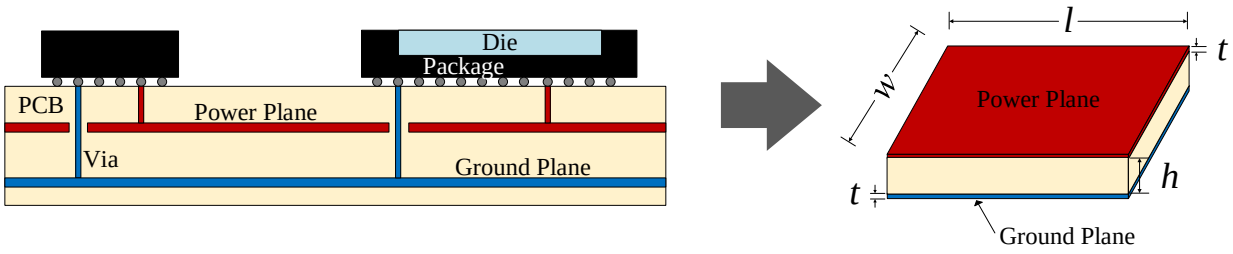


Fig. 6.2 Simplified power delivery network as two parallel metal planes.

reference planes can be shifted to de-embed feedlines to the device under test. The size of the box in the *xy* plane is determined by the size of the substrate which in turns depends on the structure to be simulated. The size in the *z* direction (see Fig. 6.1) is determined by the sum of the substrate thickness of the dielectric layers (including the air layer on top of the structure) [Sonnet Software-22].

A lossless pair of parallel metallic planes is considered as a very simplified PDN, with separation h, metal thickness $t = 0$ and dimensions $w \times l$, as illustrated in Fig. 6.2. The ground plane acts as the bottom plane of the pair, and the top plane is where the excitation port is placed.

When the top plane is touching the shielding box, the current is injected along the entire edge, as demonstrated in Section III. To avoid this, a 50-ohm microstrip line short portion is used to inject the current only at a small section of the plane edge and observe the effects of moving the placement of the excitation port.

All the EM simulations described in Sections III and IV use two different discretization resolutions in Sonnet. The first one uses 2,106 grid subsections when calculating the impedance profiles. This resolution is sufficiently high for Sonnet to reach convergence in calculating $|Z_{11}|$ response over the simulated frequency band. Calculating the impedance profile with that resolution takes approximately 33 minutes using a computer with Intel Core i7-4770 at 3.40 GHz and 16 GB RAM. However, a much higher resolution with 34,672 subsections is used in Sonnet when calculating the surface current distributions in order to obtain high-quality 2D plots. With that resolution, a frequency sweep takes approximately 36 hours of CPU time using the same computer

6.1.1 Parallel Planes Case 1

For this first simulation case, a lossless pair of parallel planes is considered with $h = 5$ mils,

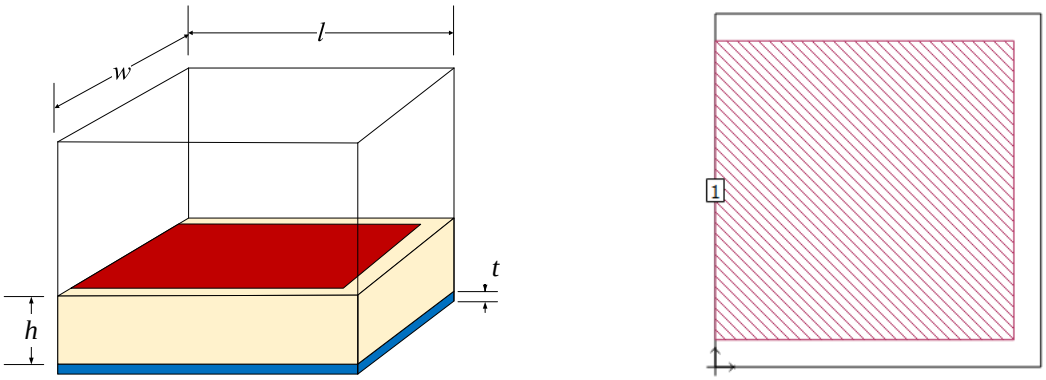


Fig. 6.3 Parallel planes Case 1, where the upper plane left edge touches the shielding box and the excitation port is at the middle of the left plane edge: a) 3D view; b) top view.

w = 306.9 mils, and l = 306.9 mils, with the left edge touching Sonnet's shielding box, as shown in Fig. 6.3. The air layer on top of the structure is 25 mils thick. Highly accurate EM simulations are obtained in Sonnet configuring the grid resolution as indicated in Section III, as in the rest of the EM simulations of this report.

The resulting impedance profile from placing the excitation port at the left edge of the planes is shown in Fig. 6.4. As expected, it is clearly confirmed a capacitive behavior at low frequencies, approximately below 1 GHz. The current distribution plots are shown in Fig. 6.5. In this case, it is seen that the current is injected on the entire left edge of the planes and is forced to spread only in the x direction. Since the current is injected on the entire edge, a different location

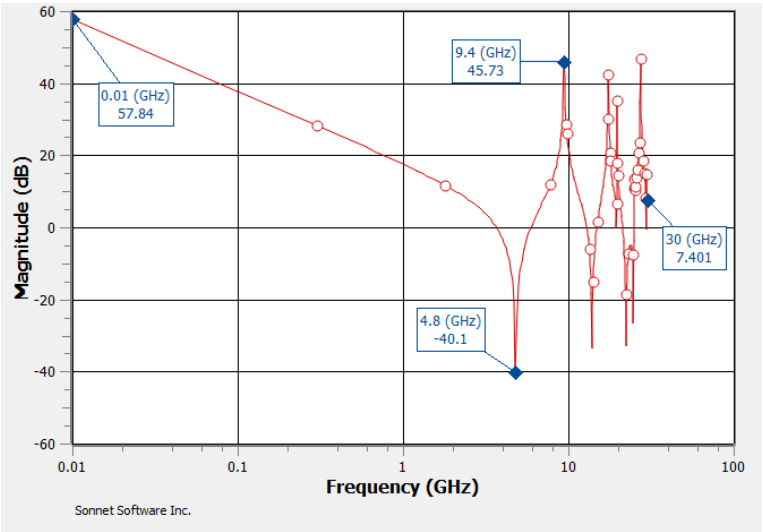


Fig. 6.4 Impedance profile ($|Z_{11}|$ in dB) of the parallel planes for Case 1.

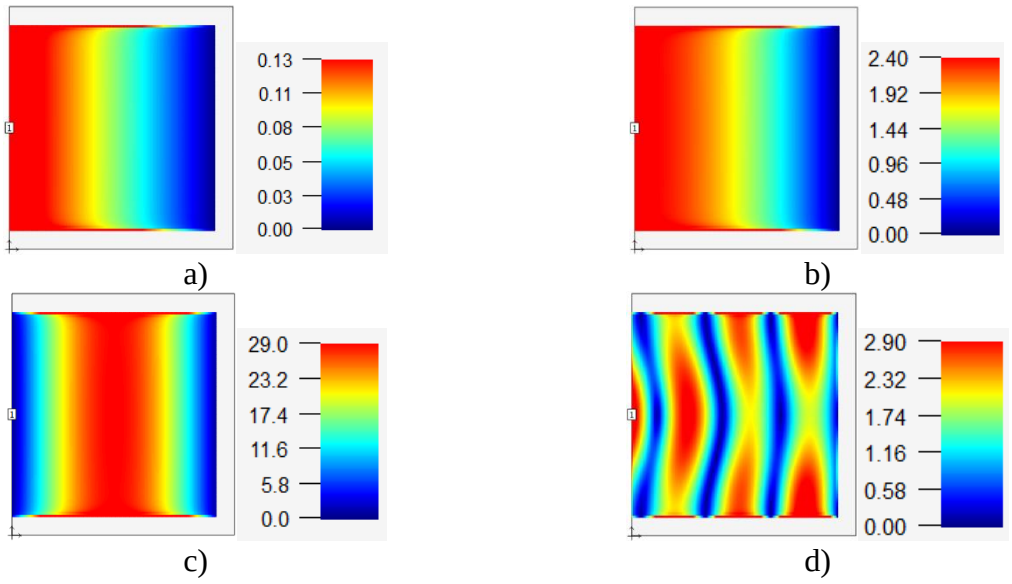


Fig. 6.5 Current distributions for Case 1 in A/m: a) 10 MHz; b) 5.025 GHz; c) 9.45 GHz; d) 30 GHz.

of the port on the left edge will not cause a different response (the corresponding experiments are omitted for the sake of brevity).

6.1.2 Parallel Planes Case 2

In this second simulation case, the same lossless pair of parallel planes as in Case 1 is considered, however, the upper plane is now not touching the shielding box and a short section of 50-ohm microstrip line on the left edge of the plane is inserted, as illustrated in Fig. 6.6. The air layer on top of the structure is still 25 mils thick.

The excitation port is placed on the short feeding microstrip line and a de-embedding

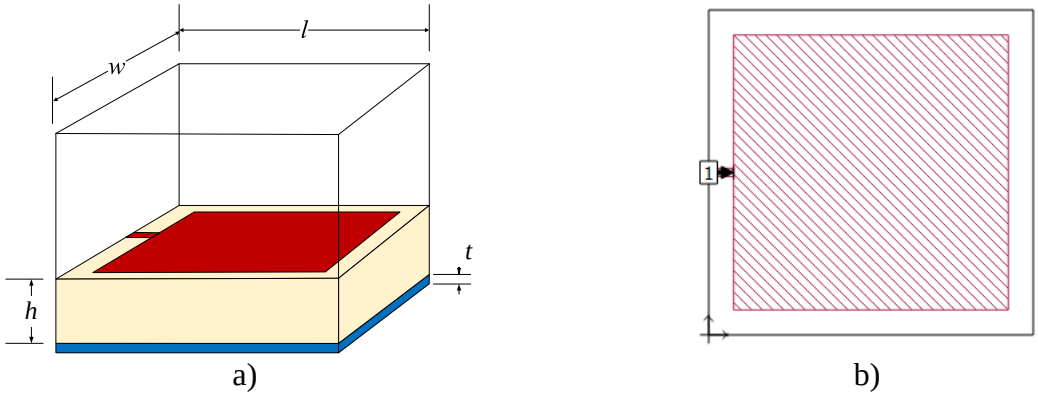


Fig. 6.6 Parallel planes Case 2a, where the upper left plane edge does not touch the shielding box and the excitation port is on a feeding short microstrip line at the middle of the plane: a) 3D view; b) top view.

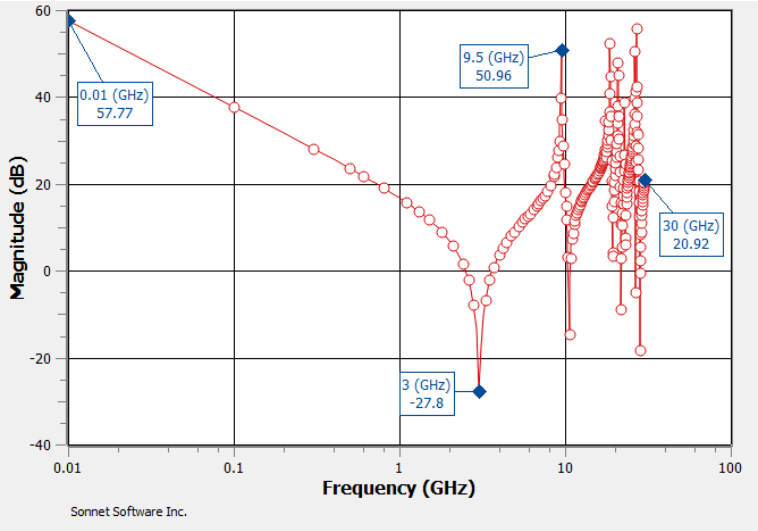


Fig. 6.7 Impedance profile ($|Z_{11}|$ in dB) of the parallel planes for Case 2a.

reference plane is used to measure the S-parameters at the plane edge. This enables to inject the current at a small section of the plane edge instead of on the entire edge, and so the location of the port will now influence the response.

6.1.2.1 Port at the Middle of the Plane Edge (Case 2a)

The feedline is first placed at the middle of the left plane edge, as shown in Fig. 6. The resulting impedance profile is shown in Fig. 6.7. It is seen that the first resonance moved from 4.8

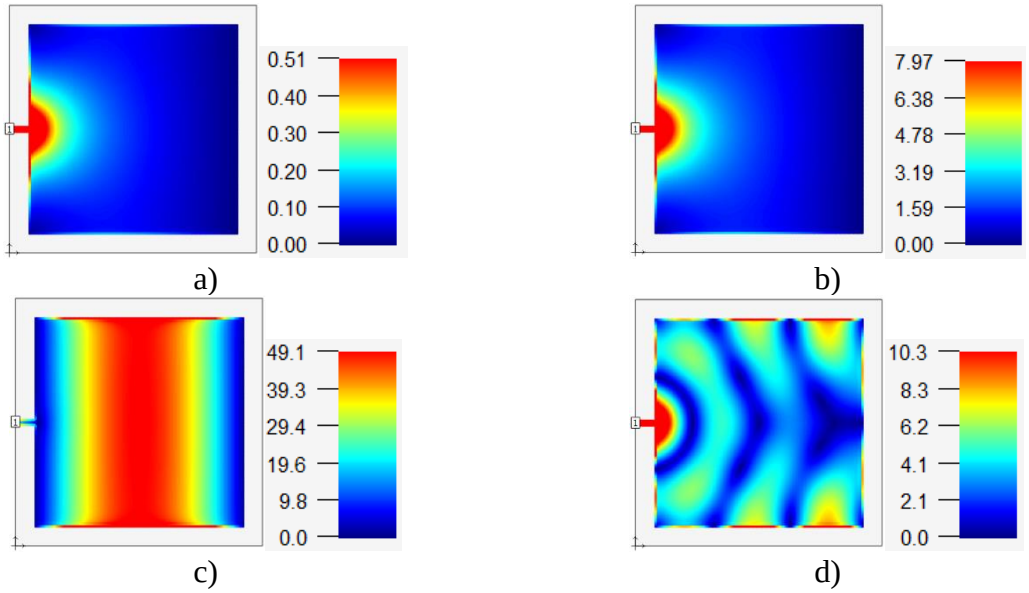


Fig. 6.8 Current distributions for Case 2a in A/m: a) 10 MHz; b) 3 GHz; c) 9.5 GHz; d) 30 GHz.

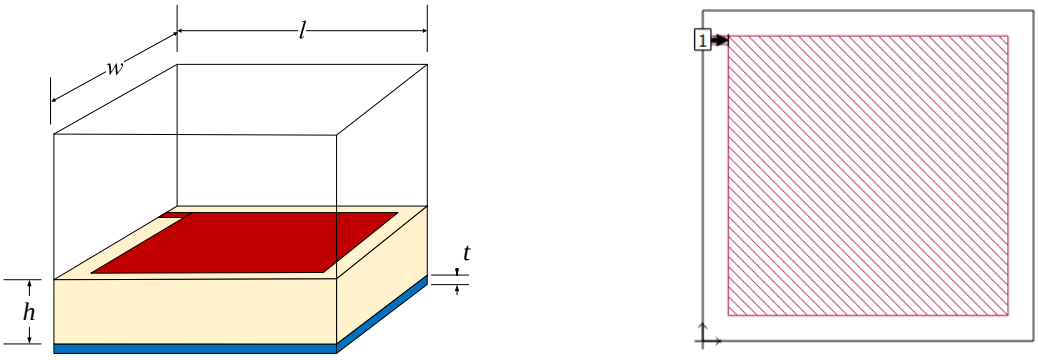


Fig. 6.9 Parallel planes Case 2b, where the upper left plane edge does not touch the shielding box and the excitation port is on a feeding short microstrip line at the top corner of the plane: a) 3D view; b) top view.

GHz to 3 GHz (compare Fig. 6.4 and Fig. 6.7). The current is injected along the entire edge of the feeding microstrip line that is touching the shielding box, however, when it reaches the PDN plane edge it is injected in the middle, and then it spreads throughout the plane in both *x* (longitudinal) and *y* (transverse) directions, as confirmed in Fig. 6.8.

6.1.2.2 Port at the Top Corner of the Plane Edge (Case 2b)

The feedline is now placed on the top corner of the left plane edge, as shown in Fig. 6.9. Everything else is the same as in Case 2a. The impedance profile for this case is shown in Fig. 6.10. It is seen that the first resonance moved from 3 GHz to 2.3 GHz (compare Fig. 6.7 and Fig.

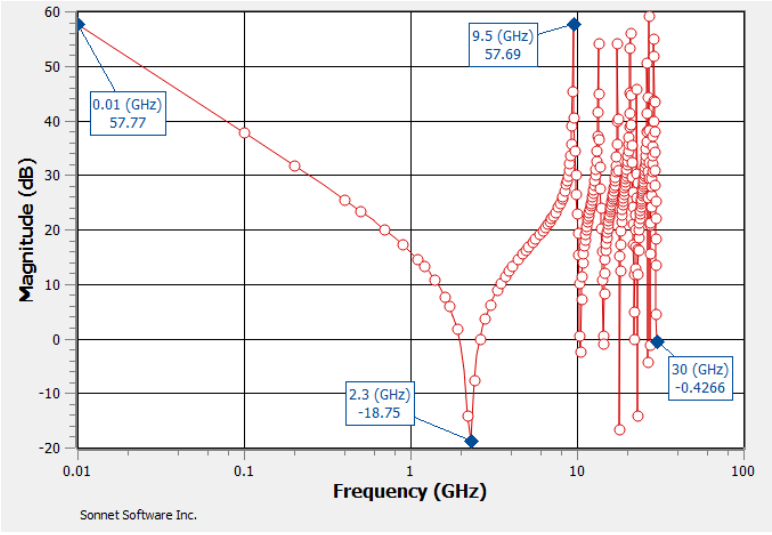


Fig. 6.10 Impedance profile ($|Z_{11}|$ in dB) of the parallel planes for Case 2b.

6.10). In this Case 2b, the current is injected at the corner and spreads throughout the plane in the

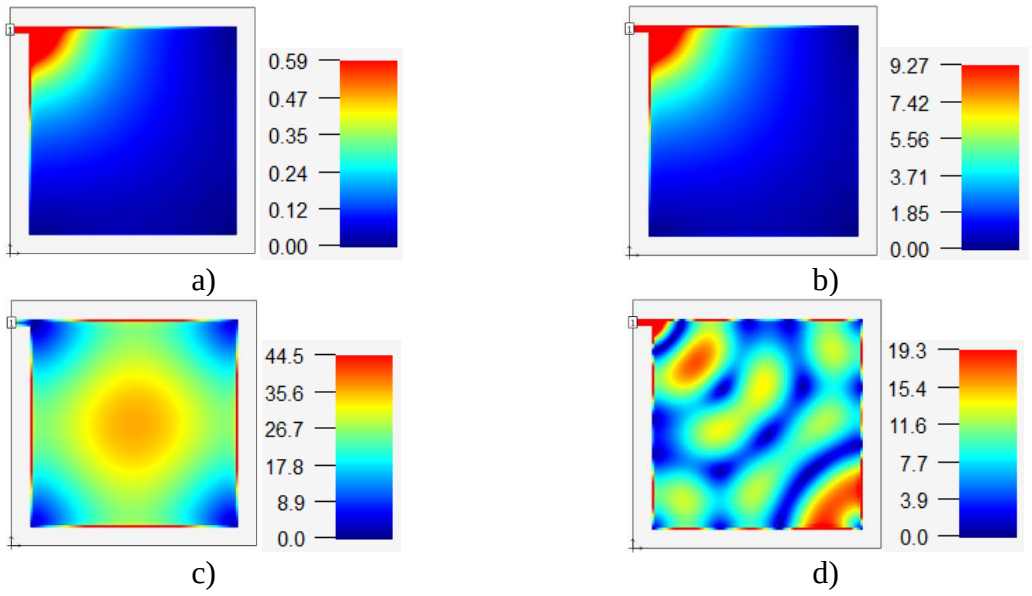


Fig. 6.11 Current distributions for Case 2b in A/m: a) 10 MHz; b) 2.4 GHz; c) 9.5 GHz; d) 30 GHz.

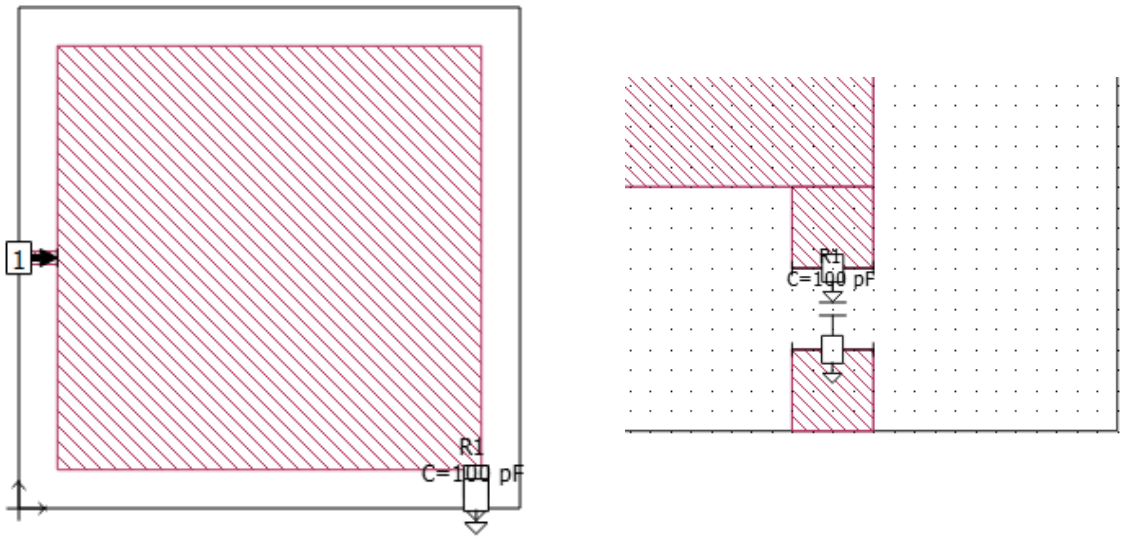
longitudinal and transverse direction in a different manner than when then feedline was at the middle of the plane edge, as confirmed in Fig. 6.11.

6.1.2.3 Port at the Middle of the Plane Edge with a Capacitor on the Far Edge Corner (Case 2c)

Finally, in this Case 2c, again the feedline is applied at the middle of the edge plane, but now an ideal lumped 100-pF capacitor is inserted on the far lower right corner of the plane connected to ground, as shown in Fig. 6.12. The corresponding impedance profile is shown in Fig. 6.13, where the effect of adding the capacitor can be clearly seen, both at low frequencies and at the resonance frequencies. The magnitude of the input impedance at 0.01 GHz decreased from around 58 dB up to 42.4 dB (compare Fig. 6.4, Fig. 6.7, and Fig. 6.10 with Fig. 6.13). From the surface current distribution shown in Fig. 6.14, it is also clearly confirmed that the lumped capacitor pulls the current to ground.

6.2. Parallel Plane Equivalent Lumped Model

Consider a simplified PDN comprised of two metallic planes with length l, width w, dielectric height h, dielectric relative permittivity ε_r, and metal thickness t. The planes can be



a) b)

Fig. 6.12 Parallel planes Case 2c, where the upper left plane edge does not touch the shielding box, the excitation port is on a feeding short microstrip line at the center of the plane, and a capacitor is inserted at bottom edge to ground: a) top view; b) zoom-in of the capacitor.

divided into smaller rectangular sections of parallel planes structures (basic cell) with an area of $\Delta_x \times \Delta_y$, as shown in Fig. 6.15. Using N cells in the longitudinal direction (x-axis) and M cells in the transversal direction (y-axis), it is seen that the planes are discretized in M rows by N columns,

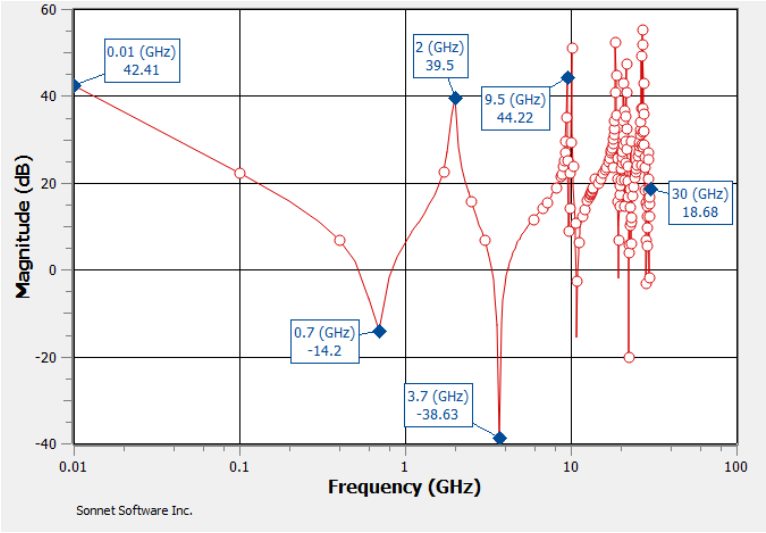


Fig. 6.13 Impedance profile ($|Z_{11}|$ in dB) of parallel planes for Case 2b.

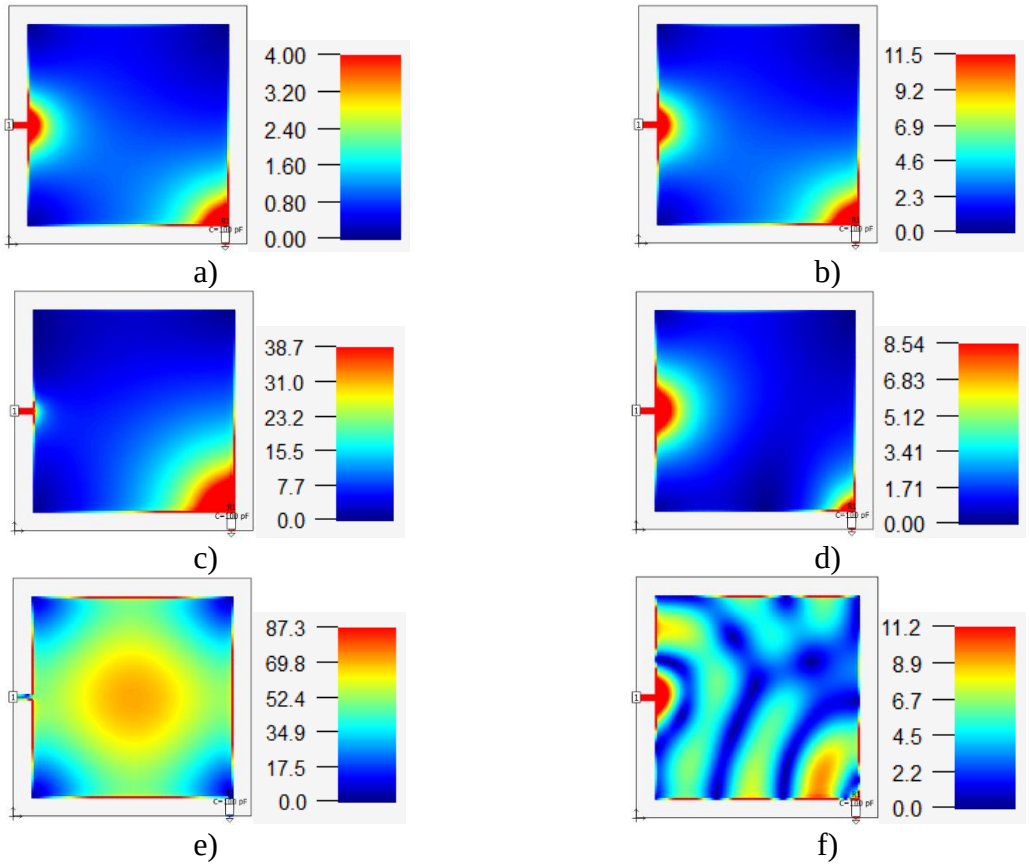


Fig. 6.14 Current distributions for Case 2c in A/m: a) 10 MHz; b) 0.7 GHz; c) 2 GHz; d) 3.7 GHz; e) 9.5 GHz; f) 30 GHz.

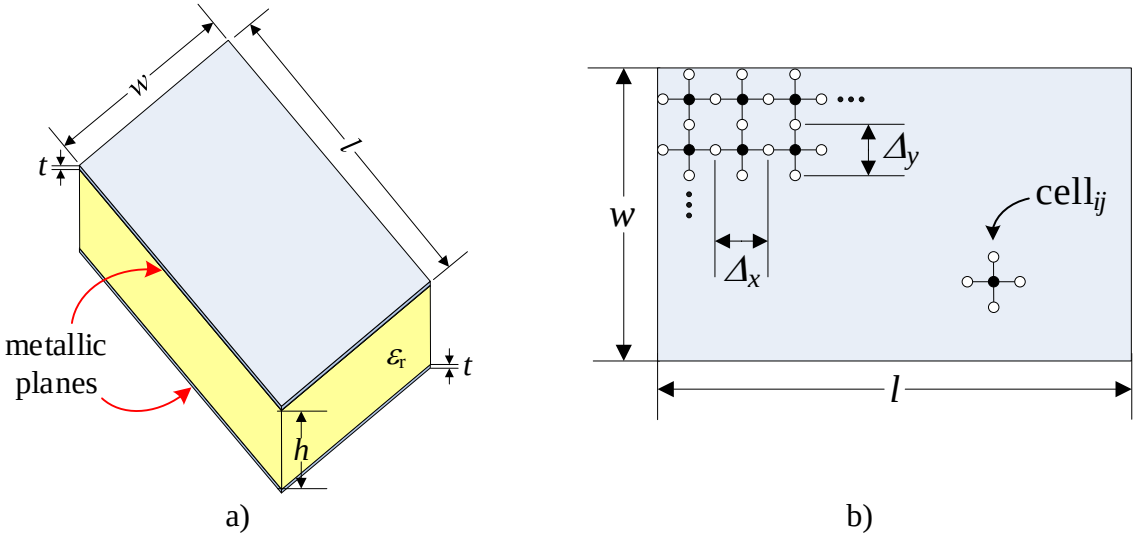


Fig. 6.15 Parallel metallic planes representing a simplified power delivery network: a) plane geometry; b) plane discretization into basic cells.

$$\Delta_x = l/N \tag{6-1}$$

$$\Delta_y = w/M \tag{6-2}$$

Each basic cell is modeled with a lumped equivalent circuit, as shown in Fig. 6.16. The two horizontal branches of the T-model consider the current flowing in the longitudinal direction, while the two vertical branches consider the current flowing in the transversal direction.

This lumped equivalent circuit allows five internal nodes (Fig. 6.16c) for calculating the impedance over the entire surface of the parallel plane structure, and additional external components can be connected in any of those nodes. Its accuracy can be controlled by the discretization resolution, meaning the size of Δ_x and Δ_y. Something to consider is that the edges of the planes are magnetic walls, which requires nodes at the edges to be terminated in open circuit [Kim-01].

For the sake of simplification, in this work lossless parallel planes are considered. The impedances and admittance of the lumped equivalent circuit are then calculated as

$$Y_z = j\omega C_z \tag{6-3}$$

$$Z_x = j\omega L_x \tag{6-4}$$

$$Z_y = j\omega L_y \tag{6-5}$$

where C_z is the cell parallel plate capacitance (F), L_x is the cell parallel plate inductance (H) in the longitudinal direction, L_y is the cell parallel plate inductance (H) in the transversal direction, and ω is the angular frequency.

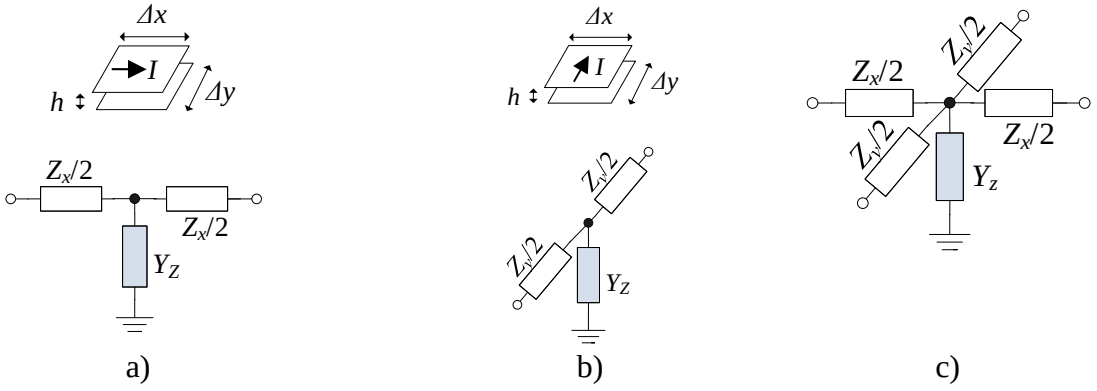


Fig. 6.16 Basic cell equivalent circuit T-model: a) current flows in the x direction; b) current flows in the y direction; c) complete T-model of the basic cell.

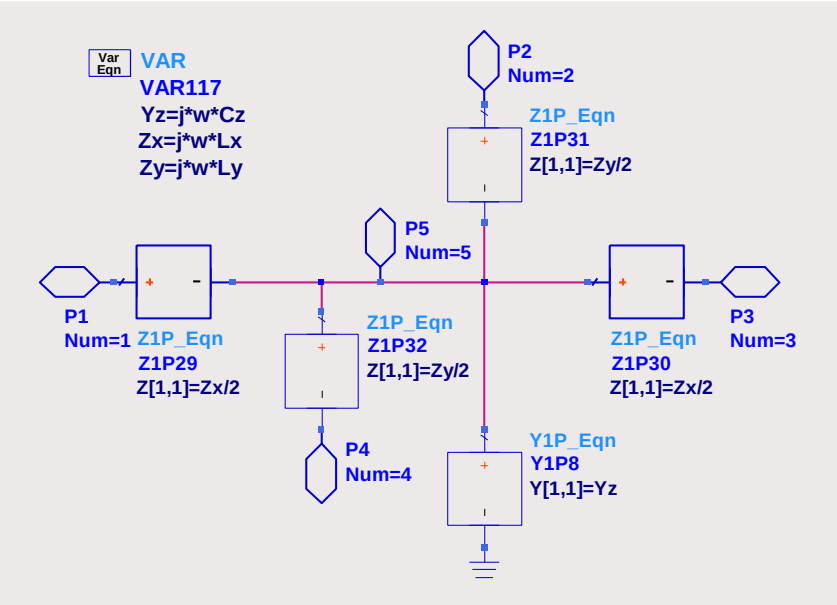


Fig. 6.17 Basic cell equivalent circuit T-model implemented in Keysight ADS.

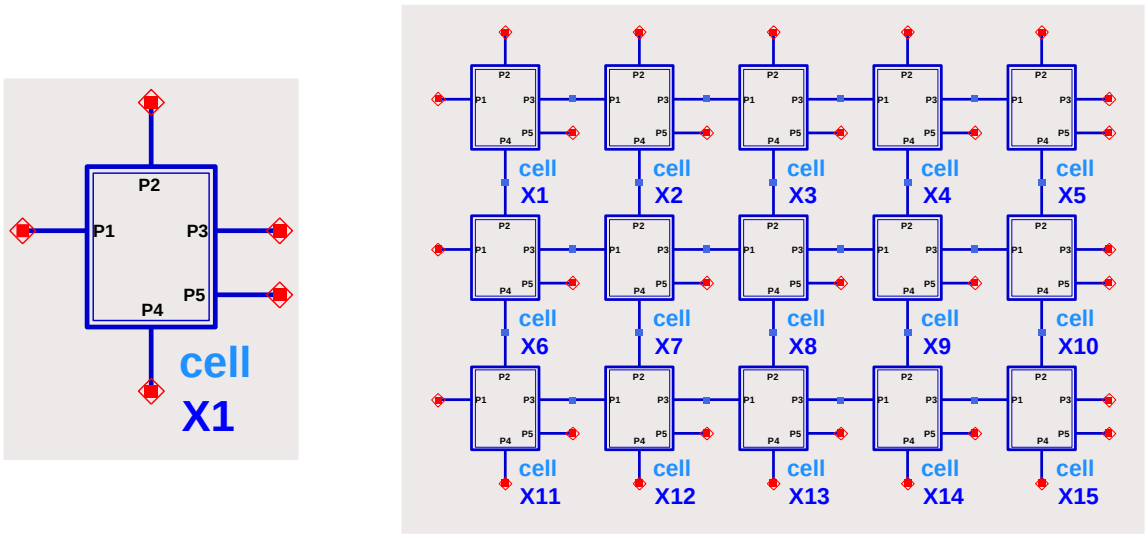
6.2.1 Equivalent Lumped Circuit Model Implementation in ADS

The equivalent lumped circuit from Fig. 6.16c is implemented in Keysight ADS using equation-based components for *Z*- and *Y*-parameters. These components allow to specify the impedance and admittance parameters in complex format. This enables the direct use of equations (6-3),(6-4)-(6-5), as shown in Fig. 6.17. To facilitate joining several cells together, the basic cell schematic is encapsulated in a subcircuit. Fig. 6.18a shows the basic cell subcircuit symbol and Fig. 6.18b shows an example of several basic cells connected in a 3 by 5 array.

6.3. Parallel Plane Equivalent Physical Models

The lumped components C_z, L_x and L_y can be calculated using several different physical models. In this section three of them are considered.

6.3.1 Lumped Component Values Using Ideal Parallel Plate Subsections (IPPS)



a) b)

Fig. 6.18 Equivalent lumped circuit implemented in Keysight ADS: a) basic cell subcircuit; b) example of a parallel plate circuit model by connecting 15 basic cells together in a 3 by 5 array.

The equivalent circuit parameter values for the basic cell can be approximated using the following ideal parallel plate equations [[Kim-01]:

$$C_z = \frac{\varepsilon \Delta_x \Delta_y}{h} \tag{6-6}$$

$$L_x = \frac{\mu \Delta_x h}{\Delta_y} \tag{6-7}$$

$$L_y = \frac{\mu \Delta_y h}{\Delta_x} \tag{6-8}$$

$$\varepsilon = \varepsilon_r \varepsilon_0 \tag{6-9}$$

$$\mu = \mu_0 \tag{6-10}$$

where $\varepsilon_0 = 8.8542$ pF/m is the permittivity of free space, and $\mu_0 = 0.4\pi$ μH/m is the permeability of free space.

Note that this physical model neglects the fringing fields at the edges of the parallel plates.

6.3.2 Lumped Component Values using Ideal Microstrip Line Approximation (IMLA)

Here, each row and column of the discretized parallel planes are assumed to be approximated by an ideal lossless microstrip line whose characteristic impedance is Z_0 and phase

velocity is v_p. Both Z_0 and v_p depend on the microstrip cross-section dimensions and materials,

$$Z_0 = f(\Delta, h, \varepsilon_r) \tag{6-11}$$

$$v_p = \frac{c}{\sqrt{\varepsilon_e}} \tag{6-12}$$

$$\varepsilon_e = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2\sqrt{1+(10h/\Delta)}} \tag{6-13}$$

where Δ is either Δ_x or Δ_y, depending on the current flow direction, c is the speed of light in free space, and ε_e is the effective dielectric permittivity.

If L and C are the transmission line per-unit length inductance (H/m) and capacitance (F/m), then

$$Z_0 = \sqrt{L/C} \tag{6-14}$$

$$v_p = \frac{1}{\sqrt{LC}} \tag{6-15}$$

Solving for L and C,

$$L = \frac{Z_0}{v_p} \tag{6-16}$$

$$C = \frac{1}{Z_0 v_p} \tag{6-17}$$

If the metal thickness is neglected, the characteristic impedance Z_0 of this lossless microstrip line can be estimated using [Gupta-81],

$$\text{if } \frac{\Delta}{h} \le 1,\ Z_0 = \frac{60}{\sqrt{\varepsilon_e}} ln\left(\frac{8h}{\Delta} + \frac{\Delta}{4h}\right) \tag{6-18}$$

$$\text{if } \frac{\Delta}{h} > 1,\ Z_0 = \frac{120\pi}{\sqrt{\varepsilon_e}} \frac{1}{\left(\frac{\Delta}{h}\right)+1.393+0.667\ln\left(\frac{\Delta}{h}+1.444\right)} \tag{6-19}$$

The lumped capacitor C_x and inductor L_x for each section of the horizontal microstrip line are calculated using $\Delta = \Delta_y$.

The lumped capacitor C_y and inductor L_y for each section of the vertical microstrip line are calculated using $\Delta = \Delta_x$.

Finally, the lumped capacitor for the equivalent circuit model in (3) is taken as the average of the previous two capacitances,

$$C_z = \frac{(C_x+C_y)}{2} \tag{6-20}$$

Notice that this physical model also neglects the fringing fields at the edges of the parallel plates.

6.3.3 Lumped Component Values Using Walker's Formulas (WF)

The electric and magnetic fields near the edges of the planes are not uniform due to the boundary conditions on the outside surfaces of the plates [Thierauf-04]. These fringing fields contribute to the total capacitance and inductance of the planes and must be taken into account.

Here each row and column of the discretized parallel planes is assumed to be approximated by a lossless microstrip line. Each of those microstrip lines has a width Δ (Δ_x or Δ_y, depending on the current flow direction), a substrate height h, and dielectric relative permittivity ε_r. Walker's formulas [Walker-90] can be used to calculate the LC parameters, as follows.

The per-unit self-capacitance C_s (F/m) and self-inductance L_s (H/m) are given by

$$C_s = \varepsilon_r \varepsilon_0 K_C \left(\frac{\Delta}{h}\right) \tag{6-21}$$

$$L_s = \frac{\mu_r \mu_0}{K_L} \left(\frac{h}{\Delta}\right) \tag{6-22}$$

where K_C and K_L are the fringing factors given by

$$K_C = \left[\frac{120\pi}{Z_{0(\varepsilon_r=1)}} \left(\frac{h}{\Delta}\right) \sqrt{\frac{\varepsilon_e}{K_L \varepsilon_r}}\right]^2 \tag{6-23}$$

$$K_L = \frac{120\pi}{Z_{0(\varepsilon_r=1)}} \left(\frac{h}{\Delta}\right) \tag{6-24}$$

where ε_e is calculated with (6-13) and the characteristic impedance Z_0 (Ω) can be calculated as [Walker-90]

$$\text{if } \frac{\Delta}{h} \leq 1,\ Z_{0(\varepsilon_r=1)} = 60\, ln\left(\frac{8h}{\Delta} + \frac{\Delta}{4h}\right) \tag{6-25}$$

$$\text{if } \frac{\Delta}{h} > 1,\ Z_{0(\varepsilon_r=1)} = \frac{120\pi}{\left(\frac{\Delta}{h}\right) + 2.42 - 0.44\left(\frac{h}{\Delta}\right) + \left(1 - \frac{h}{\Delta}\right)^6} \tag{6-26}$$

The lumped capacitor and inductor for each section of the horizontal microstrip line are calculated using $\Delta = \Delta_y$ in (6-21),(6-22),(6-23),(6-24),(6-25)-(6-26) and

$$C_x = C_s \Delta_x \tag{6-27}$$

$$L_x = L_s \Delta_x \tag{6-28}$$

The lumped capacitor and inductor for each section of the vertical microstrip line are calculated using $\Delta = \Delta_x$ in (6-21),(6-22),(6-23),(6-24),(6-25)-(6-26) and

$$C_y = C_s \Delta_y \tag{6-29}$$

$$L_y = L_s \Delta_y \tag{6-30}$$

Finally, the lumped capacitor for the basic cell equivalent circuit model is calculated using (6-20).

6.4. Lumped Equivalent Circuit vs Full Wave EM Simulation of Parallel Plates

Two general cases of EM simulations are considered. In the first case, the left edge of the top metal plane is touching Sonnet's metal shielding box. In the second case, a short microstrip feedline is used to separate the plane's edge from Sonnet's shielding box. For the second case, the placement of the feedline is explored at the middle and at the top corner of the plane's left edge, and several parallel plate dimensions are considered. The simulations results and corresponding comparisons for each case considered are described in the following subsections.

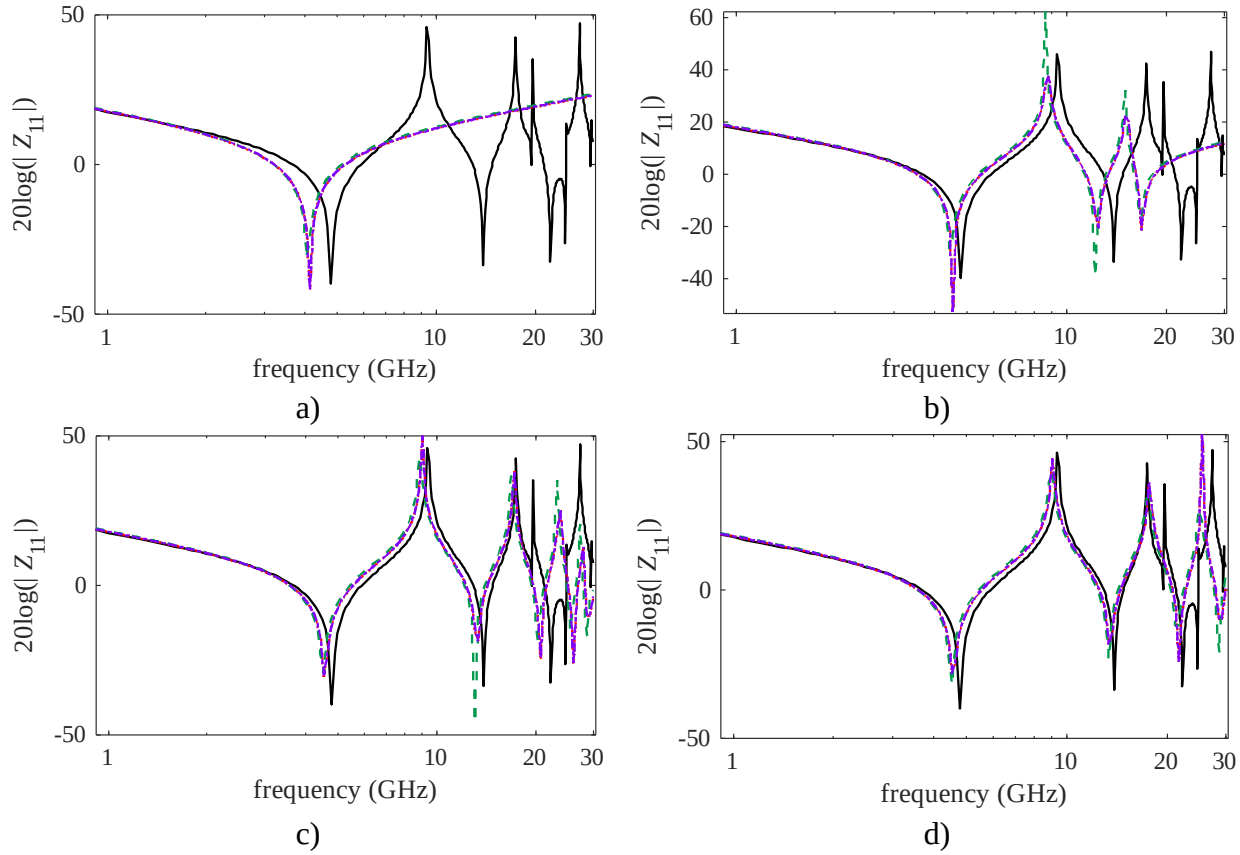


Fig. 6.19 Parallel planes with W = 306.9 mils, L = 306.9 mils, EM model Case 1 in Sonnet (black solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 1, N = 3; c) M = 1, N = 5; d) M = 1, N = 7. As N increases, the accuracy of the equivalent lumped circuit models improves.

6.4.1 Case 1

Case 1 has the top plane's left edge touching Sonnet's shielding box in the EM simulations. The corresponding EM simulations results indicate that the current is injected on the entire edge. This forces the current to only propagate in the longitudinal (*x*-axis) direction. This is verified in Fig. 6.19 to Fig. 6.21. When the lumped circuit has only one cell in the *y*-axis ($M = 1$), there is a better fit to the EM simulation up to high frequencies as more cells are added in the *x*-axis (as N increases), as confirmed in Fig. 6.19. Also, the three physical models (IPPS, IMLA and WF) have very similar results. However, when there is only one cell in the *x*-axis ($N = 1$), the lumped circuit impedance profile differs more from the EM simulation as cells are added in the *y*-axis (as M increases), as confirmed in Fig. 6.20. In this case, IMLA and WF models have very similar performance. In the case where there are equal number of cells on the *y*- and *x*-axis ($M = N$), as

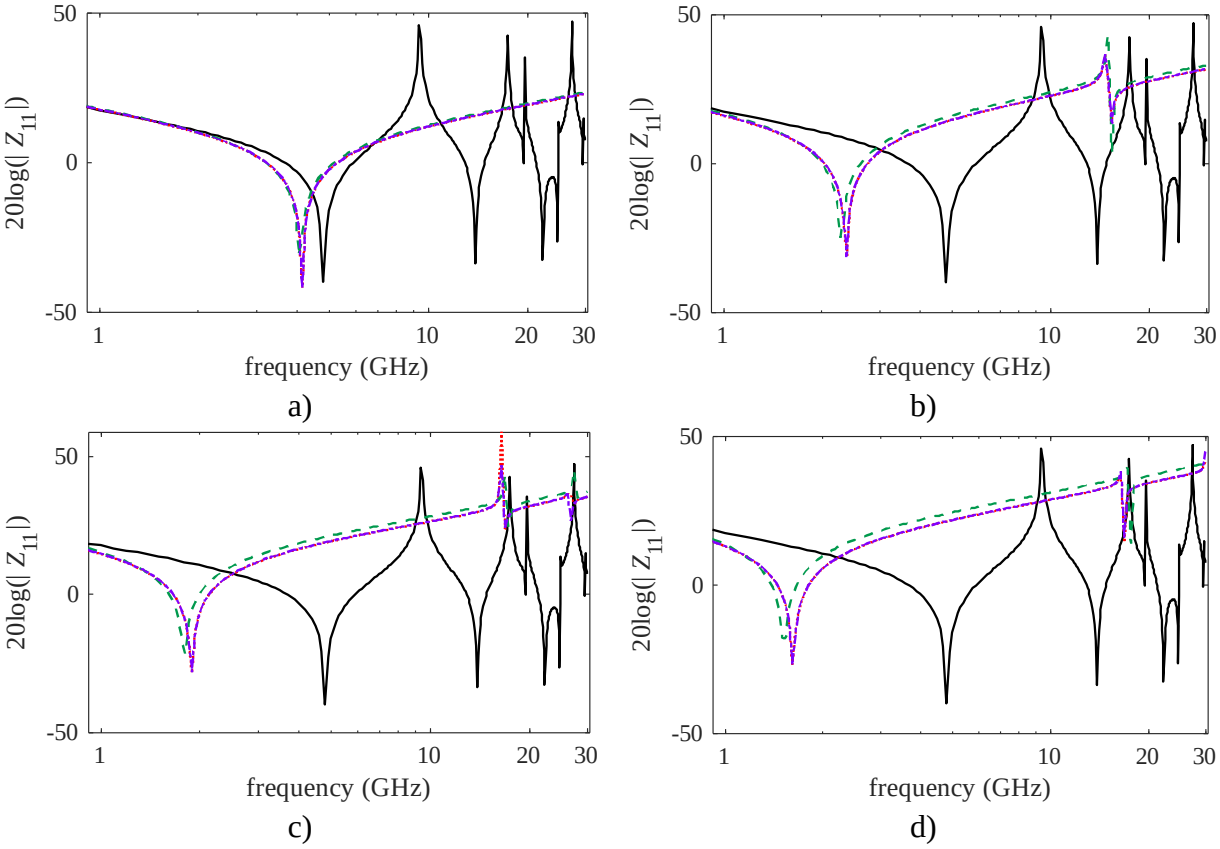


Fig. 6.20 Parallel planes with $W = 306.9$ mils, $L = 306.9$ mils, EM model Case 1 in Sonnet (black solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) $M = 1$, $N = 1$; b) $M = 3$, $N = 1$; c) $M = 5$, $N = 1$; d) $M = 7$, $N = 1$. As M increases, the accuracy of the equivalent lumped circuit models deteriorates.

more cells are added there is not a better fit to the EM simulations (see Fig. 6.21).

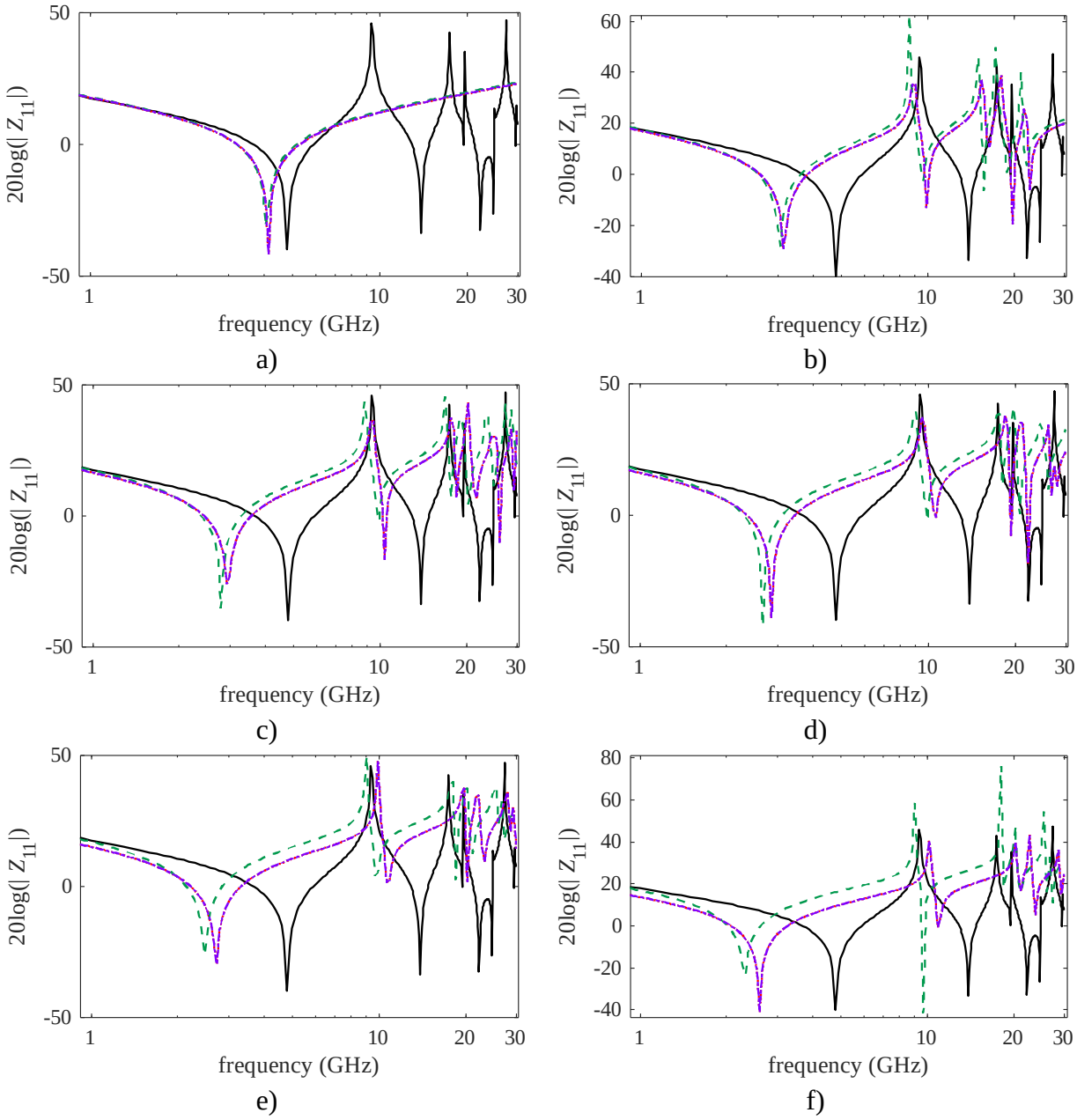


Fig. 6.21 Parallel planes with W = 306.9 mils, L = 306.9 mils, EM model Case 1 in Sonnet (black solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 3, N = 3; c) M = 5, N = 5; d) M = 7, N = 7; e) M = 13, N = 13; f) M = 25, N = 25. As both M and N increase the accuracy of the equivalent lumped circuit models deteriorates.

6.4.2 Case 2a

Cases 2a to 2d use a feedline to separate the top plane's edge from Sonnet's shielding box in the EM simulations. In these cases, the current is injected along the entire edge of the short microstrip feedline, however, when it reaches the PDN top plane, it spreads throughout the plane in both *x* (longitudinal) and *y* (transverse) directions.

In Case 2a the feedline is placed at the middle of the left edge. In Fig. 6.22 it can be see that having one cell in the *y*-axis (*M* = 1) and adding cells in the *x*-axis (increase *N*) does not provide a good fit to the EM simulations, as is also the case when there is one cell in the *x*-axis (*N* = 1) and cells are added in the *y*-axis (increase *M*) (see Fig. 6.23). When there are equal number of unit cells in both the *x*-axis and *y*-axis (*M* = *N*) (see Fig. 6.24) the fit to the EM simulations is better. However, having more than 5 cells in both directions (*x*- and *y*-axis) starts deteriorating the

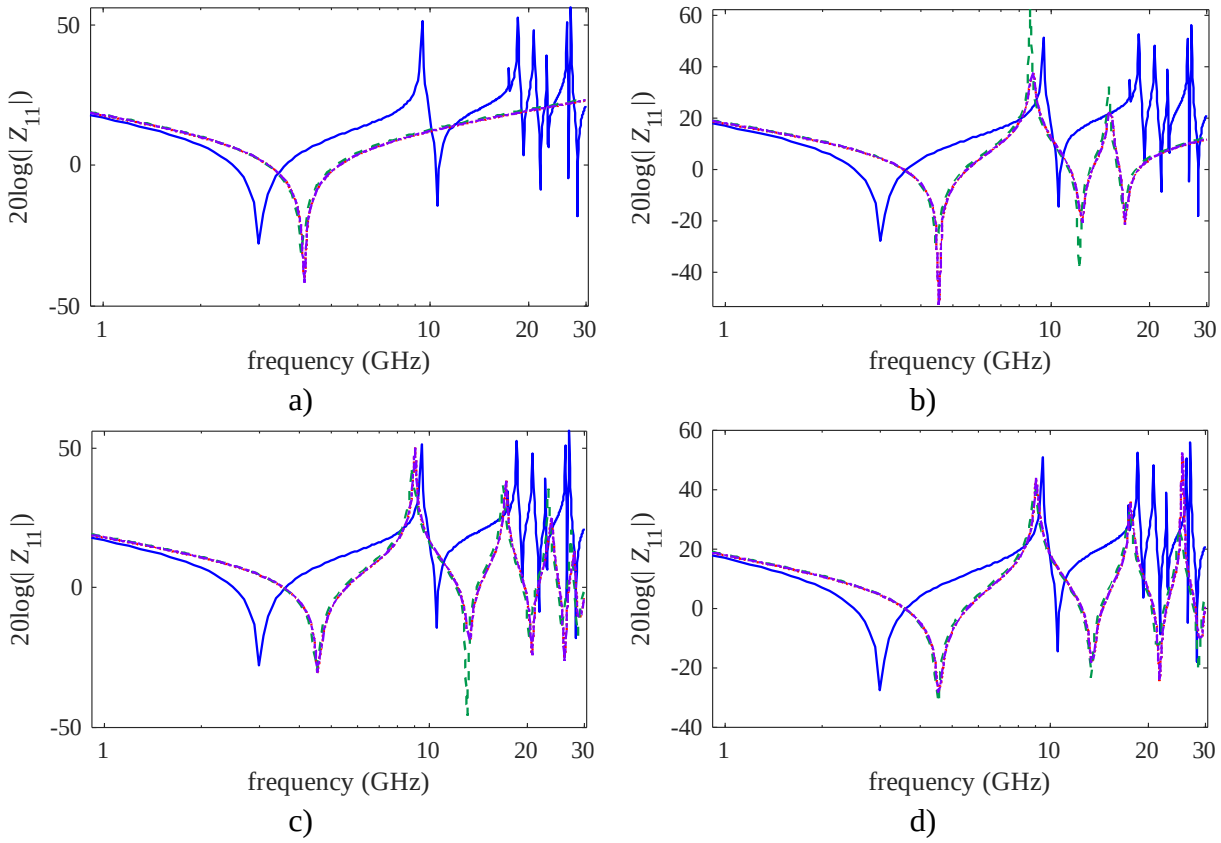


Fig. 6.22 Parallel planes with *W* = 306.9 mils, *L* = 306.9 mils, EM model Case 2a in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) *M* = 1, *N* = 1; b) *M* = 1, *N* = 3; c) *M* = 1, *N* = 5; d) *M* = 1, *N* = 7.

fit between the lumped model and the EM simulations. The IPPS physical model has the same performance as IMLA and WF models for the case where $M = 1$ and N is increased, but for the other cases IPPS has a worse fit. In all these cases (Fig. 6.22 to Fig. 6.24) IMLA and WF have very similar performance.

An additional experiment is considered in this same Case 2a by placing a 100-pF capacitor on the lower right corner of the plane to ground. Fig. 6.25 shows the equivalent lumped circuit simulation results with $M = N$. It can be seen that as more cells are added in both the longitudinal and transverse direction, the IMLA and WF models remain stable and that the IPPS model shifts the first resonance to lower frequencies.

6.4.3 Case 2b

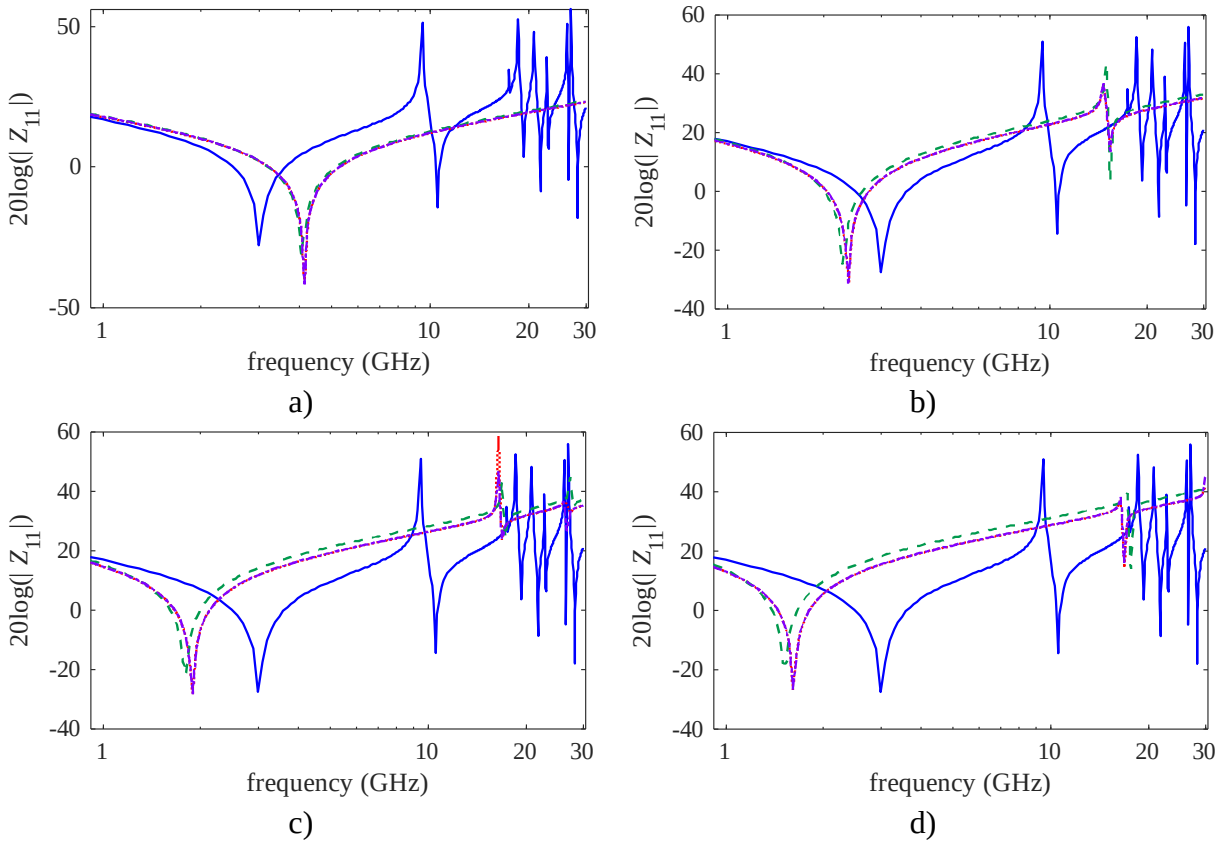


Fig. 6.23 Parallel planes with $W = 306.9$ mils, $L = 306.9$ mils, EM model Case 2a in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) $M = 1$, $N = 1$; b) $M = 3$, $N = 1$; c) $M = 5$, $N = 1$; d) $M = 7$, $N = 1$.

Case 2b has the feedline placed at the top corner of the left edge plane. In this case, the current is injected along the entire edge of the feedline and when it reaches the PDN plane it is injected at the top left corner, and then it spreads throughout the plane in both *x* (longitudinal) and *y* (transverse) directions.

Fig. 6.26 shows the equivalent lumped circuit model simulation results with an equal

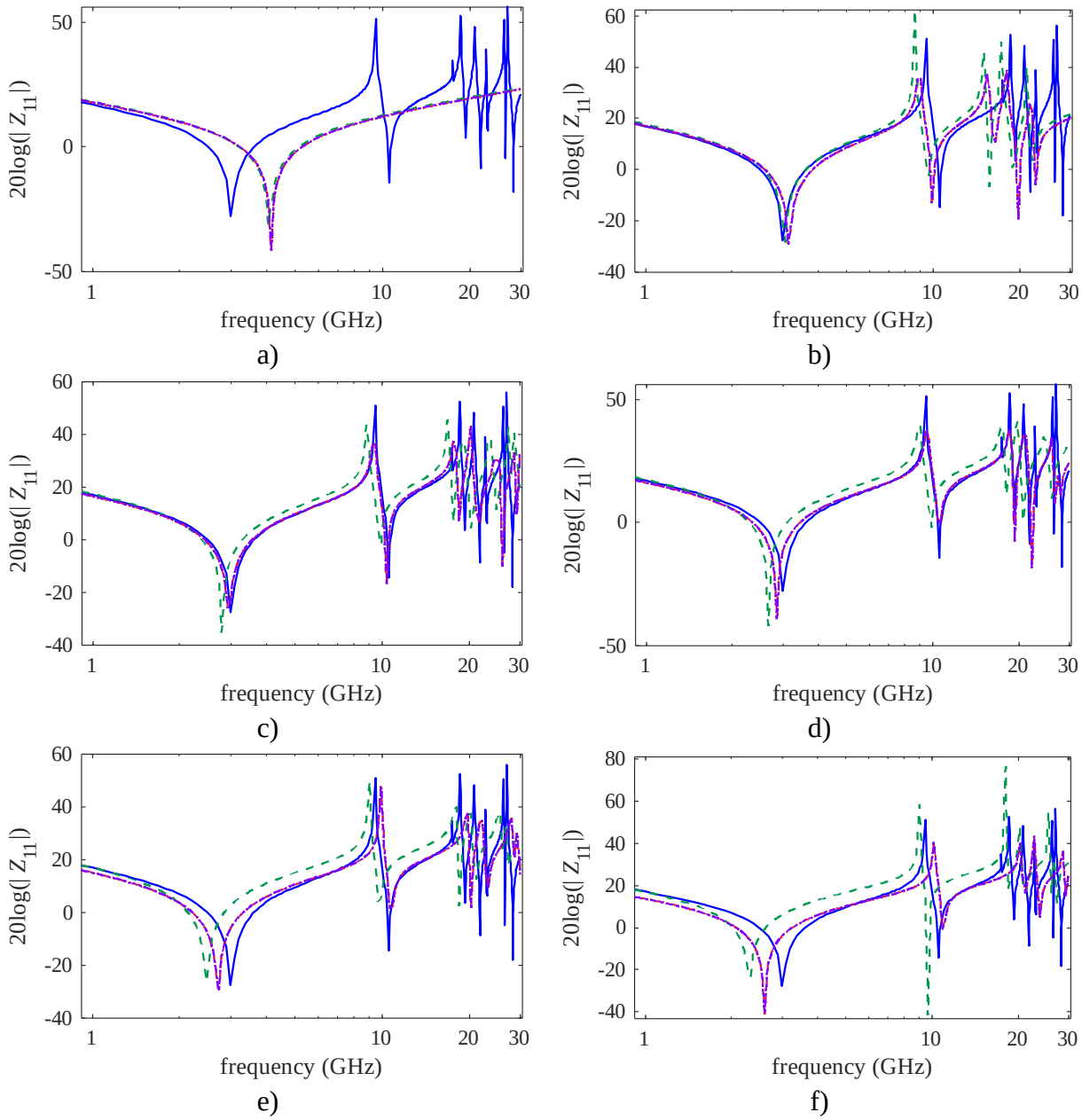


Fig. 6.24 Parallel planes with W = 306.9 mils, L = 306.9 mils, EM model Case 2a in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 3, N = 3; c) M = 5, N = 5; d) M = 7, N = 7; e) M = 13, N = 13; f) M = 25, N = 25.

number of unit cells in the *x*-axis and in the *y*-axis ($M = N$). It can be seen that for $M = 5$ and $N = 5$ IPPS has a good fit to the EM simulations. For $M = 7$ and $N = 7$ both IMLA and WF models have the best fit to the EM simulations. If cells are continued to be added in the *x* and *y* directions, IPPS has a worse fit, but IMLA and WF do not differ that much from the EM simulations.

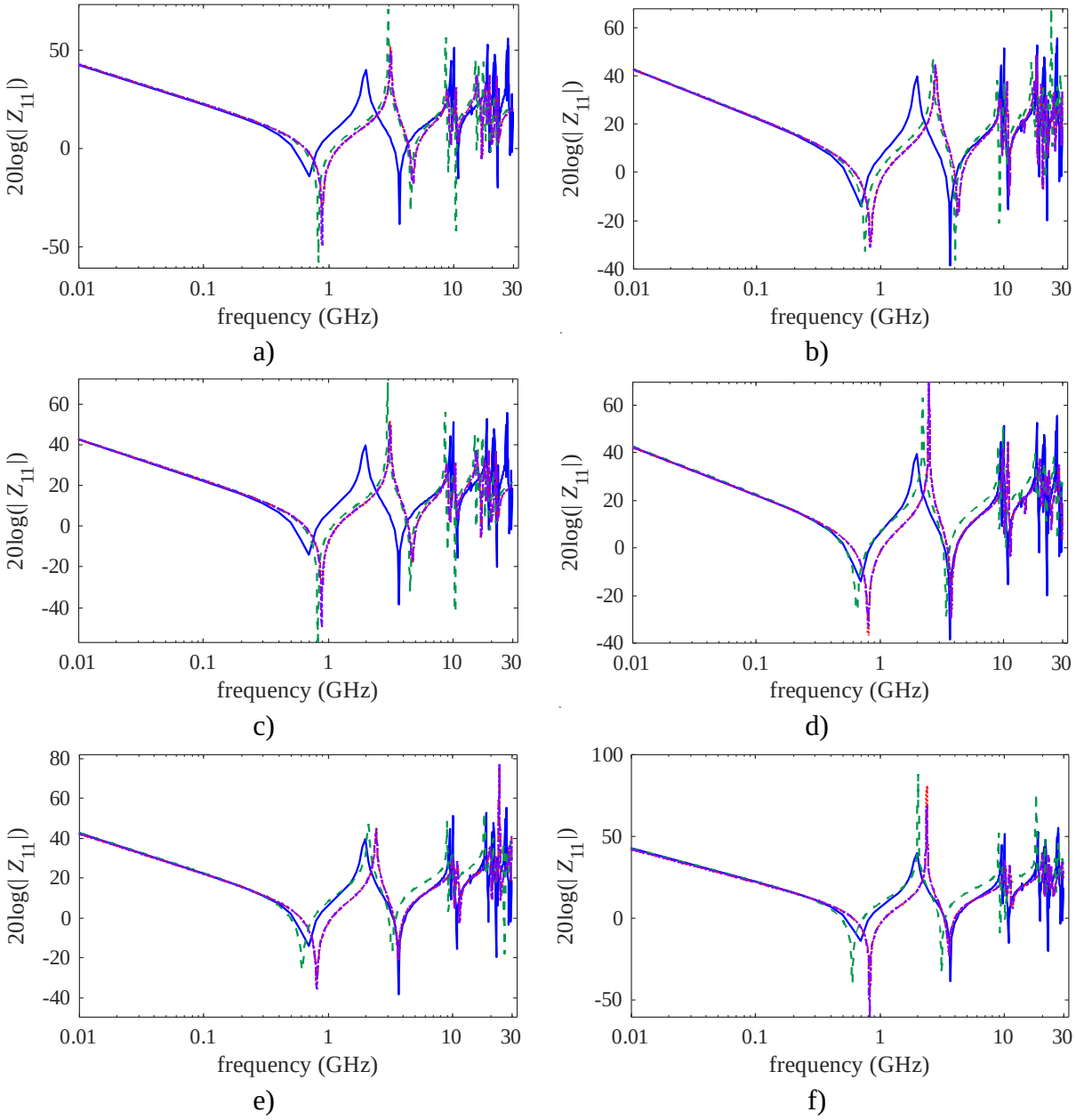


Fig. 6.25 Parallel planes with $W = 306.9$ mils, $L = 306.9$ mils, EM model Case 2a with a 100-pF capacitor in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) $M = 1$, $N = 1$; b) $M = 3$, $N = 3$; c) $M = 5$, $N = 5$; d) $M = 7$, $N = 7$; e) $M = 13$, $N = 13$; f) $M = 25$, $N = 25$.

6.4.4 Case 2c

In Case 2c the feedline is placed at the middle of the left edge plane. In this case parallel plates that are wide and short are considered, with w = 306.9 mils and l = 83.7 mils (keeping h =

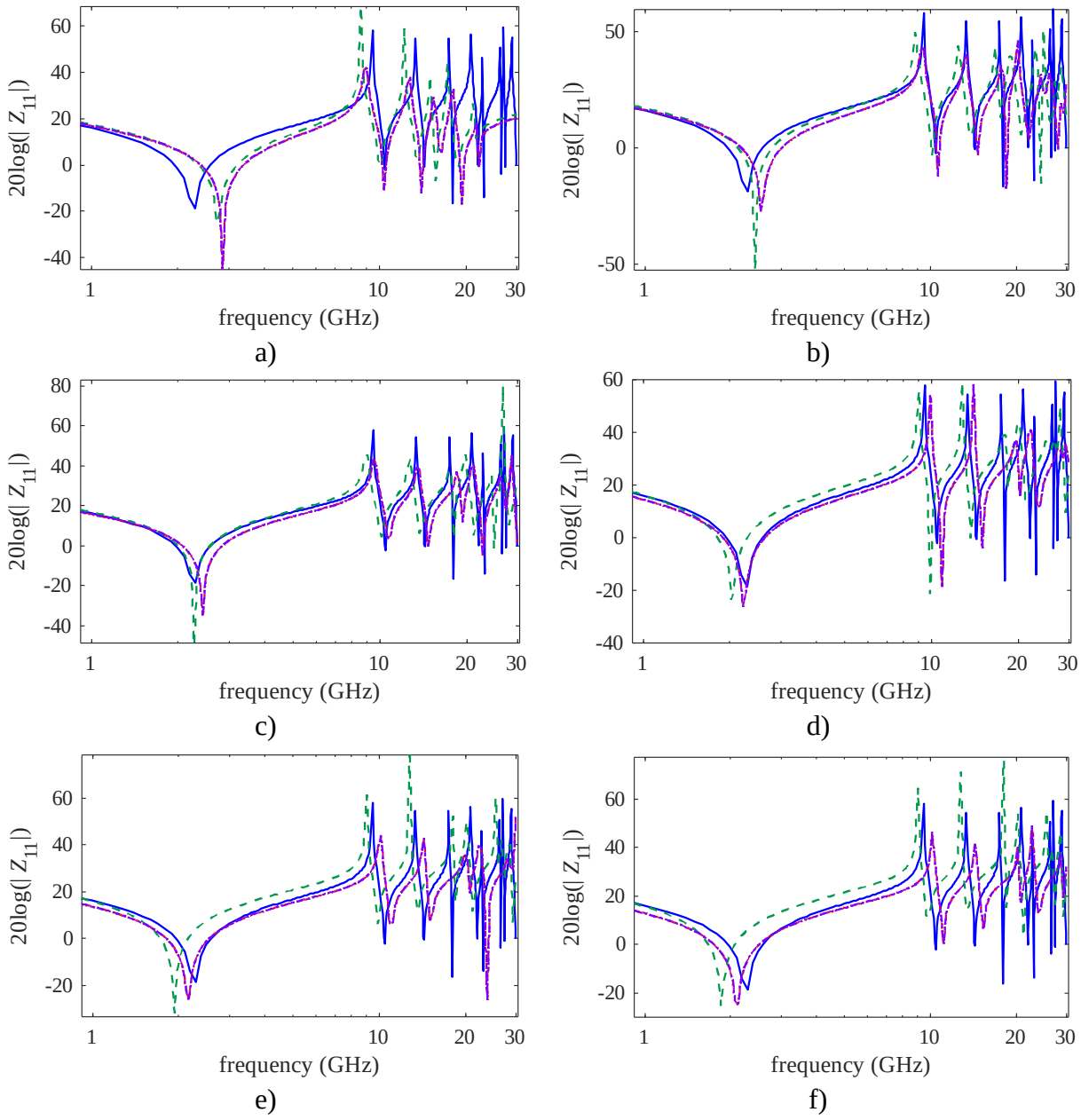


Fig. 6.26 Parallel planes with W = 306.9 mils, L = 306.9 mils, EM model Case 2b in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 3, N = 3; c) M = 5, N = 5; d) M = 7, N = 7; e) M = 13, N = 13; f) M = 25, N = 25.

5 mils and t = 0 mils). From Fig. 6.27, it can be seen that IMLA and WF physical models have a better fit to the EM simulation than IPPS. With M = 13 and N = 5 there is a good fit using IMLA and WF up to around 15 GHz, although the first resonance if shifted to the right

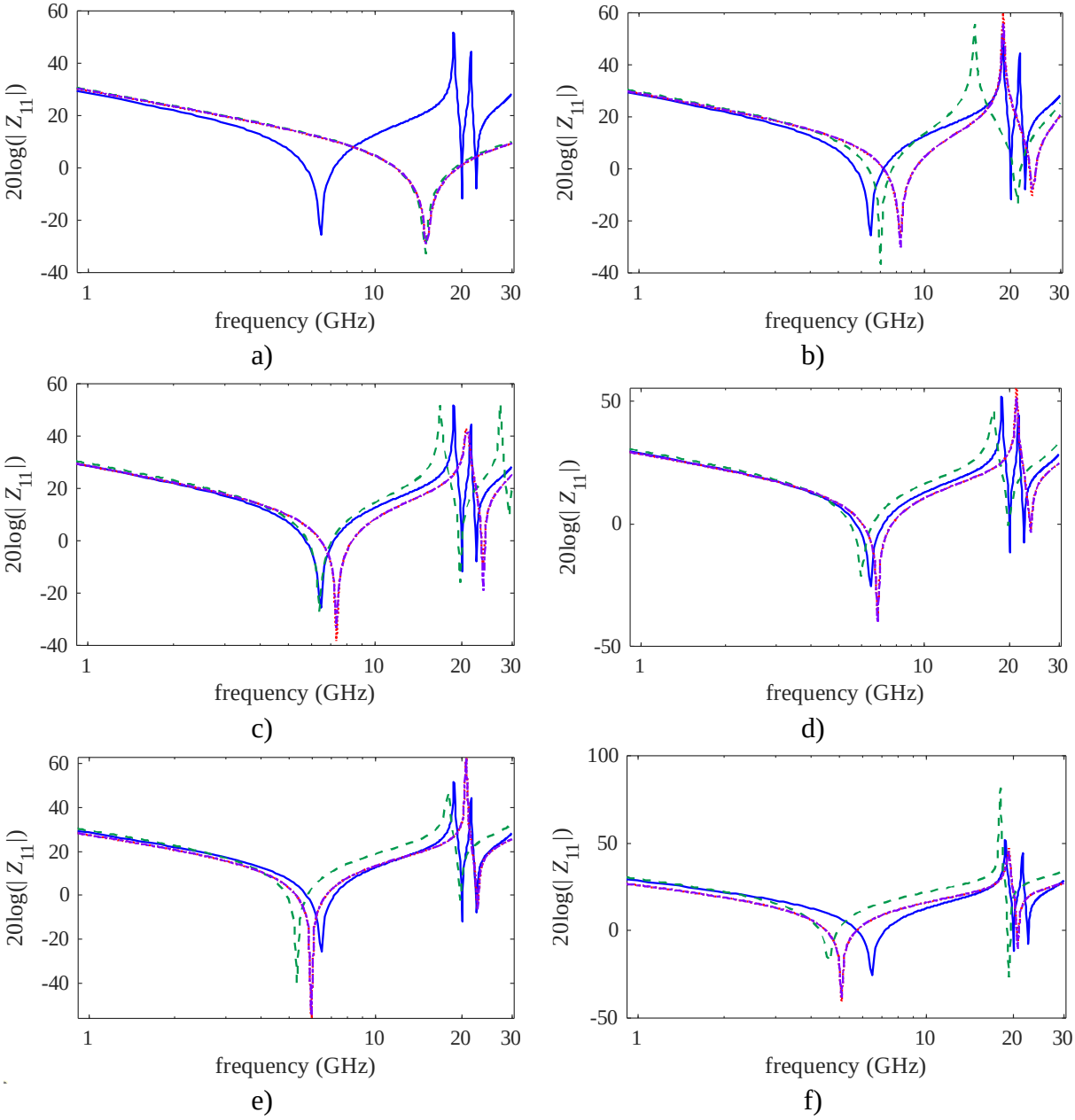


Fig. 6.27 Parallel planes with W = 306.9 mils, L = 83.7 mils, EM model Case 2c in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 3, N = 5; c) M = 5, N = 5; d) M = 7, N = 5; e) M = 13, N = 5; f) M = 25, N = 5.

6.4.5 Case 2d

Case 2d uses the feedline at the middle of the left edge plane. This case considers long and narrow parallel plates with w = 83.7 mils and l = 306.9 mils (keeping h = 5 mils and t = 0 mils).

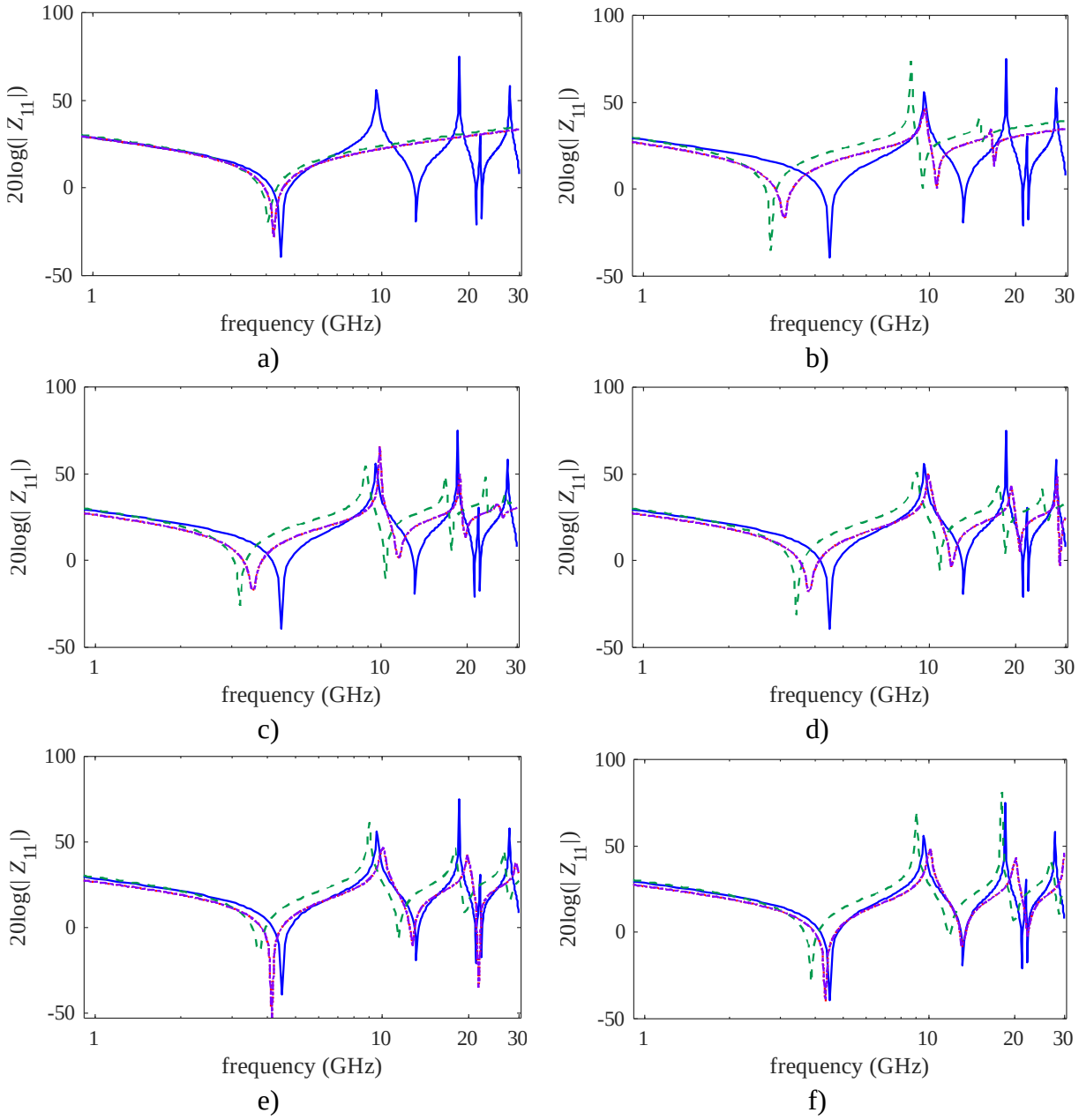


Fig. 6.28 Parallel planes with W = 83.7 mils, L = 306.9 mils, EM model Case 2d in Sonnet (blue solid line), equivalent lumped circuit using IPPS (dashed green line), IMLA (red dotted line), WF (purple dot-dashed line): a) M = 1, N = 1; b) M = 5, N = 3; c) M = 5, N = 5; d) M = 5, N = 7; e) M = 5, N = 13; f) M = 5, N = 25.

Fig. 6.28 shows that IMLA and WF physical models have a better fit to the EM simulation than IPPS, and the fit is very good with $M = 5$ and $N = 25$.

6.4.6 Discussion

In the equivalent lumped circuit model, the current flows both in the longitudinal (x-axis) and in the transverse (y-axis) directions. In the EM simulations this is only achieved by using a microstrip feedline to separate the plane's edge from Sonnet's shielding box and thus allowing a correct comparison with the lumped equivalent circuit. The use of the feedline also allows to correctly model the location of the port.

In general, the three physical models (IPPS, IMLA, and WF) have a relatively good fit to the EM simulations with $M = 1$ and increasing N. Since $M = 1$, this equivalent lumped circuit approximates the behavior of an ideal transmission line circuit as N is increased.

For the case of square parallel plates using $M = N$, the IMLA and WF models have a better fit to the EM simulations than IPPS. However, there was a limit to the number of unit cells that can be added for the fit to be acceptable. Using $N = 1$ and increasing M, all three physical models show a bad fit to the EM simulations.

For the case of wide and short parallel plates, using $M > N$ yields a relatively good fit to the EM simulations with the IMLA and WF physical models, although the first resonance is shifted.

For the case of long and narrow parallel plates, using $M < N$ yields a better fit using the IMLA and WF models than using IPPS physical model.

It should also be noticed that the impedance profile simulations using any of the equivalent lumped circuit models take less than a second, while those using the full-wave EM simulator take around 33 minutes on the same computer platform.

6.5. Conclusions

In this chapter, a simplified PDN was modeled as two parallel lossless metallic planes. Highly accurate full-wave simulations showed the effects of placing the excitation port at different locations on the top plane edge. When the plane's edge touched the shielding box, the current was

injected at the entire length of the edge, forcing the current to spread only in the longitudinal direction. A 50-ohm microstrip line short section was used as a feedline in order to inject the current at a small section of the plane edge. By using this modification, the current was free to spread in both the longitudinal and transverse directions once it arrived at the plane. Furthermore, it was possible to observe how the currents spreads differently when the excitation port is placed at different locations along the plane edge. By adding a lumped capacitor to a corner of the plane it was also possible to observe that the current was pulled to ground by the lumped capacitor. Additionally, the power delivery network parallel plates were discretized into basic cells consisting of an equivalent lumped circuit model. Three different physics-based models were considered to calculate the lumped components of the equivalent circuit model: ideal parallel plate subsections (IPPS), ideal microstrip line approximation (IMLA), and Walker's formulas (WF). The resultant equivalent circuit models for the complete parallel plates were evaluated and compared to the full-wave electromagnetic (EM) simulations. A feedline was used in the EM model to correctly model the current in both the longitudinal and the transverse directions. Different structures of parallel plates were evaluated. In general, the equivalent lumped circuit using IMLA and WF physical models presented a better fit to the EM simulations. More research is needed to determine the best discretization scheme for the equivalent lumped circuit to achieve the best approximation of the EM simulation results.

General Conclusions

A power delivery network (PDN) distributes the electrical power supply to all active devices. When the on-board modules start operating, they pull current from the PDN and can sometimes create voltage noise at the signal pads. This noise can cause setup- and hold-time errors that lead to functional failures of the computer platform. The voltage regulators (VR) have feedback loops that help maintain a steady power supply to the chips. However, even the most reliable VRs are sometimes too slow and allow unacceptable voltage drops when there are transient switching currents at the devices.

A frequent practice in the industry is to place decoupling capacitors throughout the PDN to provide local sources of charge during current surges and thus stabilizing voltage levels then the VR is too slow to do so, and to lower the impedance magnitude of the PDN to lower voltage noise. The decoupling capacitors are placed in parallel arrays and introduce parallel resonant frequencies whose analytical calculation becomes challenging in most practical cases when there are more than two capacitors connected in parallel. Frequency-domain effects of the parallel resonant frequencies are seen in the time-domain as voltage droops that can cause operational errors or failures of the platform.

In Chapter 1, a numerical procedure to find the parallel resonant frequencies of an array of more than two decoupling capacitors connected in parallel was presented. A set of analytical equations to find the parallel resonant frequencies of an array of three capacitors connected in parallel was also presented. These equations can be used to approximate the parallel resonant frequencies of more than three capacitors connected in parallel with an adequately low error.

In Chapter 2, a PDN structure was modeled in a limited frequency band as a simple lumped RLC circuit. Different types of decoupling capacitors were placed throughout the PDN to lower the impedance at certain frequency ranges. A statistical study was performed using an ideal voltage regulator with an infinite bandwidth. From this study it was seen that the active factors in the design were the cavity and package 0 capacitors with a current step of 50 nanoseconds of rise time. In order to see the effects of the third voltage droop, a current step with a slow rise time was needed. In this case with a rise time of 10 microseconds, the cavity capacitors were significant, and the bulk capacitors were significant in the time domain only due to the ideal voltage regulator.

In Chapter 3, a numerical optimization approach to determine the number of decoupling capacitors in a power delivery network was presented, looking at both the impedance profile in the frequency-domain and the resulting voltage droop in the transient time-domain. Better results were found by limiting the amount of design variables as seen in Chapter 2. Additionally, by limiting the maximum total number of capacitors allowed, a more robust formulation was obtained, capable of minimizing the number of capacitors to yield a PDN that satisfies the target impedance and minimum transient voltage supply specifications.

In Chapter 4, an optimization methodology was proposed to gradually find the best compensation parameter values of a Buck voltage regulator that ensure stability, as well as optimize the number of parallel decoupling capacitors considering simultaneously frequency- and time-domain performance specifications. By using optimal VR compensation parameter values and a minimum number of decoupling capacitors, the desired crossover frequency was met with good phase margin, while the transient voltage and the impedance profile were able to meet the design specifications.

In Chapter 5, a statistical analysis and yield prediction was performed for a PDN impedance profile, transient voltage droop, and VR stability. A mathematical formulation to perform this yield estimation was proposed. Keysight ADS statistical capabilities were exploited to save simulation time and memory, while still allowing automated data processing through Matlab. After an estimation of the required number of Monte Carlo trials for a reliable yield estimation, 9220 simulations trials were run. The impedance profile and the stability of the voltage regulator had low yield, 57% and 53% respectively. It was found that the minimum transient voltage droop was not sensitive to fluctuations in the capacitance of the decoupling capacitors, so it maintained the correct performance from the nominal optimization showing a yield of 100%. Additionally, a frequency- and time-domain yield optimization approach was proposed for nominally optimized power delivery networks considering the impact of large tolerances in the decoupling capacitors. After the optimization process, high yields were obtained on both the impedance profile (92.8%) and the VR stability (90.86%). The numerical results obtained from the proposed optimization approach demonstrated its effectiveness to assess and improve the PDN performance and reliability, confirmed by a significantly increased overall yield.

In Chapter 6, highly accurate full-wave electromagnetic (EM) simulations of a simplified power delivery network modeled as two parallel lossless metallic planes were performed. The

simulations showed the effects of placing the excitation port at different locations on the top plane edge. It was found that in order to inject the current at a small section of the plane edge, a 50-ohm microstrip line short section was need as a feedline. By using this modification, the current was free to spread in both the longitudinal and transverse directions once it arrived at the plane. Furthermore, it was possible to observe how the currents spread differently when the excitation port was placed at different locations along the plane edge. By adding a lumped capacitor to a corner of the plane it was also possible to observe that the current was pulled to ground by the lumped capacitor. The obtained impedance profiles from these highly accurate EM simulations were then used as a reference for comparison in circuital simulations. The power delivery network parallel planes were then discretized into basic cells consisting of an equivalent lumped circuit model. The discretization of the planes allows to place ports anywhere on the equivalent circuit, enabling future research about the effects of placing decoupling capacitors at different locations on the planes, avoiding the high computational cost of the corresponding full-wave EM simulations. Three different physics-based models were considered to calculate the lumped components of the equivalent circuit model: ideal parallel plate subsections (IPPS), ideal microstrip line approximation (IMLA), and Walker's formulas (WF). The resultant equivalent circuit models for the complete parallel plates were evaluated and compared to the full-wave EM simulations. Different structures of parallel plates were evaluated. In general, the equivalent lumped circuit using IMLA and WF physical models presented a better fit to the EM simulations, although further research is needed to improve their accuracy.

In summary, this doctoral dissertation proposes a series of optimization methodologies to improve the decoupling capacitor stages of a power delivery network, considering simultaneously the frequency- and time-domain effects, the stability of the voltage regulator, and large tolerances in decoupling capacitor nominal values.

Additionally, this doctoral dissertation provides the first steps into obtaining a lumped equivalent circuit of a discretized PDN that allows the placement of decoupling capacitors anywhere throughout the PDN. This equivalent circuit opens up the possibility of research into the optimization of decoupling capacitor location on a PDN by using space-mapping techniques [Bandler-04], [Koziel-08], [Rayas-Sánchez-16] to avoid costly EM simulations. The principal element limiting the efficiency of a decoupling capacitor is the parasitic inductance associated with the capacitor placement, orientation, distance from the capacitor to the power/ground planes, and

the distance from the capacitor to the device. For this reason, selecting the right set of decoupling capacitors for a PDN design must involve not only considering the desired impedance target and manufacturing variability, but also considering the space available on the PCB and the location of the decoupling capacitors on the PCB. Full-wave electromagnetic (EM) simulations provide a highly accurate way to simulate the effect of decoupling capacitor location; however, the time required to run this type of simulations can be prohibitive when conducting an optimization process. Less costly and more efficient optimization processes can be done using space-mapping techniques, where a coarse equivalent model is optimized and mapped to the finer, more costly model.

Furthermore, the methodologies proposed in this dissertation can be applied to optimize the decoupling capacitors location on the PDN planes considering both the frequency- and time-domain. Going further in the future, a yield optimization using neural space-mapping techniques [Bandler-02], [Rayas-Sánchez-06] or other surrogate-based or machine learning approaches [Leal-Romo-20], [Rayas-Sánchez-20] could be performed on the nominally optimized capacitors location considering capacitor manufacturing variability.

Conclusiones generales

Una red de suministro de potencia (PDN por sus siglas en inglés) consta de todos los dispositivos e interconexiones que distribuyen el suministro de energía eléctrica. Las señales sobre la PDN de diferentes circuitos integrados provocan picos de corriente que generan ruido de voltaje. Esto conduce a fallas funcionales en la plataforma de la computadora, ya que los circuitos centrales internos sufren errores de tiempo de *setup* y tiempo de *hold*. Además, incluso los reguladores de voltaje más confiables a veces son demasiado lentos y permiten caídas de voltaje inaceptables causadas por corrientes de conmutación transitorias en los dispositivos. Estas caídas de voltaje pueden provocar un deterioro del rendimiento y graves fallos funcionales en las plataformas de cómputo de alta velocidad. Si conocemos la tolerancia de voltaje requerida, podemos determinar un objetivo de impedancia que la PDN debería cumplir para mantener el ruido de voltaje en un nivel aceptable para todos los chips. De esta forma, el perfil de impedancia se convierte en una figura de mérito de la aceptabilidad del diseño de la PDN.

Los capacitores de desacoplo frecuentemente se utilizan para reducir la magnitud de la impedancia de la PDN y proporcionar fuentes locales de carga para mitigar los picos de corriente suministrando rápidamente corriente a los dispositivos y estabilizando los niveles de voltaje cuando el regulador de voltaje es demasiado lento para hacerlo. Estos arreglos de capacitores de desacoplo en paralelo introducen frecuencias resonantes paralelas cuyo cálculo analítico se vuelve desafiante en la mayoría de los casos prácticos cuando hay más de dos capacitores conectados en paralelo. Los efectos en el dominio de la frecuencia de estas resonancias paralelas se traducen al dominio del tiempo como caídas de voltaje en diferentes etapas, lo que puede causar errores o fallas operativas.

En el Capítulo 1 de esta tesis se presentó un procedimiento numérico para encontrar las frecuencias resonantes en paralelo de un arreglo de más de dos capacitores de desacoplo conectados en paralelo. También se presentó un conjunto de ecuaciones analíticas para encontrar las frecuencias resonantes paralelas de un arreglo de tres capacitores conectados en paralelo. Estas ecuaciones se pueden utilizar para aproximar las frecuencias resonantes en paralelo de más de tres capacitores conectados en paralelo con un error adecuadamente bajo.

En el Capítulo 2 se modeló una estructura de una PDN en una banda de frecuencia limitada

como un simple circuito RLC concentrado. Se colocaron diferentes tipos de capacitores de desacoplo en toda la PDN para reducir la impedancia en ciertos rangos de frecuencia. Se realizó un estudio estadístico utilizando un regulador de voltaje ideal con un ancho de banda infinito. De este estudio se vio que con un escalón de corriente de 50 nanosegundos de tiempo de subida, los factores activos en el diseño fueron los capacitores de cavidad y paquete 0. Para ver los efectos de la tercera caída de voltaje, se necesitó un escalón de corriente con un tiempo de subida más lento. Con un escalón con tiempo de subida de 10 microsegundos, los capacitores de cavidad fueron significativos y los capacitores de bulk fueron significativos solamente en el dominio del tiempo debido al regulador de voltaje ideal.

En el Capítulo 3 se presentó una técnica de optimización numérica para determinar la cantidad de capacitores de desacoplo en una red de suministro de energía, observando tanto el perfil de impedancia en el dominio de la frecuencia como la caída de voltaje transitorio resultante en el dominio del tiempo. Encontramos mejores resultados al limitar la cantidad de variables de diseño como se vio en el Capítulo 2. Además, al limitar la cantidad total máxima de capacitores permitidos, obtuvimos una formulación más robusta, capaz de minimizar la cantidad de capacitores para producir una PDN que satisface el objetivo de impedancia y especificaciones mínimas de suministro de voltaje transitorio.

En el Capítulo 4 se propuso una metodología de optimización para encontrar gradualmente los mejores valores de parámetros de compensación de un regulador de voltaje tipo Buck que aseguren la estabilidad, así como optimizar el número de capacitores de desacoplo en paralelo considerando simultáneamente las especificaciones de desempeño en el dominio de la frecuencia y el tiempo. Mediante el uso de valores óptimos de los parámetros de la compensación del regulador de voltaje, y una cantidad mínima de capacitores de desacoplo, pudimos cumplir con la frecuencia de cruce deseada con un buen margen de fase, mientras que el voltaje transitorio y el perfil de impedancia pudieron cumplir con las especificaciones de diseño.

En el Capítulo 5 se realizó un análisis estadístico y una predicción del rendimiento para un perfil de impedancia de una PDN, caída de voltaje transitorio y estabilidad del regulador de voltaje. Se propuso una formulación matemática para realizar esta estimación del rendimiento. Se aprovecharon las capacidades estadísticas de Keysight ADS para ahorrar tiempo y memoria de simulación, al mismo tiempo que se permitió el procesamiento automatizado de datos a través de Matlab. Después de una estimación del número requerido de pruebas de Monte Carlo para una

estimación confiable del rendimiento, se realizaron 9220 pruebas de simulación. El perfil de impedancia y la estabilidad del regulador de voltaje tuvieron un rendimiento bajo, de 57% y 53% respectivamente. Se encontró que la caída mínima de voltaje transitorio no fue sensible a las fluctuaciones en la capacitancia de los capacitores de desacoplo, por lo que mantuvo el desempeño correcto de la optimización nominal mostrando un rendimiento del 100%. En este capítulo además se propuso un enfoque de optimización del rendimiento en el dominio de la frecuencia y el tiempo para las PDN nominalmente optimizadas considerando el impacto de las altas tolerancias en los valores de los capacitores de desacoplo. Luego del proceso de optimización, se lograron altos rendimientos tanto en el perfil de impedancia (92.8%) como en la estabilidad del regulador de voltaje (90.86%). Los resultados numéricos obtenidos de nuestro enfoque de optimización propuesto demostraron su eficacia para evaluar y mejorar el rendimiento y la confiabilidad de la PDN, confirmado por un rendimiento general significativamente mayor.

En el Capítulo 6 se realizaron simulaciones electromagnéticas de onda completa de alta precisión de una red de suministro de energía simplificada modelada como dos planos metálicos paralelos sin pérdidas. Las simulaciones mostraron los efectos de colocar el puerto de excitación en diferentes ubicaciones en el borde del plano superior. Se encontró que, para inyectar la corriente en una pequeña sección del borde del plano, se necesitó una sección corta de línea microstrip de 50 ohms como línea de alimentación. Al usar esta modificación, la corriente se propagó libremente en las direcciones longitudinal y transversal una vez llegada al plano. Además, fue posible observar cómo las corrientes se propagaron de manera diferente cuando el puerto de excitación se colocó en diferentes lugares a lo largo del borde del plano. Al agregar un capacitor concentrado a una esquina del plano, también se observó que el capacitor concentrado atrajo la corriente a tierra. Los planos paralelos de la red de suministro de energía se discretizaron en celdas básicas que consisten en un modelo de circuito concentrado equivalente. La discretización de los planos permite ubicar puertos en cualquier lugar del circuito equivalente, lo que permite futuras investigaciones sobre los efectos de colocar capacitores de desacoplamiento en diferentes ubicaciones en los planos, evitando el alto costo computacional de las simulaciones electromagnéticas de onda completa correspondientes. Se consideraron tres modelos diferentes basados en la física para calcular los componentes concentrados del modelo de circuito equivalente: subsecciones de placas paralelas ideales (IPPS), aproximación de línea de microcinta ideal (IMLA) y fórmulas de Walker (WF). Los modelos de circuitos equivalentes resultantes para las placas paralelas completas se evaluaron

y compararon con las simulaciones electromagnéticas. Se evaluaron diferentes estructuras de placas paralelas. En general, el circuito concentrado equivalente utilizando modelos físicos IMLA y WF presentó un mejor ajuste a las simulaciones electromagnéticas, aunque todavía se requiere mayor investigación al respecto para mejorar su exactitud.

En resumen, esta tesis doctoral propone una serie de metodologías de optimización numérica para optimizar las etapas de los capacitores de desacoplo de una red de suministro de potencia, considerando simultáneamente los efectos en el dominio de la frecuencia y del tiempo, la estabilidad del regulador de voltaje, y grandes tolerancias en los valores nominales de los capacitores de desacoplo.

Además, esta tesis doctoral proporciona los primeros pasos para obtener un circuito equivalente concentrado de una PDN discretizada que permita la colocación de capacitores de desacoplo en cualquier lugar de la red de distribución de potencia. Este circuito equivalente abre la posibilidad de investigar la optimización de la ubicación de los capacitores de desacoplo en una PDN mediante el uso de técnicas de mapeo espacial [Bandler-04], [Koziel-08], [Rayas-Sánchez-16] para evitar costosas simulaciones electromagnéticas. El elemento principal que limita la eficiencia de un capacitor de desacoplo es la inductancia parasita asociada con la ubicación del capacitor, la orientación, la distancia del capacitor a los planos de la PDN, y la distancia del capacitor al dispositivo. Por esta razón, seleccionar adecuadamente los capacitores de desacoplo implica no solo considerar la impedancia máxima deseada y la variabilidad de fabricación de los capacitores, sino también considerar el espacio disponible y la ubicación de los capacitores en la PCB. Las simulaciones de onda completa electromagnéticas proporcionan una forma precisa de simular el efecto de la ubicación de los capacitores de desacoplo, sin embargo, el tiempo requerido para ejecutar este tipo de simulaciones puede ser prohibitivo cuando se realiza un proceso de optimización. Se pueden realizar procesos de optimización menos costosos y más eficientes utilizando técnicas de mapeo espacial, donde un modelo equivalente burdo se optimiza y se mapea al modelo más fino y costoso.

Además, las metodologías propuestas en esta tesis se pueden aplicar para optimizar la ubicación de los capacitores de desacoplo en los planos PDN considerando tanto el dominio de la frecuencia como el dominio del tiempo. Yendo más lejos en el futuro, se podría realizar una optimización del rendimiento utilizando técnicas de mapeo de espacio neuronal [Bandler-02], [Rayas-Sánchez-06] u otras similares basadas en modelos sustitutos o aprendizaje automático

[Leal-Romo-20], [Rayas-Sánchez-20], en la ubicación de los capacitores nominalmente optimizada considerando la variabilidad del proceso de fabricación de los capacitores.

Appendix

A. LIST OF INTERNAL RESEARCH REPORTS

1) A. E. Moreno-Mojica, F. J. Leal-Romo, and J. E. Rayas-Sánchez, "Power delivery network impedance profile optimization," Internal Report *PhDEngScITESO-19-03-R (CAECAS-19-04-R)*, ITESO, Tlaquepaque, Mexico, May 2019.

2) E. Moreno-Mojica and J. E. Rayas-Sánchez, "A study on the resonant frequencies of an array of decoupling capacitors for PDN applications," Internal Report *PhDEngScITESO-19-16-R (CAECAS-19-13-R)*, ITESO, Tlaquepaque, Mexico, Oct. 2019.

3) E. Moreno-Mojica and J. E. Rayas-Sánchez, "An analytical study on the resonant frequencies of an array of parallel decoupling capacitors for PDN applications," Internal Report *PhDEngScITESO-19-38-R (CAECAS-19-17-R)*, ITESO, Tlaquepaque, Mexico, Dec. 2019.

4) A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "Power delivery network impedance profile and voltage droop optimization," Internal Report *PhDEngScITESO-20-07-R (CAECAS-20-03-R)*, ITESO, Tlaquepaque, Mexico, May 2020.

5) A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "A study on capacitor effects of a PDN in the frequency- and time-domain," Internal Report *PhDEngScITESO-20-10-R (CAECAS-20-06-R)*, ITESO, Tlaquepaque, Mexico, Jul. 2020.

6) A. E. Moreno-Mojica, J. E. Rayas-Sánchez, F. J. Leal-Romo, and Z. Brito-Brito, "Optimizing a buck voltage regulator for a PDN application," Internal Report *PhDEngScITESO-20-19-R (CAECAS-20-08-R)*, ITESO, Tlaquepaque, Mexico, Aug. 2020.

7) A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "Optimizing a buck voltage regulator and the number of decoupling capacitors for a PDN application," Internal Report *PhDEngScITESO-21-01-R (CAECAS-21-01-R)*, ITESO, Tlaquepaque, Mexico, Feb. 2021.

8) A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "An enhanced formulation for optimizing a buck voltage regulator and the number of decoupling capacitors for a PDN application," Internal Report *PhDEngScITESO-21-02-R (CAECAS-21-02-R)*, ITESO, Tlaquepaque, Mexico, Apr. 2021.

9) A. E. Moreno-Mojica and J. E. Rayas-Sánchez, "Time- and memory-efficient yield analysis in Keysight ADS through Matlab," Internal Report *PhDEngScITESO-21-04-R (CAECAS-21-05-R)*, ITESO, Tlaquepaque, Mexico, Aug. 2021.

10) A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and Felipe J. Leal-Romo, "Evaluating the impact of decoupling capacitors variability on the performance of a power delivery network," Internal Report *PhDEngScITESO-21-07-R (CAECAS-21-07-R)*, ITESO, Tlaquepaque, Mexico, Sep. 2021.

11) A. E. Moreno-Mojica and J. E. Rayas-Sánchez, "Optimizing the performance yield of a PDN subject to large variability in decoupling capacitor tolerances," Internal Report *PhDEngScITESO-21-16-R (CAECAS-21-08-R)*, ITESO, Tlaquepaque, Mexico, Nov. 2021.

12) A. E. Moreno-Mojica and J. E. Rayas-Sánchez, "Full-wave EM simulations of a parallel plane power delivery network," Internal Report *PhDEngScITESO-22-05-R (CAECAS-22-03-R)*, ITESO, Tlaquepaque, Mexico, Jul. 2022.

13) A. E. Moreno-Mojica and J. E. Rayas-Sánchez, "Developing a physics-based lumped circuit model for lossless parallel plates," Internal Report *PhDEngScITESO-22-06-R (CAECAS-22-04-R)*, ITESO, Tlaquepaque, Mexico, Jul. 2022.

B. LIST OF PUBLICATIONS

1) A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "Power delivery network impedance profile and voltage droop optimization," in *European Microwave Conf. (EuMC-2020)*, Utrecht, The Netherlands, Jan. 2021, pp. 260-263. (ISBN: 978-1-7281-7039-8; e-ISBN: 978-2-87487-059-0; INSPEC: 20405031; DOI: 10.23919/EuMC48046.2021.9338232)

2) A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "Optimizing a buck voltage regulator and the number of decoupling capacitors for a PDN application," in *IEEE MTT-S Latin America Microwave Conf. (LAMC-2021)*, Cali, Colombia, May 2021, pp. 1-4. (ISBN: 978-1-7281-9359-5; e-ISBN: 978-1-7281-9358-8; INSPEC: 21435108; DOI: 10.1109/LAMC50424.2021.9601574)

3) A. E. Moreno-Mojica and J. E. Rayas-Sánchez, "Frequency- and time-domain yield optimization of a power delivery network subject to large decoupling capacitor tolerances," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 12, pp. 5610-5620, Dec. 2022. (p-ISSN: 0278-0070; e-ISSN: 1937-4151; published online: 30 March 2022; DOI: 10.1109/TCAD.2022.3163673)

Bibliography

[Agilent-00] Agilent Technologies, *Advanced Design System 1.5 Tuning, Optimization and Statistical Design*, Palo Alto, CA, 2000.

[Analog Devices-09] Analog Devices. (2009). *MT-101 Tutorial Decoupling Techniques* [Online]. Available: https://www.analog.com/media/en/training-seminars/tutorials/MT-101.pdf.

[Bandler-02] J. W. Bandler, J. E. Rayas-Sánchez, and Q. J. Zhang, "Yield-driven electromagnetic optimization via space mapping-based neuromodels," *Int. J. RF and Microwave CAE*, vol. 12, no. 1, pp. 79-89, Jan. 2002.

[Bandler-04] J. W. Bandler, Q. S. Cheng, S. A. Dakroury, A. S. Mohamed, M. H. Bakr, K. Madsen, and J. Sondergaard, "Space mapping: the state of the art," *IEEE Trans. Microw. Theory Techn*., vol. 52, no. 1, pp. 337-361, Jan. 2004.

[Basso-01] C. P. Basso, *Switch-Mode Power Supply SPICE Cookbook*. New York, NY, USA: McGraw-Hill, 2001.

[Box-05] G. Box, J. Hunter, and W. Hunter, *Statistics for Experimenters*. Hoboken, N.J: Wiley-Interscience, 2005.

[Chen-96] Y. Chen, Z. Chen, and J. Fang, "Optimum placement of decoupling capacitors on packages and printed circuit boards under the guidance of electromagnetic field simulation," in *Electronic Components and Technology Conference (ECTC-1996)*, Orlando, FL, May 1996, pp. 756-760.

[Chen-07] J. Chen and L. He, "Efficient in-package decoupling capacitor optimization for I/O power integrity," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 4, pp. 734-738, Apr. 2007.

[Chew-12] L. W. Chew, "The effect of higher order model decoupling capacitors in the design of a power delivery network," in *Asia Symposium on Quality Electronic Design (ASQED)*, Penang, Malaysia, 2012, pp. 117-122.

[DiBene-14] J. T. DiBene, *Fundamentals of Power Integrity for Computer Platforms and Systems*. Hoboken, NJ, USA: Wiley, 2014.

[Erdin-18] I. Erdin and R. Achar, "Analytical modeling of power pin impedance in parallel power & ground planes," in *IEEE MTT-S Int. Conf. Numer. Electromagnetic Multiphysics Modeling Opt. (NEMO)*, Reykjavik, Iceland, Aug. 2018, pp. 1-3.

[Erdin-21] I. Erdin, "A barrier function method for optimal placement of decoupling capacitors on resonant plane pairs," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Atlanta, GA, Jun. 2021, pp. 244-246.

[Erdin-22] I. Erdin and R. Achar, "An effective global approach for assessment of decoupling capacitors on mixed planar and transmission line PDNs," *IEEE J. Multiscale Multiphysics Computat. Techn.*, vol. 7, pp. 176-185, Jul. 2022.

[Erickson-96] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. Norwell, MA, USA: Kluwer Academic, 1996.

[Goral-16] B. Goral, C. Gautier and A. Amedeo, "Power Delivery Network simulation methodology including Integrated Circuit behavior," in *IEEE Workshop on Signal and Power Integrity (SPI)*, Turin, Italy, May 2016, pp. 1-4.

[Gupta-81] K. C. Gupta, R. Garg, and R. Chadha, *Computer-Aided Design of Microwave Circuits*. Norwood, MA: Artech House, 1981.

[Hattori-02] I. Hattori, A. Kamo, T. Watanabe, and H. Asai, "A searching method for optimal locations of decoupling capacitors based on electromagnetic field analysis by FDTD method," in *IEEE Conf. Electrical Performance of Electronic Packaging (EPEP-2002)*, Monterey, CA, Oct. 2002, pp. 159-162.

[Hur-06] K. Hur and S. Santoso, "An improved method to estimate empirical system parallel resonant frequencies using capacitor switching transient data", *IEEE Transactions on Power Delivery*, vol. 21, no. 3, pp. 1751-1753, June 2006.

[Ichimura-14] W. Ichimura, S. Kiyoshige, and T. Sudo, "EMI reduction by suppressing Q factor of total PDN with variable on-die capacitance and resistance," in *IEEE Conf. Electrical Performance of Electronic Packaging and Systems*, Portland, OR, USA, Oct. 2014, pp. 211-214.

[Kamo-00] A. Kamo, T. Watanabe, and H. Asai, "An optimized method for placement of decoupling capacitors on printed circuit board," in *IEEE Conf. Electrical Performance of Electronic Packaging* (*EPEP-2000)*, Scottsdale, AZ, Oct. 2000, pp. 73-76.

[Kim-04] J. Kim, D. Jiao, J. He, K. Radhakrishnan, and C. Dai, "Characterization of discrete decoupling capacitors for high-speed digital systems," in *Electronic Components and Tech. Conf.*, Las Vegas, NV, USA, June 2004, pp. 259-265.

[Kim-01] J. Kim and M. Swaminathan, "Modeling of irregular shaped power distribution networks using transmission matrix method," *IEEE Trans. on Advanced Packaging*, vol. 24, no. 3, pp. 334-346, Aug. 2001.

[Klokotov-14] D. Klokotov, J. Shi, and Y. Wand, "Distributed modeling and characterization of on-chip/system level PDN and jitter impact," in *DesignCon 2014*, Santa Clara, CA, Jan. 2014, pp. 93-114.

[Koziel-08] S. Koziel, Q. S. Cheng, and J. W. Bandler, "Space mapping," *IEEE Microw. Mag*., vol. 9, no. 6, pp. 105-122, Dec. 2008.

[Leal-Romo-20] F. J. Leal-Romo, J. E. Rayas-Sánchez, and J. L. Chávez-Hurtado, "Surrogate-based analysis and design optimization of power delivery networks," in *IEEE Trans. Electromagnetic Compatibility*, (early access version, published online: 24 Mar. 2020).

[Meehan-93] M. D. Meehan and J. Purviance, *Yield and Reliability in Microwave Circuit and System Design*. Norwood, MA: Artech House, 1993.

[Minitab-22] Minitab. (2022). *Effects plots for Analyze Factorial Design* [Online]. Available: https://support.minitab.com/en-us/minitab/21/help-and-how-to/statistical-modeling/doe/how-to/factorial/analyze-factorial-design/interpret-the-results/all-statistics-and-graphs/effects-plots/.

[Mitchel-01] D. Mitchel and R. A. Mammano, "Designing stable control loops," in *Texas Instruments Power Supply Design Seminar*, 2001, SEM 1400, Topic 5, SLUP173.

[Montgomery-05] D. C. Montgomery, *Design and Analysis of Experiments*. Milwaukee, WI: ASQ Quality Press, 2005.

[Moreno-Mojica-19a] A. E. Moreno-Mojica, F. J. Leal-Romo, and J. E. Rayas-Sánchez, "Power delivery network impedance profile optimization," Internal Report *PhDEngScITESO-19-03-R (CAECAS-19-04-R)*, ITESO, Tlaquepaque, Mexico, May 2019.

[Moreno-Mojica-19b] A. E. Moreno-Mojica and J. E. Rayas-Sánchez, "A study on the resonant frequencies of an array of decoupling capacitors for PDN applications," Internal Report *PhDEngScITESO-19-16-R (CAECAS-19-13-R)*, ITESO, Tlaquepaque, Mexico, Oct. 2019.

[Moreno-Mojica-19c] A. E. Moreno-Mojica and J. E. Rayas-Sánchez, "An analytical study on the resonant frequencies of an array of parallel decoupling capacitors for PDN applications," Internal *Report PhDEngScITESO-19-38-R (CAECAS-19-17-R)*, ITESO, Tlaquepaque, Mexico, Dec. 2019.

[Moreno-Mojica-20a] A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "Power delivery network impedance profile and voltage droop optimization," Internal Report *PhDEngScITESO-20-07-R (CAECAS-20-03-R)*, ITESO, Tlaquepaque, Mexico, May 2020.

[Moreno-Mojica-20b] A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "A study on capacitor effects of a PDN in the frequency- and time-domain," Internal Report *PhDEngScITESO-20-10-R (CAECAS-20-06-R)*, ITESO, Tlaquepaque, Mexico, Jul. 2020.

[Moreno-Mojica-20c] A. E. Moreno-Mojica, J. E. Rayas-Sánchez, F. J. Leal-Romo, and Z. Brito-Brito, "Optimizing a buck voltage regulator for a PDN application," Internal Report *PhDEngScITESO-20-19-R (CAECAS-20-08-R)*, ITESO, Tlaquepaque, Mexico, Aug. 2020.

[Moreno-Mojica-21a] A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "Power delivery network impedance profile and voltage droop optimization," in *European Microwave Conf. (EuMC)*, Utrecht, The Netherlands, Jan. 2021, pp. 260-263.

[Moreno-Mojica-21b] A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "Optimizing a buck voltage regulator and the number of decoupling capacitors for a PDN application," Internal Report *PhDEngScITESO-21-01-R (CAECAS-21-01-R)*, ITESO, Tlaquepaque, Mexico, Feb. 2021.

[Moreno-Mojica-21c] A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "An enhanced formulation for optimizing a buck voltage regulator and the number of decoupling capacitors for a PDN application," Internal Report *PhDEngScITESO-21-02-R (CAECAS-21-02-R)*, ITESO, Tlaquepaque, Mexico, Apr. 2021.

[Moreno-Mojica-21d] A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and F. J. Leal-Romo, "Optimizing a buck voltage regulator and the number of decoupling capacitors for a PDN application," in *IEEE MTT-S Latin America Microw. Conf. (LAMC)*, Cali, Colombia, May 2021.

[Moreno-Mojica-21e] A. E. Moreno-Mojica and J. E. Rayas-Sánchez, "Time- and memory-efficient yield analysis in Keysight ADS through Matlab," Internal Report *PhDEngScITESO-21-04-R (CAECAS-21-05-R)*, ITESO, Tlaquepaque, Mexico, Aug. 2021.

[Moreno-Mojica-21f] A. E. Moreno-Mojica, J. E. Rayas-Sánchez, and Felipe J. Leal-Romo, "Evaluating the impact of decoupling capacitors variability on the performance of a power delivery network,"

Internal Report *PhDEngScITESO-21-07-R (CAECAS-21-07-R)*, ITESO, Tlaquepaque, Mexico, Sep. 2021.

[Moreno-Mojica-21g] A. E. Moreno-Mojica and J. E. Rayas-Sánchez, "Optimizing the performance yield of a PDN subject to large variability in decoupling capacitor tolerances," Internal Report *PhDEngScITESO-21-16-R (CAECAS-21-08-R)*, ITESO, Tlaquepaque, Mexico, Nov. 2021.

[Moreno-Mojica-22a] A. E. Moreno-Mojica and J. E. Rayas-Sánchez, "Frequency- and time-domain yield optimization of a power delivery network subject to large decoupling capacitor tolerances," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 12, pp. 5610-5620, Dec. 2022. (p-ISSN: 0278-0070; e-ISSN: 1937-4151; published online: 30 March 2022; DOI: 10.1109/TCAD.2022.3163673).

[Moreno-Mojica-22b] A. E. Moreno-Mojica and J. E. Rayas-Sánchez, "Full-wave EM simulations of a parallel plane power delivery network," Internal Report *PhDEngScITESO-22-05-R (CAECAS-22-03-R)*, ITESO, Tlaquepaque, Mexico, Jul. 2022.

[Moreno-Mojica-22c] A. E. Moreno-Mojica and J. E. Rayas-Sánchez, "Developing a physics-based lumped circuit model for lossless parallel plates," Internal Report *PhDEngScITESO-22-06-R (CAECAS-22-04-R)*, ITESO, Tlaquepaque, Mexico, Jul. 2022.

[Murata-21] Murata Manufacturing Co., Ltd. (2021). *Simsurfing Multilayer Ceramic Capacitors* [Online]. Available: https://ds.murata.co.jp/simsurfing/mlcc.html?lcid=en-us.

[Nelder-65] J. A. Nelder and R. Mead, "A simplex method for function minimization," *The Computer J.*, vol. 7, no. 4, pp. 308-313, Jan. 1965.

[Pandit-11] V. S. Pandit, W. H. Ryu, and M. J. Choi, *Power Integrity for I/O Interfaces: with Signal Integrity/Power Integrity Co-Design*. Upper Saddle River, NJ, USA: Prentice Hall, 2011.

[Paul-92] C. Paul, "Effectiveness of multiple decoupling capacitors", *IEEE Transactions on Electromagnetic Compatibility*, vol. 34, no. 2, pp. 130-133, May 1992.

[Popovich-07] M. Popovich, A. V. Mezhiba, and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors*. New York, NY, USA: Springer, 2007.

[Radhakrishnan-21] K. Radhakrishnan, M. Swaminathan, and B. K. Bhattacharyya, "Power delivery for high-performance microprocessors—challenges, solutions, and future trends," *IEEE Trans. Components, Packaging and Manufacturing Technology*, vol. 11, no. 4, pp. 655-671, Apr. 2021.

[Rayas-Sánchez-06] J. E. Rayas-Sánchez and V. Gutierrez-Ayala, "EM-based Monte Carlo analysis and yield prediction of microwave circuits using linear-input neural-output space mapping," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 12, pp. 4528-4537, Dec. 2006.

[Rayas-Sánchez-16] J. E. Rayas-Sánchez, "Power in simplicity with ASM: tracing the aggressive space mapping algorithm over two decades of development," *IEEE Microw. Mag*., vol. 17, no. 4, pp. 64-76, Apr. 2016.

[Rayas-Sánchez-20] J. E. Rayas-Sánchez, F. E. Rangel-Patiño, B. Mercado-Casillas, F. Leal-Romo, and J. L. Chávez-Hurtado, "Machine learning techniques and space mapping approaches to enhance signal and power integrity in high-speed links and power delivery networks," in *IEEE Latin American Symp. Circuits and Systems Dig. (LASCAS 2020)*, San Jose, Costa Rica, Feb. 2020, pp. 1-4.

[Roy-98] T. Roy, L. Smith and J. Prymak, "ESR and ESL of ceramic capacitor applied to decoupling applications," in *IEEE 7th Topical Meeting on Electrical Performance of Electronic Packaging*, West Point, NY, Oct. 1998, pp. 213-216.

[Roy-11] S. Roy and A. Dounavis, "Efficient modeling of power/ground planes using delay-extraction-based transmission lines," *IEEE Trans. Components, Packaging, and Manufacturing Technology*, vol. 1, no. 5, pp. 761-771, May 2011.

[Sandler-06] S. M. Sandler, *Switch-Mode Power Supply Simulation: Designing with SPICE 3*. New York, NY, USA: McGraw-Hill, 2006.

[Santoso-05] S. Santoso and A. Maitra, "Empirical estimation of system parallel resonant frequencies using capacitor switching transient data", *IEEE Transactions on Power Delivery*, vol. 20, no. 2, pp. 1151-1156, April 2005.

[Sjiariel-15] R. Sjiariel, "Power integrity simulation of power delivery network system," in *IEEE Workshop on Signal and Power Integrity (SPI)*, Berlin, Germany, May 2015, pp. 1-5.

[Smith-99] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," *IEEE Transactions on Advanced Packaging*, vol. 22, no. 3, p. 284-291, Aug. 1999.

[Smith-17] L. D. Smith and E. Bogatin, *Principles of Power Integrity for PDN Design - Simplified: Robust and Cost Efficient Design for High Speed Digital Products*. Boston, MA, USA: Prentice Hall, 2017.

[Sonnet Software-22] Sonnet Software. (2022). *Sonnet Suites Documentation Release 17.56* [Online]. Available: https://www.sonnetsoftware.com/support/help-17/Sonnet_Suites/Sonnet%20Suites%20Documentation.html?index.html.

[Sotman-06] M. Sotman, A. Kolodny, M. Popovich and E. G. Friedman, "On-die decoupling capacitance: frequency domain analysis of activity radius," in *IEEE International Symposium on Circuits and Systems*, Kos, Greece, May 2006, pp. 4 pp.-492.

[Sullivan-21] L. Sullivan, Boston University School of Public Health. (2021). *Confidence Intervals* [Online]. Available: https://sphweb.bumc.bu.edu/otlt/mph-modules/bs/bs704_confidence_intervals.

[Swaminathan-07] M. Swaminathan and A. Ege-Egin, *Power Integrity Modeling and Design for Semiconductors and Systems*. Boston, MA: Prentice Hall, 2007.

[Thierauf-04] S. Thierauf, *High-Speed Circuit Board Signal Integrity*. Norwood, MA: Artech House, 2004.

[Walker-90] C. S. Walker, *Capacitance, Inductance and Crosstalk Analysis*. Boston, MA: Artech House, 1990.

[Yang-02] X. Yang, Q. Chen, and C. Chen, "The optimal value selection of decoupling capacitors based on FDFD combined with optimization," in *IEEE Conf. Electrical Performance of Electronic Packaging (EPEP-2002)*, Monterey, CA, Oct. 2002, pp. 191-194.

[Zheng-03] H. Zheng, B. Krauter, and L. Pileggi, "On-package decoupling optimization with package macromodels," in *Proc. Custom Integr. Circuits Conf.*, San Jose, CA, Sept. 2003, pp. 723-726.

Author Index

Other Authorities

Bandler 69, 71, 111, 112, 116, 125, 126
Basso 57, 125
Box 34, 125
Chen 41, 125, 129
Chew 1, 2, 3, 125
DiBene 29, 32, 55, 56, 125
Erdin 81, 125
Erickson 55, 126
Goral 1, 2, 126
Hattori 41, 126
Hur 5, 126
Ichimura 68, 126
Kamo 41, 126
Kim 68, 91, 93, 126
Klokotov 29, 30, 126
Koziel 111, 116, 126
Leal-Romo 30, 42, 81, 112, 117, 121, 122, 123, 126, 127, 128
Meehan 69, 72, 126
Mitchel 55, 127
Montgomery 34, 127
Moreno-Mojica. 5, 12, 14, 30, 36, 42, 56, 57, 60, 67, 68, 73, 75, 82, 121, 122, 127, 128
Nelder 44, 59, 77, 128
Pandit 6, 128
Radhakrishnan 68, 69, 126, 128
Rayas-Sánchez 69, 111, 112, 116, 121, 122, 123, 125, 126, 127, 128
Roy 81, 129
Sandler 56, 129
Santoso 5, 126, 129

Sjiariel 1, 129
Sotman..... 2, 129
Sullivan..... 72, 129
Swaminathan 81, 126, 128, 129
Thierauf 95, 129
Yang 41, 129

Subject Index

A

active factors, 36, 39
ADS, xv, 59, 67, 77, 78, 92, 110, 114, 122, 127
Aluminum, 68
amplifier, 56
averaged model, 56

B

board, 1, 2, 30, 32, 81, 109
Bode, 56, 57
bounds, 2, 59, 60, 76, 77
Buck, ix, xiv, 3, 55, 56, 60, 61, 65, 110, 114
bulk, 2, 29, 32, 35, 36, 39, 51, 56, 57, 58, 59, 68, 69, 70, 77, 109, 114
Bulk, 2, 31, 33, 42, 48, 70

C

capacitances, 3, 75, 77, 94
cavity, 2, 31, 33, 35, 36, 39, 51, 59, 68, 69, 70, 77, 109
cell, 82, 89, 91, 92, 93, 96, 97, 99
compensation, ix, 3, 55, 56, 57, 58, 60, 61, 62, 65, 67, 76, 77, 110
CONACYT, xi
confidence level, 72
constraint, 48
constraints, 41, 68
cost, 4, 41, 42, 82, 111
crossover frequency, 55, 56, 57, 58, 60, 61, 62, 66, 70, 110
cross-section, 94
Crosstalk, 129
current, ix, 1, 2, 5, 29, 32, 34, 36, 39, 41, 67, 68, 81, 82, 83, 84, 86, 87, 88, 91, 94, 95, 97, 99, 101, 106, 109, 111

D

decoupling capacitors, ix, 1, 2, 3, 4, 5, 6, 7, 8, 19, 20, 24, 27, 30, 33, 39, 41, 42, 44, 53, 55, 57, 58, 59, 65, 67, 68, 69, 70, 71, 72, 73, 75, 76, 79, 81, 82, 109, 110, 111, 121, 122, 123, 125, 126, 127, 128, 129
de-embedding, 85
design specifications, 3, 42, 44, 53, 59, 61, 62, 66, 75, 110
die, 2, 29, 31, 32, 34, 68, 69, 126, 129
die side, 2, 69
dielectric, 83, 88, 94, 95
discretization, 82, 83, 91, 107, 111
dispersion, 1
distributed planar impedance, 81
DoE, 32

E

Electrolytic, 68
electromagnetic, 4, 68, 81, 82, 107, 110, 112, 125, 126
EM, 4, 81, 82, 83, 84, 96, 97, 99, 102, 104, 106, 107, 110, 111, 122, 128
equivalent circuit, ix, 4, 55, 56, 81, 82, 91, 93, 94, 96, 106, 107, 111
equivalent lumped circuit, 92, 100, 101, 106, 107, 111
error function, 48, 51, 59, 60, 61
error vector function, 59, 60, 61, 70, 71, 76
eye, 41
eye diagram, 1, 41

F

factor, 1, 32, 35, 69, 126
factors, 32, 33, 34, 35, 36, 39, 95, 109
feedback, xi, 55, 57, 109
feedline, 86, 87, 88, 96, 99, 101, 103, 105, 106, 107, 111
fluctuations, 1, 2, 41, 68, 69, 73, 75, 79, 110
frequency-domain, 3, 32, 39, 41, 51, 53, 56, 70, 110
Frequency-domain, 2, 29
fringing fields, 93, 94, 95
Full-wave, 81, 112, 122, 128
functional failures, ix, 1, 2, 67, 109

I

IMLA, xv, 93, 97, 100, 102, 104, 106, 107, 111, 115
impedance, ix, 1, 2, 3, 5, 6, 7, 8, 9, 12, 14, 17, 19, 20, 24, 28, 29, 30, 31, 32, 35, 39, 41, 42, 44, 48, 51, 53, 56, 57, 58, 59, 61, 62, 66, 67, 68, 70, 72, 73, 75, 76, 77, 78, 82, 83, 84, 86, 87, 88, 91, 92, 93, 94, 95, 97, 106, 109, 110, 111, 112, 121, 123, 127
impedance profile, ix, 2, 3, 7, 8, 9, 12, 14, 24, 29, 30, 32, 35, 39, 41, 42, 44, 53, 56, 61, 62, 66, 67, 68, 70, 72, 73, 75, 76, 77, 78, 82, 83, 84, 86, 87, 88, 97, 106, 110, 121, 127
inductance, 2, 6, 7, 17, 30, 69, 81, 91, 94, 95, 111
inductances, 3, 19, 20
IPPS, xv, 92, 97, 100, 102, 104, 106, 107, 111, 115

J

jitter, 1, 41, 126

K

Keysight PathWave Advanced Design System, 67

L

land side, 2, 68
load, 2, 55, 67, 68
lumped, ix, 4, 6, 29, 30, 32, 41, 82, 88, 91, 92, 94, 95, 96, 97, 100, 101, 106, 107, 109, 111, 122, 128

M

machine learning, 42
manufacturing, 67, 69, 112
Matlab, 14, 33, 59, 67, 77, 79, 110, 114, 122, 127
microstrip, 83, 85, 87, 93, 94, 95, 96, 99, 106, 107, 111, 115
Minitab® Statistical Software, 33
MLCC, 69
Monte Carlo, 69, 72, 110, 114, 128

N

Nelder-Mead, 44, 59, 77
nodes, 91
noise, ix, 1, 2, 5, 29, 32, 39, 41, 55, 62, 67, 68, 81, 109
normal plot, 35, 36

O

objective function, 44, 60, 75, 78
open loop, 57, 60, 70
open loop gain, 57, 60
optimization, ix, 3, 4, 30, 32, 41, 42, 43, 44, 48, 51, 53, 55, 57, 58, 59, 60, 61, 65, 67, 75, 76, 77, 79, 110, 111, 112, 121, 125, 126, 127, 129
optimizing, ix, 3, 42, 56, 57, 112, 122, 127
outcomes, 69, 71, 72, 73, 75, 77
overshoots, 55

P

package, 1, 2, 29, 30, 31, 32, 34, 35, 39, 51, 59, 69, 70, 77, 109, 125, 129
parallel, ix, 2, 4, 5, 6, 7, 8, 9, 12, 14, 19, 20, 21, 23, 24, 27, 29, 31, 65, 81, 83, 85, 89, 91, 93, 94, 95, 96, 103, 105, 106, 109, 110, 121, 122, 126, 127, 128, 129
Parameter extraction, 41
PCB, 1, 112, 116
PDN, xiii, xiv, xv, 1, 2, 3, 5, 6, 7, 27, 29, 30, 31, 32, 33, 39, 41, 42, 44, 48, 51, 53, 55, 56, 57, 58, 59, 60, 61, 67, 68, 69, 70, 72, 73, 75, 76, 77, 78, 81, 83, 87, 88, 99, 101, 109, 110, 111, 112, 113, 114, 116, 121, 122, 123, 126, 127, 128, 129
performance, ix, 2, 5, 7, 65, 67, 68, 69, 70, 71, 73, 75, 77, 79, 97, 100, 110, 122, 127, 128
phase margin, 55, 56, 57, 60, 61, 62, 66, 110
phase velocity, 94
port, 41, 82, 83, 84, 85, 106, 111
power delivery network, 1, 2, 3, 55, 56, 68, 70, 81, 109, 110, 111, 122, 125, 127, 128, 129
Power delivery networks, 1
power supply, 1, 2, 41, 55, 67, 68, 109
power transmission lines, 81
printed circuit board, 1, 126

R

reliability, 1, 3, 55, 68, 69, 79, 110
resonances, 2, 5, 28, 29, 32, 81
resonant frequencies, ix, 2, 3, 5, 19, 20, 21, 23, 24, 27, 109, 121, 126, 127, 129
ringing, 55, 62
ripple, 1, 55, 56, 67, 73, 75

S

scholarship, xi
screening experiment, 34, 35
Screening experiments, 32
shielding box, 82, 83, 84, 85, 87, 96, 97, 99, 106
Sonnet, xv, 82, 83, 84, 96, 97, 99, 106, 129
space-mapping, 111, 112
SPICE, 33, 59, 125, 129
stability, ix, 3, 55, 56, 57, 62, 65, 67, 70, 73, 75, 76, 77, 78, 110, 111
standing wave, 81
stopping criteria, 45
substrate, 83, 95
surrogate, 41
switching, ix, 1, 2, 3, 5, 55, 56, 67, 68, 81, 109, 126, 129

T

Tantalum, 68
target impedance, 3, 29, 42, 43, 44, 53, 59, 62, 110
third droop, 32, 36
time-, 3
time-domain, ix, 3, 29, 32, 41, 42, 53, 56, 65, 67, 79, 110, 111, 112, 121, 127
T-model, 91
tolerance, 2, 29, 69, 72
transient, 2, 3, 5, 29, 32, 34, 41, 42, 43, 53, 55, 57, 58, 59, 61, 62, 66, 67, 68, 70, 71, 73, 75, 77, 78, 109, 110, 126, 129
transmission line, 94, 106
trials, 72, 110

V

variations, 29, 67, 69
voltage, ix, 1, 2, 3, 5, 29, 32, 36, 39, 41, 42, 43, 44, 48, 51, 53, 55, 56, 57, 58, 59, 61, 62, 67, 68, 69, 70, 71, 73, 75, 77, 78, 109, 110, 111, 121, 122, 123, 127
voltage droop, 3, 29, 36, 39, 42, 53, 56, 59, 61, 62, 67, 70, 71, 73, 75, 78, 109, 110, 121, 127
voltage drops, 2, 32, 67
voltage regulator, ix, 1, 3, 29, 32, 39, 55, 57, 59, 67, 68, 73, 75, 78, 109, 110, 111, 121, 122, 127
voltage regulators, 55, 56
Voltage regulators, 2, 55, 67, 68
VR, xiv, 1, 2, 33, 55, 57, 58, 59, 60, 61, 62, 65, 67, 68, 70, 71, 75, 76, 77, 79, 109, 110
VRs, 2, 67

W

WF, xv, 95, 97, 100, 102, 104, 106, 107, 111, 115
worst-case, 1, 41

Y

yield, ix, 3, 21, 53, 67, 69, 71, 72, 73, 75, 76, 77, 78, 110, 112, 122, 127, 128

Z

Z-score, 72