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Departamento de Electrónica, Sistemas e Informática

DOCTORADO EN CIENCIAS DE LA INGENIERÍA

DESARROLLO DE INTERCONEXIONES RENTABLES DE ALTA VELOCIDAD EN TARJETAS DE CIRCUITO IMPRESO FABRICABLES EN MASA PARA EL VEHÍCULO CONECTADO

Tesis que para obtener el grado de

DOCTOR EN CIENCIAS DE LA INGENIERÍA

presenta: Juan Rafael del Rey Acuña

Director de tesis: Dr. Zabdiel Brito Brito

Co-director de tesis: Dr. José Ernesto Rayas Sánchez

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TÍTULO: **Desarrollo de interconexiones rentables de alta velocidad en tarjetas de circuito impreso fabricables en masa para el vehículo conectado**

AUTOR: Juan Rafael del Rey Acuña
Ingeniero en Sistemas Electrónicos (ITESM Campus Guadalajara, México)
Maestro en Diseño Electrónico (ITESO, México)

DIRECTOR DE TESIS: Zabdiel Brito Brito
Departamento de Electrónica, Sistemas e Informática, ITESO
Ingeniero en Comunicaciones y Electrónica (IPN, México)
Maestro en Ingeniería Electrónica (IPN, México)
Doctor en Teoría de la Señal y Comunicaciones (Universidad Politécnica de Cataluña, España)
Miembro del Sistema Nacional de Investigadores (SNI), CONACYT

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ITESO – The Jesuit University of Guadalajara

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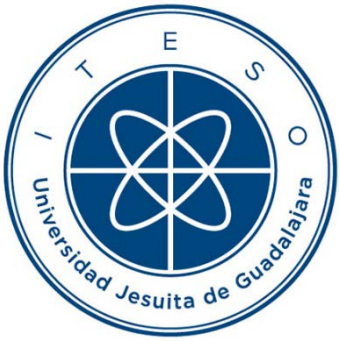

DEVELOPMENT OF COST-EFFECTIVE HIGH-SPEED PRINTED CIRCUIT BOARD INTERCONNECTS FOR MASS PRODUCTION TOWARDS THE CONNECTED CAR

Thesis to obtain the degree of

DOCTOR IN ENGINEERING SCIENCES

Presents: Juan Rafael del-Rey-Acuña

Thesis Director: Dr. Zabdiel Brito-Brito

Thesis Co-director: Dr. José Ernesto Rayas-Sánchez

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PHD IN ENGINEERING SCIENCES (2018) ITESO, Tlaquepaque, Jal., Mexico

TITLE: **Development of Cost-Effective High-Speed Printed Circuit Board Interconnects for Mass Production towards the Connected Car**

AUTHOR: Juan Rafael del-Rey-Acuña
Bachelor's degree in electronics systems engineering (ITESM, Mexico)
Master's degree in electrical engineering (ITESO, Mexico)

THESIS DIRECTOR: Zabdiel Brito-Brito
Department of Electronics, Systems, and Informatics, ITESO-The Jesuit University of Guadalajara
Bachelor's degree in electrical engineering (IPN, México)
Master's degree in electronics engineering (IPN, México)
Ph.D. degree in signal theory and communications (*Universidad Politécnica de Catalunya* (UPC), Spain)
Member of the Mexican National System of Researchers (SNI), CONACYT

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To my wife Lidia.

To my sons Leonardo and Daniel.

For their understanding, patience, and continuous loving support they gave me to reach this goal.

Resumen

Dispositivos cada vez más inteligentes, más pequeños y más económicos están conectando todo en todas partes. Las “cosas” del internet de las cosas (IoT por sus siglas en inglés) son más que aparatos electrónicos, dispositivos médicos, o dispositivos integrados al atavío (*wearables*). Los vehículos automotores se están convirtiendo en la próxima frontera del IoT. Los sistemas de transportación inteligente y los automóviles conectados junto con el IoT, tienen el potencial de proveer sistemas de transporte sustentables, más eficientes, y más seguros, que minimizan el impacto al medio ambiente. A medida que la tecnología de semiconductores se enfoca en el ecosistema del IoT, se requieren soluciones electrónicas avanzadas y asequibles para lograr que su adopción sea transparente para el usuario. En particular, se tornan esenciales los esquemas para reducir los costos de implementación de las tarjetas de circuito impreso (PCB) y de las interconexiones de alta velocidad. Esta tesis doctoral aborda en términos generales algunos de los objetivos de optimización de costos más relevantes en la electrónica de la industria automotriz, y enfatiza en las soluciones de interconexión de PCB más adecuadas que ofrecen un alto desempeño electromagnético, mecánico y térmico para el área de la industria automotriz. Los principales retos son identificados desde la perspectiva de ingeniería eléctrica y de manufactura, considerando las demandas del cómputo de alto desempeño del estado del arte contra los criterios requeridos por la industria automotriz, tales como bajo costo, producción en serie, y alta confiabilidad aún en condiciones climáticas adversas. Los resultados generales presentados en esta tesis doctoral demuestran que las interconexiones robustas y de alta velocidad propuestas para los PCB, pueden lograrse de manera rentable en producción en masa. De hecho, durante este trabajo doctoral fue concebida una invención que ha sido formalizada mediante una solicitud de patente en México, en la que se describe una geometría de interconexión novedosa, económica, térmicamente robusta y tolerante a la deformación por efectos térmicos, en concordancia con los requerimientos del automóvil conectado, el cual constituye una de las aplicaciones más impactantes y trascendentales asociadas con el IoT, así como una de las tendencias tecnológicas más relevantes hoy en día.

Summary

Cheaper, smarter, and smaller devices are connecting everything everywhere. The “things” in the Internet of Things (IoT) is more than appliances, wearables, or medical devices. Automotive vehicles are becoming the next frontier for the IoT. Intelligent transportation systems and connected vehicles along with the IoT have the potential of providing safer, more efficient, and sustainable transportation systems that minimize the impact on the environment. As semiconductor technology focuses on the IoT ecosystem, advanced high-performance and cost-competitive electronic solutions are required for seamless customers’ adoption. Particularly, schemes to reduce the implementation cost of printed circuit boards (PCB) and high-speed interconnects are becoming essential. This doctoral dissertation addresses in general terms some of the most relevant cost optimization goals in the electronics automotive industry. It emphasizes the most suitable PCB interconnecting technology solutions aimed at solving these cost optimization goals while keeping high electromagnetic, mechanical, and thermal performance for the automotive industry arena. The main challenges are identified, from an electrical engineering and manufacturing perspective, in matching high-speed state-of-the-art computing demands against the criteria needed by the automotive industry, such as low-cost, mass-production, and high-reliability even in harsh environmental conditions. The overall results presented in this thesis work demonstrate that the proposed high-speed robust PCB interconnects can be cost effectively achieved in mass production. In fact, a Mexican patent application has been officially formalized based on a novel, thermally robust, warpage tolerant, and cost-effective interconnect that has been conceived during this doctoral thesis work. The proposed invention is in alignment with the connected car scenario, which is one of the most relevant and impactful applications associated to the IoT, and one of the most relevant technology trends nowadays.

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Contenido

Contents

List of Figures

List of Tables

Introduction

Over the next decade, most devices connected to the Internet will not be used by people in the familiar way that personal computers, tablets and smart phones are. Billions of interconnected devices will be monitoring the environment, transportation systems, factories, farms, forests, utilities, soil and weather conditions, oceans and resources [DaCosta-13].

This broad yet transformational phenomenon is being pushed by the so-called “Internet of Things” (IoT) that represents a vision in which the Internet extends into the real world embracing everyday objects [Mattern-10]. At the core of IoT is the staggering proliferation of “smart things,” typically former analog devices and objects transformed into digital ones as the result of increasingly smaller and cheaper sensors and chips [Baumgarten-14].

Today's typical car is a marvel of connectivity — the world’s most technologically advanced consumer product and a key part of the Internet of Things [Ansys-18]. With more than 100 million lines of code, it has more computing power than a jet aircraft. More than 50 microcomputers and dozens of sensors and actuators are helping to run everything from the engine and the powertrain to the instrument cluster, infotainment, communications, and driver-assistance systems. Clearly the design of today’s cars is becoming an enormously complex business. And the complexity is only increasing as car technology rapidly advances toward more sophisticated driver-assistance systems and self-driving cars. Modern vehicles now reach real-time traffic and weather information, custom routes in navigation, can monitor and adjust a vehicle’s position on the highway, and even alert drivers and slow down if they start to drift out of their lane or if they get too close to the vehicle ahead of them [Miller-18].

In fact, according to major key players in the automotive and the information technology (IT) industry [O’Brien-15], we are entering the age of the connected car. This concept is mainly defined as a branch of the Internet of Things in which the presence of devices in a vehicle that connect to other devices within it, and/or devices, networks, and services outside the car, including other cars, home, office, or infrastructure [Auto Conn. Car N.-15].

In fact, the automotive industry is currently undergoing major and accelerated changes. Stricter government regulations, pollution constraints, more driving assistance and an increasing awareness of safety and security are driving the development of the so-called connected car

[Danne-2014]. Along with the potential of making lives more convenient, journeys safer, and vehicles greener [Everis-14], the automotive market is shifting towards greater connectivity.

The potential to improve road safety means that the technology is attracting interest from governments from the entire world. In the United Kingdom, the Department of Trade and Industry (DTI) has put nearly £1 Million (GBP) into a car-to-car project called Traffimatics, based on using 2.4 GHz Wi-Fi networks to disseminate in-vehicle sensor data to a dynamically formed mobile ad hoc network of nearby vehicles to help improve traffic control, road safety, and other services to drivers [Bilchev-04]. In Europe, more than 30,000 people died in 2011 in traffic accidents and the European Commission wants to halve this figure by the year 2020 using a range of measures including road infrastructure and inter-vehicle communications [Evans-Pughe-05].

To fulfill this trend, fully digitized automobile vehicles with 5G connectivity, advanced infotainment systems, real-time location services and advanced driver assistance systems, require powerful computing entities with state-of-the art interconnects. These interconnects should be able to withstand automotive temperature ranges alongside single-digit parts per million (PPM) in quality while maintaining the typical cost-effectiveness relationship required by this market.

Traditional automotive electronics used to be focused on optimizing the vehicle's operation. With the ubiquitous computing evolution, automotive electronics is now developing the car's ability to digitally connect with the outside world, enhance the in-car experience, increase safety, and even drive autonomously. There is no doubt that the connected car will shape the future of the automotive industry, but, are the consumers going to pay for it?

As the computational power continues to rise, the technology required to allow smarter cars and devices entails higher performance electronics, increasing naturally the manufacturing costs of them. For hi-tech companies involved in the so called Internet of Things phenomenon and the connected car, decreasing costs is crucial to remain competitive in the market.

The connectivity-related revenues are expected to increase approximately 7 percent by 2020 in the European premium car segment. Nevertheless, this growth is expected to be compensated by a decline in the base price, keeping more or less unchanged the life cycle spend, just as it has remained since 1980. The global connected car market will grow, but overall car life cycle revenues are expected to remain stable [Habeck-14].

For this reason, and considering that there is not much margin to spend in the now required automotive high-performance computing, cost reduction approaches need to be explored to keep

up sustaining the technological requirements for the connected car in a cost-effective manner.

Trends toward miniaturization, modularity and the continuing increase in performance for the electronics industry have driven a need for finding corresponding ways to increase the interconnection density of the printed circuit board (PCB) substrate. With the introduction of fine-pitch packaging techniques, such as the ball grid array (BGA), chip-scale packaging (CSP), and chip-on-board (COB), traditional PCB technology has approached some point where alternative ways of providing high-density interconnection (HDI) must be developed [Coombs-08]. Smaller chip packages, as those shown in Fig. I, allow products to become more compact and convenient, however, they complicate design efforts to place decoupling capacitors where they will be most effective for reducing EMI.

For such devices, as long as the frequency increases in their interconnection technology, close attention must be paid to the printed circuit board layout and impedance matching because these issues can seriously affect the output performance and deteriorate the results [Texas Instruments-11]. This has been tackled by a tighter process control in the manufacture, requiring an increased precision in the machinery involved, along with more processing steps and time. These manufacturing practices can increase the cost exponentially, and as long as the precision increases, the product will deal with a reduced set of manufacturers in the world that are able to accomplish it.

For this reason, further research must be taken into account in order to enable methodologies that allow interfacing state of the art technologies with cheaper manufacturing capabilities. This thesis dissertation intends to show non-trivial proposals to implement high-speed interconnects for semiconductor ICs in low cost standard PCBs.

Therefore, the design of Continental AG module in package (MiP) technology is portrayed. Such design predominantly targets to lower the overall PCB materials' cost by reducing the PCB high density interconnection technology (HDI) usage to the bare minimum while considering the automotive industry environment and constraints.

State of the art impedance matching and EM modeling techniques are exercised in Chapter 1, along with the employment of optimization algorithms to enhance their response in low cost PCB substrates, constrained to requirements for mass manufacturing.

Subsequently, Chapter 2 introduces to the challenges in the connected car requirements from a hardware perspective by matching the main PCB cost drivers with high-speed state of the

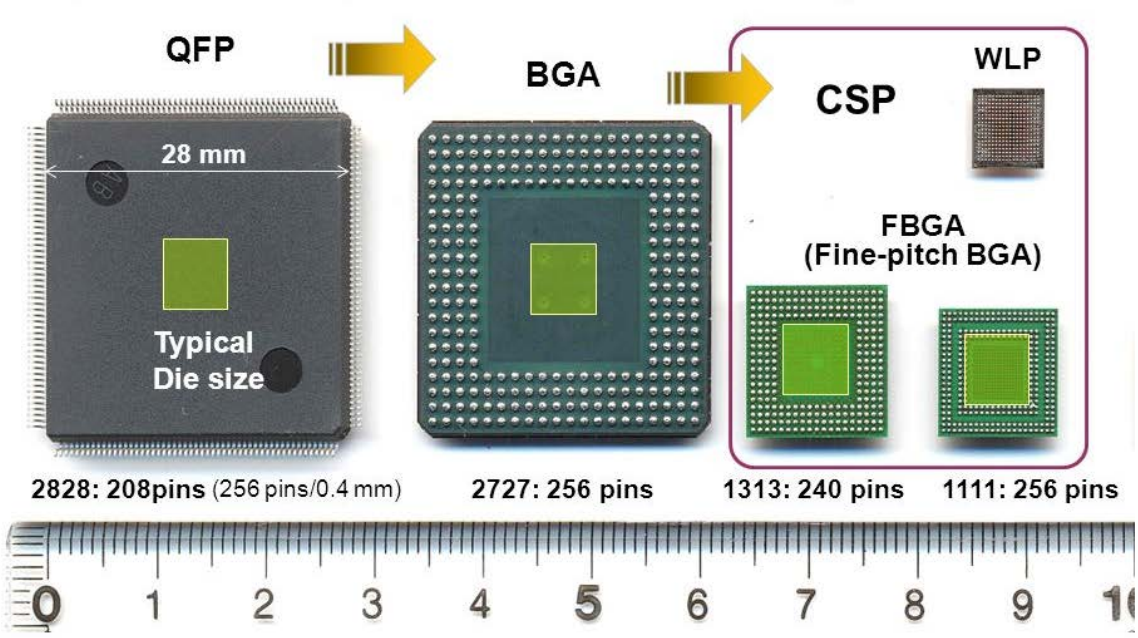


Fig. I QFP, BGA, CSP packages (ruler dimensions are in cm). From [Renesas-10].

art computing within the automotive requirements, providing with several proposals for cost reduction.

Moreover, Chapter 3 carries out with the cost reduction proposals and introduces board to board interconnecting technologies as a cost optimization technique, along with a benchmark of three different connectorless board to board interconnects and an evaluation on several solder balling interconnect technologies, focused in the advanced automotive requirements.

Furthermore, an industrial-grade automotive-oriented module in package (MiP) is described in Chapter 4, whose interconnects' design and unique properties intended to fulfill the automotive specifications towards the connected car scenario, carried out the formalization of a Mexican patent application.

In the general conclusions, the most relevant remarks about this doctoral dissertation are summarized, discussing the overall results, along with how the proposed interconnects can lower the overall PCB materials cost into an automotive oriented SiP-like package, where some future research avenues in this field are briefly mentioned

Finally, Appendix A shows the reference list of the thirteen internal research reports written during the doctoral studies, and Appendix B depicts the list of conference papers and along with the Mexican patent application published.

1. EM Modeling and Optimization Aproaches to Cost-Effective High-Speed Interconnects

Analysis of impedance matching in low cost printed circuit board structures is useful for the IoT, where smaller, cheaper, smarter, even wearable devices are planned to be everywhere. In addition to their frequency domain, performance, and speeds, the electromagnetic compatibility (EMC) requirements increase the challenge to approve the required certifications for electronic devices, including standards such as FCC in the United States, CE in Europe, TELEC in Japan, CNCA in China, etc.

This Chapter analyzes a USB differential pair built in an inexpensive standard PCB laminate that is aimed for the IoT ecosystem. An introductory electromagnetic design analysis is presented in Section 1.1 along with the analysis of a known and well characterized differential structure, in order to set its response as a calibration reference.

Additionally, the modeling of a transmission line reference structure in three different commercially available high-frequency simulators is presented in Section 1.2, focusing in an accurate representation towards a cost-effective manufacturing implementation. Such models are expected to present some differences between their responses and simulation time, due to their internal algorithms differences.

Moreover, an impedance matching optimization of a low-cost PCB differential interconnect is performed in Section 1.3, achieved in an inexpensive standard PCB laminate that is aimed for the IoT ecosystem. An initial fast and coarse simulation model in Sonnet Suites EM simulator of the structure is accomplished. A classic optimization algorithm is applied to this coarse model. This coarse model optimization is intended to comprehend the first part of a space mapping algorithm optimization scheme such as [Bandler-04], [Bandler-94], and [Rayas-Sánchez-16] in future research.

Furthermore, Section 1.4 discerns the frequency response (up to 15 GHz) of several automotive-grade microstrip transmission line structures over a temperature span from -40 to 105 Celsius degrees. To ensure precise measurements, S-parameter responses from several test PCBs based on Cu over FR4 substrate are attained through a vector network analyzer in a controlled

environment. Results show that temperature has a major impact on these high-speed interconnects in frequencies above a few GHz, setting the need of employing accurate multi-physical models.

1.1. Impedance Matching Analysis of a Low-Cost PCB Differential Interconnect

For decades, optimization techniques have been used in the engineering field for device, component, system modeling, and computer-aided design (CAD) [Steer-02]. The target of circuit design is to determine a set of physical parameters that satisfy certain design specifications. Traditional optimization techniques such as [Bandler-88] and [Bandler-85], directly utilize the simulated responses and possibly available derivatives to force the responses to satisfy the design specifications. Electromagnetic (EM) simulators, long used for design verification, need to be exploited in the optimization process [Bandler-04].

On the other hand, electromagnetic compatibility issues have been around since the early days of telegraphy and radio. With the increasing popularity of broadcasting, and then with the use of electronic equipment in commercial and military applications, the rules to prevent radio interference and equipment malfunctions became necessary. The result has been a sequence of EMC standards and regulatory procedures worldwide [Gubisch-07].

The development of Freescale Freedom Platform by Freescale Semiconductor is taken as precedent for this work. It was developed following rules of thumb and engineering judgment to fulfill a USB 2.0 compliant transmission in the lowest cost available PCB stack-up. The method presented in this report is based on trace impedance calculations, and later the resultant structures are simulated in an EM full-wave simulator. It exploits the current standard PCB manufacturing capabilities. It also describes how to implement it in a practical engineering environment.

For this reason, this Section intends to set the foundation to achieve a method for impedance matching in low cost materials for complex printed circuit structures through EM models' analysis and optimization methods, aiming at achieving enough speed to fulfill current transmission technologies and EMC requirements at a minimum cost.

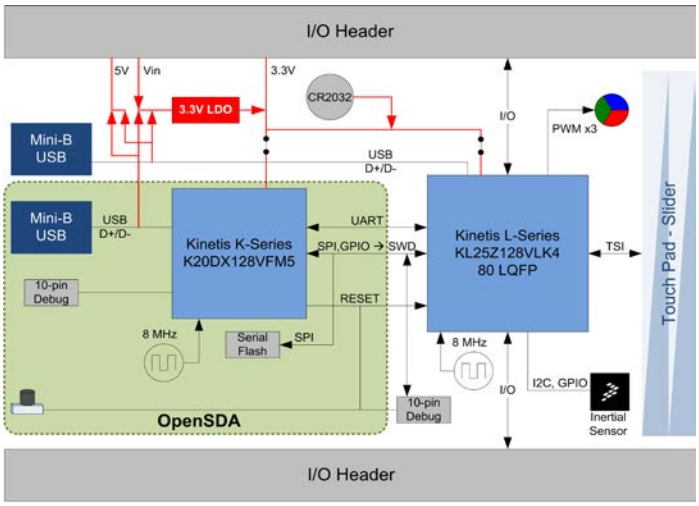


Fig. 1.1 Reference platform block diagram.

1.1.1 Freescale Freedom Platform USB description

This platform has an aggressive price target for ultra-low-cost development since it specifies a bill of materials (BOM) less than $5.00 USD. For this reason, a standard 0.047” 2-layers PCB stack-up was chosen since it was a zero-cost adder against the most popular 0.062” thick. Two USB 2.0 full speed ports shall be supported along with IEC61000-4-2 electro-static discharge (ESD) standard compliance to fulfill the USB-Implementers Forum certification [USB-IF-2014]. In addition, Federal Communications Commission (FCC) in the U.S. compliance for unintentional transmission devices was required. The hardware architecture is based on Kinetis L series KL25Z [Freescale-14] and is shown in Fig. 1.1.

To support USB connector hot swap insertion, Kinetis L series KL25Z microcontroller is compliant with the Human Body Model (HBM) for ESD protection. This allows the IC’s USB interconnects to support a current peak of 8 kV at a connector insertion event due to human interaction. As per graph shown in Fig. 1.2, this protection is not enough to achieve IEC61000-4-2 standard for ESD pulses, so external ESD protection must be added, like the diodes in reference designator U2 shown in Fig. 1.3.

Additionally, in order to support USB 2.0 bus per USB-IF [USB-IF-2014], 90 ohms differential transmission lines are required; for this reason, a 4-layer stackup is recommended by the USB-IF since impedance control in two-layer geometries is unavailable by PCB vendors. This is where engineering judgment is needed to achieve the cost target of a cheaper 2-layer stackup.

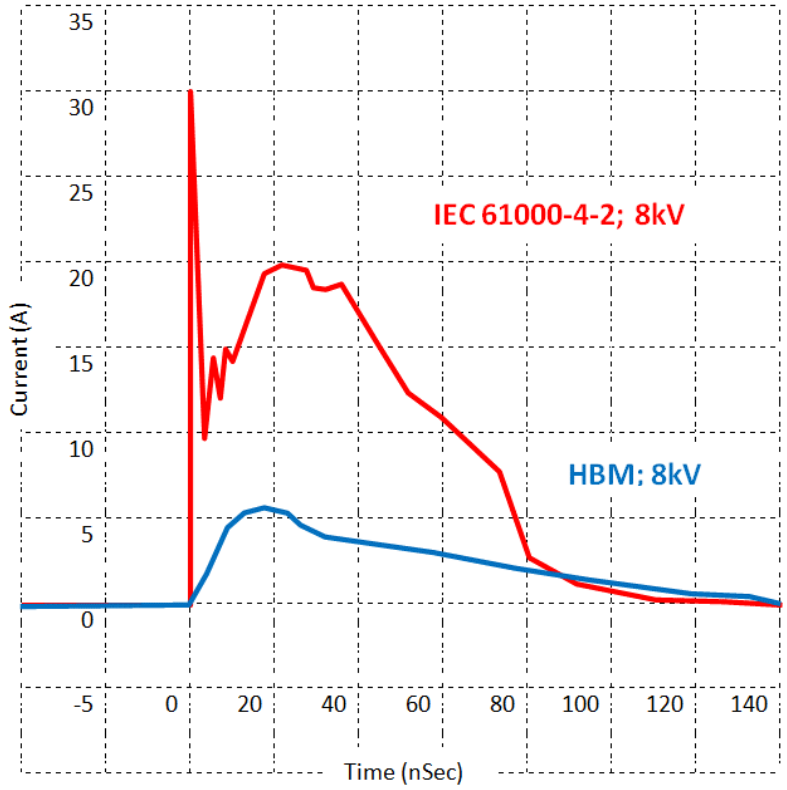


Fig. 1.2 Comparison of IEC 61000-4-2 and Human Body Model standards for ESD pulses that a connector should handle.

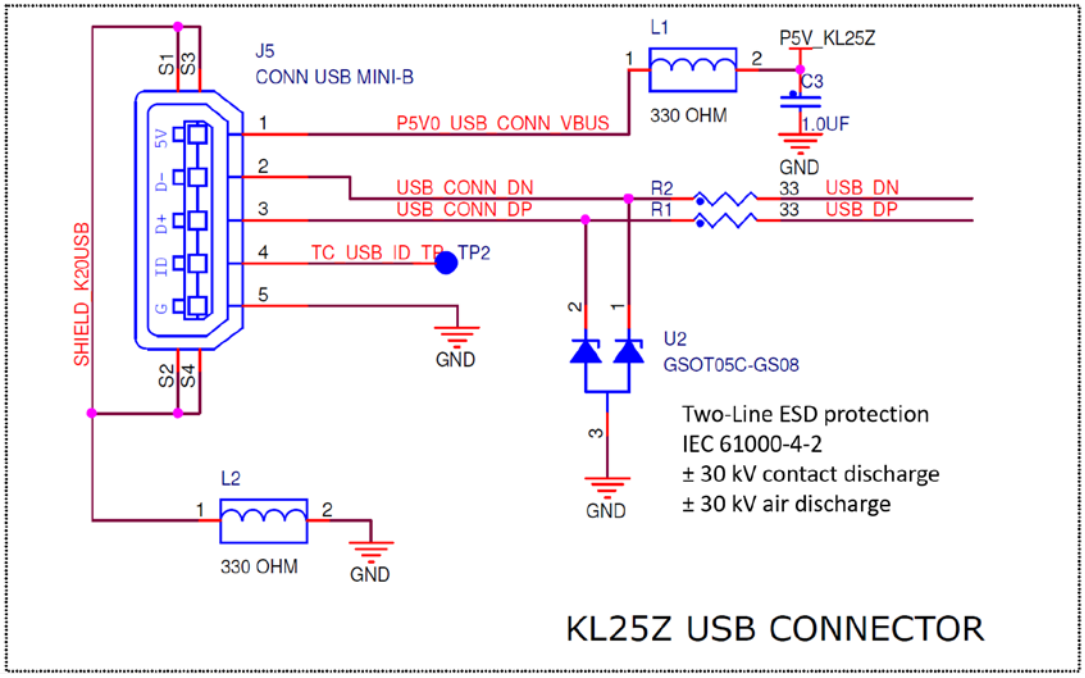


Fig. 1.3 Schematic configuration for Freescale Freedom USB port.

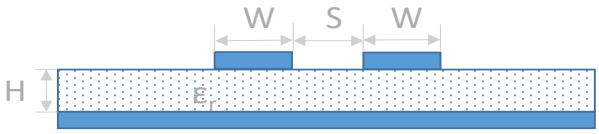


Fig. 1.4 Cross section of a planar differential microstrip transmission line design.

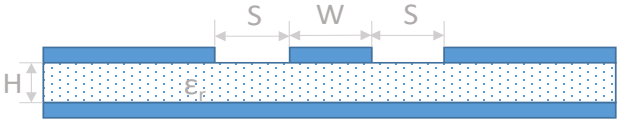


Fig. 1.5 Cross section of a grounded coplanar waveguide design.

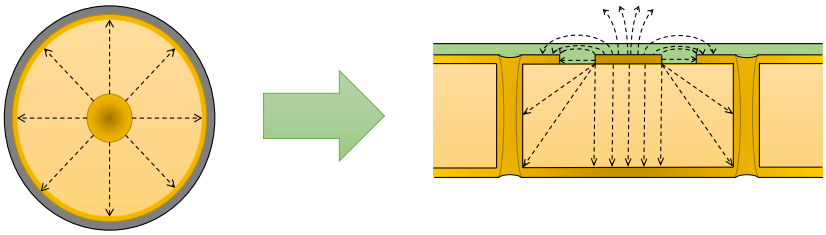


Fig. 1.6 A coplanar structure is proposed to reduce losses in a planar construction due to its slight resemblance to a coaxial cable.

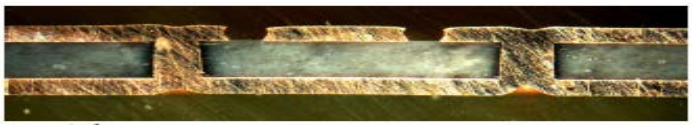


Fig. 1.7 Cross section photograph of a grounded coplanar transmission line.

Thus, in order to reduce the losses and dispersion of a planar structure with a slightly above low-quality dielectric, co-planarity impedance matching is anticipated to enhance the return path of the signal; also maintaining a microstrip reference plane. Hence, the structure proposed is a mixture of differential microstrip planar impedance (see Fig. 1.4) and grounded coplanar impedance (see Fig. 1.5) for the differential transmission line, etched in a standard FR4 PCB substrate with two copper conductor outer. The structure resembles to some extent a coaxial cable embedded into a PCB, as illustrated in Fig. 1.6.

To implement in reality a grounded coplanar waveguide, several “stitching vias” are required to enclose the signal within its reference GND path as shown in Fig. 1.7. The maximum length between stitching vias was calculated considering the parameters shown in Table 1.1.

TABLE 1.1. MAX STITCHING VIA LOCATION

Tr: rise time. BW: bandwidth. Tprop: propagation time. λ: wavelength.
Tr = 4nS full speed
BW ≈ 0.35/ Tr
BW ≈ 87.5 MHz
Tprop FR4 ≈ 180ps/in
λ=1/(Td * BW)
λ ≈ 1.6m (63.5 inch)

TABLE 1.2. PARAMETERS FOR THE FREESCALE FREEDOM PLATFORM DIFFERENTIAL BUS (USB) INTERCONNECT

Dimension	Magnitude
h	.047”
w	.022”
Differential gap	.006”
Coplanar ground gap	.005”
Final routing length	1.44”

The resultant geometry implementation that merges both differential and grounded coplanar was calculated empirically by matching at 100 ohms two single ended (SE) grounded coplanar structures as differential pair, and averaging values from two different impedance calculators: Cadence Allegro Transmission Line Calculator[1] and Saturn PCB Toolkit V5.8[2]. Calculated parameters are shown in Table 1.2.

A cross-section of the implemented transmission line is illustrated in Fig. 1.8, whose geometry is intended to perform in both the differential impedance and the coplanar impedance at the same time. For the PCB implementation, the model built for the 2-layer coplanar differential transmission line is shown in Fig. 1.9. In order to review how good its EMC is performing according to FCC, their FCC pre-scan results for emissions from 30 MHz to 1 GHz are shown in Fig. 1.10; it can be seen in this figure that the highest peak is 10 dB below the compliance margin (red line), so the implementation is fully achieving the purpose.

[1] Cadence Allegro PCB Designer v16.6, Cadence Design Systems Inc., San Jose, CA, 2014.
[2] Saturn PCB Toolkit v5.8, Saturn PCB Design Inc., Orlando, FL, 2014.

Fig. 1.8 Cross section photograph of the implemented transmission line.

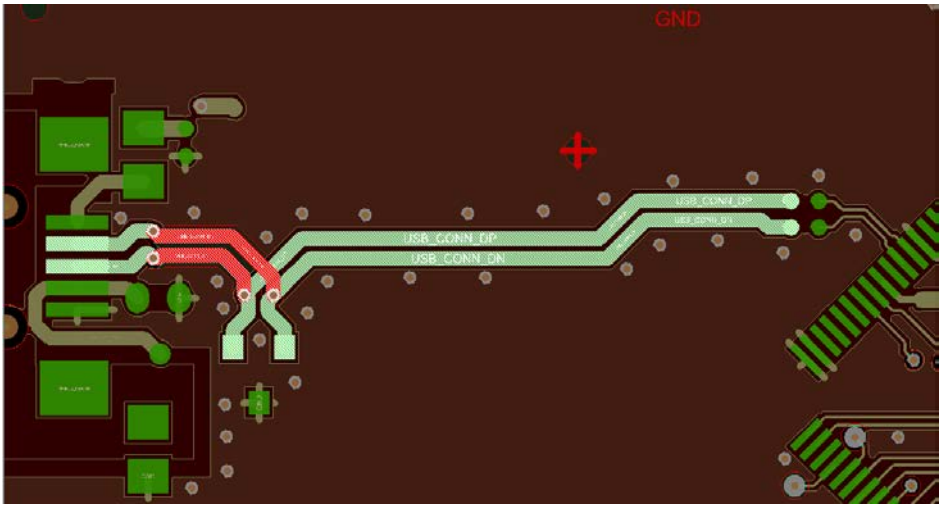


Fig. 1.9 Model built for coplanar transmission line as a differential bus (green: top layer, red: bottom layer).

After these results, its basic transmission line structure was simulated in Sonnet EM[3] confirming that the proposed interconnect was acceptable enough, as described next.

For the Freescale Freedom USB Sonnet EM model, the geometry parameters were drawn according to Table 1.2 and the resulting model can be seen in Fig. 1.11. The simulated differential S-parameters are shown in Fig. 1.12, where we can see an acceptable transmission line behavior, with good insertion and return losses below 1 GHz, which is the estimated bandwidth of operation of the USB port.

In order to validate our approach and assess if the geometry could be improved, a previous step to implement an optimization algorithm in the EM domain was decided. This previous step consists of simulating a well characterized and similar transmission line, taking as reference the Samtec Golden Standard from Samtec Inc[4], since it is a blend of a coplanar and a microstrip differential transmission line geometries, and a copious amount of data is available to validate the accuracy.

[3] Sonnet v14.52, Sonnet Software Inc., North Syracuse, NY, 2014.
[4] Samtec Golden Standard, Samtec Inc., New Albany, IN, 2005.

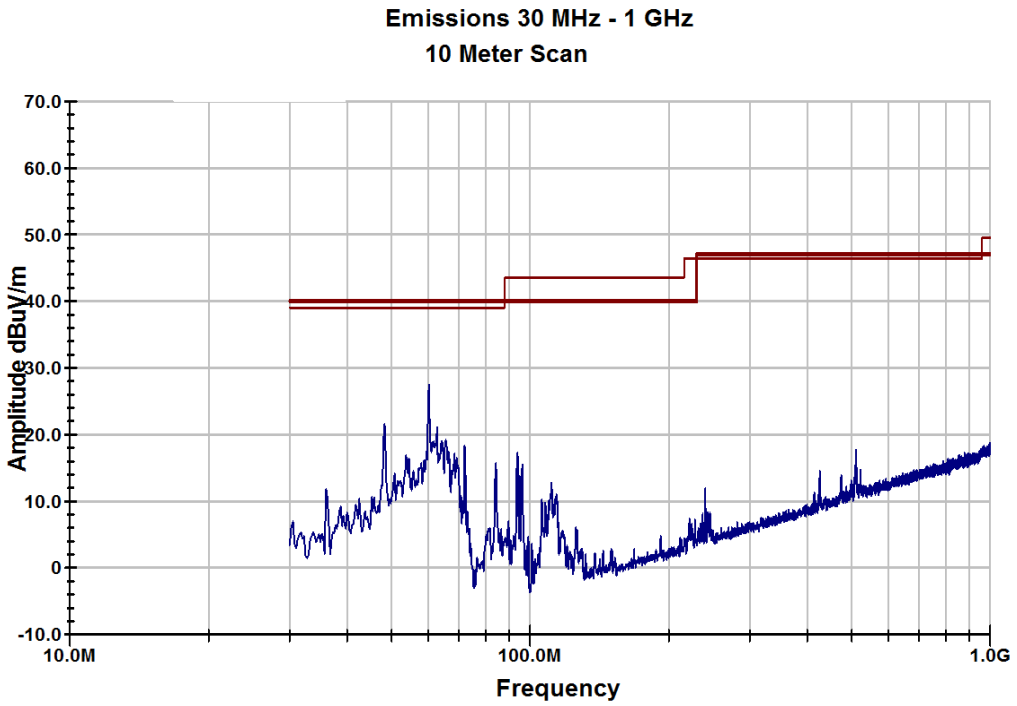


Fig. 1.10 EMC pre-scan of model built for emissions, for 30 MHz to 1 GHz, according with FCC requirements

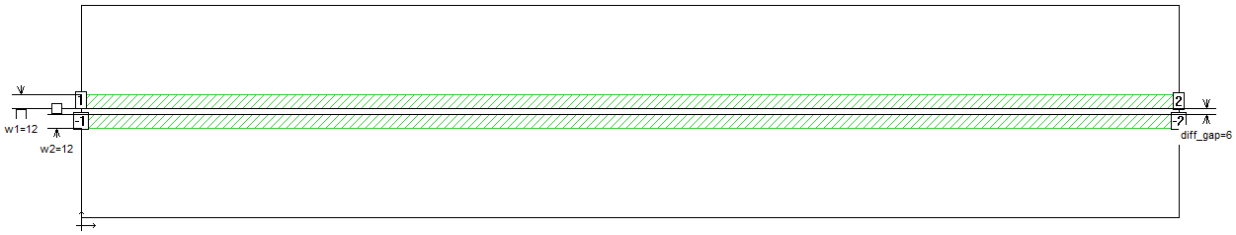


Fig. 1.11 Geometrical model of the Freescale Freedom USB transmission line.

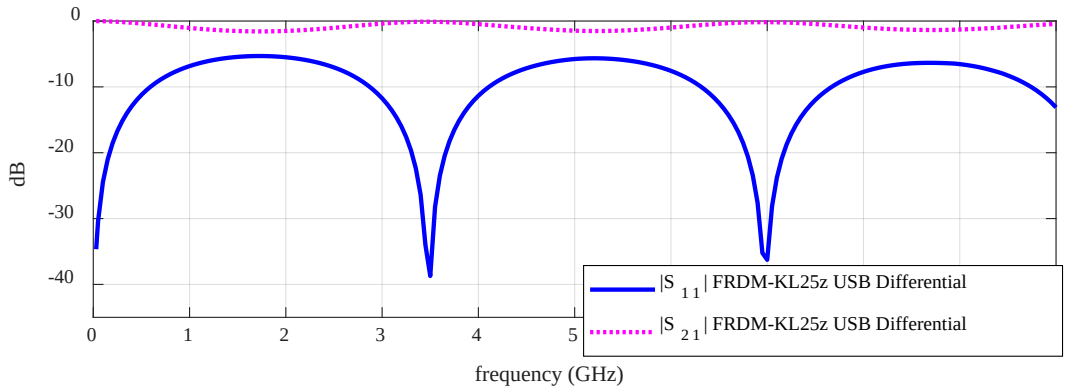


Fig. 1.12 Freescale Freedom USB transmission line frequency response.

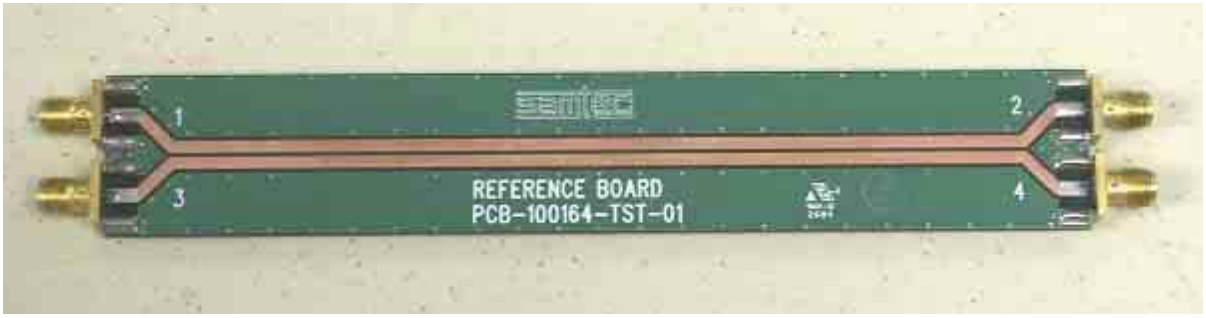


Fig. 1.13 Samtec Golden Standard reference board.

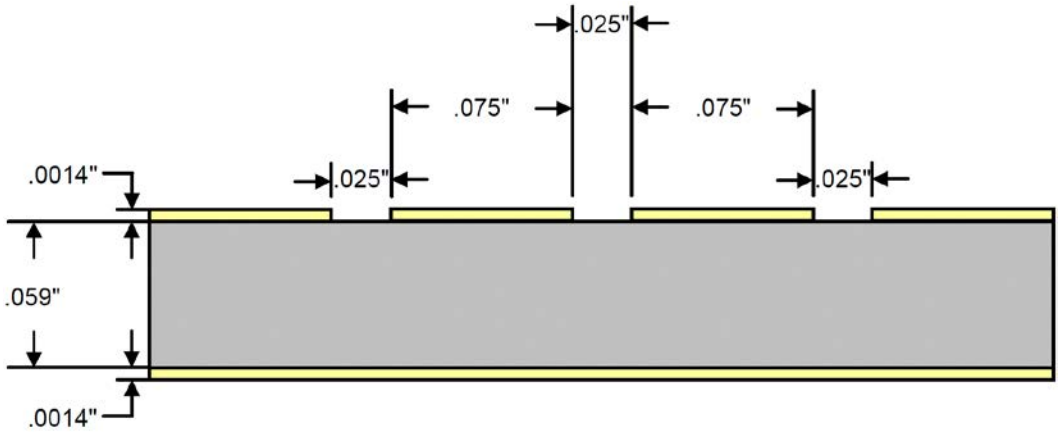


Fig. 1.14 Samtec Golden Standard Cross Section View.

1.1.2 Samtec Golden Standard

The Samtec Golden Standard is a reference structure for validating and debugging electromagnetics simulation software and high-speed/high frequency test and measurement methods. It is based on the two-conductor coupled microstrip design shown in Fig. 1.13. The Golden Standard was used to setup Sonnet EM simulation of the transmission line model in previous section.

The structure consists of two microstrip traces of 0.075” width separated by a space of 0.02”. Each trace is separated from the top ground plane by 0.025” gaps. Conductors can be considered ideal lossless metals, 0.0014” thick. The upper and lower conductors are separated by a dielectric 0.059” thick. The total width is 1.00”. The total coupled length is 5.15”. The ideal implementation requires an infinite ground plane below and on both sides of the microstrip traces, but very “wide” ground planes are sufficient. Three to four times the width of the traces was found

TABLE 1.3. PARAMETERS FOR THE SAMTEC GOLDEN STANDARD INTERCONNECT

Dimension	Magnitude
h	.059”
w	.075”
Differential gap	.025”
Coplanar ground gap	.025”
Final routing length	6.165”

to be acceptable. In the Samtec analysis, material properties were chosen to closely approximate standard FR4 PCB laminate[4]. Cross-sectional view of this geometry is shown in Fig. 1.14. Table 1.3 summarizes the Samtec Golden Standard parameters.

1.2. Modeling of a Low-Cost PCB Differential Interconnect Using Several Commercially Available Simulators

The factor which often limits the usefulness of modern simulation tools is not only the capability of the simulation engine in terms of speed, capacity or robustness, it is also a limitation with the accuracy or availability of the models used within the simulation [Morris-12]. Henceforth, a good tradeoff between accuracy and speed, depending on the complexity of an electromagnetic (EM) model should be appraised through wary engineering judgment. In fact, not any full wave EM simulator is suited to scope all high frequency circuits, and correspondingly, not any circuital EM simulator is meant to be inaccurate.

In order to obtain a fast but accurate enough coarse model along with a precise fine model, three different commercially available simulators are exercised in this work, attempting to build each model with the best accuracy possible. The full-wave EM simulators evaluated were Sonnet EM Simulator[5] and CST Studio Suite[6] as candidates for an EM fine model; similarly, AWR Microwave Office[7] was exercised for a fast-circuital EM coarse model.

[5] ***em***™ Suite version 15.52 2015, Sonnet Software Inc., 100 Elwood Davis Road, North Syracuse, NY, 13212.
[6] CST Studio Suite® version 2015.00, CST AG., Bad Nauheimer Str. 19, Darmstadt Germany, 64289.
[7] NI AWR Design Environment™ version 12.01r, AWR Corporation., 1960 E. Grand Avenue Suite 430, El Segundo, CA, 90245.

1.2.1 EM Models

Even though the Samtec Golden Standard was fully described in Section 1.1.2, its physical implementation was found to deviate from geometry documented in [Samtec-05]. From the provided drawing exchange format (DXF) file used to manufacture the Samtec Golden Standard physical sample, the coplanar ground gap value in Table 1.3 changes from 0.025” to 0.030” and final routing length changes from 6.165” to 6.675”. Thus, all EM models will follow DXF drawing data rather than PDF information. DXF graphical representation is depicted in Fig. 1.15.

1.2.1.1 Sonnet EM Model

A Sonnet EM fine model was done via an extraction of the fabrication files for the PCB, provided by Samtec, Inc. This model can be seen in Fig. 1.16. A comparison between the simulated single-ended S-parameters versus measurements provided by Samtec is shown in Fig. 1.17.

Due to its highly expensive computational cost (about one week in a 3.8 GHz 6-core Intel i7 processor with 12 GB of RAM), and the early stage of the simulations, the model had to be simplified into a coarser model as that one shown in Fig. 1.18

This coarse Sonnet model has the via field and the coaxial connector attachment removed, including the removal of the differential pair decoupling for the coaxial connector attachment, reducing the model box length from 6” to 5.1375”. Additionally, the width was reduced from 1” to 0.5” in order to remove all estimated box resonances in the field solver.

The EM simulation of this coarse model took less than two hours to solve in the same computing system and its response is depicted in Fig. 1.19. It is seen that the coarse model behavior is reasonably similar to measurements, since a good match of the frequency lobes is observed in the low-frequency range, as well as a good match for the insertion loss is also observed in the low frequency range.

Fig. 1.15 Graphical plot of Samtec Golden Standard DXF drawing data.

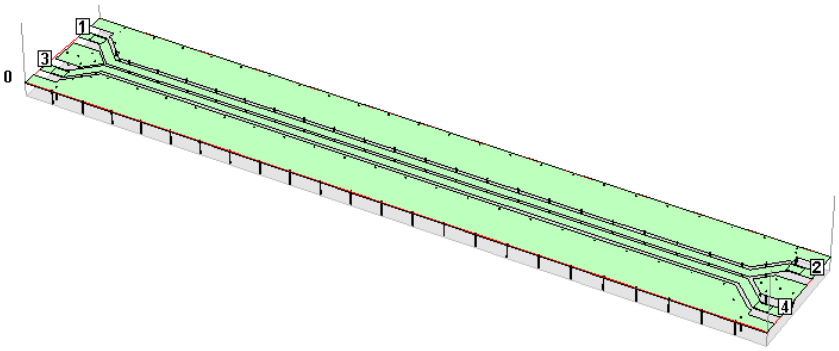


Fig. 1.16 Sonnet fine model of Samtec Golden Standard.

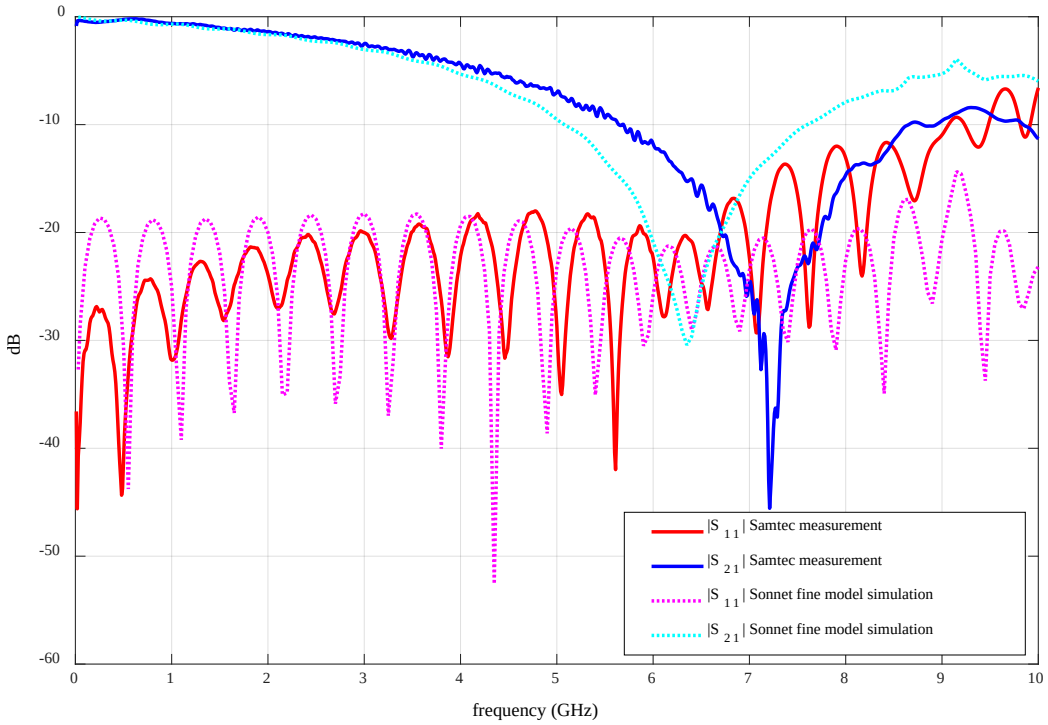


Fig. 1.17 Sonnet fine model of Samtec Golden Standard.

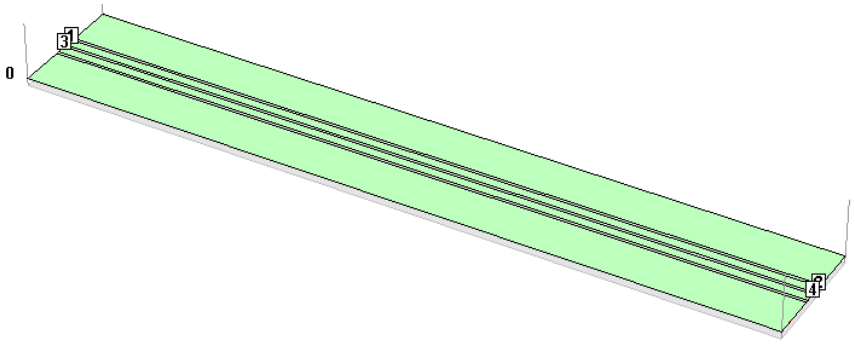


Fig. 1.18 Sonnet coarse model of Samtec Golden Standard.

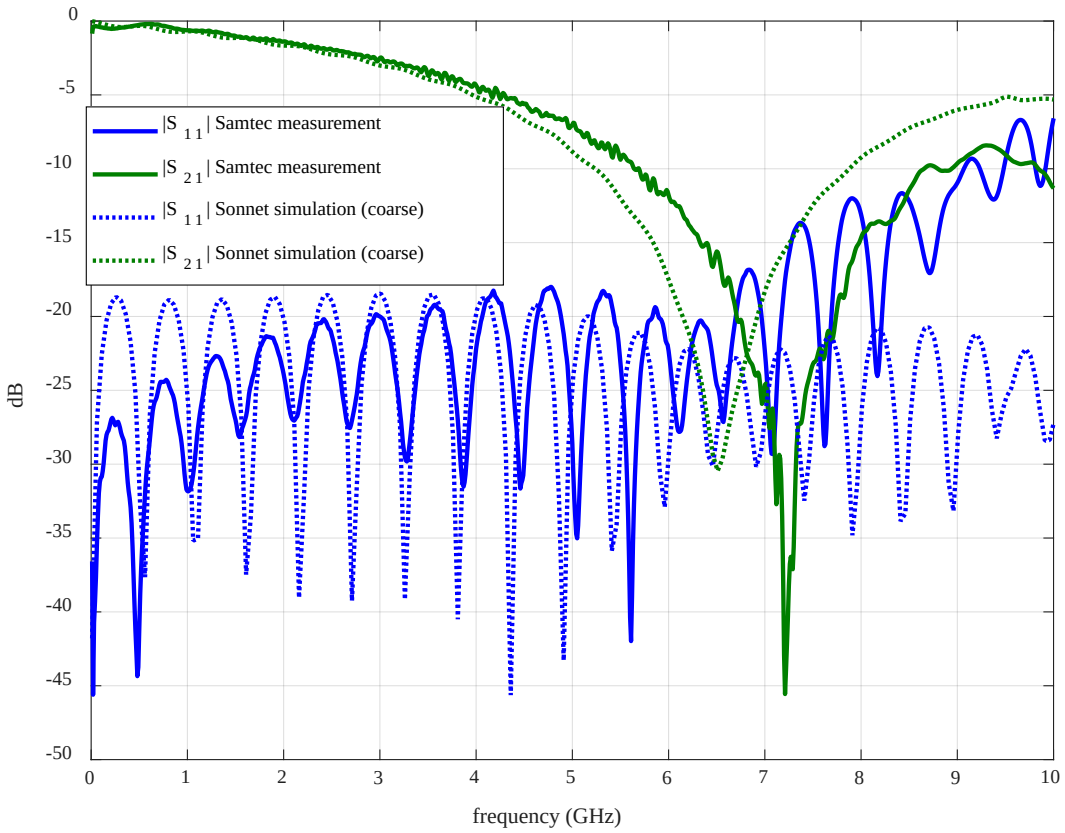


Fig. 1.19 Sonnet coarse model response of Samtec Golden Standard.

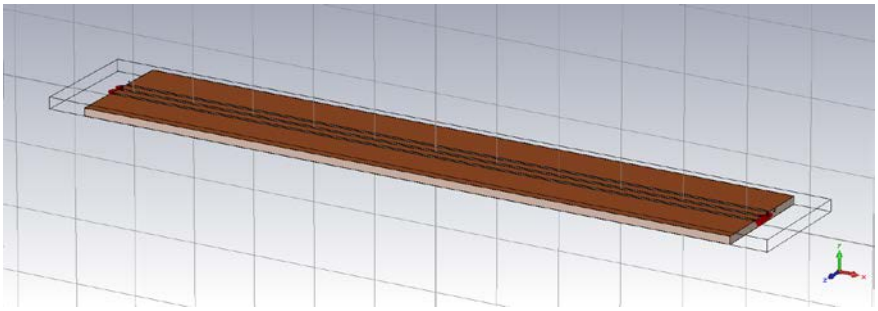


Fig. 1.20 CST full-wave EM model.

1.2.1.2 CST Model

CST can handle either a full wave EM model or a circuital model. Both approaches are explored in this research, but due to the lack of precision in setting accurately the circuital model only the full wave EM model is presented in this work. In the same fashion as Sonnet model, CST representation is drawn with the exact same values as those used in the corresponding DXF file. This model is illustrated in Fig. 1.20.

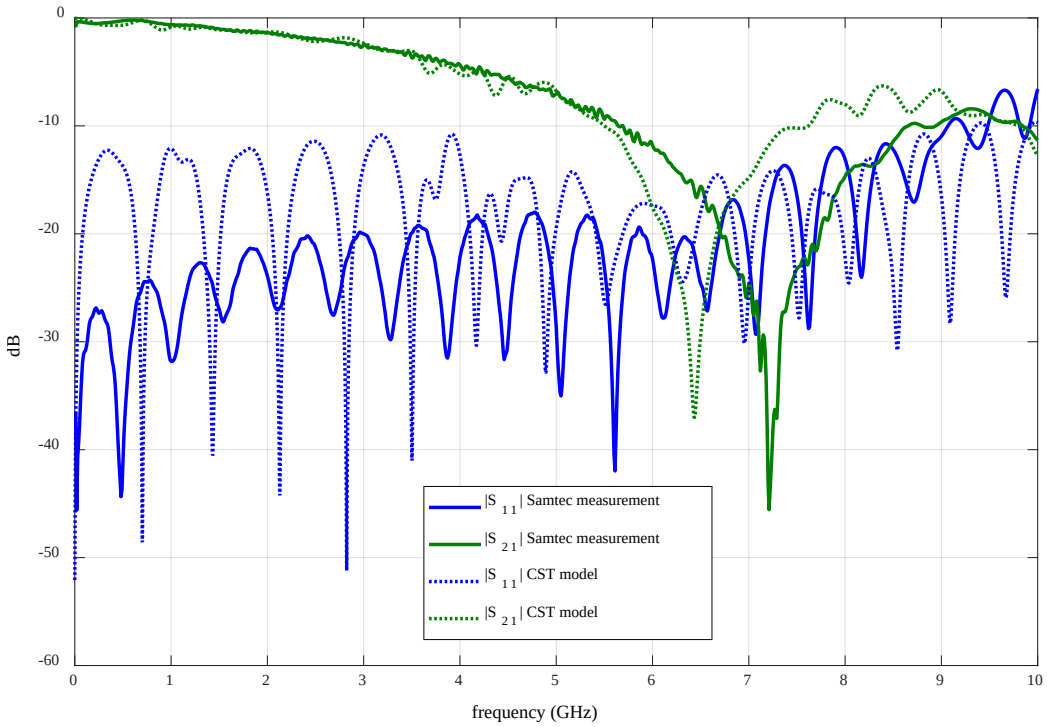


Fig. 1.21 CST EM model response.

For this model, two different general-purpose field solvers can be chosen: frequency domain or time domain; their usage is dependent on the relation between wavelength vs. geometry dimensions. For larger geometries time domain is recommended by CST and simulation time for this geometry was about twice as fast in this mode. CST model response, shown in Fig. 1.21 took about 1 minute to complete in time domain field solver and its differences against frequency domain simulation were negligible. Insertion and return loss responses are similar to Sonnet responses and as can be seen, it still needs tuning, but fortuitously, it did not present any resonance.

1.2.1.3 AWR Model

Circuital model implementation in AWR is significantly different from 3D sketching a full wave EM model. To best match the ideal expected response, a microstrip asymmetric coupled transmission line element (MACLIN) is employed using same geometries as previous models. Single-ended microstrip transmission line components have been included to represent the non-coupled transmission line strips required to attach the SMA connectors as the ports in the physical model, as illustrated in Fig. 1.22. All materials properties (relevant to EM modeling) are also considered in AWR model.

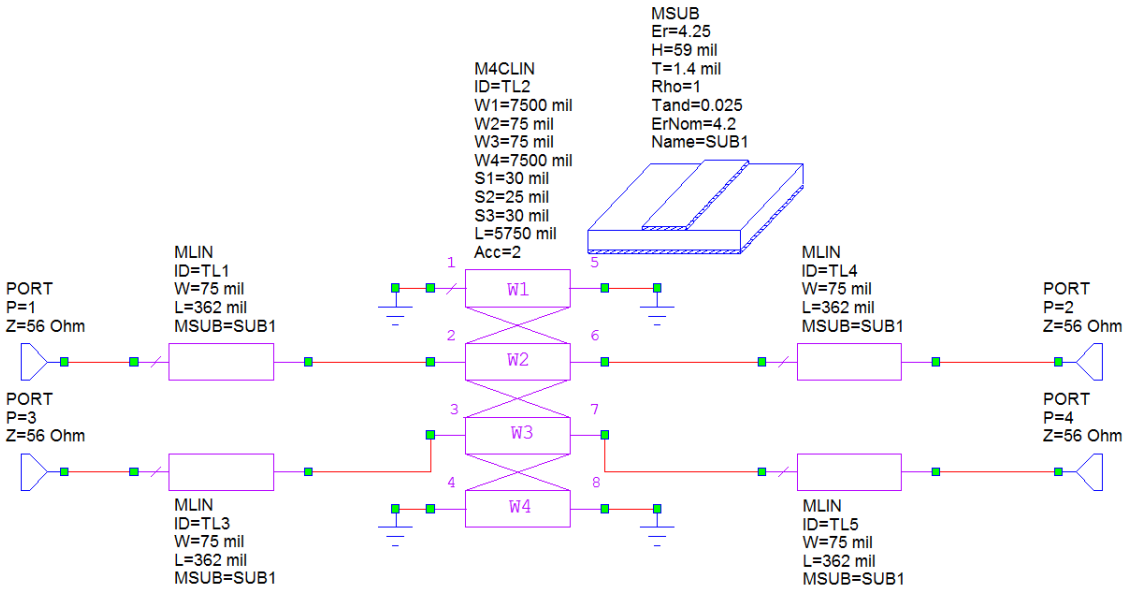


Fig. 1.22 AWR circuital EM model.

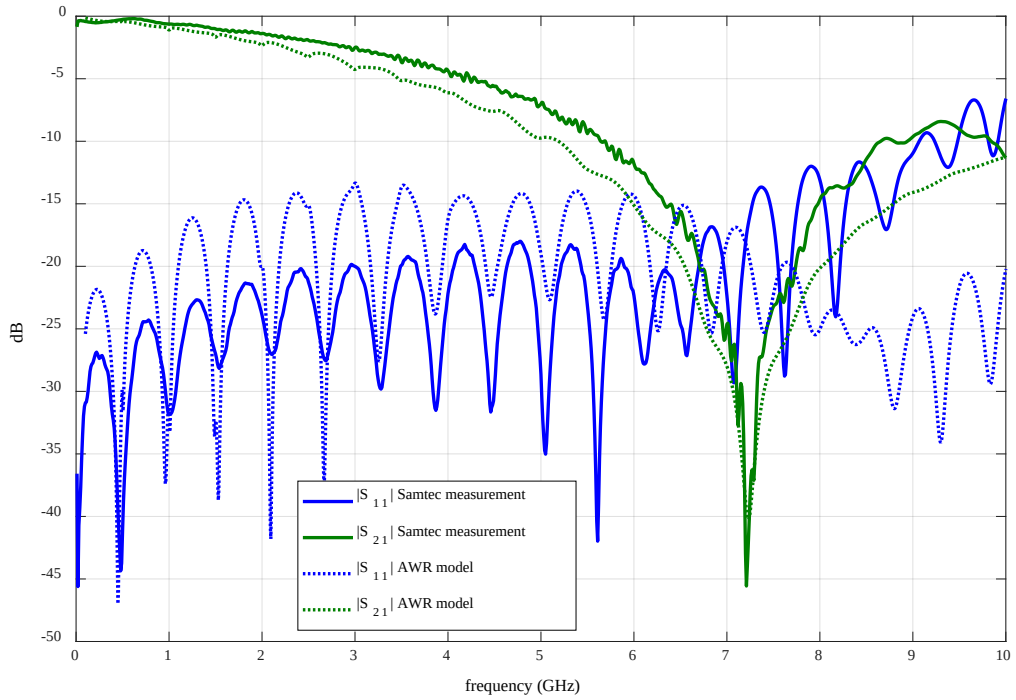


Fig. 1.23 AWR EM model response.

This model took an average 3 seconds to complete since it is based in a quasi-static approximation. Response was found to behave particularly dependent on W1 and W4 ports of MACLIN element (see Fig. 1.22) that corresponds to coplanar grounding. This is particularly risky

for letting an optimization algorithm to vary parameters freely. According to EM theory, the ideal solution requires an infinite ground plane below and on both sides of the microstrip traces, but very “wide” ground planes are sufficient. More than three times the width of the traces is known to be acceptable; but for this circuital element, algorithm for coupling is generalized and was not even expected to behave like a ground plane. The model response can be seen on Fig. 1.23.

1.3. Impedance Matching Optimization of a Low-Cost PCB Differential Interconnect

Several high-speed interconnects come in a differential (odd mode) fashion, because of their effective isolation from power systems, noise immunity, and improvement in S/N ratios [Brooks-03]. These interconnects are intended to be deployed in a PCB which is usually a planar structure, due to their reliable and cost-effective characteristics.

Unfortunately, in a physical application, any imperfection in the differential pair will make signals to slightly mismatch, exciting the microstrip’s even-mode behavior, resulting in degraded differential signaling; i.e., imperfections or asymmetries in the differential pair trajectory yields to mode conversion. As it is known in radio frequency, it is possible to obtain a desired microstrip differential impedance by adjusting the trace’s height above the return plane distance and its edge-to edge spacing [Thierauf-04]. Various combinations of these parameters will result in the same differential impedance, but due to material and construction parasitics, some combinations are less prone to obtain a good stability in the impedance for the manufacturing yield.

Hence, this Section presents an impedance matching optimization of a non-conventional microstrip differential interconnect implemented in an inexpensive standard PCB laminate. The resultant geometry is intended to get the best performance on insertion and return losses for high-speed digital signaling, with cost effective manufacturing processes and materials. An initial fast and coarse simulation model of the structure in Sonnet full-wave EM simulator is developed, along with the application of a classic optimization algorithm in this coarse simulation model.

Fig. 1.24 Initial simulation model implemented in Sonnet.

1.3.1 Simulation Model Implementation

Simulation models were developed in Sonnet EM Simulator[8] given its adequacy for accurate 3D planar EM simulations [Sonnet Software-09], making sense for our utterly planar PCB structure proposed.

1.3.1.1 Initial Simulation Model

The initial simulation model consists of two parallel strips of copper, 0.022" width with a pair to pair spacing of 0.006", etched-alike over an FR4 laminate with a thickness of 0.042" and ε_r = 4.5, and it is based in the geometry proposed for the Freescale Freedom platform in Section 1.1.1. Simulation box is 6" length and 0.5" width with 0.45" height where parallel copper strips are centered and drawn through box length.

A coplanar and microstrip reference is also included, by adding a couple of copper strips adjacent to box walls, and outside the parallel strips with a spacing of 0.005" to the parallel strips. Perfect electric conductor (PEC) simulation box completes the microstrip referencing by acting as a solid ground plane on the secondary side. In order to simplify computing, no stitching GND vias are added to the simulation model even though the structure proposed contains them; electromagnetic field enclosing and electrical interconnection to GND is still obtained due to the box adjacency with outer reference copper strips (see Fig. 1.24). The response for the initial simulation model can be observed in Fig. 1.25.

The accuracy and reliability for this initial simulation model is unknown since there is no data to compare with. The circuit with the interconnect structure implementation is at hand, but it's response is expected to vary significantly due to the numerous differences in the routing path required for the accomplishment of the functional circuit (see Fig. 1.9). For this reason, a test vehicle structure is required to correlate simulation data with electromagnetic measurements.

1.3.1.2 The Samtec Golden Standard Simulation Model

The Samtec Golden Standard became the test vehicle structure proposed to correlate simulation to measurement results. It was chosen due to the extensive field measurements and

[8] Sonnet v15.52, Sonnet Software Inc., North Syracuse, NY, 2013.

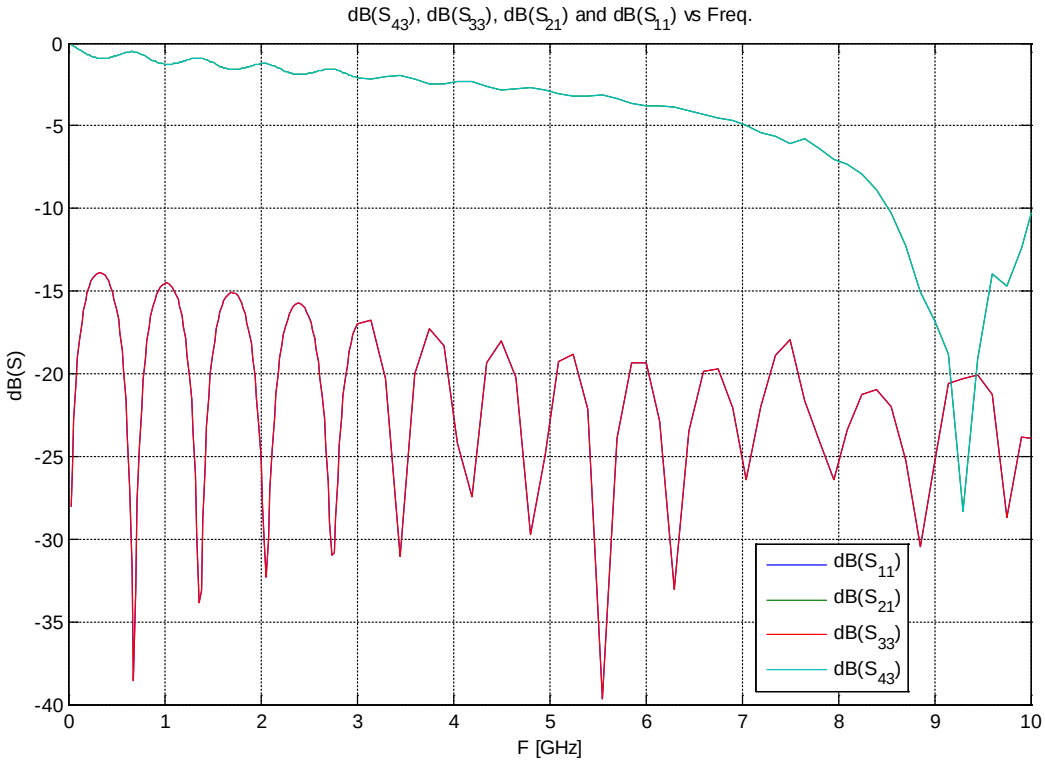


Fig. 1.25 Simulation response of the initial Samtec Golden Standard model.

analysis data provided by Samtec that can be taken as a trustworthy reference. It consists of a two-conductor coupled microstrip design, but the coplanarity property added to that design is intended as an engineering practice for enhanced EMI shielding instead of an impedance match application. However, this structure did not consider matching coplanar with microstrip impedance, therefore, the target impedance is expected to differ from the calculated impedance.

For the extents of this report and due to computational cost, only a coarse model was exercised, whose dimensions have been parameterized in order to modify them with a Matlab[9] script or driver by using SonnetLab Toolbox[10]. Implemented parameters can be seen in Fig. 1.26. Initial or seed dimensions for these parameters are in accordance with parameters from Section 1.1.1, where substrate height, differential gap, and coplanar ground gap parameters are expressed as w, d_g, and c_g variables, respectively. The objective function is tailored by vector $\boldsymbol{x}_0$, whose contents correspond to $\boldsymbol{x}_0 = [d_g \;\; w \;\; c_g]^T$.

[9] MATLAB, Version R2014a Student, The MathWorks, Inc., 3 Apple Hill Drive, Natick MA 01760-2098, 2014.
[10] SonnetLab Toolbox, Sonnet Software Inc., North Syracuse, NY, 2013.

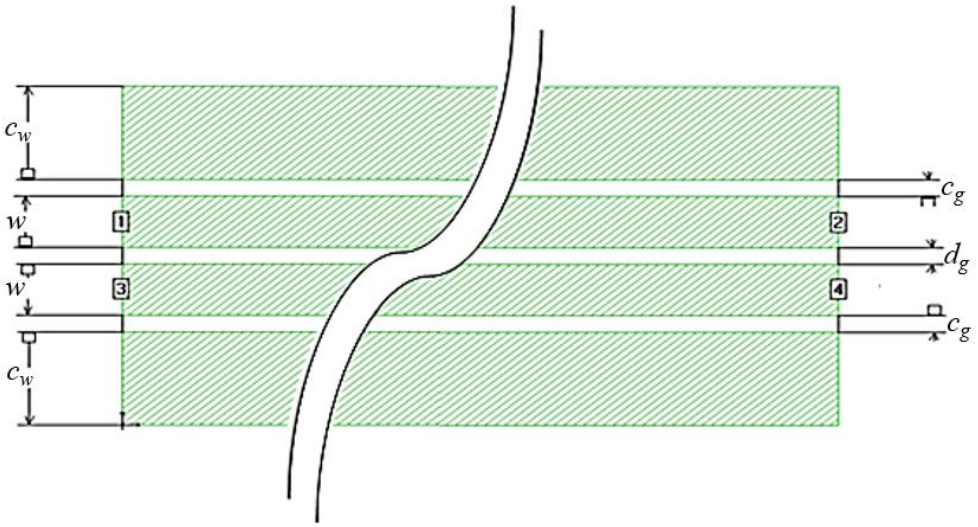


Fig. 1.26 Parameters applied to the Sonnet coarse model of Samtec Golden Standard.

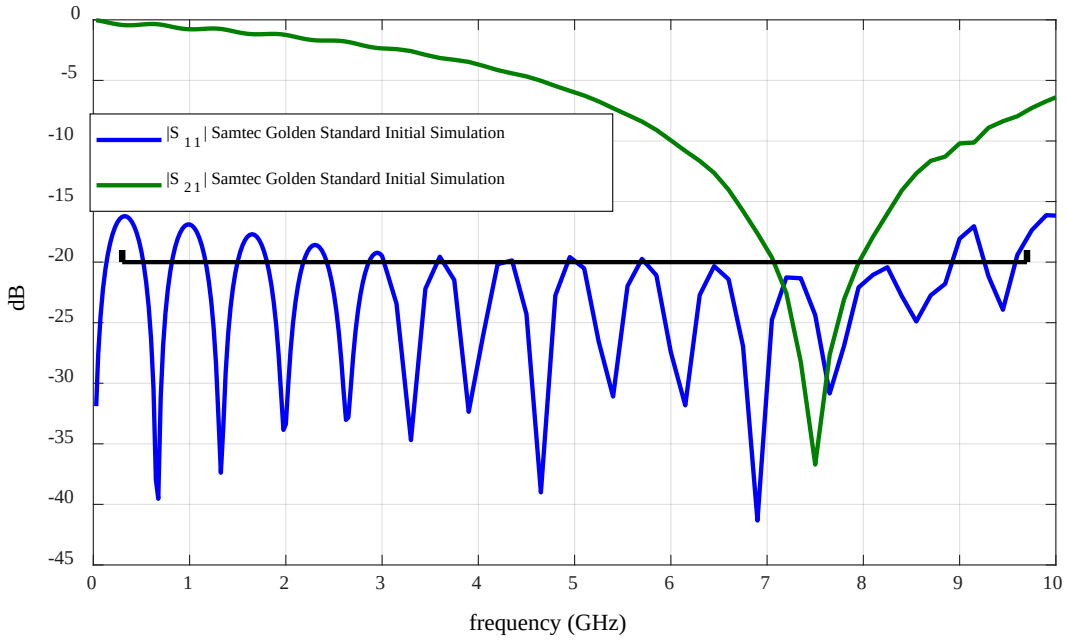


Fig. 1.27 Simulation response of Samtec Golden Standard coarse model at the seed or starting point.

A script was written in Matlab, which sets the new parameters in the geometry, and then auto centers the geometry in the box, making sure the coplanar planes touch the metal box, expecting to work as a simplified version of the via walls in the proposed design. Additionally, an auto snap to grid is set, in order to ensure Sonnet analysis is accurate.

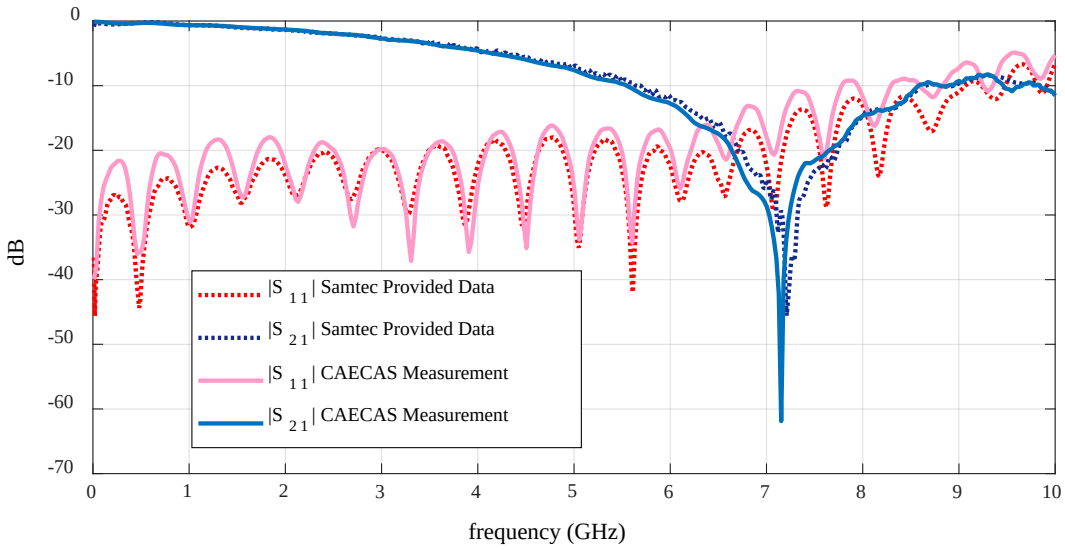


Fig. 1.28 Measured response for Samtec Golden Standard. Dotted lines come from [Samtec-15], and continuous lines come from measurements performed in CAECAS.

The initial seed response for Samtec Golden Standard model using $\boldsymbol{x}_0$ = [0.025" 0.075" 0.025"]^T can be seen in Fig. 1.27. Notice that a few $|S_{11}|$ lobes are violating the specification band (horizontal line in black), which was chosen by industry experience as a relatively good enough value. Considering the specification band is not very restrictive, structure response was expected to be below this band since impedance coupling was carefully selected, tested and measured by Samtec engineers.

It becomes evident that Samtec engineers back in 2004 did not mean to tune the coplanar reference to the microstrip differential transmission line impedance; nevertheless, optimization algorithms can achieve better results, aiming to reduce the losses in higher frequencies, which are considerably large, as shown in measurements in Fig. 1.28.

1.3.2 Formulation of the Optimization Problem

A classic or conventional optimization method is exercised in this Section as the first approach to apply optimization, due to the relative simplicity of the selected coarse model. The chosen method was the Nelder-Mead algorithm, which is widely used in engineering fields due to its good performance with highly nonlinear, discontinuous, non-differentiable, and noisy objective functions [Brito-Brito-13]. Henceforth, the following optimization problem should be solved,

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}\in X} U\left(\boldsymbol{R}(\boldsymbol{x})\right) \tag{1-1}$$

where U: $\Re^n \rightarrow \Re$ corresponds to the objective function expressed in terms of the design specifications, $\boldsymbol{R}(\boldsymbol{x})$ contains the responses of the structure evaluated at the design variables in $\boldsymbol{x} \in \Re^n$, and $\boldsymbol{x}^*$ contains the optimal design.

Due to the fact that U is typically defined as a combination of multiple objectives with conflicting criteria [Rayas-Sánchez-15], when using EM simulators, inequality design specifications are easier to incorporate by using a minimax formulation.

1.3.2.1 Minimax Formulation for Design Optimization

In order to obtain a suitable transmission response, per industry practice, enforcing a $|S_{11}|$ below −20dB at all frequencies would be a reasonable target. Thus, an error function is defined to fulfill this specification, as follows:

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} \max\{\ldots e_k(\boldsymbol{x})\ldots\} \tag{1-2}$$

$$e_k(\boldsymbol{x}) = \frac{R_k(\boldsymbol{x})}{S_k^{ub} + \varepsilon} - 1 \tag{1-3}$$

where $e_k(x)$ is the error function at the k-th frequency point, ε is an arbitrary small value in the order of 1×10^{-4}, $S_k{}^{ub}$ corresponds to −20dB, and $R_k = |S_{11}|$. Henceforth, the maximum error found is returned as the objective function value being minimized by Nelder Mead algorithm.

1.3.3 Optimization Results

When the optimization algorithm was implemented, after 39 function evaluations and about 1 hour of runtime, the Nelder-Mead algorithm found the response in Fig. 1.29 with $\boldsymbol{x}^*$ = $[2.852315\times10^{-2} \quad 6.862500\times10^{-2} \quad 2.705440\times10^{-2}]^T$ (inches). This response is not perfect, and after resetting the algorithm several times, the best response obtained was very similar. We assume that the losses in the structure, along with the simulator box resonances, make very difficult to enhance this response. However, the optimal response found is much better than the initial response shown in Fig. 1.27, sustaining the benefit of this optimization.

As seen in the results, the optimization algorithm was able to enhance the transmission line response. The coarse model selected for this optimization technique was shown to be effective in

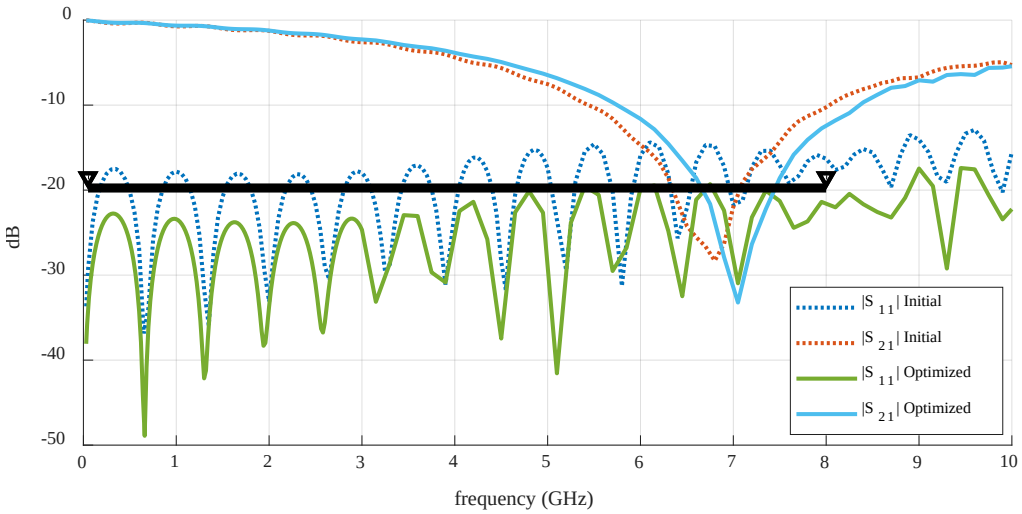


Fig. 1.29 Simulation response of Samtec Golden Standard coarse model after optimization.

terms of computational cost, and hence suitable towards a space mapping optimization such as [Bandler-04], [Bandler-94], and [Rayas-Sánchez-16].

1.4. Temperature Effects in Automotive-Grade High-Speed Interconnects

Current automotive computing design is mostly based on semiconductor vendors' models, typically neglecting temperature effects on interconnects. The effects of temperature performance have been studied mainly for antenna applications with Teflon-based materials, such as Polytetra Fluroethylene (PTFE), Tetra Fluroethylene (TFE) as in [Elrashidi-11], and also with Poly Vinylidene Fluoride (PVDF), whose performance is studied in [Yadav-10]. It is important to remark that Teflon-based materials are not cost-effective for automotive electronics' applications.

In this section, we assess these temperature effects by considering five different FR4-based microstrip transmission lines (TLs). We built three test printed circuit boards (PCBs), intending to spot the sensibility to temperature through different microstrip geometry relationships: two TLs with same length but different widths and two TLs with same width but different lengths. These TLs are designed with a characteristic impedance of approximately 50 ohms. We also consider the Samtec Golden Standard again [Ferry-05], as trustworthy reference to control environment setup and calibration, and particularly useful as a test case for temperature effects on near-end and far-end crosstalk.

TABLE 1.4. 4-LAYER TEST PCB STACKUP

Layer	Thickness (mil)	Material	Tolerance (mil)
	1	Solder resist	± 0.2
1	1.4	1 oz. Cu	
	6.7	FR408 prepreg	± 0.67
2	0.7	0.5 oz. Cu	
	47	FR408 core	± 4.7
3	0.7	0.5 oz. Cu	
	6.7	FR408 prepreg	± 0.67
4	1.4	1 oz. Cu	
	1	Solder resist	± 0.2

1.4.1 Transmission Line Structures

As mentioned before, several transmission lines with different-widths were built in the same PCB anticipating a homogeneous behavior between them. These interconnects are shown in Fig. 1.30. A four-layer FR-408 PCB stackup (see Table 1.4) was chosen in order to create a planar TL geometry from layers 1 to 2 and another one from layers 1 to 3. TL lengths were fixed at 1.7". According to the PCB manufacturer, the PCB substrate has an ε_r of approximately 3.6 and a loss tangent of 0.0117 [Isola-14].

Initial impedance matching was calculated using APLAC[11]. A more accurate estimation was performed with Sonnet[12] using a thick metal model due to the 1 oz. outer conductor layer thickness in the PCB stackup. TL widths were calculated at 13.5 mils and 117.5 mils, respectively. Connectors used in this test PCB were Samtec part number SMA-J-P-H-ST-MT1, being chosen first for its temperature range, from −65 to 125 °C, and also because of its geometry, due to the absence of via interconnects in the signal path, which simplifies simulation models.

Similarly, transmission lines with different lengths were implemented with separate machine milled PCBs in a standard FR4 substrate. The short trace TL is laid out with a length of 2", while the long trace TL is defined at 6" long. Impedance match is achieved using Saturn PCB Calculator[13] with an ε_r of 4.6 and a loss tangent of 0.018. Under those circumstances, TL width is

[11] APLAC, ver. 8.1 2015, APLAC Solutions Corporation, Atomitie 5 C, Helsinki, Finland, FIN-00370.
[12] Sonnet *em*™ Suite version 15.52 2015, Sonnet Software Inc., 100 Elwood Davis Road, North Syracuse, NY, 13212.
[13] Saturn PCB Toolkit V6.88 2016, Saturn PCB Design, Inc., 2737 Bishop Lane, Deltona, FL, 32725

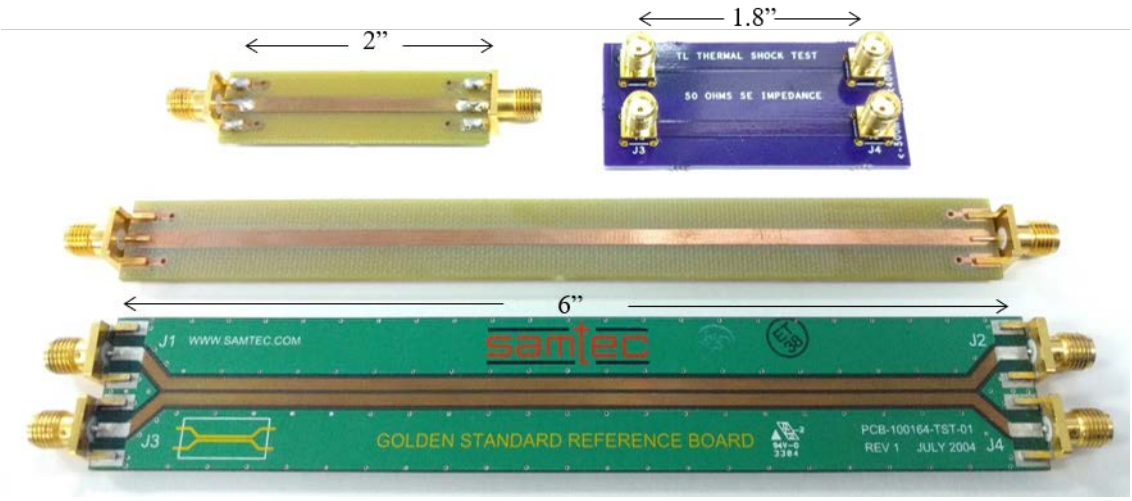


Fig. 1.30 Tested transmission line structures. From top to bottom and left to right: 1) 2” long FR4-STD TL; 2) 1.7” long FR408 13.5 mil and 117.5mil width TLs; 3) 6” long FR4-STD TL; 4) Samtec Golden Standard with 6” long 100 ohm differential impedance.

calculated at 122 mils. Connectors used are Molex part number 0732511150, selected to attach the microstrips directly at connector launch and due to its temperature range, from −65 to 165 °C.

The last transmission line structure tested was the Samtec Golden Standard, which is an accurately matched 100-ohm microstrip differential pair with a length of 6” as described in Section 1.1.2 and thoroughly modeled in Section 1.2. Its end launch SMA connectors are Johnson Components part number 142-0701-851 and are rated at an operating temperature of −65 to 165 °C, which makes the Samtec Golden Standard an ideal candidate for this analysis.

1.4.2 Test Set Up

To perform the measurements, a 20 GHz Keysight E5071C vector network analyzer (VNA) was used for broadband frequency measurements from 0.5 to 15 GHz. The VNA was calibrated with a Keysight 8052B Calibration Kit, rated from 0 to 20 GHz.

Device under test (DUT) was placed inside a Thermotron Industries model S-1.5-3800 environmental test chamber and connected to the VNA through Semflex 2121-DKF-0036 3.5 mm coaxial assembly cables. These cables were chosen since they are rated up to 26 GHz and have a temperature range from −65 to 200 °C.

Even though the environmental test chamber calibration was professionally tested

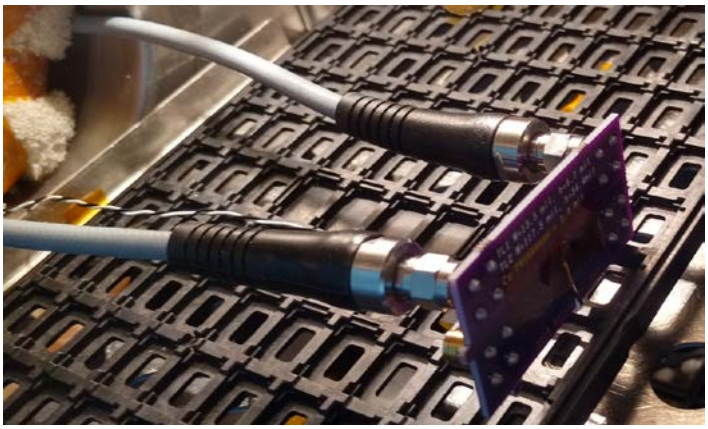


Fig. 1.31 DUT setup inside environment test chamber. A thermocouple is stick to the rear face of the DUT for accurate temperature control.

beforehand, a thermocouple was attached to the bottom surface of the test PCBs (see Fig. 1.31), in order to discard any temperature mismatch. Thermocouple maximum resolution is 0.001 °C.

All VNA connections to DUT were carefully tighten at 0.90 N-m with a Keysight 8710-1765 torque wrench. Error introduced for cables' length was removed using short-open-load-thru (SOLT) calibration, with the cables inside the environmental test chamber at 25 °C. To verify the behavior of test setup, a measurement in different temperatures was performed without DUT (cables only connected to themselves).

Results of this measurements in Fig. 1.32 show that no effect is introduced by the test setup due to the temperature change, even though some behavior in $|S_{11}|$ will be added to the DUT response, since we are focusing in the temperature change or difference in the response and not in the final waveform.

For guaranteeing the repeatability of the results, three different temperatures in a six-step sequence was set for S-parameters capture: 25 °C, 105 °C, −40 °C, 25 °C, −40 °C, 105 °C. This sequence was intended to raise any discrepancy between measurements, stressing the DUT from hot to cold and vice versa.

To eliminate any uncertainty in the measurements, each temperature was measured twice and with a tolerance < 0.1 °C. Additionally, the test sequence was applied uninterruptedly to each DUT PCB to maintain homogeneous humidity and atmospheric pressure conditions.

Each S-parameters capture was timestamped and plotted against the same temperature measurements to validate repeatability. In case of a discrepancy, the whole test procedure was reevaluated and restarted from the beginning.

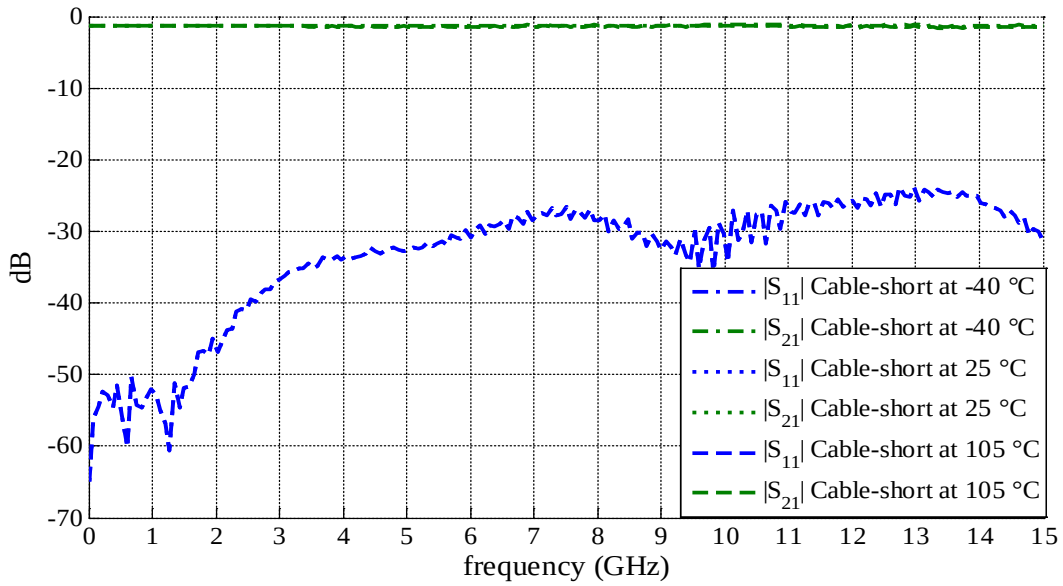


Fig. 1.32 Cable only test (without DUT) S-parameter responses at different temperatures.

1.4.3 Measurement Results

Besides S-parameters, impedance was measured with the TDR functionality of E5071C VNA. The thin TL impedance measured 58 ohms while the thick TL impedance measured 43 ohms. This mismatch from ideally calculated impedance resulted from the broad tolerances given by PCB manufacturer and the connectors effects. The short and long TLs resulted both at 50.2 ohms since they were built in the same process.

Measured S-parameters and temperature differences can be seen in Fig. 1.33-1.36. As can be seen, Fig. 1.33 shows the thin (13.5 mil width) and the thick (117.5 mil width) responses in which we can spot differences of up to 5 dB above 10 GHz. Fig. 1.34 shows the Samtec Golden Standard responses in Single Ended S-parameters (although 4 ports S-parameters were measured) in which differences larger than 20 dB are noticeable above 13 GHz. Fig. 1.35 shows short (2") and long (6") transmission lines S-parameters responses in which differences of up to 10 dB are spotted above 14 GHz.

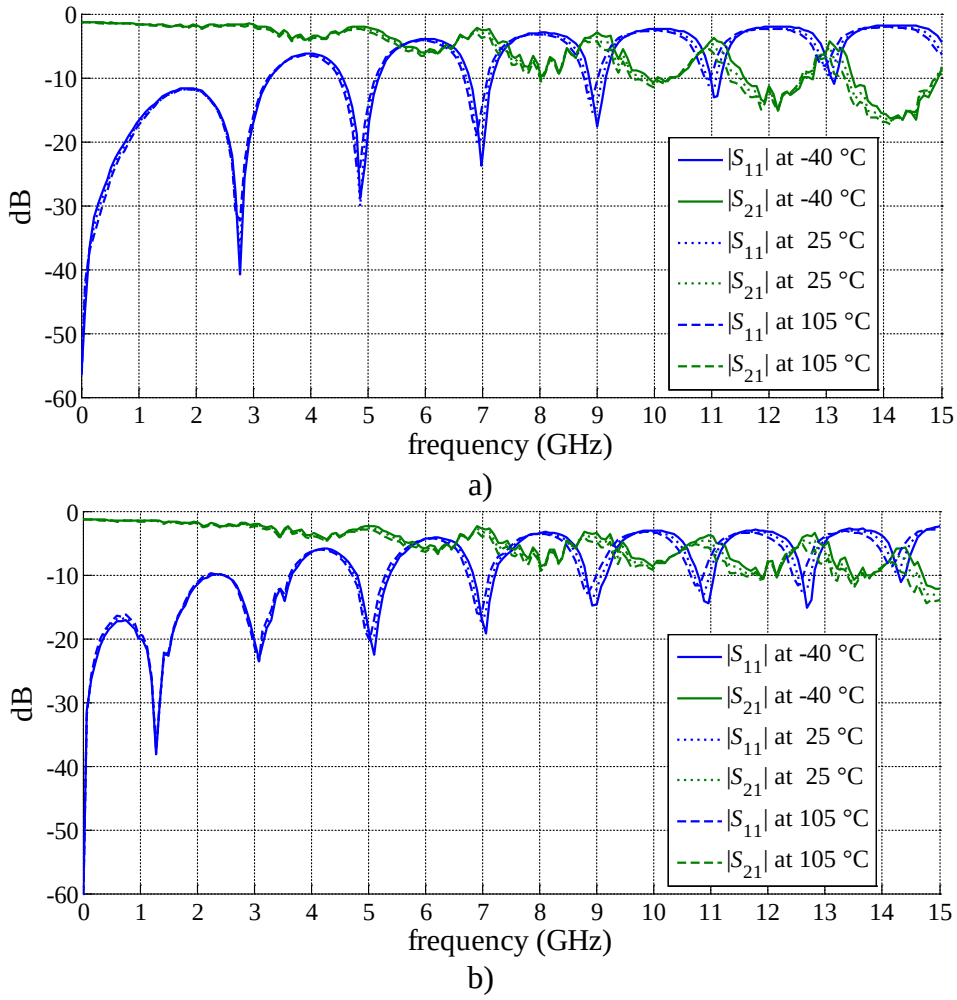


Fig. 1.33 Thin and thick TLs S-parameter responses at different temperatures: a) thin TL, b) thick TL.

Sensitivity of S-parameters to temperature is more noticeable above 3.5 GHz in most plots, especially for near-end crosstalk and far-end crosstalk, as confirmed in Fig. 1.36. It is seen that the Samtec Golden Standard, being a differential interconnect, presents the largest effects related to temperature at high frequencies on single-ended S-parameters.

Moreover, the smallest changes in insertion losses over temperature were registered with shorter and/or thinner TLs, as confirmed in Table 1.5. Conversely, the best performance for return losses over temperature was observed with thicker and/or longer TLs. Designing based on these observations must be subject to engineering criteria, since trading-off emissions and signal integrity performance is usually subject to equalization techniques available and EMC regulations.

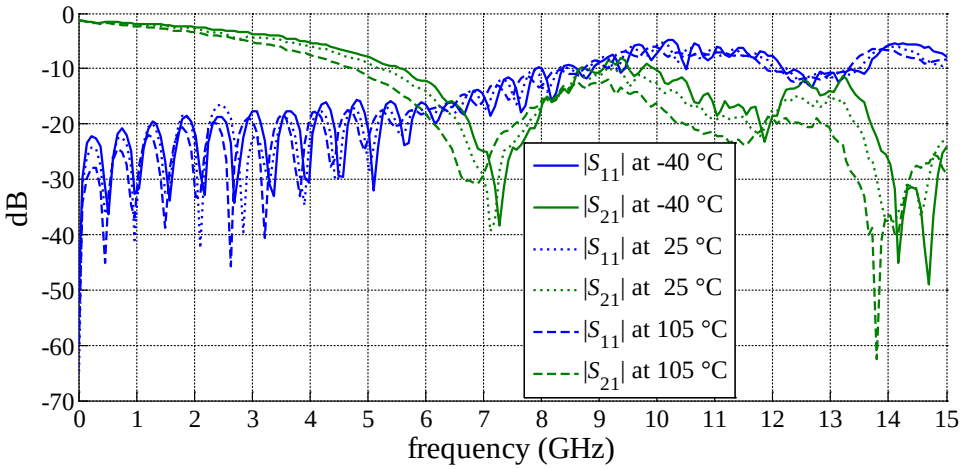


Fig. 1.34 Samtec Golden Standard S-parameter responses at different temperatures.

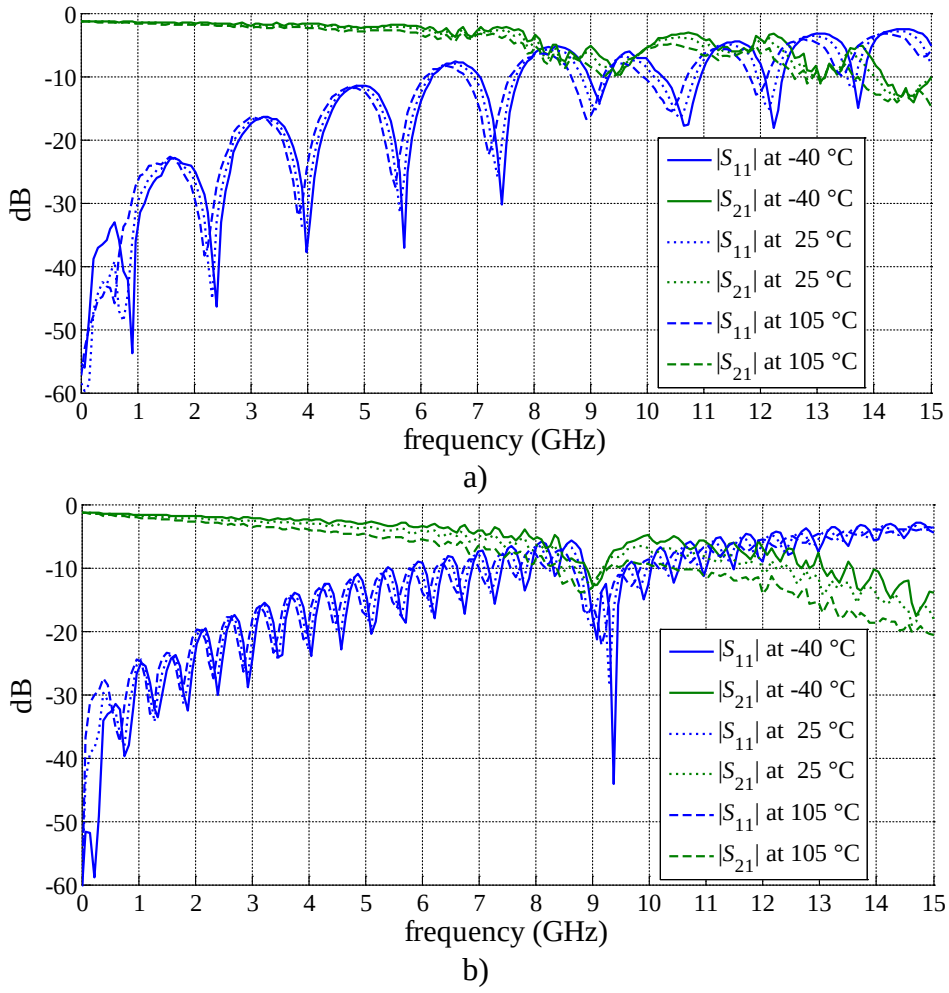


Fig. 1.35 Short and long TLs S-parameter responses at different temperatures: a) short TL, b) long TL.

TABLE 1.5. MAX CHANGE IN S-PARAMETERS (0.5 TO 15 GHZ) FROM −40 TO 105 °C

DUT	$\|S_{11}\|$ (dB)	$\|S_{21}\|$ (dB)
Thin TL	8.81	4.37
Thick TL	7.25	4.66
Short (2”) TL	19.08	5.87
Long (6”) TL	13.56	8.39
Samtec Golden Standard (SE)	22.39	40.19

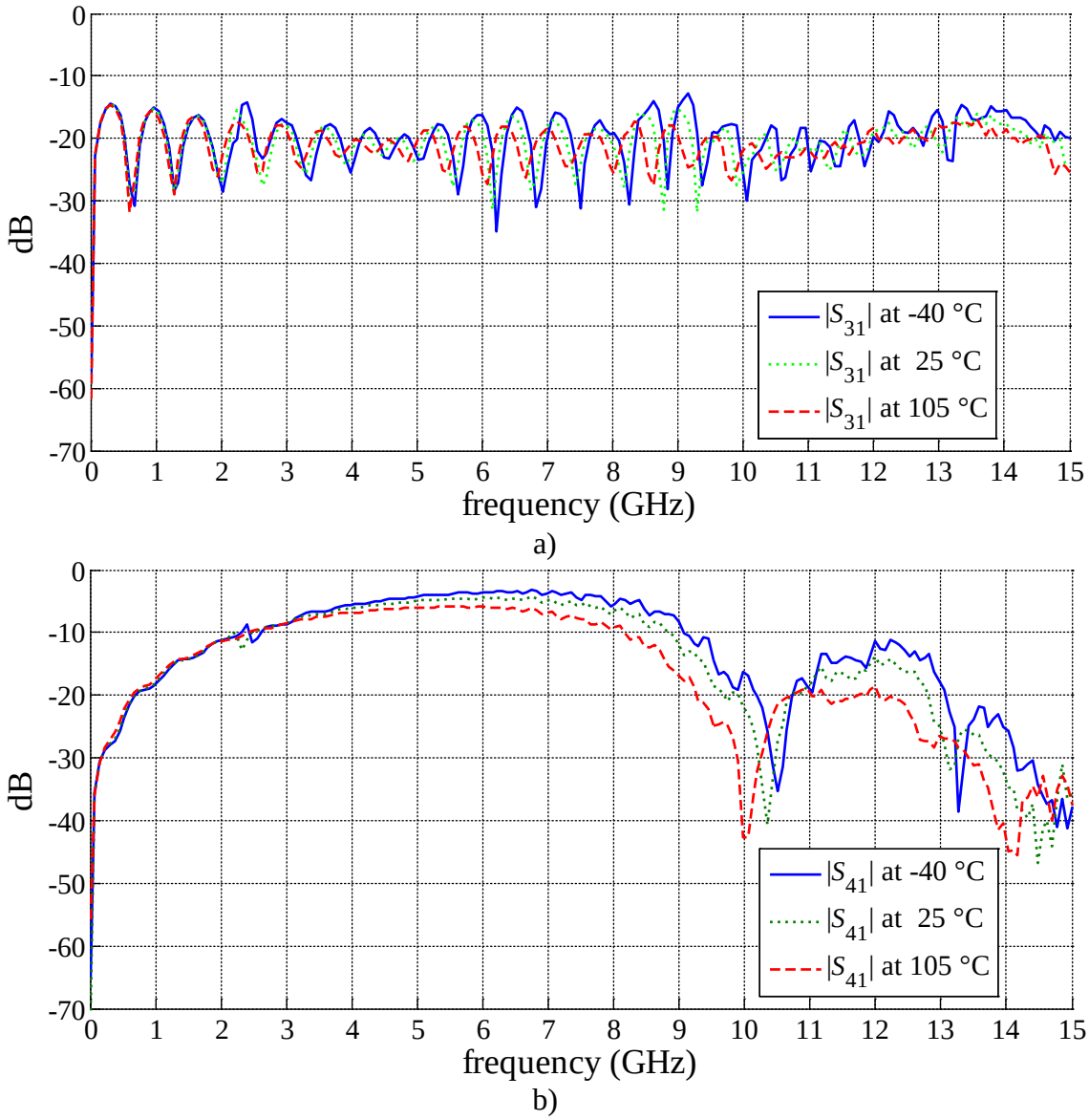


Fig. 1.36 Samtec Golden Standard S-parameter response at different temperatures; a) near-end crosstalk, b) far-end crosstalk.

1.5. Conclusions

In this Chapter, an unconventional PCB structure was proposed to achieve a USB differential pair built in an inexpensive 2-layer standard PCB laminate. In addition, The Samtec Golden Standard, used as a reference transmission line structure due to its similarities with the proposed geometry, aided to accurately model and evaluate the performance of the proposed geometry.

In order to ensure the accuracy of the EM simulation, three different CAD models of the Samtec Golden Standard were exercised, with the purpose to obtain a good compromise between accuracy and computational cost as an aid for enabling cheaper manufacturable interconnects. Models were found to behave alike the reference measurement provided, with some differences between them. Best results were obtained with Sonnet and AWR, making them good candidates for fine and coarse models respectively, which are useful for space mapping optimization. In fact, Sonnet EM simulations of the Samtec Golden Standard model were reasonably similar to measurements provided, giving a high level of confidence as a reference for the proposed transmission structure.

Correspondingly, the implemented coarse model optimization is intended to comprehend the first part of a space mapping algorithm optimization scheme such as [Bandler-04], [Bandler-94], and [Rayas-Sánchez-16], useful to reduce computational cost in more complex real industry use cases. The S-parameters responses along with EMC emissions pre-scan of the proposed geometry implemented in the Freescale Freedom platform proven its success and potential to enable more robust and cost-effective interconnects for the Internet of Things ecosystem.

Moreover, experimental measurement results indicate that current cost-effective, FR4-based PCB technology might become vulnerable above a few GHz in typical automotive temperature ranges. The coupled EM-thermal behavior observed settles the necessity of implementing multi-physics models and simulations for future automotive computing interconnects, such as in the connected car.

2. Challenges in the Connected Car Requirements from a Hardware Perspective

This Chapter outlines the requirements for the technology-driven trend of the Connected Car as a subset of the Internet of Things, which is currently acquiring more relevance towards the fully automated car in global economies. The challenges to solve these requirements are acknowledged from a hardware perspective, such as matching high-speed state-of-the-art computing against environmental automotive requirements in next-generation driver information systems, while maintaining cost effective as their legacy counterparts. In addition, several proposals are addressed for cost effective PCB interconnect schemes aimed at the connected car. Design constraints are described along with technology requirements specifically for harsh environments like automotive systems.

To give a broader overview of this automotive technological trend, the status quo of the connected car is briefly described in Section 2.1. along with a review of the legacy automotive human-machine interfaces (HMI) and the technical requirements aimed at the connected car. Subsequently, the main PCB cost drivers are portrayed in Section 2.2 together with proposals for PCB cost reduction, finalizing with some discussion and Chapter conclusions in Section 2.3 and 2.4, respectively.

2.1. The Connected Car

Due to the high importance of the connected car trend for global economies, in 2015 the IEEE Connected Vehicles Initiative was launched by the IEEE Vehicular Technology Society (VTS) to promote technical activities, networking, publications, standards, and access to technical information in connected vehicles, as connected vehicles emerge from the convergence of the three areas of interest of VTS: automotive electronics, mobile radio, and transportation systems. Connected car features fall into several categories, including safety, navigation, infotainment, diagnostics/efficiency, and payments.

During the next five years, the proportion of new vehicles equipped with these capabilities

will increase dramatically, making connected cars a major element of the IoT [Velosa-14]. By 2020, there will be quarter billion connected vehicles on the road, enabling new in-vehicle services and automated driving capabilities. Seamless integration of vehicular network, mobile devices, edge computing and storage platform pose numerous challenges, such as environmental and safety regulations, partnerships among automotive original equipment manufacturers (OEMs), telecommunication carriers, software development companies and governments, among others [Datta-16].

As an example, Tesla Motors, being the first car maker to produce high performance battery electric vehicles (BEV) in serial production [Moritz-15], set the benchmark for what the connected car could be, with the launch of the model S in 2012 [Teslarati-17]. The company is also creating strategic alliances and working by themselves on every single aspect to speed up the introduction of the self-driving vehicle. They have currently enabled inter-vehicle communication, self-navigation, diagnostics, and over-the-air software updates, among other connected car features. For instance, its Chief Executive Officer, Elon Musk, claims that the company will achieve fully autonomous driving by the end of 2019 [Electrek-17].

2.1.1 Legacy Automotive Human-Machine Interfaces

Car instrument clusters in contemporary automotive systems generally consist of a small cost-effective micro-controller unit (MCU) intended for processing sensor data from Engine Control Unit (ECU) aided with a real-time operating system (RTOS). The MCU displays this data through small actuators, such as stepper motors meant to manipulate instrumentation dials. It also drives small segmented displays and light emitting devices, such as LEDs and lightbulbs, with the purpose to light a function or warning icon. All this information is driven in the range of kHz. This data is received through a robust low speed network, such as CAN or LIN buses. For some automotive original equipment manufacturers (OEMs), the anti-theft features reside in this module, in which a dedicated immobilizer circuitry requires that the MCU supports cryptographic algorithms [Freescale-14].

Current infotainment devices mainly exert a small screen, ranging from a segmented display, up to a color liquid crystal display (LCD) not usually bigger than 7” for the information display and human machine interfaces (HMI) interaction. Functions like global positioning

systems (GPS), radio and audio or even video playback are found in these devices. In some cases, this module connects to the instrumentation cluster to retrieve a few car parameters, such as tire pressure monitoring and lighting functions and to playback alert chimes such as door open and hazard lights (see Fig. 2.1). Infotainment devices are not required to withstand uninterrupted operation and because of that, RTOS usage is not typical.

To reach cost targets, both applications are usually fulfilled with a 16-bit MCUs and lately with low-end 32-bit MCUs. This is mainly because 8-bit and 16-bit MCUs started end of life in 2010. In the case of the infotainment devices, external memories are required for multimedia playback, but exerting legacy buses such as SDRAM and DDR with speeds below 200 MHz.

2.1.2 Technical Requirements for The Connected Car

One of the reasons today's cars do not have cutting edge technology found in high-end mobile phones or high-performance computers is that automotive electronics have far more

Fig. 2.1 Legacy automotive HMI: Touchscreen infotainment system from 1989 Oldsmobile Toronado Trofeo, called the Visual Information Center (VIC). The touchscreen was powered by a pair of 8-bit processors and gave the driver access to everything from the radio to engine management data. From [Business Insider-17].

rigorous size and power constraints, as well as mission-critical operating requirements than most electronics applications [Sheth-07]. Safety regulations require non-stop operation to several car components, such as headlamps, anti-lock braking systems (ABS), and hazard information to the driver. For this reason, standards developing associations, such as society of automotive engineers (SAE), require passing tough environmental and electromagnetic compatibility tests to ensure years of continuous operation in extreme weather conditions[14].

Typically, a connected car has a head-unit which performs the main computing processing, an infotainment unit to display vehicle passenger's comfort functions and navigation information, an in-dash system which displays the main driver information and vehicle data (see Fig. 2.2). The constant increase in usage of digital content within the vehicle, along with more sophisticated navigation and automated driving functions, is driving the need for more sophisticated infotainment systems.

Fig. 2.2 State of the art connected car systems: fully integrated head unit, infotainment unit, and in-dash system. From [Continental-15]-

[14] SAE International. Testing standards. Dec. 5, 2017, http://topics.sae.org/tests-and-testing/standards/automotive/.

Fig. 2.3 The need for more sophisticated infotainment systems creates new opportunities for different players onscreen and under the hood. From [Lochbridge-17].

Faster, more capable and multi-core application processors are required, along with dedicated graphics accelerators and image processing devices, multiple radars and lidars, bigger displays and novel human-machine interface technologies, such as head tracking [Velosa-14], as illustrated in Fig. 2.3. High-end computing buses like DDR3 and DDR4 memory interfaces, LVDS display interface and Gigabit Ethernet, whose frequencies work in the gigahertz range with rise times of a few tenths of picoseconds [JEDEC Sd JESD79-4A], are now part of these connected car head units, which should withstand the automotive environmental robustness standards while maintaining cost effective. Jumping into these technologies entails handling microwave theory and impedance matching techniques, EM model simulations, electromagnetic interference and compatibility, among others, as discussed in Chapter 1.

Cost effectiveness is required not only to hit the high competition in the market or to increase profit while providing more competitive products to a broader population, but also to decrease the energy required for production and thus contribute to reduce the carbon footprint. For this, any cost optimization techniques and design to cost (DTC) strategies are highly demanded. Reducing waste by increasing yield, reducing either the amount of raw materials, the design's bill of materials (BOM) cost, or the amount of processing steps through advanced calculations, are all becoming essential.

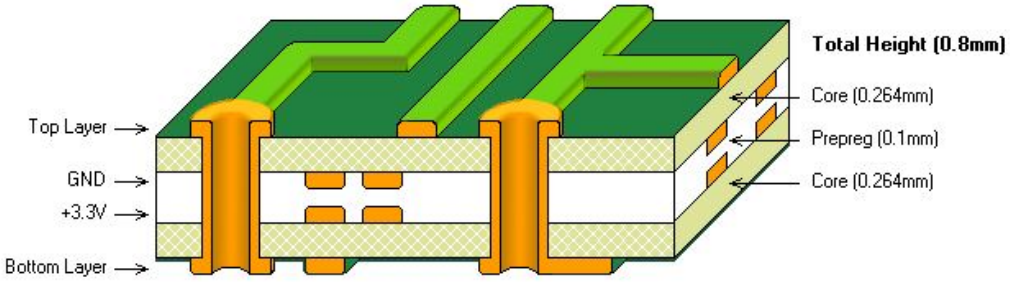


Fig. 2.4 Standard PCB stack-up. Image depicts a four layer PCB. From [Stack Exchange-15].

2.2. Cost Reduction Approaches for Systems Requiring High-Speed High-Density PCB Interconnects

An HDI PCB is characterized by its high density of components and routing interconnections that use the latest PCB technologies [Sierra Circuits-16]. Multiple manufacturing process steps are added in comparison to a standard PCB, as shown in Fig. 2.4, allowing for more complex via technologies, such as via in pad, stacked, blind, and buried vias. This allows designers to harness more PCB real estate to place components even closer together [Epec-16]. An HDI PCB stack up can be seen in Fig. 2.5. On the other hand, a PCB needs to be designed for the best cost-to-performance ratio possible, since the finished product in which the PCB is installed must meet a price point that compares favorably against competing products [Wright-15], and HDI technology can increase the cost up to 200% due to the increased number of manufacturing process steps.

When dealing with semiconductor technology smaller than 45 nm, currently required for computing in the connecter car, the high number of transistors present on-die along with fast switching times demand a big amount of energy supplied immediately. Henceforth, the inductance in the path from the power supply to the load at silicon pin needs to be as low as possible. To counteract this inductance, critical capacitor arrangements are needed on-board as close as possible to silicon in order to provide enough energy to supply the worst demand case of the circuitry.

These filter arrangements in the power distribution network must be located as close as $1/6^{th}$ of the transition time wavelength to the silicon power supply pins [Freescale-10]. For instance, in current 32 nm HCMOS technology, the rise time is equivalent to 110 picoseconds

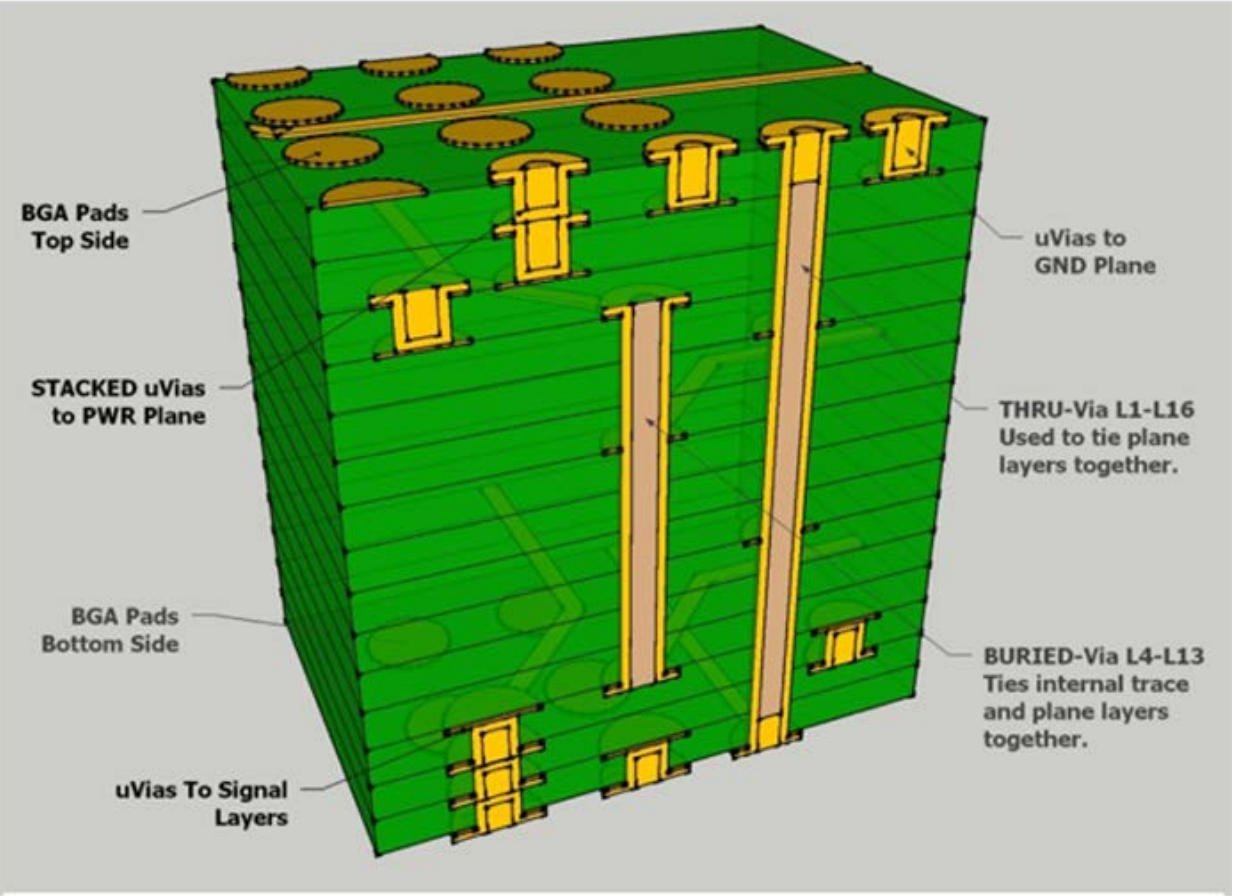


Fig. 2.5 Typical construction of an HDI PCB stack-up. Image depicts a 16 layer PCB. From [Optimum D. A.-17].

[Puttagunta-11]. Hence, decoupling capacitors should be located at a maximum of 5.5 mm to the chip interconnect. This often leads to employ state-of-the-art component structures by using different substrate materials with much higher dielectric properties than FR4, or to place some of these capacitors on the secondary PCB side directly under chip location, the so-called inside board design team' jargon "premium real state" due to the limited amount of space available.

In Chapter 1, several analysis and design efforts are applied to enable a PCB based high-speed interface with the lowest possible number of conductive layers. This is achieved by calculating the best impedance matching with the inclusion of optimization algorithms over EM simulations. When using BGA technology, the array nature of such geometry often makes impossible to implement such layer count by fully breaking out signal pins. Fig. 2.6 shows a sample routing scheme. PCB-conductive layer count can be estimated by

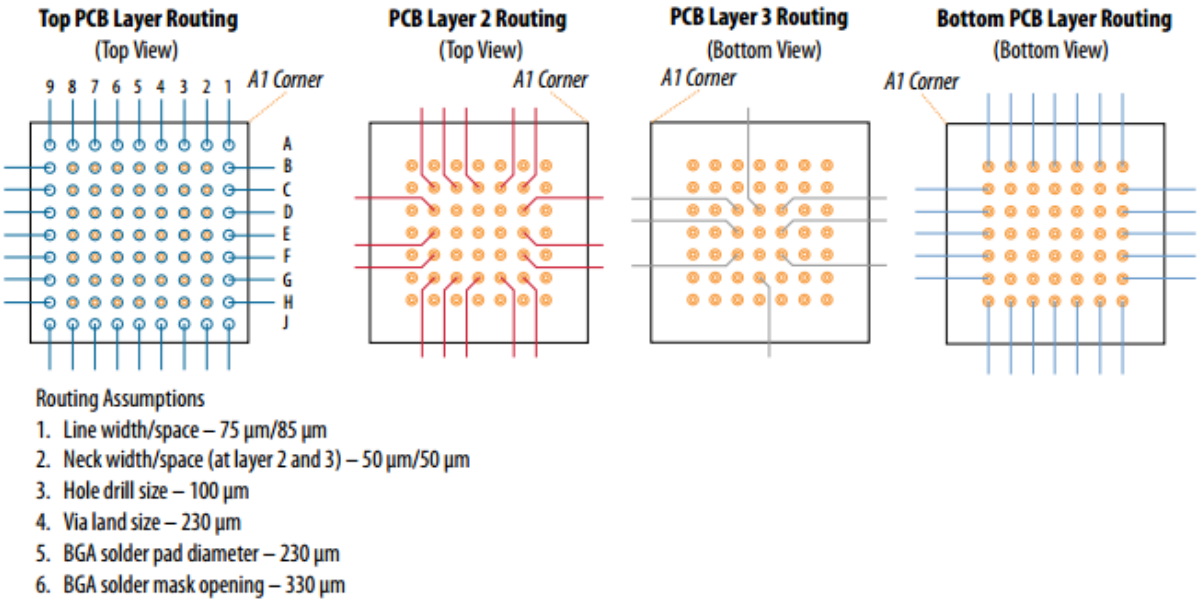


Fig. 2.6 A sample PCB routing scheme on 4 layers for 0.4-mm 81-pin VBGA. From [Intel-17].

$$Layers = \frac{Signals}{RoutingChannels * RoutesPerChannel} \tag{2-1}$$

Routing channels are given by the BGA number of rows and columns, and the routes per channel are usually the best compromise of manufacturing capabilities (i.e. tighter conductive traces) against BGA pitch [Xilinx-16]. In particular, for BGA pitches smaller than 0.65 mm, sometimes not even one route per channel is possible, as shown in Fig. 2.7, forcefully requiring the usage of HDI technologies to remove inner layer contacts [Würth Elektronik-14].

2.2.1 PCB Cost Drivers

The base for each PCB design lies on the IPC – Association Connecting Electronic Industries standards: IPC-2220 – IPC-2226 [FineLine-17]. In general, cost drivers in a PCB are directly proportional to the amount of processing steps in its manufacture, the production time, the degree of accuracy, and the final manufacturing yield, which is dependent of all of the above. There are several cost-contributing factors, such as the size of a single unit, the usage of expensive surface treatment materials like thick gold, the material utilization and amount of waste, and the material selection [NCAB Group-15]. They can be classified from major to minor cost drivers.

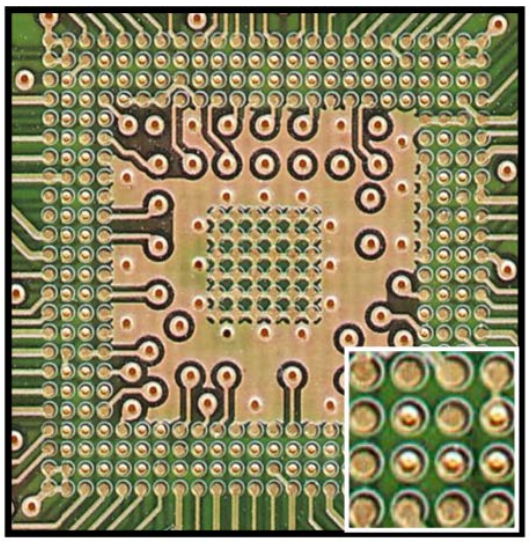


Fig. 2.7 Example of a 0.50 mm pitch BGA routing in which traces between pads are impossible. From [Würth Elektronik-13].

2.2.1.1 Major Cost Drivers

PCB size/raw materials usage, layer count, build complexity, material choices, effective utilization of material, and yield, are among the major cost drivers. The amount of raw materials required due to PCB size and features becomes critical in high-volume production, up to the point that any single small feature that can be avoided turns into a significant cost reduction factor, such as the amount of metal added for a specific feature.

For the layer count, increasing the number of layers means more production steps, such as: developing, etching, and automated optical inspection (AOI) for each layer. Care must be taken with the cost increase for each pair of layers, as depicted in Fig. 2.8. In contrast, if reduction of layer count is achieved by means of more complex technology such as HDI, reduction of layer count does not always decrease cost.

Build complexity is one of the largest “hard cost” drivers, due to the increased processing steps, specially where the manufacturing process holds several bond and drill cycles [Cirtech EDA-15]. For example, HDI features such as blind and buried vias increases the processing steps from a 6-layer standard PCB stack up that requires only 1 drilling operation, 1 plating cycle, and 1 bond cycle, as shown in Fig. 2.9, to at least 3 mechanical and 4 laser drilling operations, 3 plating cycles and 3 bond cycles, as depicted in Fig. 2.10. The amount of processing steps increase depending on the amount of via levels required, as portrayed in Fig. 2.11.

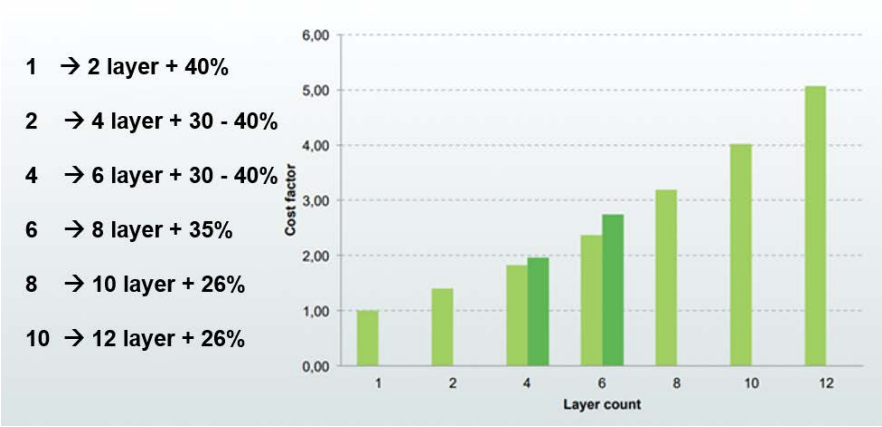


Fig. 2.8 Cost rate increments of a multilayer PCB. From [NCAB Group-15].

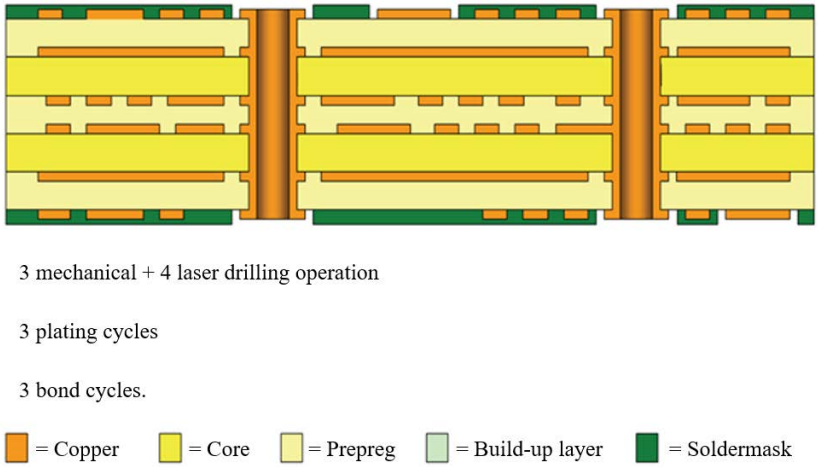


Fig. 2.9 6-layer standard PCB stack-up which needs only 1 drilling operation, 1 plating cycle and 1 bond cycle. From [NCAB Group-15].

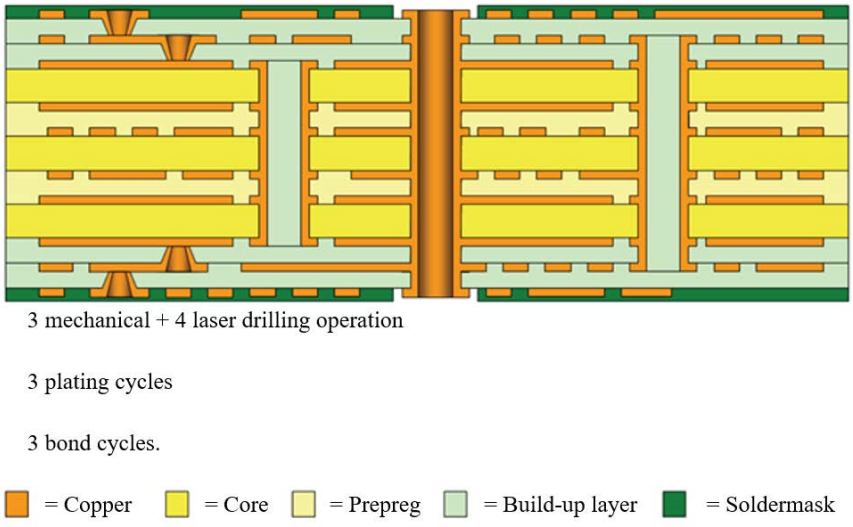


Fig. 2.10 10-layer HDI PCB stack-up. From [NCAB Group-15].

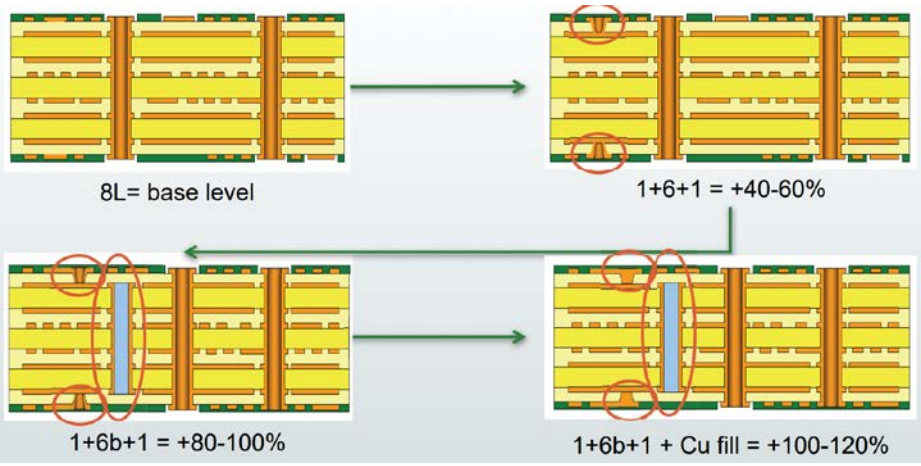


Fig. 2.11 Processing steps comparison from 8-layer base level PCB to the addition of HDI blind and buried vias. Percentages represent cost increments. From [NCAB Group-15].

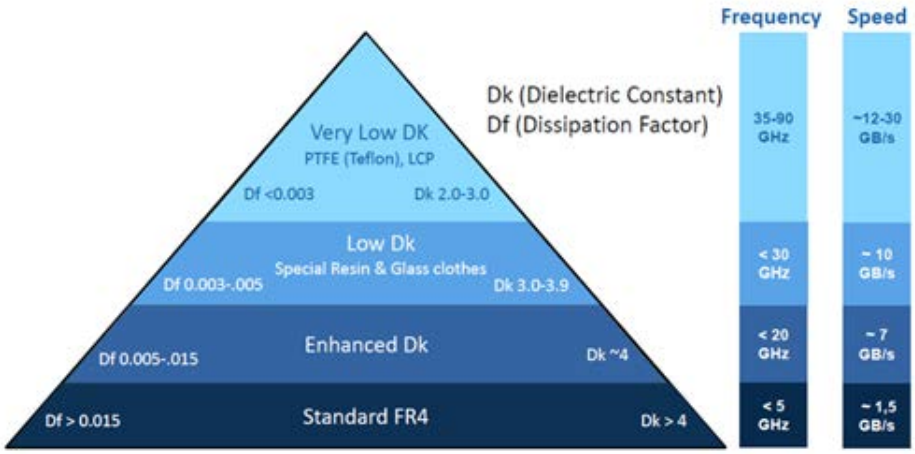


Fig. 2.12 PCB substrate laminates available for the electronics industry and their performance comparison. From [FineLine-17].

Moreover, exotic materials result in exotic pricing. Best EM performance can be easily attained with peculiar, very homogeneous materials such as ceramic compounds, which cost is often four or five times higher than standard FR4 per square metre [MA Business-11]. Fig. 2.12 shows a comparison between PCB substrate laminates and their performance; the higher the frequency the more important is the choice of materials. A list of them can be seen in Table 2.1. Nevertheless, similar performance can be achieved with less expensive materials through usage of optimization techniques in the impedance geometry [del-Rey-14a].

TABLE 2.1. PCB SUBSTRATE LAMINATES AVAILABLE FOR THE ELECTRONICS INDUSTRY. FROM [FINELINE-17].

Material Group	Manufacturer/Type	Cost Factor
Phenolic FR4	ITEQ 180A	1
High speed / mid low loss	ITEQ 200LK	1.2
High speed / mid low loss	Nelco 4000-13 EP	1.3
High speed / low loss	Nelco 4000-13 EPSI	3
High speed / low loss	ITEQ 968	3.5
High speed / low loss	Panasonic Megtron 6	4
Polymide	Nelco N7000-2	3
High frequency	Arlon 25N	4
High frequency	Rogers 4350B, RO4003	5
BT packaging substrate	Nelco N5000-32	3
PTFE based microwave materials	Rogers 3000, 5000, 6000	10-50

2.2.1.2 Medium Cost Drivers

Most medium cost drivers are equipment dependent and is therefore specific to the manufacturer. For instance, smaller track widths and the gap distances need a technology shift in precision machinery and thus increase the cost, as shown in Fig. 2.13. The same happens with tight tolerances, which at certain point will result in a decrease of the manufacturing yield.

The amount of holes and their sizes are the next cost driver. Smaller drill bits have shorter flute length which limits the number of boards that can be drilled in one stack. Additionally, each hole increases the processing time. Plating thickness also increases processing time, and the cost per gram of the metal being plated. For instance, prices of both metals, copper, and gold, have been rising since the past decades. Lastly, the necessity of controlled impedance increases the number of process steps and material waste by creating a test impedance pattern, also called test coupon, meant for measuring the finished impedance. Examples of impedance test coupons are shown in Fig. 2.14. All PCBs that are not compliant with the target impedance are trashed, decreasing the manufacturing yield.

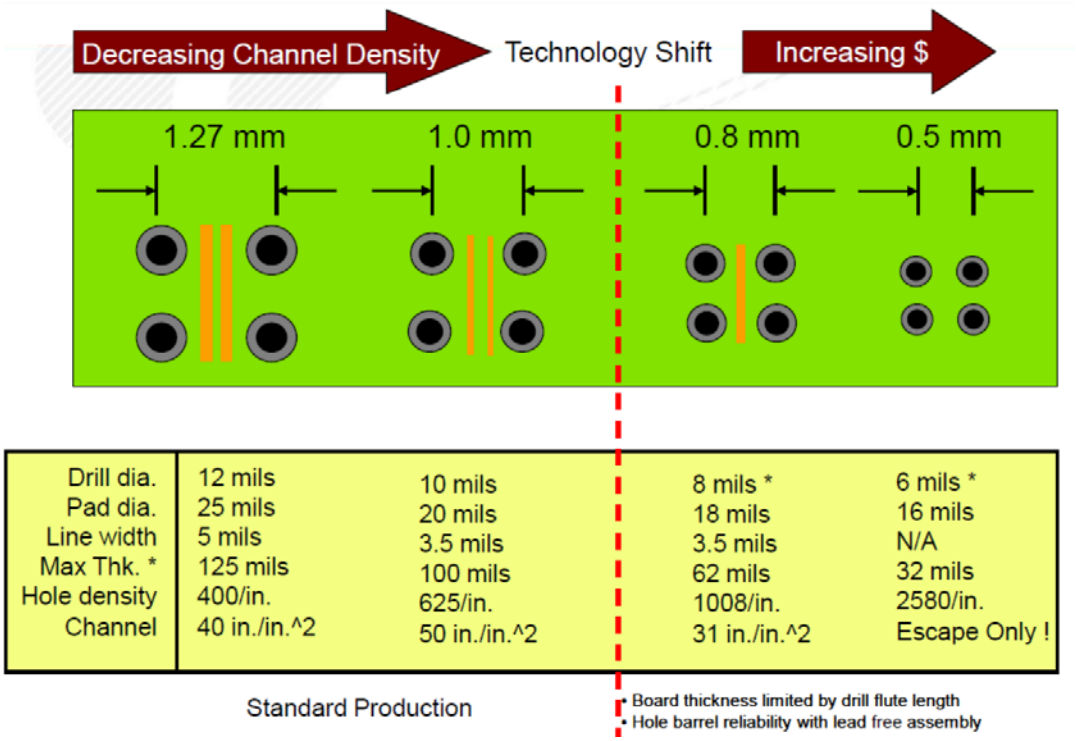


Fig. 2.13 Relationship between precision increment in technology shift for track and gap. From [FineLine-17].

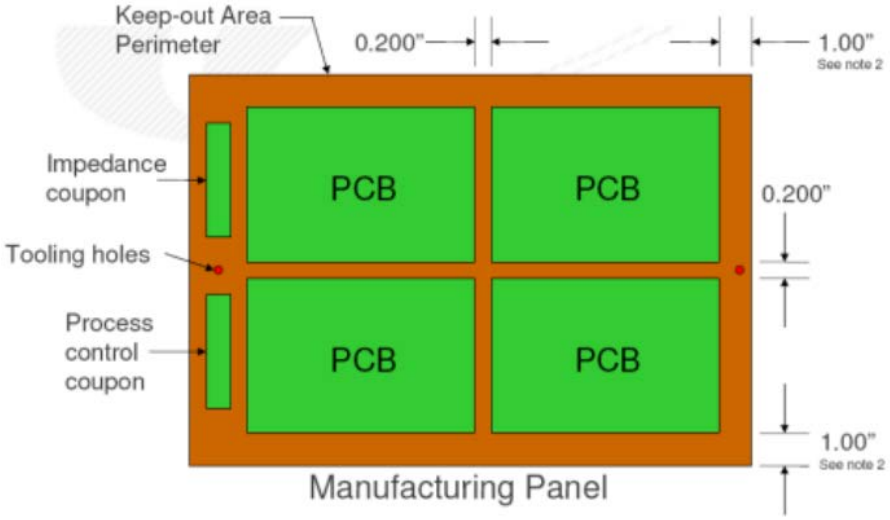


Fig. 2.14 Impedance test coupons examples for a PCB panel. From [FineLine-17].

TABLE 2.2. SURFACE TREATMENTS. FROM [FINELINE-17]

Finish	Shelf life time
HASL	12
Immersion Au	12
ENIG	12
Immersion Ag	2.5 – 3
Immersion Sn	1.5 – 2.5
Organic OSP	2 – 3

2.2.1.3 Minor Cost Drivers

The finishing of the PCB such as the surface treatments, contour of the PCB, printed legends, are features that represent the minor cost drivers. They are usually not crucial. For instance, surface treatments determine the shelf life of an unassembled PCB as portrayed in Table 2.2. Demanding PCB shapes also increases the processing time. Printed legends add an extra processing step, but not having them make the assembly error prone.

2.2.2 Proposals for PCB Cost Reduction

There are several technical opportunities for PCB cost reduction. Many of them are currently common industry practices. This work is focusing in the non-trivial ones that can be achieved through deep EM understanding and modeling, including the impedance control, layer count reduction, and board to board interconnects.

2.2.2.1 Impedance Control

Impedance requirements have been present in digital computing since clock speeds increased dramatically in early 1990s. Impedance controlled PCBs surged as a requirement to fulfill such speeds [MA Business-11].

However, as stated in Section 2.2.1, this requires designing and plotting an additional impedance test coupon for each single PCB panel, wasting extra finished PCB material and requiring to perform a TDR measurement for each test coupon. Subsequently, accurate TDR

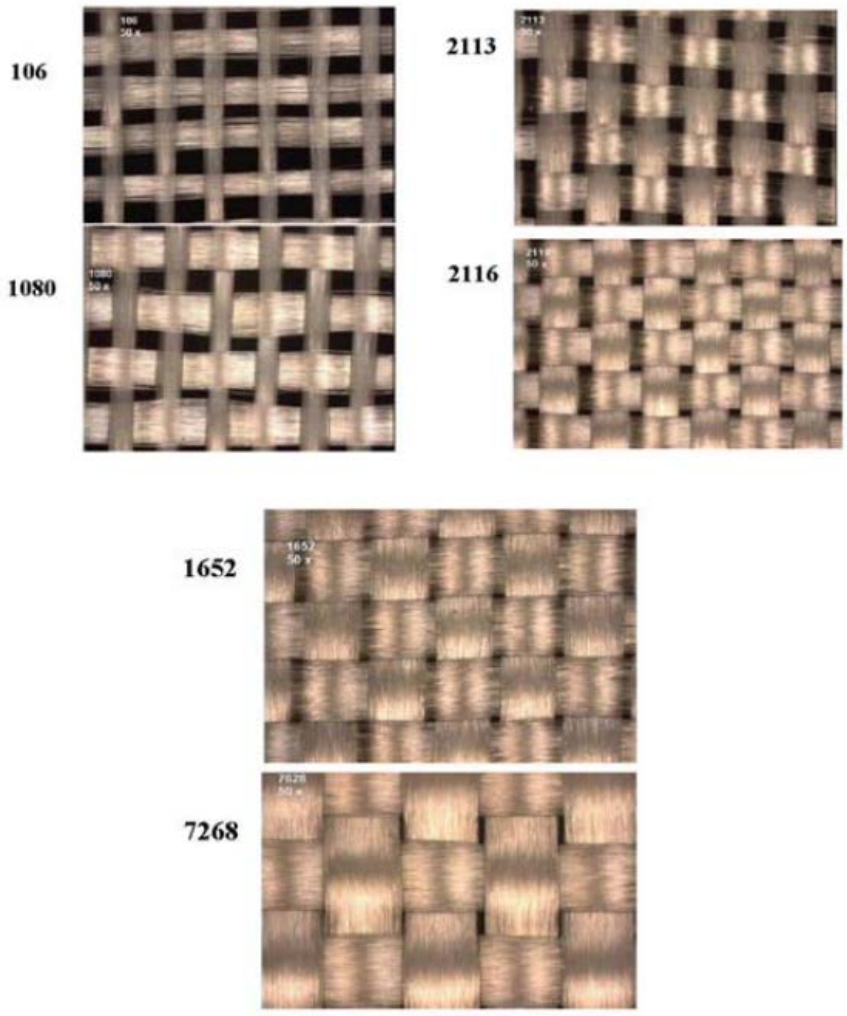


Fig. 2.15 Different fiber glass fabric categories. From [Isola-11].

measurements are not trivial and errors might represent a big risk for the PCB manufacturers, since in case of an error, they will have to reimburse for the failing PCBs, the bill of materials (BOM) and logistics expenses. The extra charge for controlled impedance can be up to 20% more for each PCB piece.

An alternative that PCB manufacturers have been doing for years for the automotive industry is called “calculated impedance”. This is done by calculating the theoretic impedance given by the materials properties and the PCB stackup dimensions, which is usually performed with an EM field solver. No test coupon is added. In order to ensure reproducibility, the PCB manufacturer takes a cross-section measurement of a finished PCB stackup every few samples, and correlates with the dimensions specified in the PCB stackup specification.

Due to the anisotropic nature of more popular dielectrics used in the electronics industry, this statistically-controlled alternative gives a much broader deviation than the controlled impedance process, but it is quite acceptable for less demanding impedance requirements, such as allowing for a 10 to 15% tolerance. However, if the design or the quality control need to reduce this tolerance, the chosen alternative in the automotive industry is to spend more in the use of some more homogeneous materials, such as the Nelco or Rogers' alternatives listed in Table 2.1.

Nonetheless, cheaper and more rugose substrate materials, such as low-grade FR4 woven glass fabric 106 (see Fig. 2.15), or even composite epoxy material (CEM), can be successfully employed by proposing more stable geometries through an optimization of the planar structure that controls the geometry. This is achieved through several simulations of an EM model of the design under test, as described in [del-Rey-15] and Section 1.2, which are conducted by a well suited optimization technique, as presented in Section 1.3.

2.2.2.2 Layer Count

According to [Würth Elektronik-14], HDI technologies can niftily reduce layer count, and for some cases, they might be the best fit. Nevertheless, care must be taken to evaluate the whole solution since there are more cost drivers involved, as stated in Section 2.2.1. For next-generation automotive designs, very high speed buses must coexist with very low-speed signals in relatively big extents as compared to mobile electronics.

For instance, due to mechanical features like precision instrumentation dials for speed and revolutions per minute (RPMs), automotive instrument clusters can measure up to 350 × 140 mm. An example of an automotive instrument cluster of these dimensions can be seen in Fig. 2.16. For infotainment devices, high-speed wireless communications are in high demand, such as long-term evolution modems (LTE) along with 4k display resolutions.

In order to enable high video resolutions (HD), such as full HD for instrument clusters or 4k for infotainment devices, fast multi-core processors are chosen which are usually designed for mobile markets. These processors have packages with 20 × 20 pins in average, and a pin-to-pin pitch in the range of 0.5 mm to 0.8 mm. For this reason, multilayer PCBs are required, and most of the time also HDI.

These requirements can represent up to 30% of the total product cost. Additionally, due to the average sizes of automotive instrument cluster applications, an HDI or a high layer count PCB

Fig. 2.16 Example of a full size automotive instrument cluster with mechanical and digital features. From [Gunaxin Media-17].

becomes prohibitive. Some alternatives to reduce layer count includes optimizing the power integrity through EM simulations, control carefully the high-speed signals' return path by using a mixture of stripline, microstrip, and coplanar transmission lines. All of them can be performed before manufacturing through EM models and virtual prototyping. Lastly, exploring board to board applications can improve the layer count per area usage by stacking the entire system with several different sized PCBs optimized for the required cost-performance.

2.2.2.3 Board to Board Applications

Board to board applications can wittily enhance the area usage per technology, such as applying HDI to the minimum necessary in a standalone PCB. These applications can be achieved through mechanical mating connectors, board to connector, or even conductor to conductor interconnects, such as direct metal to metal traces' attachments, carbon prints, conductive glue, solder-made interconnects, and soldered ball interconnects. System in package (SiP) technology relies in the last one to allow for a repeatable manufacturing process.

Impedance matching problems associated with use of mechanical connectors for connecting conductive traces are known [Handforth-01]. If the connector chosen is not designed for high frequency signals, their structures can contribute to problems such as impedance mismatches and cross-talk to adjacent signal layers. The extent of the problem depends upon the type of connector used and related size and material characteristics. When evaluating dedicated

TABLE 2.3. AEC AUTOMOTIVE TEMPERATURE GRADES. FROM [HANDFORTH-01]

Grade	Temperature Range	Typical Application
0	–50 to +150°C	All automotive
1	–40 to +125°C	Most under hood
2	–40 to +105°C	Passenger compartment hotspots
3	–40 to +85°C	Most passenger compartment
4	0 to +70°C	Non-automotive

high frequency connectors in the automotive industry, the reliability of the connector, the higher difficulty to control the system's EM emissions, or even the increase in cost can become significant to forsake the decision.

Connector-less board to board interconnects are preferred options for the automotive, but there is not yet a good tradeoff between environmental and manufacturing robustness, and the capability to withstand high frequency signals. BGA SiP interconnects are currently the closest alternative, being capable of stacking logic and giga-bit class memory into a single package [EE Times-07], but long term thermal and mechanical reliability is still a known cause of failure.

Nevertheless, board-to-board applications do not currently have a broad usage in the automotive industry due to the diminished reliability of the state of the art solutions, as compared to a non-board-to-board application. This is completely dependent on the attaching method and sizes of the boards due to physical materials' behavior to temperature changes and vibration found in the automotive environment. High-end high-speed connectors and SiP applications present a limited solution since their implementation is not always cost effective, nor reliable, nor EMC friendly. For this reason, there is a fantastic opportunity in enhancing the reliability of a high density, cost-effective SiP towards the connected car.

2.3. Discussion

Since the early 1990s, with the rise in consumer electronics, automotive companies were no longer the biggest priority for component suppliers [Lawrie-15]. Recognition of this is given to the fact that temperature and vibration conditions in automobiles can vary greatly, with the most

TABLE 2.4. STRUCTURE OF AUTOMOTIVE INDUSTRY. FROM [HEARST-NEWSPAPERS-17]

Product Supplier	Supply chain description
Original equipment manufacturer (OEM)	Company that makes the final product for the consumer marketplace, e. g., Ford Motor Company, BMW AG
Tier-1	Direct parts and systems suppliers to OEMs, e. g., Continental AG, Denso Corp.
Tier-2	Key suppliers to tier one suppliers such as component suppliers
Tier-3	Raw materials suppliers to higher-tier suppliers
Aftermarket	Automotive solutions suppliers direct to customer, not directly involved in the supply chain

demanding locations being in the engine, transmission, and brake systems [Slovick-14]. Temperature ratings required by the automotive industry through the Automotive Electronics Council (AEC) grades, as shown in Table 2.3, are not common requirements for the most predominant silicon market, e. g., mobile computing. Therefore, silicon makers are rarely focused in performing a complete set of environmental tests in the whole automotive system, beyond sole AEC requirements for standalone integrated circuit (IC) package, leaving this burden to the automotive OEMs and their system suppliers, also called Tier-1 manufacturers (see Table 2.4) [15].

Due to high competition in automotive industry, Tier-1 manufacturers usually have a commitment to lower manufacturing prices every year and run through a design-to-cost process. For this reason, cost effective alternatives should be considered during the system architecture definition. Additionally, as stated in Section 2.2.2, car instrument clusters used to be mostly digital electromechanical devices with low computing complexity. Hence, substrates like flame retardant glass-reinforced epoxy laminate (FR4) have been considered even too expensive for decades in this area of applications, and cheap laminates like composite epoxy material (CEM) were prevalent for these applications.

For instance, NEMA [16] grade CEM-1 laminates are composed of a cellulose paper core, sandwiched between two layer/piles of continuous woven glass fabric, infiltrated with a flame-

[15] Continental Automotive GmbH, internal information. Jan 5, 2015 Hannover, Germany.
[16] The Association of Electrical Equipment and Medical Imaging Manufacturers, All standards. Jul. 14, 2015. https://www.nema.org/Standards/Pages/All-Standards.aspx

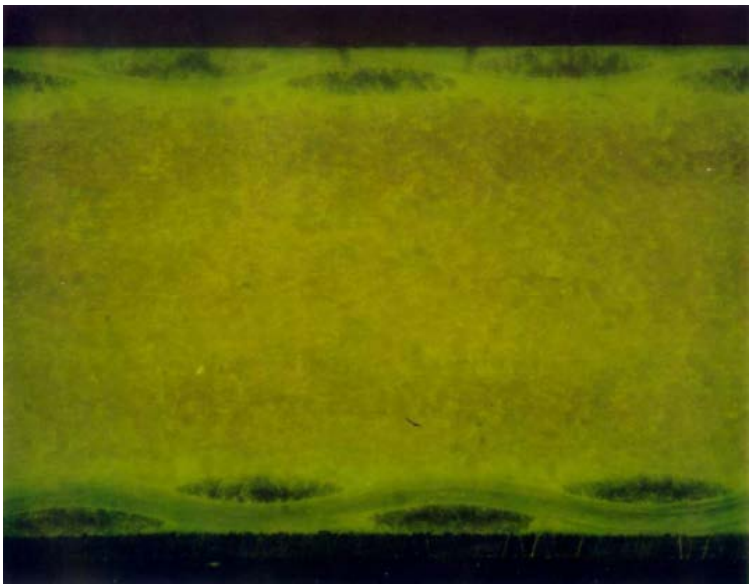


Fig. 2.17 Optical cross-sectional view of a CEM substrate showing the inner core sandwiched by resin-filled woven glass fibers. From [DFR Solutions-11].

resistant epoxy resin binder, as illustrated in Fig. 2.17. NEMA grade CEM-3 laminates are similar, but with a chopped glass fiber core [DFR Solutions-11]. Due to the higher ruggedness than FR4 of CEM woven fabrics, their coefficient of thermal expansion (CTE) and stiffness against temperatures and humidity, CEM laminates are not suited for high-performance/high-speed circuitry required by state of the art computing, forcing to jump into FR4 and better performing laminates and setting the need for applying different techniques for cost reductions.

Also, due to legacy designs' conventions and low-cost orientation, precise impedance control required by state of the art computing is never take into budget. Designers make a big effort to calculate and predict a good yield without having any control in the PCB manufacturing process. This situation is a fantastic opportunity to introduce optimization techniques to find interconnect geometries with lower sensibility to relatively large manufacturing and materials' tolerances.

The list of significant PCB price drivers is not small. However, very few price drivers can be tweaked for an automotive application. Nevertheless, a very significant part of the final PCB cost can be saved with these few remaining price drivers, such as the impedance control, the layer optimization and specially, the area optimization through a board to board application since this one removes a direct raw material usage.

2.4. Conclusion

With the advent of the so called connected car as the next frontier for Internet of Things based platforms and services, the potential of providing a more efficient and sustainable transportation systems that increases safety and minimizes the impact on the environment is attracting interest from governments in the entire world, starting comprehensively with the European Union Commission. The connected car is so important that the IEEE Vehicular Technology Society launched the Connected Vehicle initiative in 2015 to promote technical activities and standards.

This trend is driving the need for more sophisticated infotainment systems and instrumentation clusters, requiring high end computing hardware with interfaces that communicate in the gigabit range that should withstand the automotive environmental robustness standards while maintaining cost effective. For this reason, to achieve similar costs as legacy in-dash systems like today's instrument clusters, there is a large opportunity to introduce optimization techniques to find interconnect geometries with lower sensibilities to geometry fluctuations due to tolerances and material properties.

High-performance upcoming semiconductor technologies are driving a need to increase the interconnection density. This is currently solved at a reasonable cost with the inclusion of HDI technology for non-critical applications, such as mobile phones and consumer electronics, or by switching to more exotic materials in high performance computing and telecommunications industries.

For the automotive industry, with the imminent need to fulfill the connected car requirements, different approaches must be taken for keeping the current low-cost and robustness of low-end computing systems currently in use. To satisfy the faster rise times and the smaller but at the same time denser IC package pin-to-pin pitch of forthcoming semiconductor generations, their power distribution network and EM performance should be optimized with the same robustness and reliability of current automotive systems, at a reasonable price.

3. Board to Board Interconnecting Technologies Intended for Advanced Automotive Electronics

As the connected car evolves, keeping the automotive industry cost-effective is required for seamless customers' adoption. This Chapter addresses in general terms some of the most relevant cost optimization goals in the electronics automotive industry in Section 3.1, as well as several board to board interconnecting technology solutions focused on solving these cost optimization goals, with the criteria needed by the automotive industry towards the connected car scenario.

Additionally, Section 3.2 presents a benchmark between three different connectorless board to board interconnects: via castellation or post stamp, ball grid array, and land grid array. Thermal and mechanical robustness tests are performed to all of the interconnects. This comparison is intended to identify the best concept and use cases for each one of them in the automotive electronics.

Moreover, Section 3.3 evaluates common solder balling technologies for board to board and system in package applications envisioned for automotive systems. In it, several options are presented, along with a comparison of their performance in the automotive electronics environment.

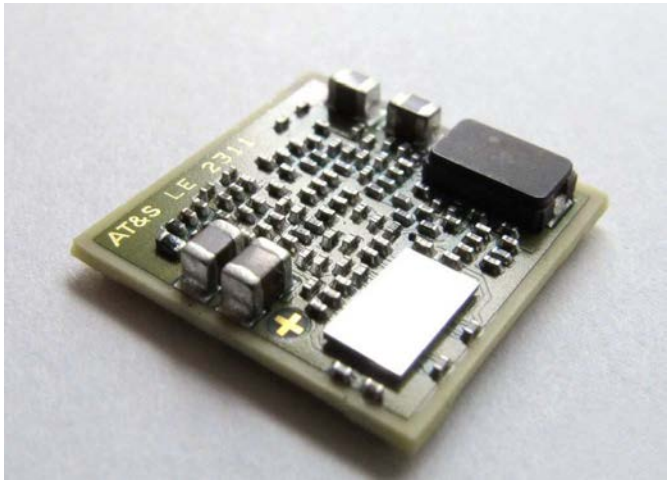


Fig. 3.1 Complete electrical modules ready for attachment to a system application board. From [Seitz-15].

Fig. 3.2 Board to board concept. An automotive application board hosts different system in packages (SiP) for specific functions.

3.1. An Overview of Board to Board Interconnecting Technologies for the Advanced Automotive Industry

This section focuses on describing the criteria for applying board to board interconnecting technologies in the automotive industry, as one of these cost reduction approaches described in Section 2.2, being highly relevant since it targets one of the most expensive components in the system: the printed circuit board (PCB).

3.1.1 Cost Optimization Goals

One of the most crucial goals for an automotive manufacturer to reach the connected car ecosystem is the time to market. This is mainly due to the development of new technologies and processes to fulfill this trend in a holistic way. To speed up the time to market, the time invested for research and development must be harnessed to the fullest.

For instance, high-speed development associated with state-of-the-art computing is cost intensive. Nevertheless, by using the board-to-board (B2B) concept, variants on an electrical design required to satisfy a broad range of vehicle models and production options can share these costs by reusing fully tested electrical modules, developed only once as standalone components of the system [Wolf-14], such as the module shown in Fig. 3.1.

Additionally, the very same product can switch between low, mid, and premium trims by standardizing the B2B module interconnects. Hence, a different microprocessor module can be attached to a single application board or mainboard unit that encloses the electromechanical

Fig. 3.3 Complete microprocessor module. From [Elektrotechnik-14].

product requirements, adding scalability to the design, as shown in Fig. 3.2. This approach also allows for selecting a second source supplier to help negotiating better component's prices.

Currently, an important segment of the microprocessors' architectures is driven by the smartphone market, and the smartphone product lifetime is usually in the range of 2-3 years, in contrast to the 10-15 years of an automotive platform. A B2B methodology can allow for updating only the microprocessor subsystem within the same automotive platform, as illustrated in Fig. 3.3, where a complete microprocessor module is shown.

Furthermore, each silicon generation is delivered in a denser I/O package, currently requiring fine pitch and high-density interconnect technologies. By employing a B2B approach, the application board unit's layer count can be reduced to the bare minimum, letting the complexity into the smaller attached computing module, as depicted in Fig. 3.4.

3.1.2 Automotive Criteria for Board to Board Interconnects

Along with the time to market, scalability, and cost reduction in materials, there are specific requirements for a board to board technology to hit the automotive industry, as described below [Schulmeister-14].

3.1.2.1 Handling Effort

Every added part in a mission critical system increases the probability of failures, being logistic one of the most important entry points for mistakes. Handling effort in an added standalone electrical module should be minimum in order to reduce the chances of errors.

Fig. 3.4 Board to board modular design. From [Wolf-14]

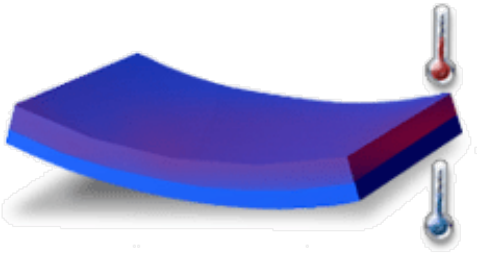


Fig. 3.5 Warpage effect. Temperature differences due to the thermal properties of two different materials laid out together cause them to bend or twist out of shape. From [Autodesk-17]

3.1.2.2 Robustness

Robustness is not about employing thick stiff materials, but rather about allowing enough flexibility to withstand and compensate for mechanical and thermal stress. It is expected that the interconnection process is warpage-compensable due to the hindrances needed to mechanically balance a heterogeneous PCB based electrical design. Here, warpage refers to the uncontrolled dimensional distortion or change of shape or outline developed in a laminate material exposed to varying temperatures, as illustrated in Fig. 3.5. Additionally, the final standalone B2B electrical module should withstand a complete set of tests, such as extreme (low and high) temperature exposure tests, low and high temperature operation tests, power cycle thermal test, thermal shock resistance, vibration, audible noise, mechanical shock, mechanical stability, temperature humidity cycling, dust test, water protection, and chemical resistance to become automotive qualified. A typical automotive qualification test flow diagram is shown in Fig. 3.6 [Richter-98].

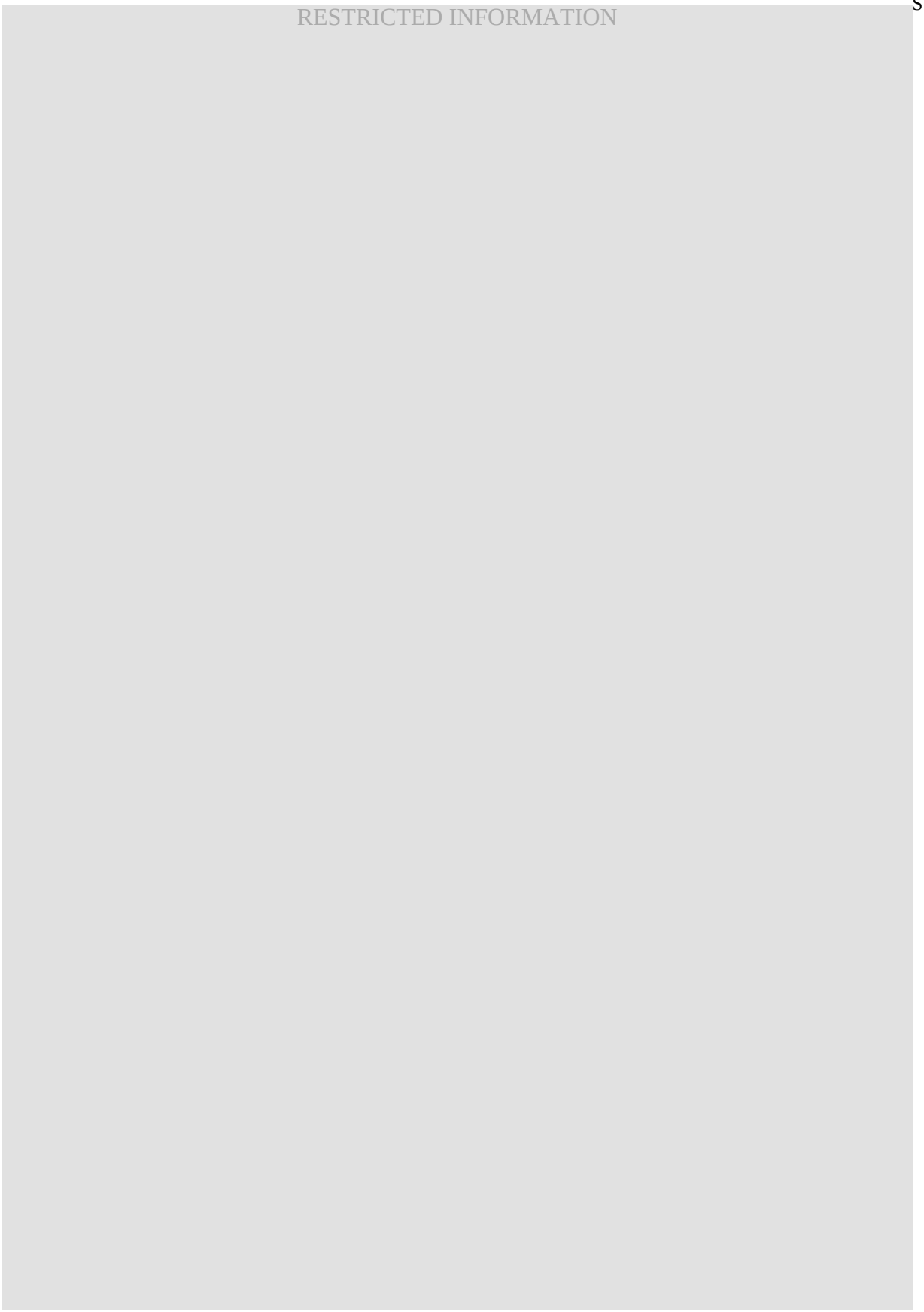


Fig. 3.6 An automotive qualification test flow chart. From [Richter-98]

3.1.2.3 Interconnection Influence

The shape, size, and location of the B2B electrical module should not influence the customers' final product sketch. Therefore, the size and shape of the interconnects should allow a harmonic insertion of the full product features. For example, heatsink solutions and peripherals I/O should not get compromised due to the usage of a B2B electrical module.

3.1.2.4 Inspection

A 100% of interconnections' yield should be guaranteed on each part. For this reason, state-of-the-art inspection technologies such as automatic optical inspection (AOI), X-ray, computerized axial tomography (CT) scan solutions should be available and effective to catch all errors within assembly line. If a B2B electrical module's geometry difficults the automatic inspection, a different geometry should be proposed in order to qualify with the required interconnections' yield.

3.1.2.5 Signal Quality

Digital data transfer for high-speed and differential signals should be assured. Also power integrity and current drop. Interconnects' geometry in a B2B electrical module should allow for high quality and low emissions signaling, almost as good as if there were no B2B interconnects.

3.1.3 Board to Board Interconnects

Board to board interconnects can be classified in two main types: connector based and connectorless interconnects. This work will briefly describe a comparison of those that are better suited for the automotive market at a conceptual level.

3.1.3.1 Connector-Based Interconnects

These interconnects give the best mechanical robustness. However, insertion cycles are sometimes cumbersome, depending on the connector geometry design. Most of them add parasitic capacitance, hence, the frequency response requirements should be verified carefully. The most relevant for automotive applications are shown in Fig. 3.7 and Fig. 3.8:

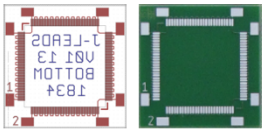
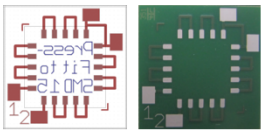
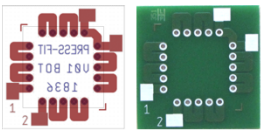
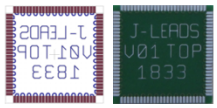
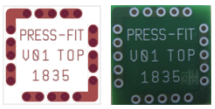
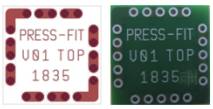
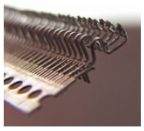
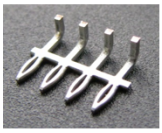
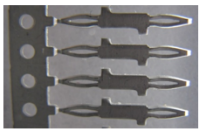
Layouts	J-Leads	Press-Fit to SMD	Press-Fit to Press-Fit
Geometry			
Bottom Boards			
Top Boards			
Details	**- Pitch:** 0,635mm **- I/Os:** 4x26 = 104 **- Standoff:** 1,77mm; 	**- Pitch:** 2,54mm **- I/Os:** 4x5 = 20 **- Standoff:** 4,0 mm 	**- Pitch:** 2,54 mm **- I/Os:** 4x5 = 20 **- Gap:** 4,0 mm 

Fig. 3.7 Basic topology of connector-based board-to-board interconnects. From [Wolf-14]

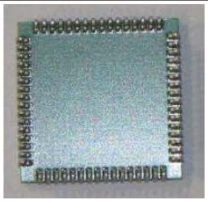
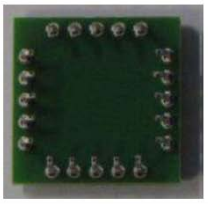
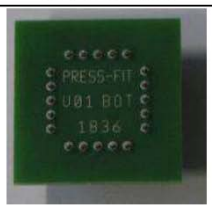
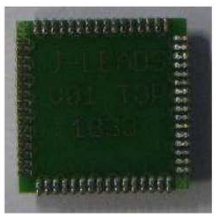
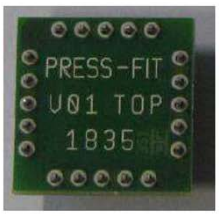
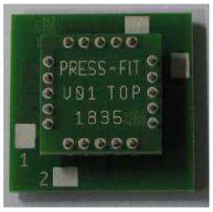
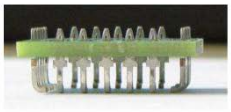
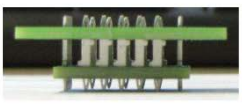
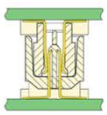
	J-Leads	Press-Fit to SMD	Press-Fit to Press-Fit	Mezzanine
Bottom Boards				
Top Boards				
Side				

Fig. 3.8 Types of connector-based board-to-board interconnects for the automotive. From [Wolf-14] and [Gamperl-14]

a) J-Lead

The J-Lead technology involves no plated through holes. Interconnects are attached to the sides of the B2B module, and then soldered to the application board through an SMD process as the SMD press-fit.

b) Press-fit to SMD

This concept is similar to THMT press-fit. Pins are added to the B2B module by compression, with the difference that the interface to the application board is via soldering through an SMD process.

c) Press-fit to press-fit, or THMT press fit

These interconnects consist in a metal stud that is attached by compression inside metal plated through holes located in both, the application board and the B2B module.

d) Mezzanine connectors

Commonly found in mobile PCs and scalable communications devices, mezzanine connectors are off the shelf solutions for high-speed interconnects [Amphenol-15]. Depending on

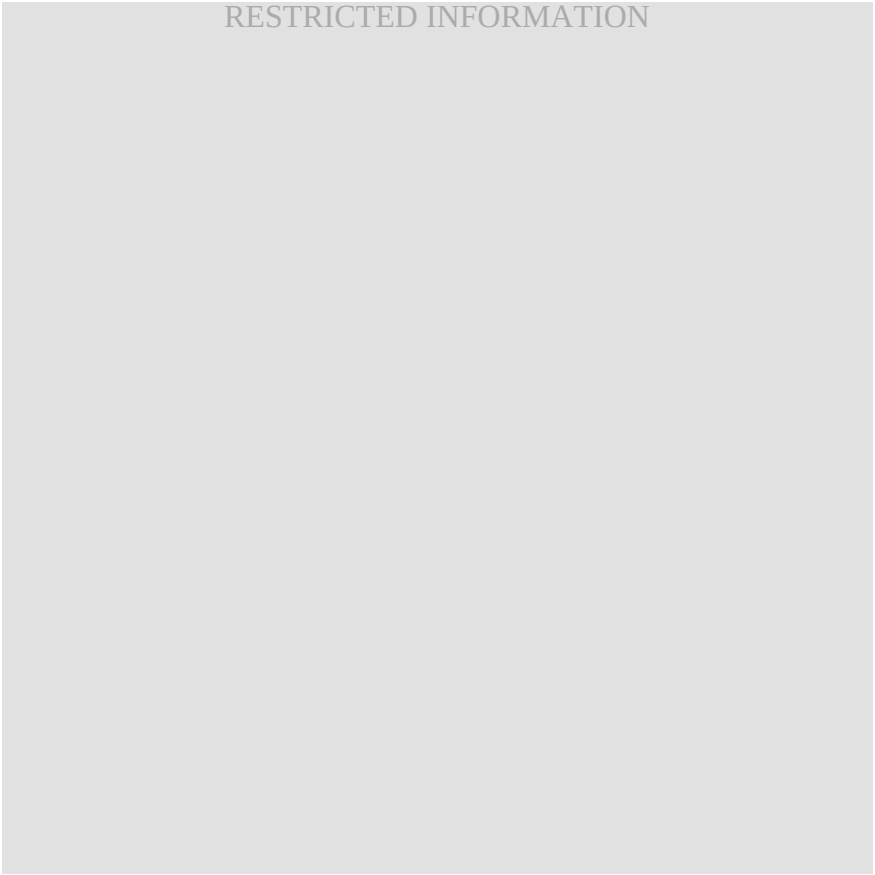


Fig. 3.9 Post stamp SiP. From [Strahl-12]

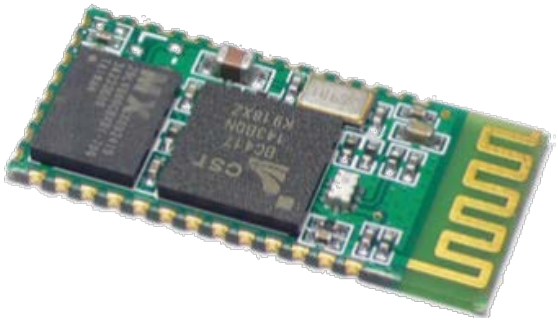


Fig. 3.10 Via-castellated PCB module. From [Gamperl-14]

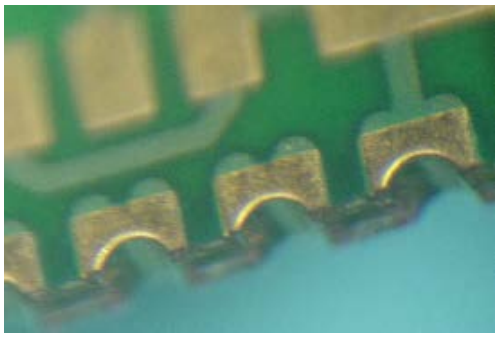


Fig. 3.11 Via castellation. From [Strahl-12]

the geometry, high frequency performance is completely characterized, and mechanical robustness is ensured by screwing both boards together. Usage is discouraged in automotive due to their high costs and temperature ranges are not usually broad.

3.1.3.2 Connectorless Interconnects

These interconnects are usually inexpensive and highly repeatable, at the cost of less mechanical reliability. A tradeoff must be made in-between I/O density and robustness. Among the principal types of connectorless interconnects are:

a) Post-stamp design (via castellation)

Several off the shelf communication modules are built as systems in packages (SiP) in this form factor, such as the diagram in Fig. 3.9. Interconnects are created on the sides of the B2B module or SiP through a process called via castellation [Gamperl-14], as seen in Fig. 3.10. Half vias are generated, then cut in half and finally plated, as illustrated in Fig. 3.11, creating a big robust interconnect due to the big solder fillet attachment created after SMD reflow, as the assembly shown in Fig. 3.12.

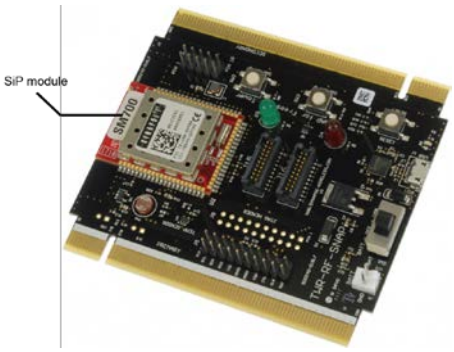


Fig. 3.12 Post stamp SiP module soldered. From [Element 14-12]

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a) b)

Fig. 3.13 Small LGA board-to-board module: a) top view, b) bottom view.

a) b)

Fig. 3.14 Big LGA board-to-board module: a) top view, b) bottom view.

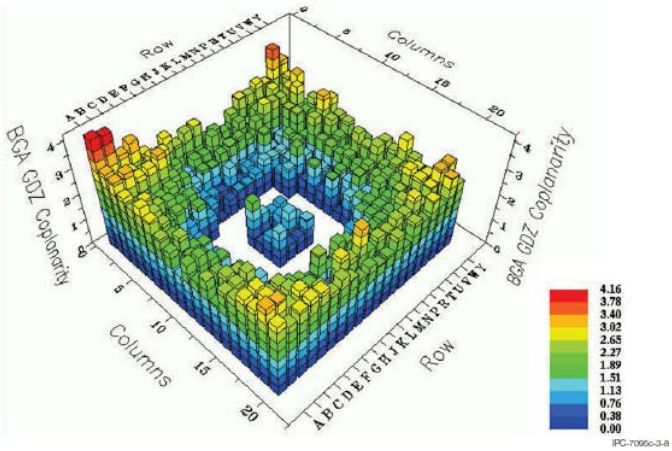

Fig. 3.15 LGA warpage sensitivity. From [IPC Sd IPC-7095C].

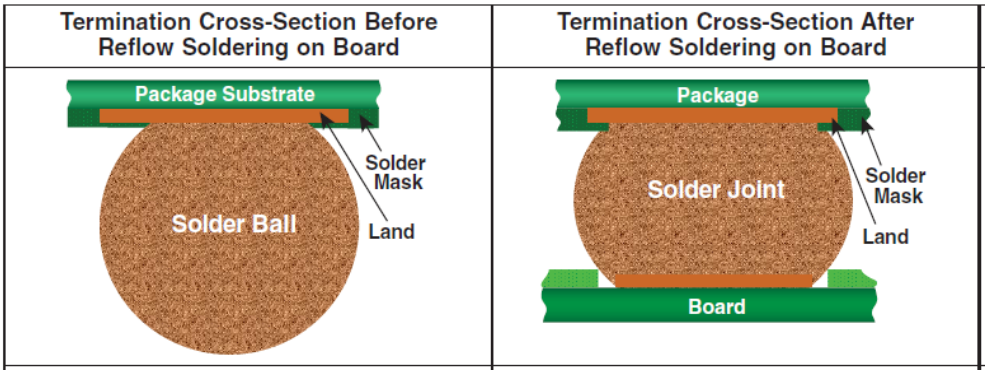

Fig. 3.16 Ball grid array. From [IPC Sd IPC-7095C]

Fig. 3.17 Head-on-pillow phenomenon in BGAs. From [Indium-08]

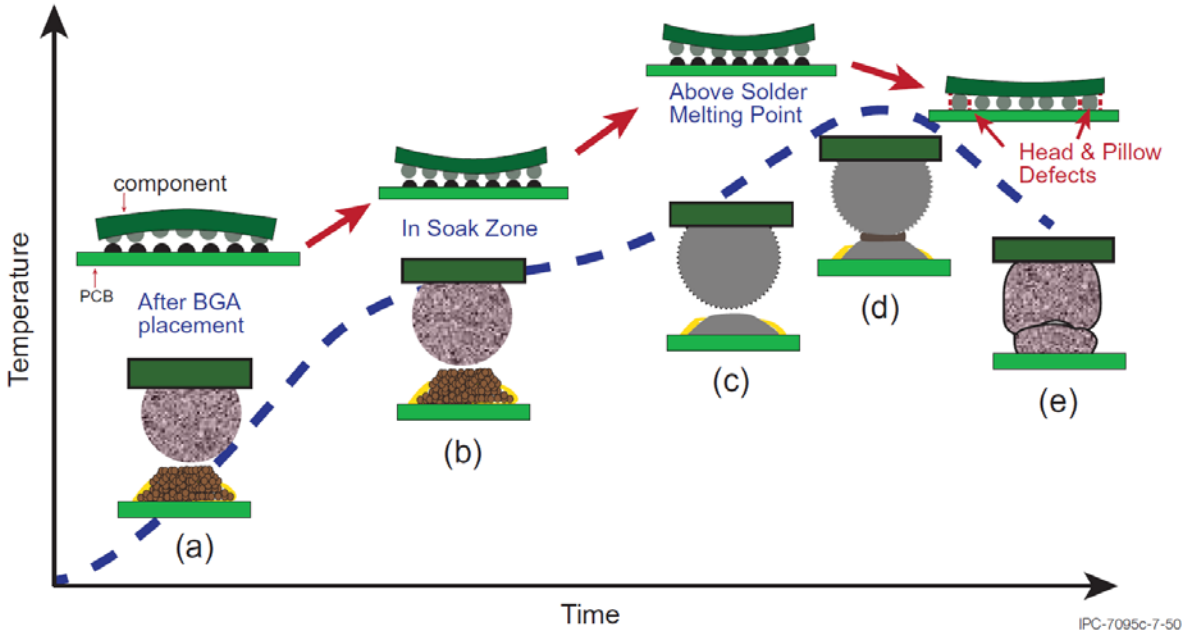

Fig. 3.18 Head-on-pillow process sequence ocurrences. From [IPC Sd IPC-7095C].

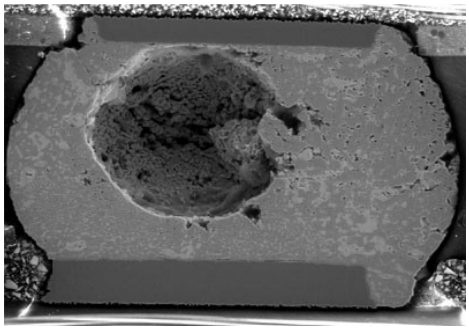

Fig. 3.19 Solder ball void example. From [Indium-16]

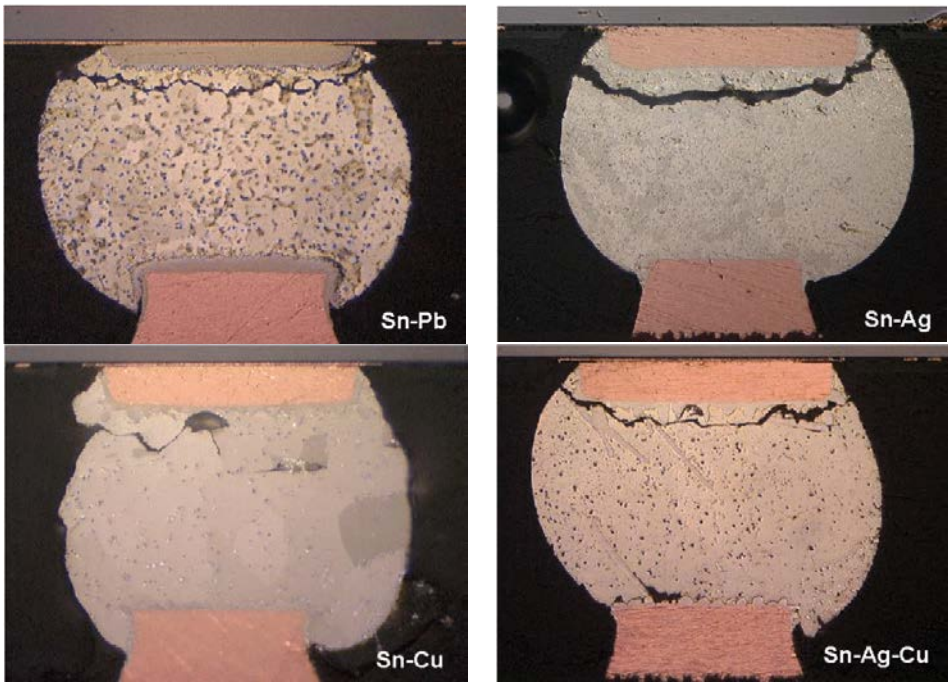

Fig. 3.20 Several solder ball crack examples. From [Frear-01]

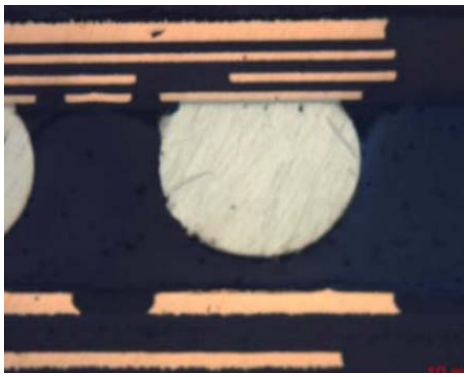

Fig. 3.21 Example of BGA open joints. From [IPC Sd IPC-7095C]

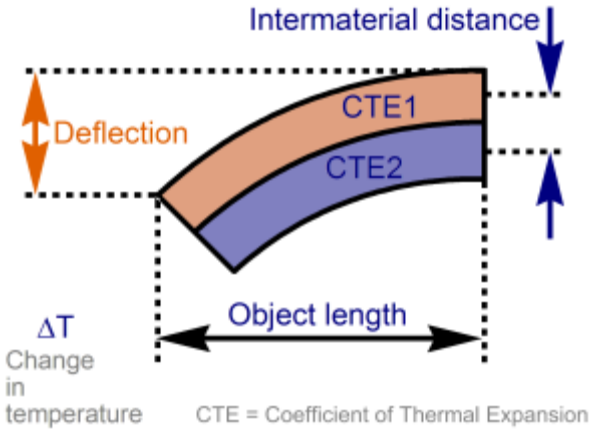

Fig. 3.22 CTE mismatch. From [CalcTool-08]

b) Land grid array (LGA)

LGAs are grid array packages with terminal pads on the bottom surface, as those shown in Fig. 3.13 and Fig. 3.14. The LGA solder interconnect is formed solely by a thin layer of solder paste applied at board assembly. This results in a low standoff height of approximately 0.06 mm to 0.10 mm [Peregrine Semi.-16]. LGAs allow a significantly higher density than post-stamp designs, but their low-profile nature makes them the most warpage sensitive B2B interconnects, as illustrated in Fig. 3.15.

c) Ball grid array (BGA)

They are grid array packages with preformed metal spheres attached to their terminal pads on the bottom surface, as illustrated in Fig. 3.16. They allow the highest density of interconnects. These structures are the best performer in high frequency applications due to the relatively small size to wavelength ratio of the ball interconnects. However, attaching the metal spheres to the B2B module is not a trivial process.

Among their limitations, they can present reliability problems within the assembly process [IPC Sd IPC-7095C], such as voids, open joints, solder cracks, the head-on-pillow phenomenon in which metals do not reflow properly, moisture sensitivity, etc., as illustrated in Fig. 3.17-Fig. 3.21. Additionally, large die sizes can cause coefficient of thermal expansion (CTE) mismatch between the PCB and the package laminate material, which can create package warpage [IPC Sd IPC-7095C]. The graphical description of CTE mismatch concept can be seen in Fig. 3.22.

3.2. A Comparison Between Connectorless Board to Board Interconnects for the Automotive Electronics Industry

An introduction and overview on board to board interconnecting technologies in the context of modern automotive industry is presented in Section 3.1. To benchmark the principal solderless interconnects intended for automotive board to board (B2B) applications, an initial comparative study between different kinds of B2B interconnects was performed by Andreas Bernhardt (Continental Automotive GmbH, Powertrain Division, Regensburg, Germany), in collaboration with Passive Safety & Sensorics business unit [Schulmeister-14]. The objectives of this comparison were to clarify several possible issues with the introduction of this technology to the automotive environment [Seitz-15], particularly:

a) General criteria selection for the automotive qualified interconnection technology
b) New application compatibility evaluation: high frequency digital data transfer
c) Thermal robustness of interconnection technology
d) Mechanical robustness of interconnection technology
e) PCB warpage
f) Mockup of targeting concept.

The above items come from the automotive sector and manufacturing experience, in which failure modes are tested to mimic the worst environmental cases, guaranteeing reliability.

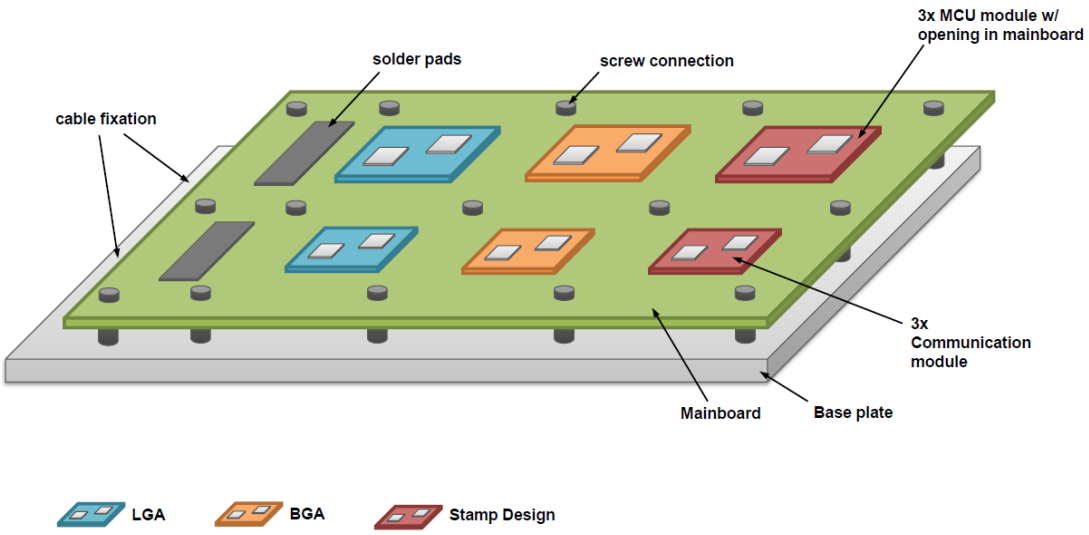

Fig. 3.23 Test mainboard definition, enabling six different interconnect test cases. From [Schulmeister-14]

Fig. 3.24 Communication module interconnects' test definition. From [Schulmeister-14].

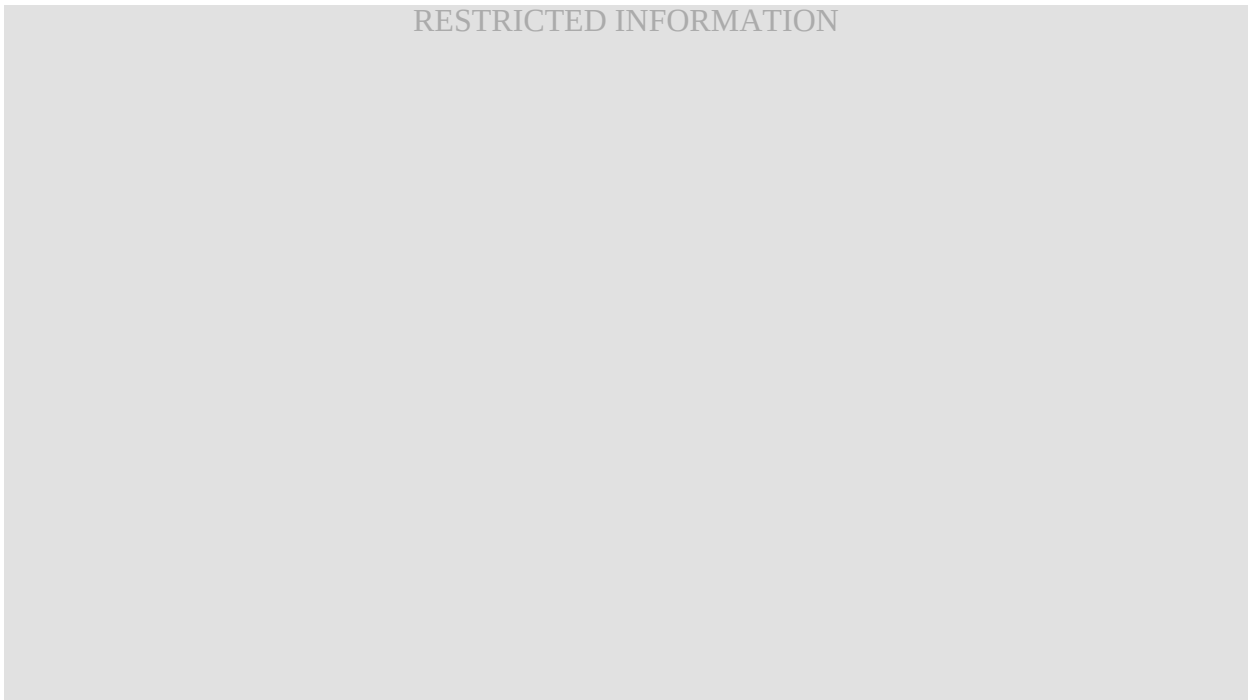

Fig. 3.25 Microcontroller module interconnects' test definition. From [Schulmeister-14]

In the following sections, a qualitative comparative study is performed considering the following connectorless board to board interconnects: via castellation or post stamp, ball grid array, and land grid array. First, the test vehicle utilized is defined. Next, the most relevant test parameters are selected in the context of the automotive industry, and finally the qualitative results are presented and discussed. At the end, some conclusions are drawn.

3.2.1 Test Vehicle Definition

A test mainboard was proposed to fit six different interconnect test cases, as depicted in Fig. 3.23. These test cases consist of two different module applications, one for a communications system with 4 FR4 layers, as shown in Fig. 3.24, and another one for a microcontroller, also FR4 with 8 layers, depicted in Fig. 3.25.

Each of the applications' modules will exert a ball grid array (BGA), a land grid array (LGA), and a via castellation (post-stamp) interconnection scheme, as shown in Fig. 3.26. Due to the electrical nature of a communications module, a significant amount of passive components could be required on its bottom side. For this reason, mechanical robustness is also tested by routing a hole in mainboard under communications modules' landing geometries, as depicted in Fig. 3.27, with the purpose of allocating an area for placing filter arrangements on secondary side of communications module.

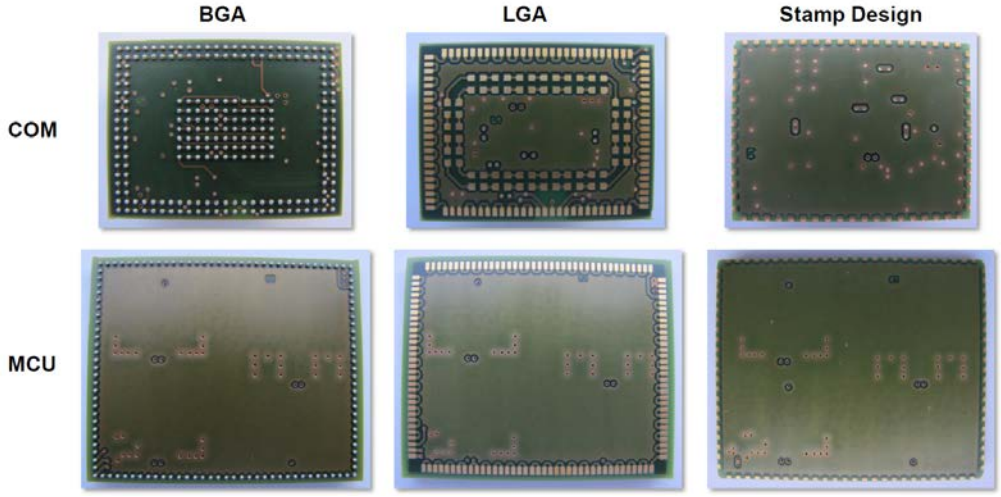

Fig. 3.26 Test interconnects' patterns for a communication module and for a microcontroller module: ball grid array (BGA), land grid array (LGA), and via castellation (post-stamp).

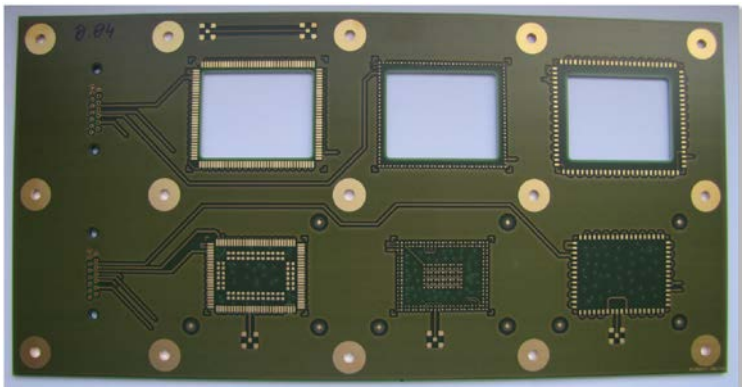

Fig. 3.27 Bareboard PCB of mainboard.

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Fig. 3.28 Test DC signal injection diagram for evaluating opens and shorts circuits.

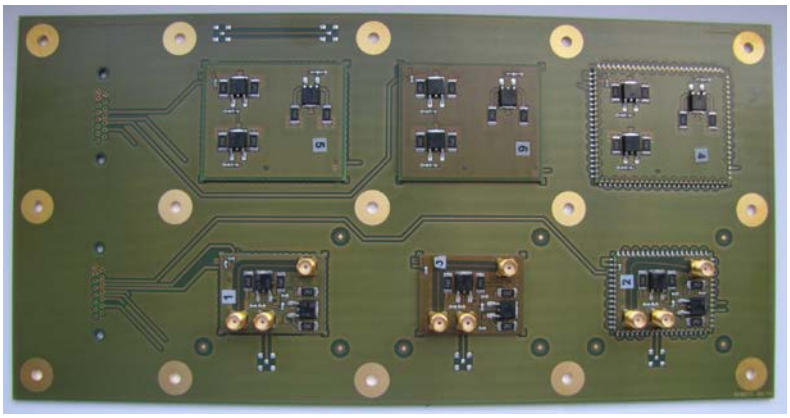


Fig. 3.29 Test signal injected with press-fit headers and SMA connectors to measure the impedance and frequency response of the interconnects..

Since BGA and LGA interconnects are not externally visible, cross-sectioning and x-ray inspections are needed in order to check the interconnects [Ponsolle-11]. As a quick aid for evaluating opens and shorts circuits resultant from manufacturing process, a DC signal injection is provided through a couple of test connectors to each of the modules. Fig. 3.28 shows the corresponding test signal injection diagram. Additionally, SMA connectors are added to extract the impedance and frequency response of the interconnects, as seen in Fig. 3.29.

3.2.2 Test Parameters

A total of six parameters are evaluated for this test concept. Warpage [Palomar Tech.-10] is measured for assessing the interconnect flexibility due to the differences in the coefficient of thermal expansion (CTE) between two matching printed circuit board assemblies (PCBAs). Mechanical and thermal robustness are evaluated for interconnect's life prediction. Mechanical and thermal shock is tested for assessing the worst-case scenario in all automotive weather conditions [Richter-98], and S-parameters are assessed for digital data transfer performance. Tests are performed as follows.

a) Warpage

   Evaluated from 25 °C to 250 °C. Measured with a cross-section of the assembly.

b) Mechanical robustness

   Wide-band random vibration. Test duration is 8 hours for each spatial axis. [redacted]

c) Mechanical shock

   Half-sine waveform. Sample rate of 1 ms [redacted]

d) Thermal robustness

   Powered module cycling over temperature with temperatures of –40 °C, 25 °C, 105 °C. [redacted]

e) Temperature shock

   Thermal shock with immediate change from –40 °C to 125 °C, for a minimum of 1000 cycles. [redacted]

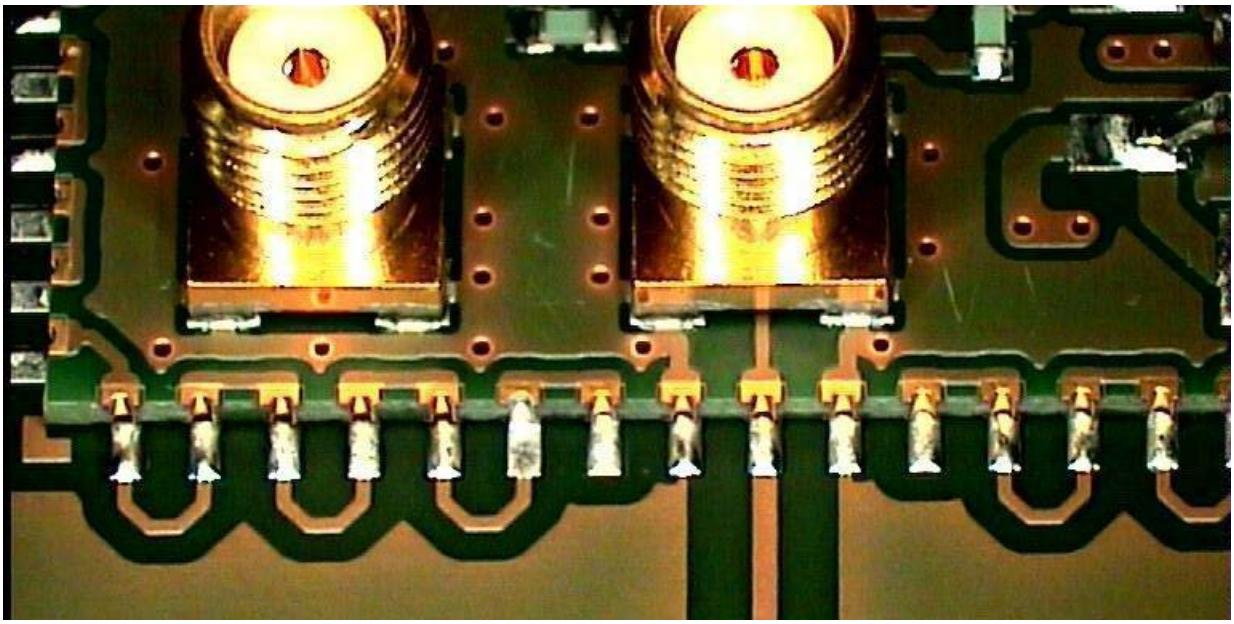


Fig. 3.30 Post stamp finished interconnects.

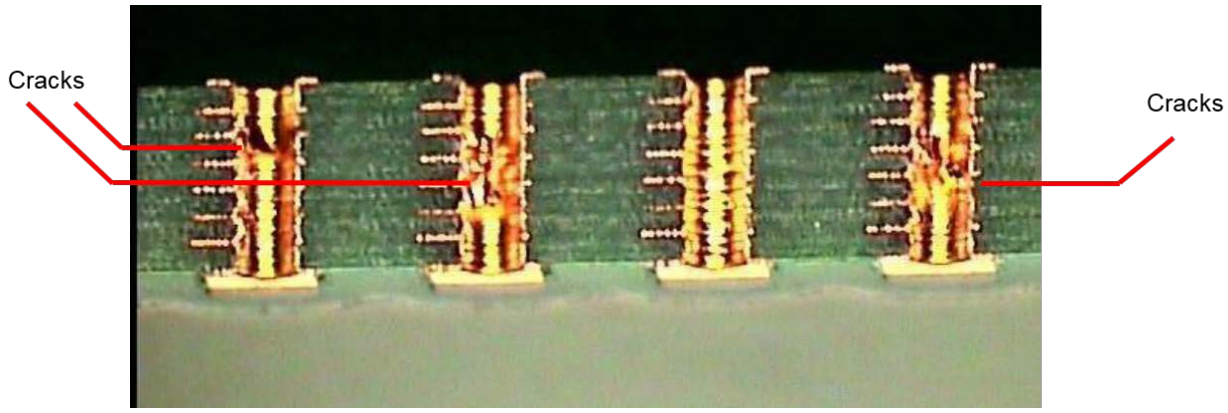


Fig. 3.31 Multilayer via castellation after tests. Cracks were found in some via structures due to multilayer PCB stackup.

f) Digital data transfer

DC signal injection through press-fit headers and oscilloscope measurement.

Impedance analysis and S-parameter extraction with Keysight E5061B vector network analyzer (VNA) and a frequency range from 0.1 to 3 GHz.

3.2.3 Test Vehicle Results

Results have been correlated with the designs' geometries as follows.

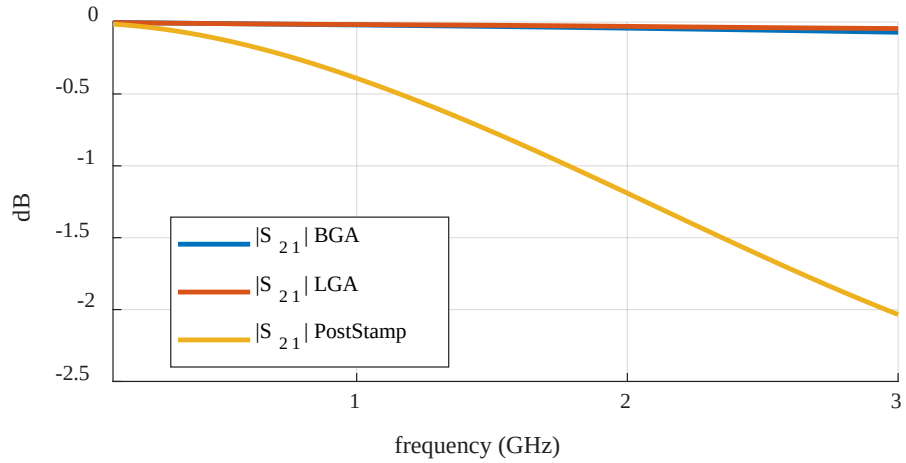


Fig. 3.32 Insertion loss comparison of tested interconnects.

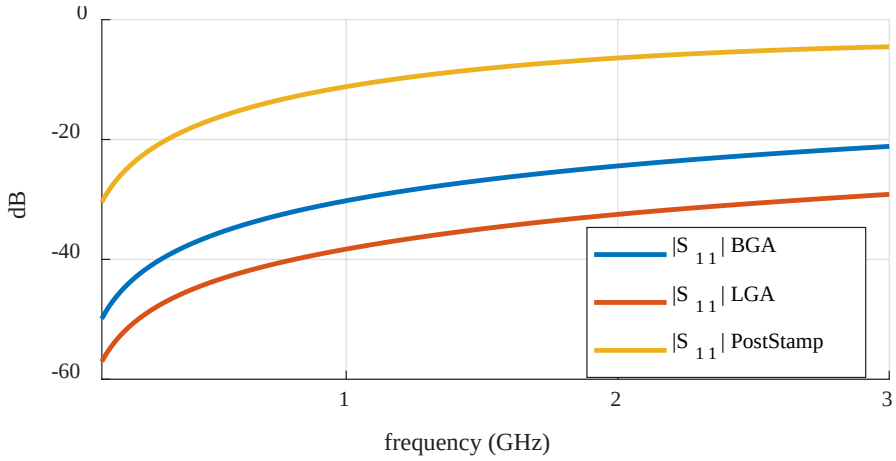


Fig. 3.33 Return loss comparison of tested interconnects.

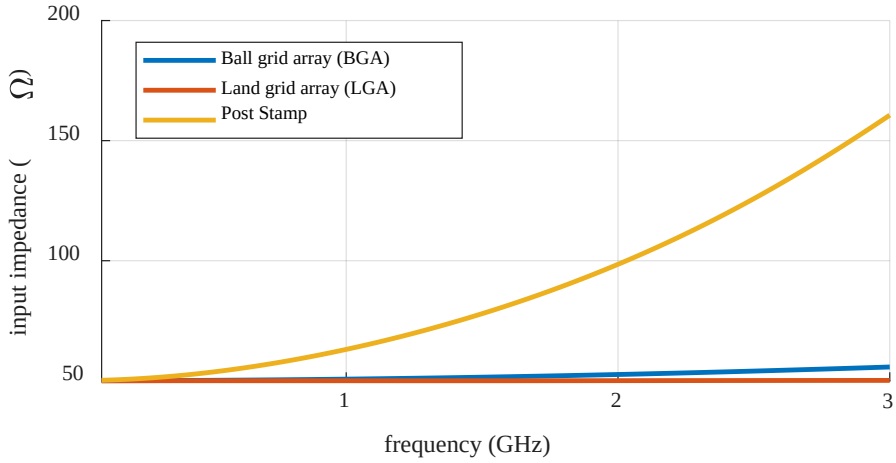


Fig. 3.34 Impedance comparison of tested interconnects.

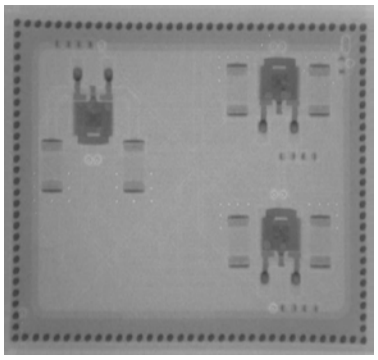


Fig. 3.35 BGA interconnect attachment.

a) Post-stamp design (via castellation)

This geometry presented a very good mechanical attachment, and a great stability against warpage. DC signal injection exhibited 100% of interconnects working after all the mechanical tests. However, solder-fillets for the interconnections (created between castellated vias and landing pads) need tuning, as seen in Fig. 3.30, since they are not completely covering the side of the via castellated pads. Furthermore, cracks were found in via structure due to multilayer PCB stackup, as depicted in Fig. 3.31. However, considering the 3 GHz frequency range, it is seen from Fig. 3.32-3.34 hat its acceptable RF performance is approximately limited to frequencies up to 0.3 GHz, quickly deteriorating at higher frequencies.

b) Ball grid array (BGA)

This geometry presented a good stability against warpage. As seen in Fig. 3.35, interconnect bonding is very homogeneous, but mechanical attachment presented a few design flaws. Ball weight-support calculation was not performed beforehand and weight of components on top of module collapsed interconnects, as depicted in Fig. 3.36, increasing the risk of short-circuit between them. RF performance was very good, as shown in Fig. 3.32-3.34, with a good performance within the 3 GHz frequency range.

c) Land grid array (LGA)

LGA did a mixed performance with respect to the previous interconnects, since it gave the best RF performance, as shown in Fig. 3.32-3.34, and a good enough interconnect attachment, as depicted in Fig. 3.37. Warpage was the biggest concern in this type of geometry, since it was the main cause of creating voids inside some of the interconnects, as shown in Fig. 3.38.

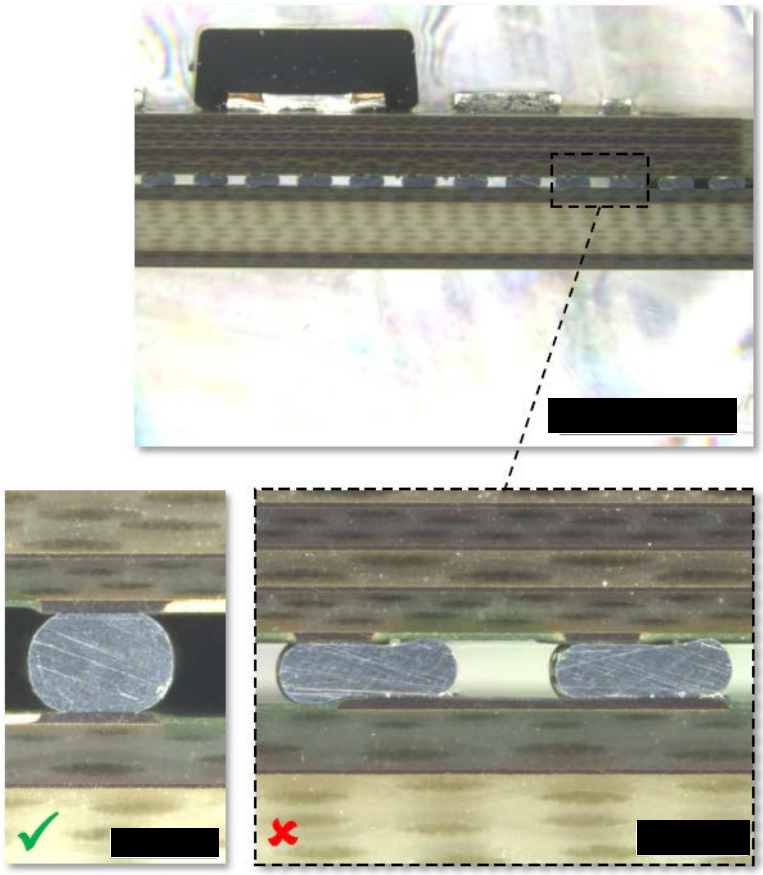


Fig. 3.36 Cross section of BGA interconnect.

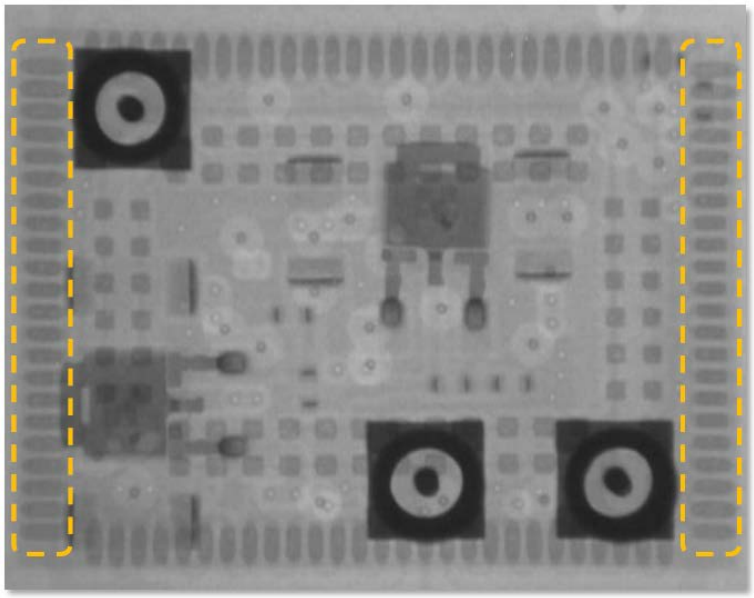


Fig. 3.37 LGA interconnect attachment.

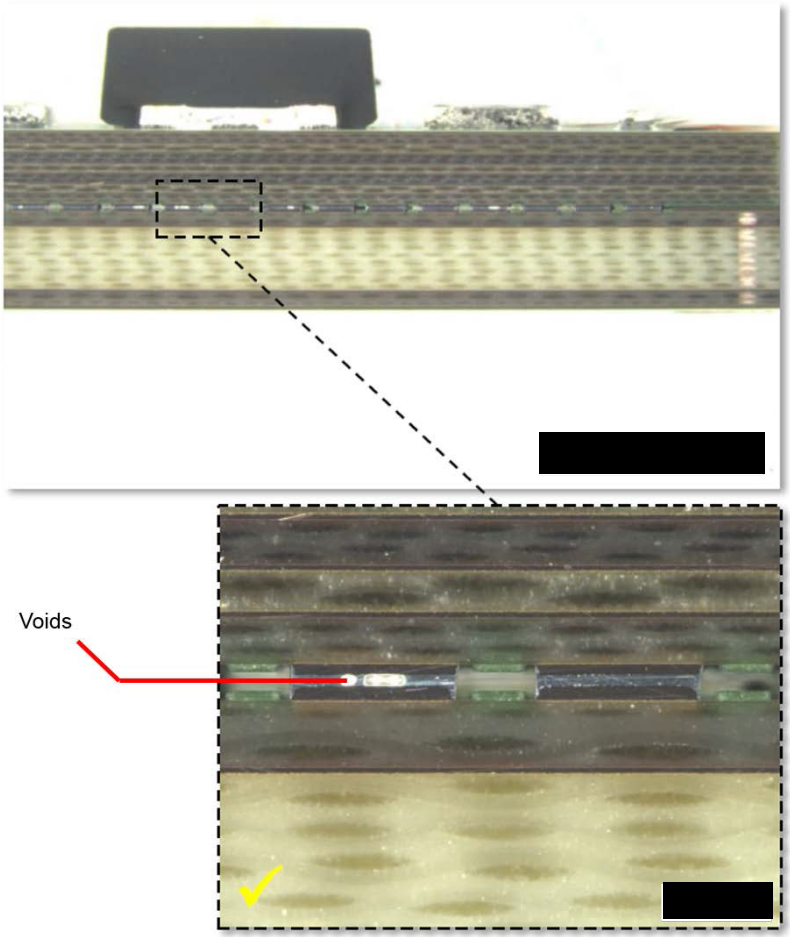


Fig. 3.38 Cross-section of LGA interconnect: warpage can create voids in this type of geometry.

3.3. Solder Ball Technologies for System in Package and Board to Board Solutions for the Automotive

The term “solder balling” refers to the production step to get solder bumps on a substrate, as depicted in Fig. 3.39. Solder bumps are the small spheres of solder material (solder balls) that are bonded to contact areas or pads of semiconductor devices [Palomar Tech.-10], or in some cases they are bonded to printed circuit boards. This method provides electrical connections with minimum parasitic inductances and capacitances [Sarawi-97] which are crucial to enable state-of-the-art automotive systems.

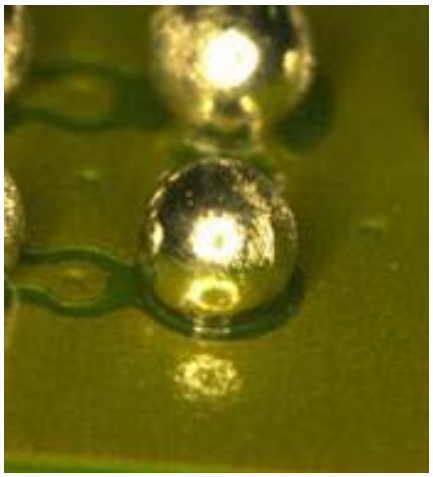


Fig. 3.39 Solder ball on a PCB. From [Palomar Tech.-10].

Nevertheless, solder balling processes are mainly just executed by semiconductor and packaging companies [Dengler-16] because solder balls are necessary for technologies like flip chip or ball grid array packages (BGA). Thus, it is crucial to evaluate which of the current solder balling technologies have a better fit for automotive systems in packages (SiP) and module in packages (MiP).

Additionally, there are high demands on thermal and mechanical robustness, as well as on reliability and lifetime, of the module and the solder connections [Dengler-16]. Therefore, this report analyzes different industrially-available solder balling procedures for assembling a MiP, evaluated from an automotive industry point of view.

3.3.1 Existing Methods

Currently there are several different solder bumping techniques available for usage in semiconductor wafers' mass production. These technologies include electro-plating, solder paste transfer-printing, evaporation, and preformed solder ball direct adhesion methods [Chipbond-17]. In the case of substrate panels, such as printed circuit board (PCB) assemblies, only solder paste transfer-printing along with preformed solder ball direct adhesion methods, work in a reliable cost-effective way [Dengler-16]. The main production steps to generate solder bumps on a PCB substrate are illustrated in Fig. 3.40.

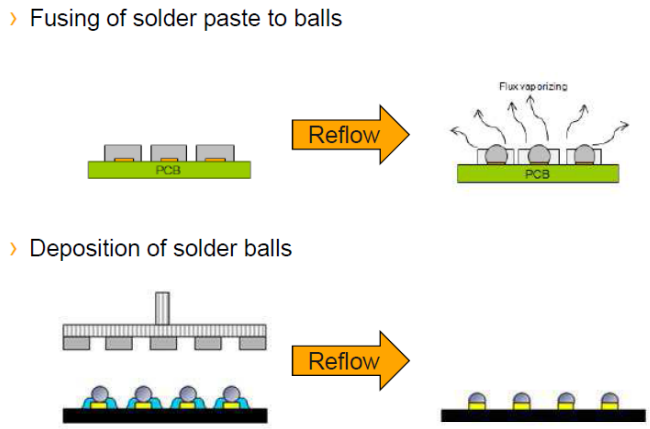


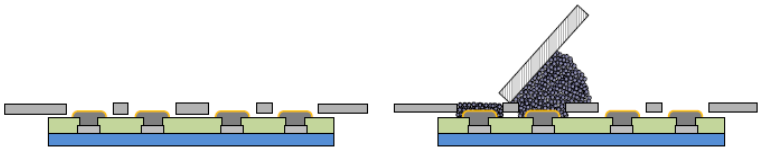
Fig. 3.40 Production steps to generate solder bumps on a PCB substrate. From [Dengler-16].

3.3.2 Balling Procedures with Solder Paste

Solder paste balling procedures have been the cost-saving alternative for high-volume production in the wafer manufacturing industry [Manessis-04]. They have the advantage to be fully compatible with pre-existing surface mount technology (SMT) assembly printing equipment, as well as its capability of producing solder bumps from a wide spectrum of solder paste's composites, including halogen and lead-free solders, which have been the hot issue of strict environmental legislative rules [Manessis-04]. Their adaptation from wafer to PCB substrates is transparent. The principal balling procedures are stencil printing and high speed jetting, both described below.

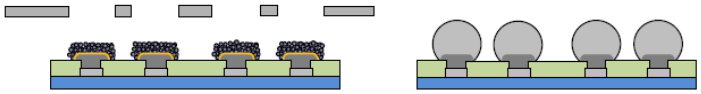
3.3.2.1 Stencil Printing

This technology has been developed to deposit solder pastes onto circuit boards for mounting surface mount components. As shown in Fig. 3.41, a template or stencil with micrometrical controlled apertures is aligned to the interconnecting geometries of a printed circuit board (PCB) panel. Then a bead of solder paste is pushed (rolled) across the stencil surface by a squeegee blade. Said solder paste bead is squeezed through apertures in the stencil and on to the bond pads of the wafer. The stencil then is separated from the wafer, leaving local paste deposits adhering to contact pads [Pac Tech-13]. In order to ensure that there are no failures on the board,



a) Align stencil to PCB substrate b) Squeegee print solder

Fig. 3.41 Stencil printing process: solder paste is deposited on a PCB by: a) aligning a stencil template, and b) rolling a bead of solder paste over it. From [Pac Tech-13].



a) Raise stencil b) Reflow and clean

Fig. 3.42 Stencil printing process: a) after removing stencil template, b) quasi-spherical bumps are formed after reflow process. From [Pac Tech-13].

the deposits are checked by a three-dimensional solder paste inspection system (3D SPI). Afterwards, the panel must pass through a regular SMT reflow process in which the solder paste fuses to quasi-spherical bumps, as depicted in Fig. 3.42 [Dengler-16].

Alignment, print speed, print mode (e.g., on or off contact, single or double stroke) and squeegee pressure are the major tool adjustments that can be made that affect print quality. Other factors, like stencil quality, squeegee choice, and paste rheology, also affect print quality [Pac Tech-13]. Its main advantages are:

a) It is a well-known process. Success rate does not rely in a complex operator training.
b) It provides an extremely high output: about one million bumps per hour can be achieved.
c) Cheap production costs: no additional machinery investment is needed within a SMD assembly line.

In contrast, its main disadvantages are:

d) Limited in pitch between solder bumps.
a) Challenging to achieve standard geometries for minimum ball height against solder bump to solder bump pitch per the JEDEC Design Guide 4.14 for Ball Grid Array Package [JEDEC Sd 95].
b) Tends to form solder bridges (short circuits), depending on minimum solder bump to solder bump pitch and solder bump height, along with the temperature and humidity control during process.

c) Solder paste composite selection is crucial to avoid voids, volume reduction by flux evaporation, and solder bridging avoidance.

d) Very difficult to tune solder bump geometry design parameters for high repeatability, such as soldermask opening, metal pad diameter, stencil aperture, and stencil height.

3.3.2.2 Solder Paste Dispensing or High Speed Jetting

As shown in Fig. 3.43, this process consists of a piezoelectric printing head attached to a computer numerical control printing bed for accurately dispensing solder bumps directly from a solder paste cartridge. The dispensing needle of the printing head stops above the surface of the panel and applies the paste in desired volumes, one by one [Dengler-16]. That is a quite slow process compared to stencil printing process, in which all interconnects are complete at one single squeegee blade stroke.

In contrast, this process does not present solder paste excess or relatively big differences in solder paste volumes like the stencil printing, making this process cleaner, more accurate, and with less material waste. Its main advantages are:

a) Less material consumption / low material waste.

b) High flexibility; it can be used either for solder bumping, solder paste printing for SMD components, or even as a repair tool for any other bumping technology.

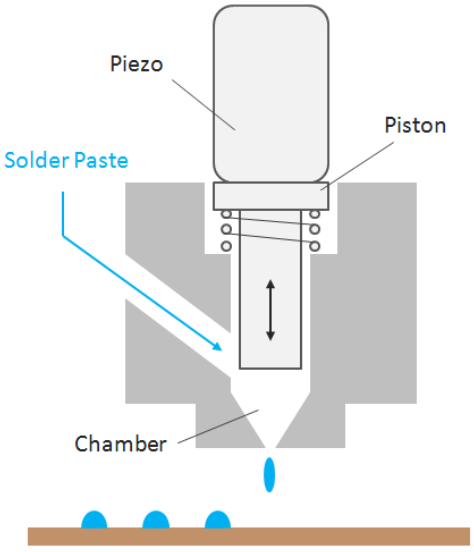


Fig. 3.43 Solder paste dispensing printing head process, also known as high-speed jetting. From [Dengler-16]

In contrast, its main disadvantages are:

c) Low process speed: output about 175,000 balls per hour.

d) Ball size, it has the same limitations of solder paste printing process.

e) Minimum solder bump to solder bump pitch: small pitches are not possible.

3.3.3 Balling Procedures with Preformed Solder Balls

These procedures employ different techniques to bond preformed solder balls to a substrate by a later reflow process, or either by applying local heat to bond each of the solder balls. It has the advantage to present highly repeatable quasi-perfect spheres that are compliant with sizes from the Joint Electron Device Engineering Council (JEDEC) standards by also keeping whimsically fine solder ball to solder ball pitches, which may contain metal alloys or even polymers coated in solder that enhance cost and robustness while increase conductivity and reducing losses. The principal balling procedures with preformed solder balls are manual stencil balling, automated stencil balling, pick and place, and laser jetting, as described below.

3.3.3.1 Manual Stencil Balling

This process consists of aligning a stencil template on a PCB panel, previously printed with solder paste, in a regular SMD solder paste printing process. Then, a cup of solder coated metal spheres is spilled over the stencil. The spheres should be distributed on the stencil surface by hand, which are supposed to fit individually inside each stencil aperture, as portrayed in Fig. 3.44. After that, all the untapped balls should be manually collected into a bowl to reuse them. The stencil

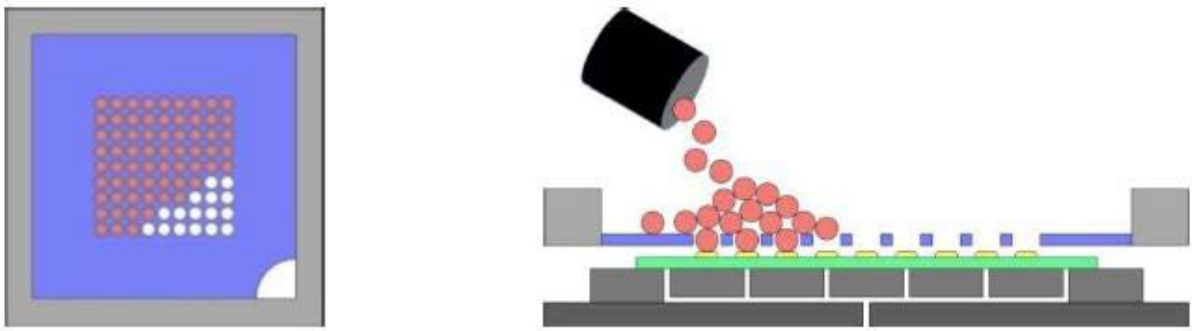


Fig. 3.44 Manual stencil balling process. From [Dengler-16]

should be removed vertically to avoid misaligning the placed spheres. Finally, the PCB panel with the placed spheres is subject to a standard reflow process [Dengler-16]. Its main advantages are:

a) A broad range of preformed metal spheres' materials and sizes can be applied.
b) Low cost; no machinery investment within a SMT assembly facility.
c) Little mechanical expenditure, only a fixture is needed.
d) Equipment with high availability.
e) Moderate amount of solder balls output: about 200,000 balls per hour.

In contrast, its main disadvantages are:

a) Completely manual process.
b) Isolated application.
c) Needs manual handling and transportation to the reflow unit.
d) Not suitable for mass production.
e) Requires skilled technician.

3.3.3.2 Automated Stencil Balling

This is a variation of the manual stencil balling, in which a placement head aligns and fills the stencil apertures with solder coated metal spheres loaded into a magazine, one individual ball per aperture, as shown in Fig. 3.45. The firm ASM Assembly Systems provides a solution called DirEKt placement head, in which said head is mounted in a solder paste printer instead of the

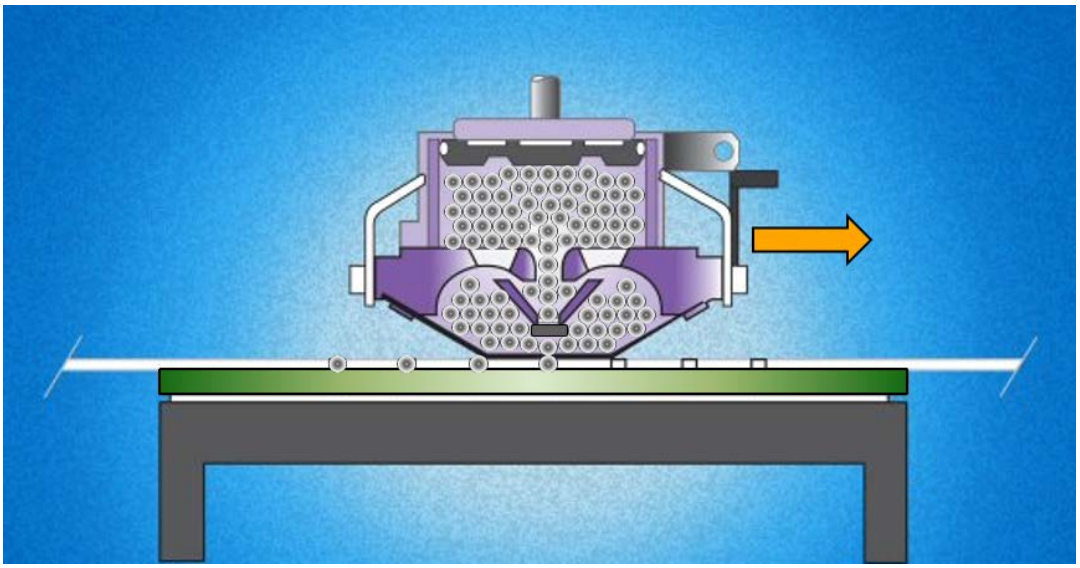


Fig. 3.45 Automated stencil balling. From [JEDEC Sd 95].

squeegee blade [Dengler-16]. As with manual stencil balling, the PCB should be previously printed with solder paste in a different solder paste printer. For this reason, the overall processing time is double of the solder paste printing process. Its main advantages are:

a) Completely automated process.
b) It achieves a high output: about 500,000 balls per hour.
c) A broad range of preformed metal spheres' materials and sizes can be applied.
d) A SMT solder paste printer can be reused in a SMT assembly facility.

In contrast, its main disadvantages are:

e) Impossible to rework a device. A complete substrate must be scrapped for only one missing ball.
f) Not as fast as the solder paste stencil printing method.
g) Extra machinery and processes involved against solder paste stencil printing method.
h) Investment needed for a special printing head.
i) Minimum solder bump to solder bump pitch: small pitches are not possible.

3.3.3.3 Vacuum Stencil Balling

This technology uses a patterned vacuum tooling fixture to simultaneously pick up preformed metal spheres to a template, as shown in Fig. 3.46, and transfer them all over to the PCB substrate at once. First, the PCB substrate is printed with flux, then the metal spheres are filled in a vibrating depot. When vacuum is applied to the tooling fixture, the solder spheres start to jump, sucked into the openings of the stencil. The stencil is then aligned to the PCB substrate and lowered to bring the solder spheres into contact with their corresponding PCB pads. Finally, the vacuum is released, the tooling fixture is raised, and the spheres are then reflowed [Oppert-11]. In this step, the spheres get bonded to the substrate and the flux is removed by evaporation.

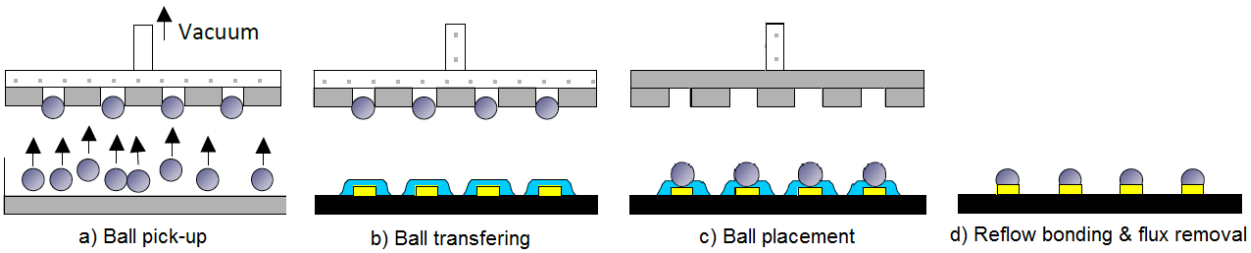


Fig. 3.46 Vacuum stencil balling process. From [JEDEC Sd 95].

There are optical inspections before and after assembling, in order to ensure that no missing or extra balls are applied. Its main advantages are:

a) Suitable for mass production.
b) Fluxing and inspections included in the same machinery.
c) Favorable equipment.

In contrast, its main disadvantages are:

d) Impossible to add devices on balling side.
e) Isolated application.
f) Relatively slow as compared to solder paste stencil printer and automated stencil balling: it can achieve an output of about 250,000 balls per hour.

3.3.3.4 Pick and Place

This is another technology developed to place surface mount components, in which the metal spheres are loaded into a standard SMT placement machine. The challenge is that the balls must be located at a well-defined location, which can be achieved by a special bulk case feeder or even pre-packaging the spheres in a reel for SMD components. Since spheres are loaded one by one, the processing time increases by each placed ball, so the technology is not feasible for a significant number interconnects or mass production. Its main advantages are:

a) Favorable equipment.
b) No need for additional machinery in a SMT assembly facility.
c) No need for additional expertise in technicians at a SMT assembly facility.

In contrast, its main disadvantages are:

d) Very slow: output of about 3,750 balls per hour.
e) Not suited for mass production.
f) Very expensive, especially if solder balls must be taped into a reel.

3.3.3.5 Laser Jetting

This technique employs a laser inside a placement head which drops a single metal sphere from a reservoir onto the desired bond pad location. Subsequently, a laser beam fuses the sphere to the bond pad, as shown in Fig. 3.47. Like the pick and place process, this technique also has a

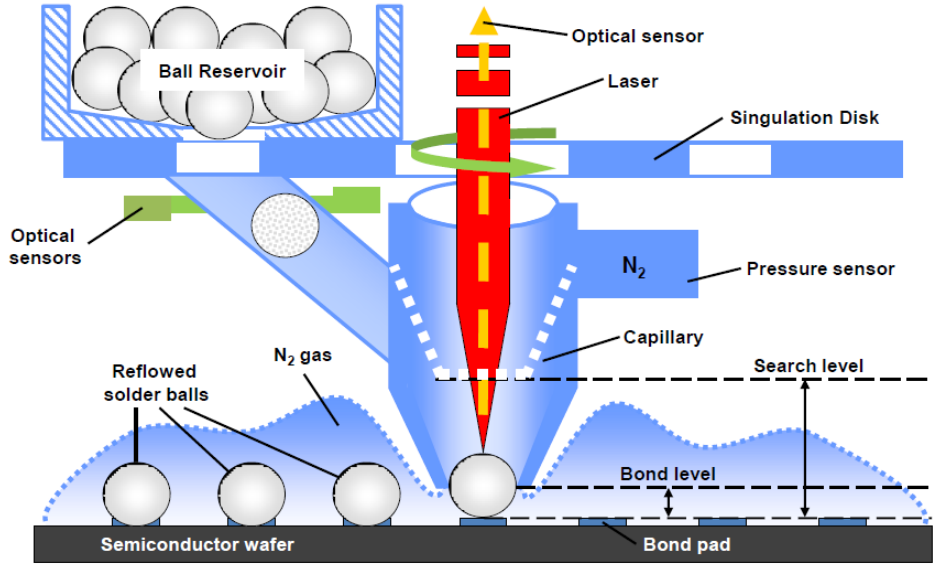


Fig. 3.47 Laser jetting process. From [Dengler-16].

processing time that increases by each placed ball, but it has the advantage of not needing to reflow the substrate, eliminating chemical and heating interactions with the device [Oppert-11]. Its main advantages are:

a) No chemicals added, since no flux is needed.

b) No reflow process required.

c) Flexibility; this process can be applied into a finished PCB assembly.

In contrast, its main disadvantages are:

d) High production costs.

e) Relatively slow process: output of about 25,000 balls per hour.

f) Substantial machinery investment.

3.4. Discussion

Optimizing for each market of the electronics industry require quite different parameters to focus on. For example, in the consumer electronics market, only 1-2 years of uninterrupted operation are expected, without considering temperature operating conditions far outside the typical room temperature ranges. In this electronics industry segment, techniques to achieve the lowest manufacturing cost are emphasized. When dealing with the computer industry, another key

parameters are involved, such as the time to market and lately the performance per Watt or energy efficiency.

The automotive industry is inheriting these parameters due to the connected car trend, but with a much more stringent attention to robustness since unreliable operation involves risking lives. In this electronics industry segment, the best way to speed up time to market while keeping cost-effectiveness is to standardize variants and reuse development resources as much as possible. This explains the recent high interest in board to board technologies, and the ways to adapt them to fully support the connected car.

For impedance controlled signaling, such as automotive Ethernet, and low-voltage differential signaling (LVDS) buses for displays, connector-based board to board interconnects, with the exception of mezzanine connectors, are out of the question. Mezzanine connectors, on the other hand, have the best impedance handling but a very weak tolerance to vibration and extreme temperatures, along with a hefty price tag. These disadvantages makes them undesirable for most automotive applications.

From the brief descriptions given in Section 3.1.3, it can be inferred to choose post-stamp interconnects for robustness, LGA for performance, and BGA for density, but a tradeoff must be taken in order to fulfill the automotive requirements. While achieving the maximum robustness, the post-stamp is unable to deal with high-speed signals. Similarly, the LGA technology is quite constrained in area due to warpage. BGA seems better balanced in this tradeoff, but it is more expensive to build with current re-balling methods.

By the same token, robustness was proven to be application dependent since post-stamp interconnects, whose interconnect density and RF performance is not good enough for a high-speed digital design, presented cracks in the multilayer structure of castellated vias. Similarly, LGA presented the best RF performance, but has the disadvantage of requiring a significantly larger pad size, as compared to BGA.

After these test results, it was found that warpage plays a key role in the criteria to select a B2B interconnect for the automotive industry. The best way to mitigate warpage is to reduce the module area and keep the module as round as possible. For this reason, LGA is still useful for low density, low area modules, exhibiting the best RF performance.

On the other hand, when dealing with high-density high-speed modules, balancing CTE between mainboard and modules is quite a complex task since PCB layout is focused on solving a

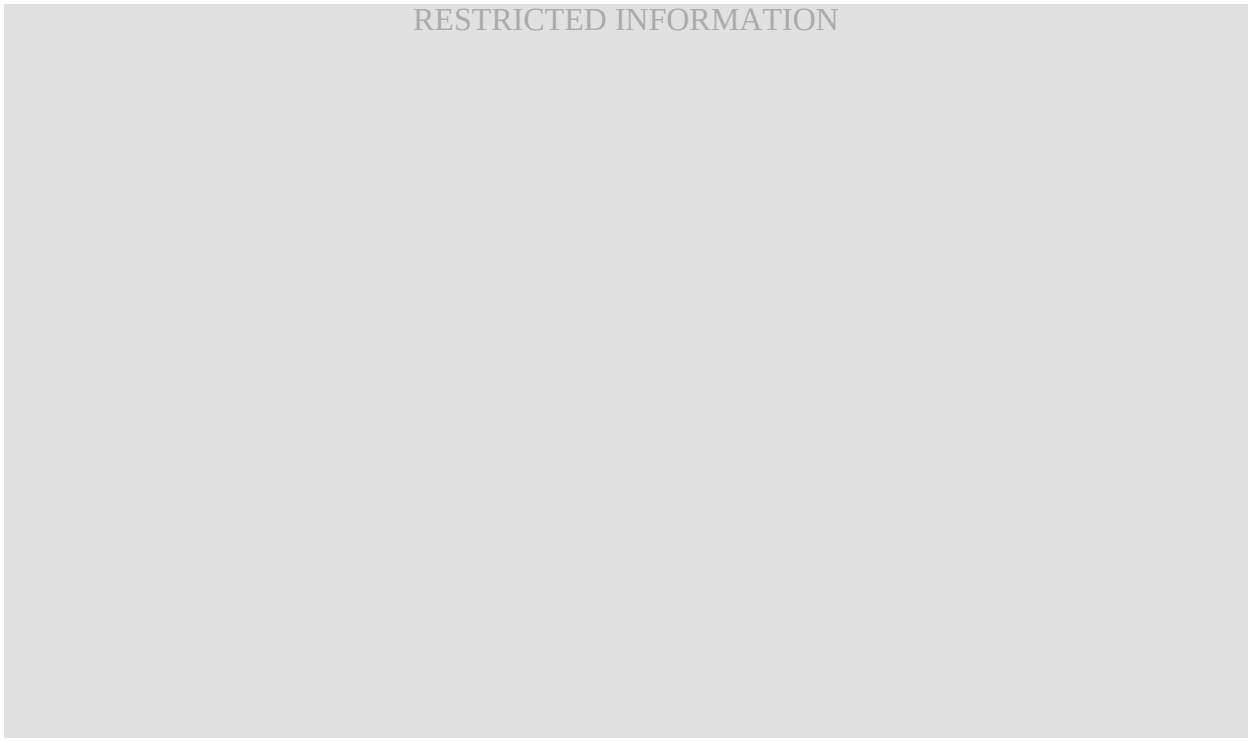


Fig. 3.48 Evaluation matrix of balling procedures from the automotive perspective.

microwave transmission problem in the most cost-effective way. Latter suggestions from manufacturing experts inside Continental involve calculating the amount of metal for each conductive layer in each board: the module and the mainboard, which is still very difficult to match. This implies the necessity to employ a less warpage-susceptible interconnect for these modules.

Moreover, in order to better showcase these balling procedures, a comparison matrix based on automotive needs is shown in Fig. 3.48. As has been noted in previous sections, the stencil printing process is a practical alternative for an automotive mass production SiP / MiP, since it has the lowest cost of all the processes, and also the highest speed, even though it does not qualify for JEDEC standard in smaller pitch/size ratios. Likewise, the automated stencil balling is also relevant due to its capability to use high quality solder coated preformed metal spheres in a cost-effective but still fast enough fashion.

However, the laser jetting is relevant to rework and replace missing balls since it can allow the addition of preformed solder spheres without requiring a reflow process. This is especially important after a finished PCB assembly, since some devices like memories and multi core processors are not able to withstand more than 2 reflow processes.

3.5. Conclusion

When comparing between different board to board interconnects, very different optimization parameters can be applied to them. In the case of looking for extreme robustness and no impedance control, the connector-based interconnects are the recommended choice, while handling more sophisticated signaling demands using connectorless interconnects, in which area, speed, and density must be taken into account in order to choose between via castellated post-stamp interconnects, LGA, and BGA.

In addition, the results presented in this Section 3.2 depicted the electromechanical performance of three different board to board interconnects, with the objective of clarifying several possible issues highly relevant for the automotive environment, such as the mechanical and thermal robustness. Therefore, the chosen interconnect should be robust enough to surpass the thermal and mechanical shock tests, but also less susceptible to warpage effects.

For this reason, the BGA interconnect resulted in the best balance between RF performance, high density, and warpage stability. However, this analysis still needs an assessment of static forces in the BGA interconnect, in order to support the weight of the module's required components which can be evaluated in a future research.

Moreover, common solder balling technologies for board to board and system in package applications for automotive systems were evaluated and contrasted in Section 3.3. Technologies considered include stencil printing, high speed jetting, manual and automated stencil balling, pick and place, and laser jetting. Among these technologies, the best compelling processes for automotive SiPs and MiPs are stencil printing and the automated stencil balling. However, due to its high-density, high-speed, and low-cost properties, the stencil printing process is selected for an exhaustive evaluation in a future work.

4. The Module in Package (MiP): a System in Package Tailored for the Automotive Environment

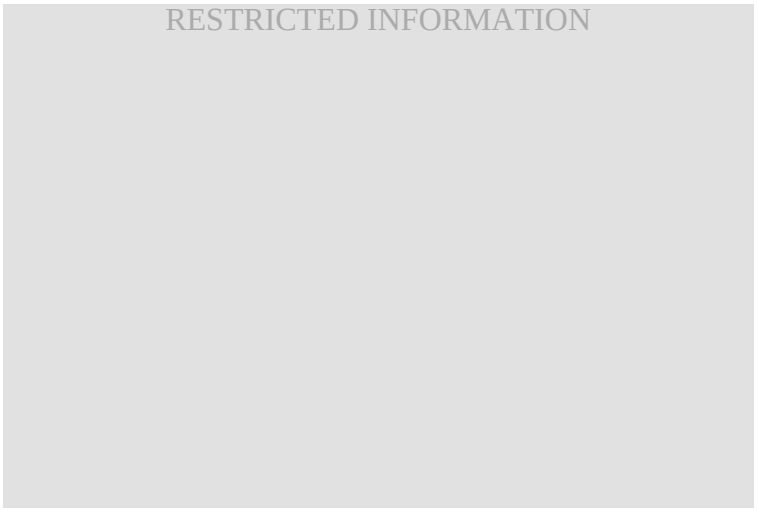
This Chapter depicts the design of a Module in Package (MiP) for automotive instrument clusters. A brief background about applied research work in this area is overviewed in Section 4.1 along with design constraints and a detailed design description. Moreover, the assembly process of said MiP is described in detail in Section 4.2. Robustness test results are portrayed along with the electrical performance of the resultant interconnects.

As a result, a patent invention is disclosed in Section 4.3, which proposes to apply a cost-effective interconnect geometry between two printed circuit boards, that allows the transfer of a big amount of high frequency signals by the coalescence or fusion of a vastly malleable metal alloy, whose flexibility guarantees the interconnect integrity without fractures against multiple thermal shocks in a temperature range of –40 °C to 105 °C.

4.1. Design of a Module in Package Tailored for the Automotive Environment

As consumers demand high definition (HD) video of up to 5k resolution in the automotive instruments, high-end mobile computing processing is needed. This entails the use of high density interconnect (HDI) printed circuit board (PCB) technology, with more than 10 conductive layers and with laser precision, which increases production costs significantly.

In order to provide a cost-effective solution, developing with a module in package technology (MiP) approach for an automotive instrument application is considered in this report. A brief description of the conceptual design and background is depicted in Section 4.1.1. Subsequently, the design constraints are portrayed in Section 4.1.2. Then, a full design description is described in Section 4.1.3.



a) b)

Fig. 4.1 MIP concept: a) top side, b) bottom side.

4.1.1 MiP Concept

Continental AG module in package (MiP) technology is an electrical board-to-board bonding of the integration of a graphics processor, memory, and power supplies into a SiP-like package, tailored for automotive environments and automotive manufacturing processes, as that one shown in Fig. 4.1, attached to a full digital automotive instrument cluster (FDC). It pursues lowering the overall PCB materials' cost by reducing HDI technology usage to the bare minimum. In this case, HDI usage applies only to the PCB of the MiP which can be a complex multilayer PCB (8-layer or more), thus requiring only a standard low-layer-count PCB for the FDC application board, such as a 4-layer, 1.6 mm thick standard PCB, as shown in Fig. 4.2.

Additionally, the FDC design may become scalable by allocating different processor/suppliers in the same FDC design through a standardized MiP concept. In fact, the validation efforts can be reduced within different stock keeping units (SKU), variants or product trims for the FDC.

In order to achieve a MiP with the frequency response required by a high-end mobile computing processor, the automotive environmental requirements, and the low cost but robust manufacturing approach, several cost reduction techniques have been applied, such as those described in [del-Rey-14], [del-Rey-14a], [del-Rey-14b], [del-Rey-15a], [del-Rey-16]. Therefore,

Fig. 4.2 Application board with MIP concept.

impedance matching analysis, EM modeling, and optimization of transmission lines for high-speed digital I/O were exerted in a model-based design approach through virtual prototyping before manufacturing, along with the correlation of EM simulations against measurements, and the thermal performance of the overall design.

Additionally, to accomplish a successful robust and low-cost PCB to PCB bonding with high frequency performance and EMC requirements into consideration, several approaches for board-to-board bonding technology have been investigated in [del-Rey-17a], [del-Rey-17b], [del-Rey-17c], [del-Rey-18].

4.1.2 Design Constraints

High frequency effects and electromagnetic compatibility (EMC), part handling, package bumping, manufacturing, and reliability are the top constraints enforced to guarantee a robust automotive design, as described below.

4.1.2.1 High Frequency Performance and EMC

For the signal integrity, the fastest interconnects in the automotive instrument cluster are the processor to memory and the processor to display buses. Since memory is included inside the MiP concept, its handling is the same as in any high-speed digital design. For the processor to

display bus, which interconnects through MiP external I/Os, the low-voltage differential signaling (LVDS) display channel in a resolution of 1920 × 1080 pixel @ 60 Hz works at a clock frequency of 148.5 MHz (dotclock), and maximum data frequency of 519.75 MHz for the serializer clock by using two LVDS channels in split mode [NXP-16]. Therefore, in order to maintain a good-enough data transmission, the MiP interconnects should allow for at least the fifth harmonic of the fastest signal, which corresponds to a frequency precisely of 2.59875 GHz for the LVDS serializer clock [Johnson-11].

Likewise, a good power integrity is needed for any processor demanding high core frequencies. The processor vendor provides the maximum impedance response specification needed to allow enough energy for uninterrupted operation for the CPU core's power rail. A good power distribution network (PDN) design should be considered for fulfilling this requirement.

EMC is the most difficult-to-predict part in an automotive electrical design, due to the high amount of interaction with mechanical parts in the instrument clusters. However, its impact can be minimized by applying good PCB layout techniques that enhance the signal and power integrity considerations at the same time.

4.1.2.2 Part Handling

In order to become competitive, a MiP-based design should comprise a minimum handling effort. The system-in-package MiP should be able to be mounted as easy as a large IC chip.

4.1.2.3 Package Bumping

A robust cost-effective bumping technology must be used for the MiP to FDC application board bonding and interconnection. Based on the assessment made in [del-Rey-18], a stencil solder paste based printing process is followed.

4.1.2.4 Manufacturability

In order to warrantee repeatability in the mass production manufacturing, the standards from the association connecting electronic industries (IPC) should be followed. The most applicable IPC standard is the IPC-7095C, which refers to the design and assembly process implementation for BGAs [IPC Sd IPC-7095C]. Additionally, care must be taken for components

placement sequence, since available components certified by the automotive electronics council (AEQ-Q200) are the most rugged ones, being able to withstand up to 3 reflow processes. PCB layout must ensure that the components non-compliant with 3 reflow processes are placed in a side that will not be subject to 3 or more reflow processes.

4.1.2.5 Robustness

In order to have a design useful for the automotive environment, a specific robustness criterion is defined for an automotive system to surpass vibration, humidity, mechanical shocks, and thermal shocks. Vibration is controlled with the solder paste alloy and its reflow process and the AEQ-Q200 certification of the components. This is currently a standard practice in any automotive electronics manufacturing facility.

In order to minimize humidity concerns, the moisture on the PCBA surface is controlled by covering the sensitive circuitry (e.g., high voltage networks). A mechanical back cover is typically specified for all automotive instrument cluster products.

Mechanical and thermal shocks are controlled with a good mechanical design. The product housing, lens, covers, and the mounting holes, tabs, and clips are crucial to minimize mechanical fatigue of the electrical circuits.

Finally, in the electronics design arena, a good PCB layout and the substrate material

Fig. 4.3 Design of experiments (DoE) study conducted at Continental AG to obtain the maximum weight a solder bump is able to withstand. From [Seitz-15]

Fig. 4.4 MIP rough cost estimation. An inflection point is depicted in which the cost savings increases with the PCB area.

selection / symmetry can reduce the warpage that can occur in a thermal event, along with the weight balance of the component placement. In order to prevent the collapse of certain BGA bumps, a design of experiments (DoE) study was conducted in Continental in 2015, in which it was found that a 0.75 mm diameter BGA ball can support up to 0.1 grams, as illustrated in Fig. 4.3 [Seitz-15].

4.1.2.6 Cost

The complete MiP assembly, including logistic costs, should provide a competitive advantage against not using it. Potential costs for scrapping material due to the inclusion of a new technological process should also be included into the calculation. The inclusion of a board to board methodology incurs in additional costs up to an inflection point, where the FDC application PCB area cost is higher due to layers and materials usage, rather than applying a low complexity PCB for the application board with the MiP approach. Such inflection point can be seen in Fig. 4.4.

4.1.3 Design Description

Design description of MiP in this Section is segmented in the architecture of the high-frequency graphics processor, the geometrical solution customized for the automotive, the high-frequency design details, the solder paste print stencil design specification, and a power calculation

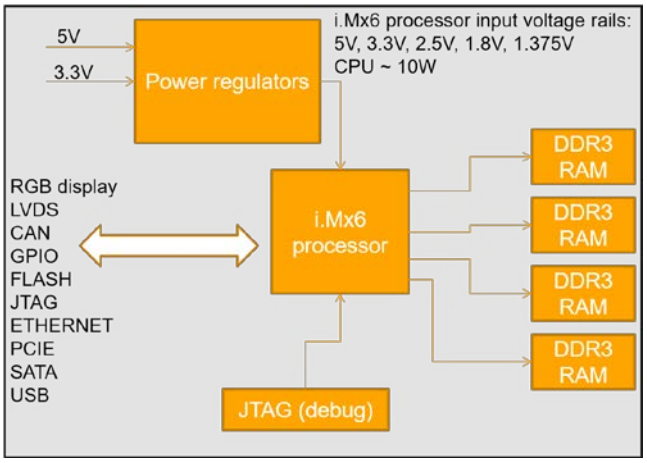


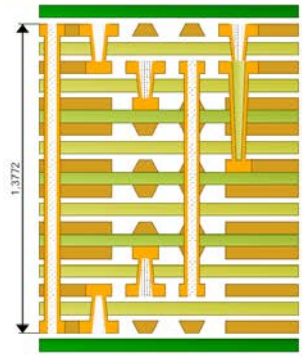
Fig. 4.5 MIP architecture is based in the i.MX6 processor.

Fig. 4.6 Rounded-rectangle ring interconnects.

and expected thermal behavior. Additionally, the test FDC application board is described along with brief testability requirements.

4.1.3.1 MiP Architecture

MiP design is based on the i.MX6 processor from NXP Semiconductors. Its corresponding architecture's block diagram is shown in Fig. 4.5. To take advantage of its highest available bandwidth, four DDR3 memories, 4 Gb each (256 M × 16) at 800 MHz have been selected. A dedicated voltage regulator is placed inside MiP for the i.MX6 core voltages power supply, and another dedicated voltage regulator is placed for the DDR3 power supply. A program/debug JTAG connector is also provided inside MiP in order to enable in-house standalone testing. All I/Os are routed through MiP interconnects, including eMMC and synchronous NOR flash memories, whose usage is left open for the FDC design to maximize flexibility within different application projects.



Lagenaufbau	Basisdicke	verpresste Dicke	Kupferverteilung	εr	Type	Beschreibung	Masken-Dicke	Farbe	Impedanz ID	Hersteller	Herstellerbezeichnung
				4,000	SolderMask	Liquid Photolmageable Mask	0,025	Green		Peters	SM/001
	0,012	0,037	80,000		Copper	Copper Foil			1, 2	Polar Samples	FO/004
	0,078	0,070		3,910	PrePreg	1080				Isola	IS400
	0,012	0,037	80,000		Copper	Copper Foil				Polar Samples	FO/004
	0,078	0,070		3,910	PrePreg	1080				Isola	IS400
	0,018	0,018	80,000						3, 4		
	0,250	0,250		4,340	Core	2 x 2165				Isola	IS400
	0,018	0,018	80,000								
	0,078	0,070		3,910	PrePreg	1080				Isola	IS400
	0,018	0,018	80,000								
	0,200	0,200		4,420	Core	1 x 7628				Isola	IS400
	0,018	0,018	80,000								
	0,078	0,070		3,910	PrePreg	1080				Isola	IS400
	0,018	0,018	80,000								
	0,250	0,250		4,340	Core	2 x 2165				Isola	IS400
	0,018	0,018	80,000						5, 6		
	0,078	0,070		3,910	PrePreg	1080				Isola	IS400
	0,012	0,037	80,000		Copper	Copper Foil				Polar Samples	FO/004
	0,078	0,070		3,910	PrePreg	1080				Isola	IS400
	0,012	0,037	80,000		Copper	Copper Foil			7, 8	Polar Samples	FO/004
				4,000	SolderMask	Liquid Photolmageable Mask	0,025	Green		Peters	SM/001

Fig. 4.7 Ten layers PCB stackup with HDI used in MIP. From [MOS-13]

RESTRICTED INFORMATION

Fig. 4.8 MIP package geometry (ball side).

4.1.3.2 MiP Geometry

The best way to obtain a high density of interconnects between the board to board interface is by resembling the ball array of a BGA. In order to reduce warpage during a thermal event, a symmetrical grid array must be laid out. Also, round-alike bonding geometries work better for reducing warpage, but rectangular geometries save space and maximize placement area. Hence, a rounded rectangle ring is selected as the best electromechanical interface for the MiP to the FDC board, as shown in Fig. 4.6.

The MiP maximum package size is [redacted] mm, and this limit is driven by the available pick and place machine[17] automated optical inspection (AOI) needed for aligning the component during the placement process. Driven by the i.MX6 processor, which comes in a 21 × 21 mm package with 0.8 mm ball pitch and an array of 25 rows and 25 columns, a 10-layer stackup with HDI is chosen for the first prototype, as shown in Fig. 4.7 [MOS-13]. HDI is needed to avoid thru hole vias interfering with the MiP interconnection grid ball-out. The package geometry of the MiP can be seen in Fig. 4.8.

4.1.3.3 High Frequency Design

NXP i.MX6 processor comes in a FCPBGA 624 package, which consist of 107 pads for ground connection (GND), 113 pads for core power rail, 121 pads for DDR interface, and 283

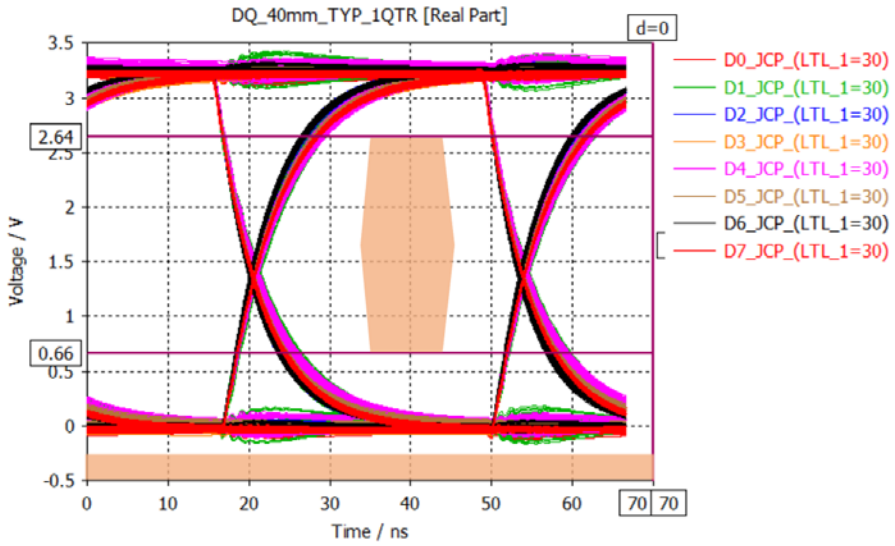


Fig. 4.9 NAND flash memory I/O bus simulation.

[17] Siplace X-series Pick and Place Solution, ASM Assembly Systems GmbH & Co., Munich, Germany, 2016.

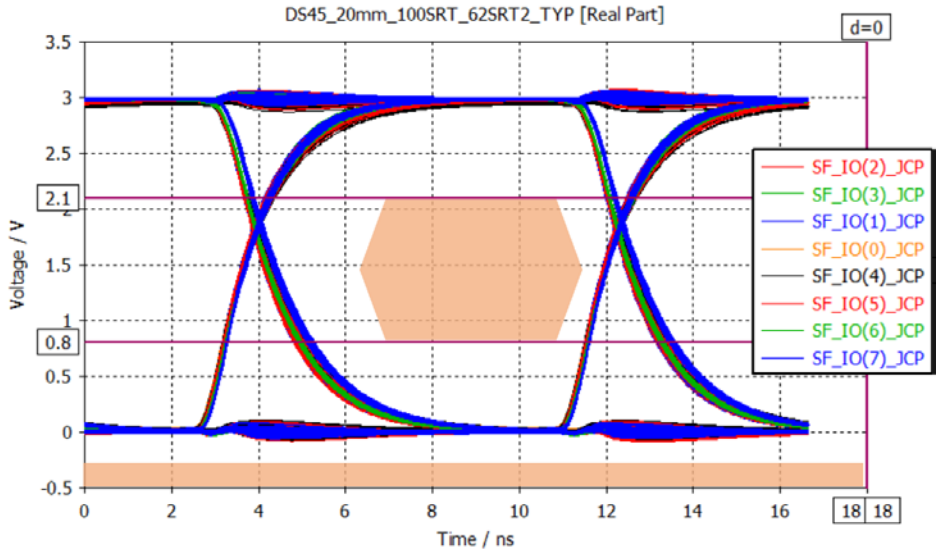


Fig. 4.10 NOR flash memory I/O bus simulation.

pads for I/O buses, which must be routed to the application board. The complete MiP with its components resulted in a weight calculation of [redacted] g. For this reason, a total of [redacted] I/Os have been defined to interconnect the MiP to the applications board, which translates in supporting the double of the weight calculated, allowing for some mechanical stress. To enhance the EMC performance, a third of these interconnects are selected to connect to ground, which are spread over the entire MiP, with the purpose to contain the electric fields within the circuitry.

In order to fulfill the high frequency requirements of the applications processor chosen, vendor recommendations from [NXP-16] were followed and simulated for every different signal technology, such as NAND and NOR flash memories, low-voltage digital signaling (LVDS), and ethernet media independent interface (MII). Correspondingly, Fig. 4.9 shows the I/O bus eye-diaram simulation of NAND flash memory, Fig. 4.10 shows the the I/O bus simulation of serial NOR flash memory, Fig. 4.11 shows the I/O bus simulation of LVDS display, and Fig. 4.12 shows the I/O bus simulation of ethernet media independent bus (MII). All these eye diagram simulations depict an irregular hexagon added as the success criteria.

Additionally, the ball interconnect was modeled using a 3D full-wave electromagnetics simulator, as shown in Fig. 4.13. It is seen from Fig. 4.14 that its EM frequency response is almost ideal in the selected frequency range. This EM model was later incorporated into circuital and behavioral simulations, as shown in Fig. 4.15. The tool used for EM simulations is CST[18].

[18] CST Microwave Studio 2016, CST AG, Darmstadt, Germany, 2016.

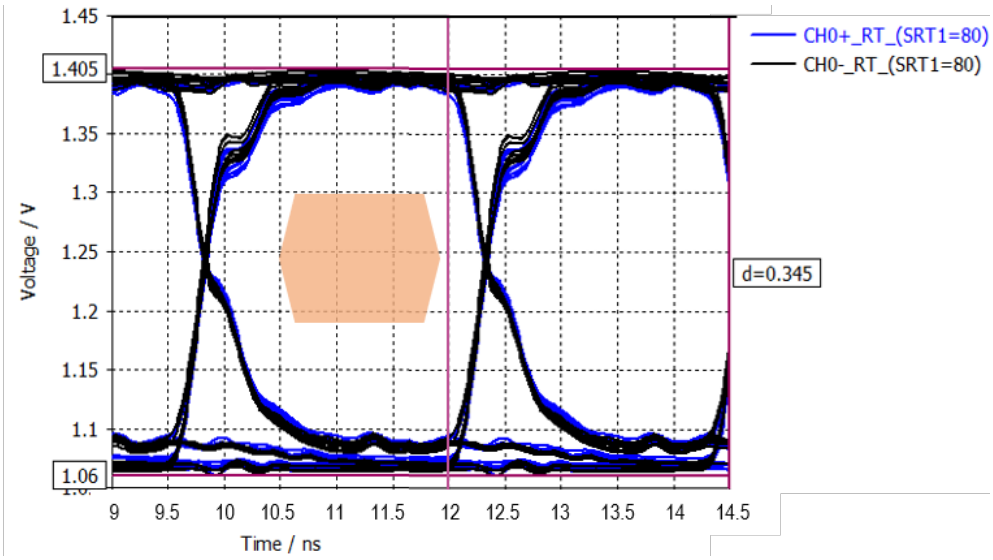


Fig. 4.11 LVDS display bus I/O simulation.

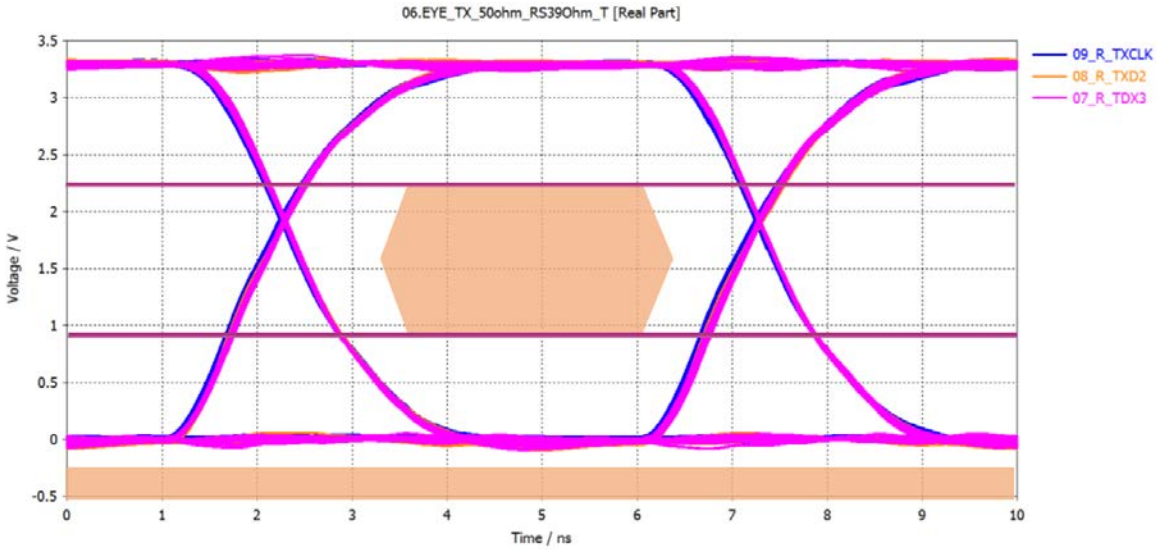


Fig. 4.12 MII (ethernet) media independent bus I/O simulation.

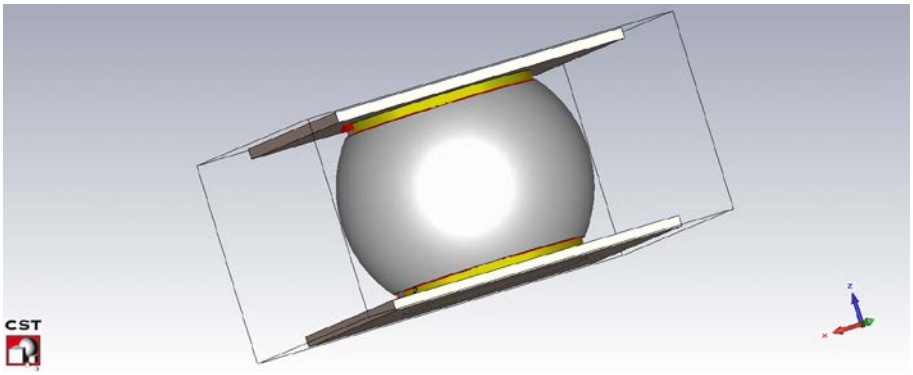


Fig. 4.13 MIP ball interconnect 3D EM model.

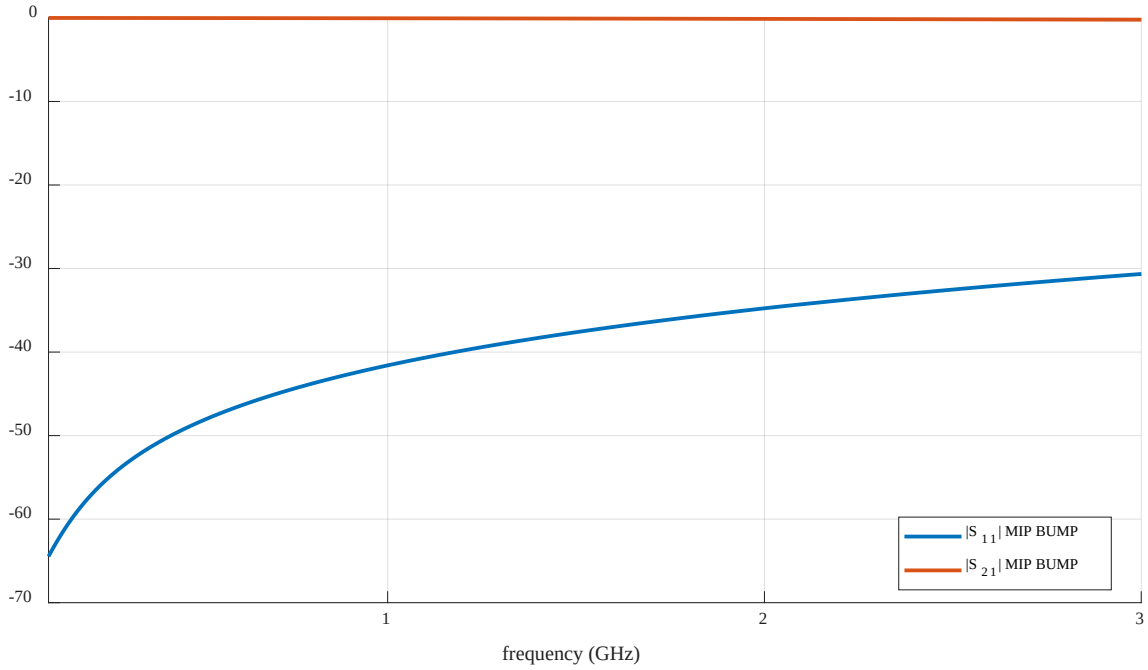


Fig. 4.14 Frequency response of MIP ball interconnect model.

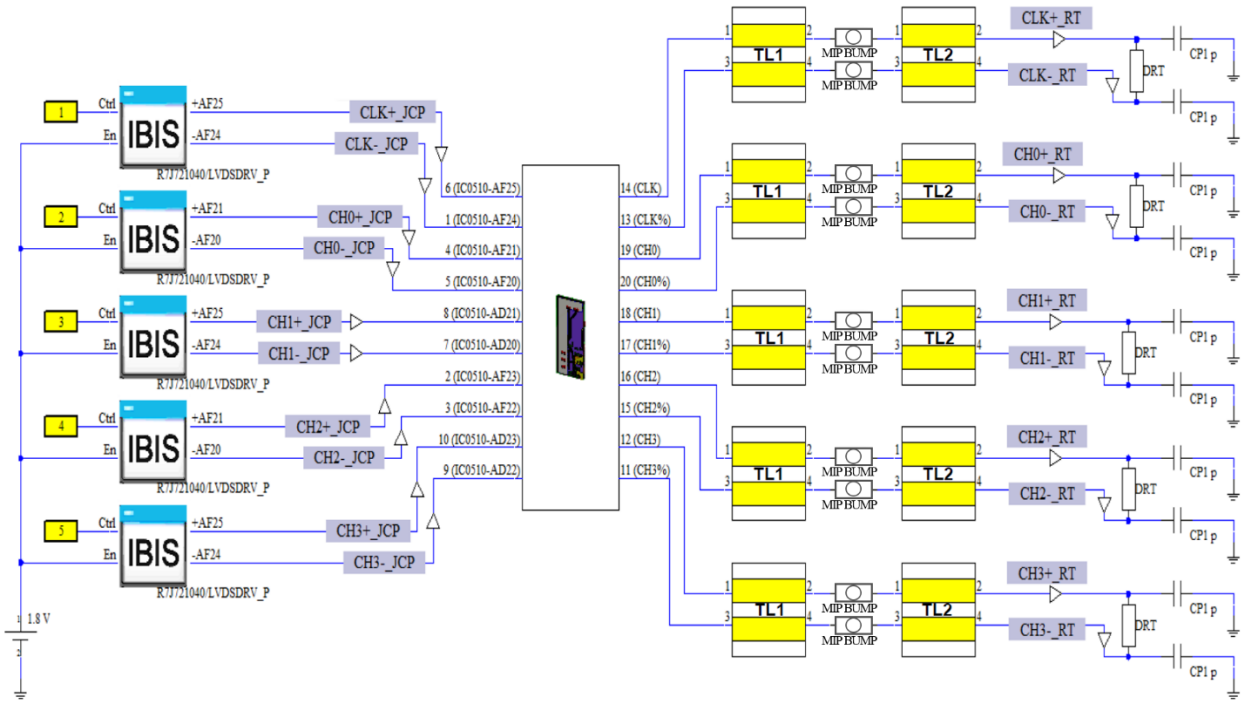


Fig. 4.15 EM simulation model including MIP ball interconnect model.

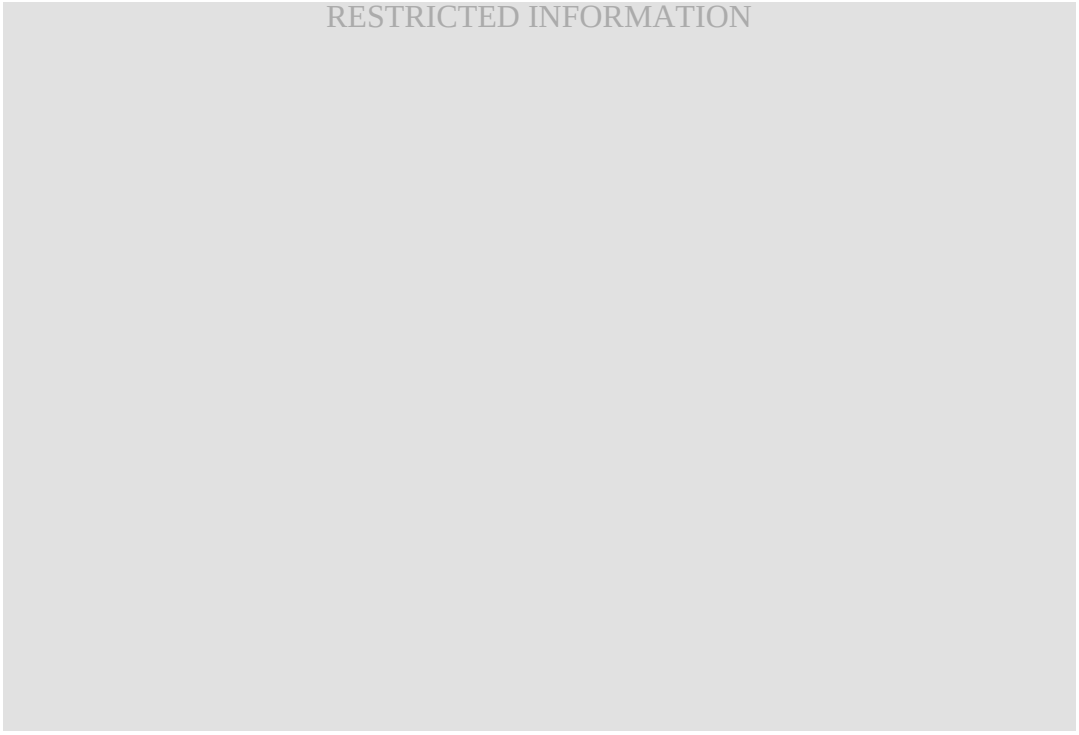


Fig. 4.16 Fanout of MIP landing in application board, with a cutout to allow passives underneath MIP.

Reducing the inductance of the PDN is crucial for minimizing the number of decoupling capacitors needed. Thus, allowing decoupling capacitors placement as close as possible to their respective processor interconnect is anticipated. The closest location to the processors' interconnects is right underneath the processor, on the secondary side of the MiP. In order to achieve that, a square hole is proposed to be added to the application board, beneath MiP placement and centered within MiP ball grid interconnects, as shown in the landing description of the MiP on the application board schematized in Fig. 4.16, and later laid out in CAD as shown in Fig. 4.17.

Consequently, to accomplish the PDN response required by i.MX6 processor, the MiP should present a PDN with a maximum impedance response specified by the vendor. Therefore, an impedance behavior is required in MiP to be equal or below the VDDARM_CAP plot [NXP-16]. Hence, a total of 130 capacitors were placed into the design, resulting in the simulated response shown in Fig. 4.18 for the VDDARM_CAP voltage rail.

Fig. 4.17 Application board for the MIP design, with a cutout hole to allow passives underneath

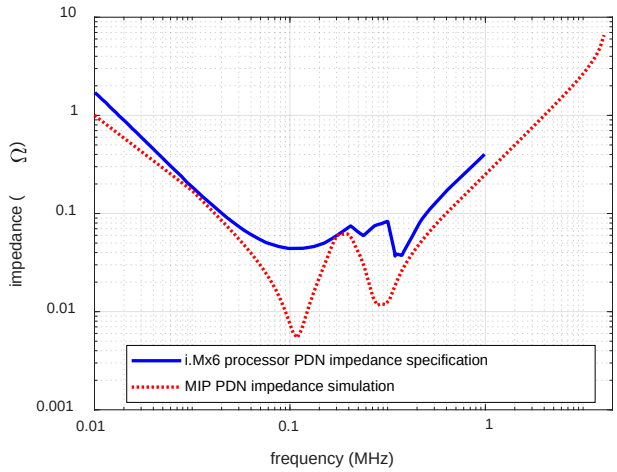


Fig. 4.18 Core power rail impedance specification requirement from i.MX6 processor vendor as compared against MIP design simulation.

4.1.3.4 Solder Paste Print Stencil Design for MiP Interconnection Bumping

According to IPC standards IPC-7095C [IPC Sd IPC-7095C] and IPC-7351B [IPC Sd IPC-7351B], "the land pattern of the component (where the ball is attached) and the land pattern of the substrate mounting structure (printed board) should be as similar as possible". Henceforth, we will calculate the PCB landing pad in a practical way with a reduction in percentage from the calculated interconnecting ball diameter, as shown in Table 4.1 [IPC Sd IPC-7351B]. The target nominal ball diameter is [redacted] mm for this design, and thus, we can choose a land diameter in the range of [redacted] mm and [redacted] mm.

TABLE 4.1. LAND APPROXIMATION FOR COLLAPSIBLE SOLDER BALLS

Nominal Ball Diameter (mm)	Reduction	Nominal Land Diameter (mm)	Land Variation (mm)
0.75	25%	0.55	0.60 – 0.50
0.65	25%	0.50	0.55 – 0.45
0.60	25%	0.45	0.50 – 0.40
0.55	25%	0.40	0.50 – 0.40
0.50	20%	0.40	0.45 – 0.35
0.45	20%	0.35	0.40 – 0.30
0.40	20%	0.30	0.35 – 0.25
0.35	20%	0.28	0.33 – 0.23
0.30	20%	0.25	0.25 – 0.20
0.25	20%	0.20	0.20 – 0.17
0.20	15%	0.17	0.20 – 0.14
0.17	15%	0.15	0.18 – 0.12
0.15	15%	0.13	0.15 – 0.10

Due to the square hole proposal to allow passive components underneath the processor on MiP, the stencil design for obtaining a highly repeatable and robust interconnection bumping on the MiP surface is not trivial. The IPC-7351B standard [IPC Sd IPC-7351B] specifies a maximum volume of solder paste for surface mount components (SMD) per pad landing area, and the volume control for the MiP solder bumps can not only be controlled with the aperture diameter. For this reason, a laser etched step stencil is chosen. The height of the finished bump after the reflow process can be estimated using

$$B = \frac{\left[3vq^{\frac{1}{2}} + \left(\left(\left(\frac{y}{2}\right)^{6}\pi^{2} + 9qv^{2}\right)^{\frac{1}{2}}\right)\right]^{\frac{2}{3}} - \pi^{\frac{2}{3}}\left(\frac{q}{2}\right)^{2}}{\left(\pi^{\frac{1}{3}}q^{\frac{1}{2}}\right)\left[3vq^{\frac{1}{2}} + \left(\left(\frac{y}{2}\right)^{6}\pi^{2} + 9qv^{2}\right)^{\frac{1}{2}}\right]^{\frac{1}{3}}} \tag{4-1}$$

where y is the bond pad diameter, q is the truncated sphere shape factor (a value of 1.2, commonly), v is the volume of metals in stencil aperture (usually corresponds to the stencil aperture area ×

stencil height × ζ), ζ is the solder paste composition ratio or metals/flux resins, and *B* is the bump height. Following [Pac Tech-13], the finished bump diameter can be estimated by

$$B1 = \left[\frac{v}{\left(\pi q^{\frac{1}{2}} + q^{\frac{1}{2}} \frac{B}{3} \right)} + q^{\frac{1}{2}} \frac{B}{3} \right]^2 \tag{4-2}$$

Solder paste particle size also affects the occurrence of solder bumps, due to the increased amount of oxidized-metallic surface area in the solder paste [Arra-02]. In order to successfully accomplish a solder bump through a stencil printing process, two guiding principles must be followed [Indium-10]:

a) Sbiroli's Rule

This rule states that the width of the stencil opening must be at least the size of 7 solder paste particles or greater.

b) Anglin's Rule

An aperture ratio should not be less than 1.6, which can be calculated using

$$\frac{a}{2h\left(\frac{p}{2} \right)} \geq 1.6 \tag{4-3}$$

where *a* is the area, *p* is the perimeter, and *h* is the height of the stencil aperture.

The empirical rule given by (4-3) originates from boundary-layer-type considerations of release from the stencil walls by the pseudoplastic/thixotropic solder paste material.

In an internal experiment at Continental AG [Seitz-15], it was found that solder paste powder size must be in a range of [redacted] to [redacted] µm, with a flux proportion of [redacted]%, estimated by weight, since these parameters and its viscosity are important concerning the solder paste removing behavior.

Additionally, the solder mask has been reported to be one of the most important factors affecting the generation of solder balls [Arra-02]. Since a rougher surface reduces the adhesion of the solder to the solder mask, the solder mask aperture should be controlled to maximize adhesion while minimizing unintentional solder shorts or bridges.

Thus, the resulting ball diameter is [redacted] mm for a land diameter of [redacted] mm, a solder mask opening diameter of [redacted] mm for non-solder mask defined pads (NSMD) and a ball to ball pitch

Fig. 4.19 MIP ball interconnect geometry.

of [redacted] mm, as shown in Fig. 4.19. This geometry resulted in the best controllable solder paste volume by also using [redacted] Pb-free solder paste in a Dek[19] solder paste printer, as shown in Fig. 4.20. Said solderpaste has a powder size in the range of [redacted] to [redacted] µm [Senju-04]. Consequently, solder paste step stencil design is tailored with a base thickness of [redacted] µm and an overall height of [redacted] µm, as shown in Fig. 4.21. A component keepout zone is enforced in PCB layout placement, due to the proposed step in the solder paste print stencil, since some solderpaste will remain deposited within the step in the solderpaste print stencil, as shown in Fig. 4.22.

4.1.3.5 Power Calculation, Power Budget, Thermal

i.MX6 processor has a current consumption in the range of 3.86 to 4.125 A with a core VDD supply rail of 1.42 V, which translates in a worst-case power dissipation of 5.8575 W. Due to thermal resistance inside i.MX6 package, whose calculation procedure is shown in Fig. 4.23, the processor junction to case temperature can rise up to 117 °C, and thus, a heat spreader solution is mandatory. For this reason, a thermal simulation was conducted in FloTHERM[20], as shown in Fig. 4.24, in order to predict the amount of metal in the heat sink.

To effectively dissipate the heat generated, a metal plate with a minimum dimension of 164.7 × 127 × 4.6 mm resulted from this simulation. This volume of metal can be provided with a back cover made of a thermal conductive material, such as cast aluminum.

[19] Dek Galaxy Series Printing Solution, ASM Assembly Systems GmbH & Co., Munich, Germany, 2016.
[20] FloTHERM v10.0, Mentor Graphics Inc., Wilsonville, OR, 2016.

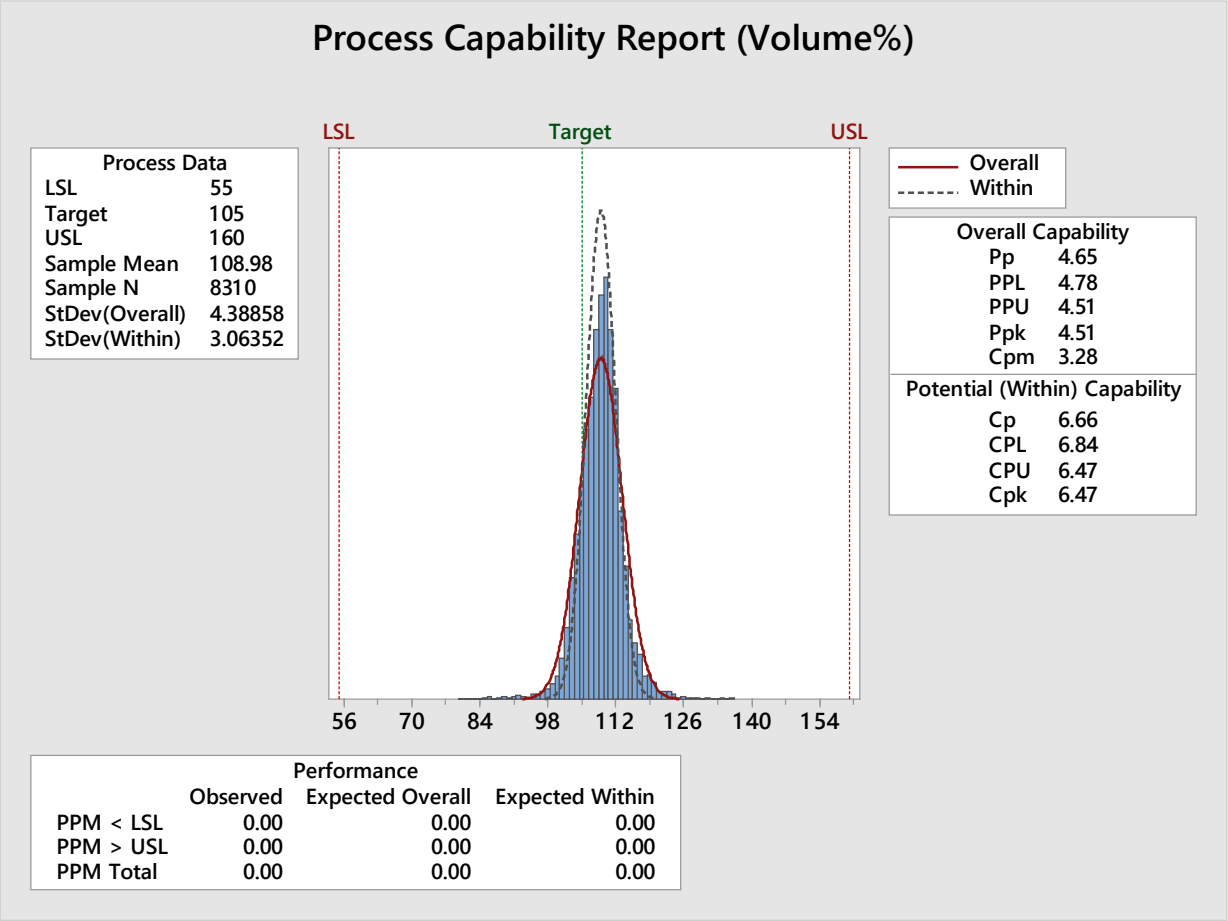


Fig. 4.20 Statistical analysis of solder paste printed volumes for MIP ball interconnects.

Fig. 4.21 Step stencil design geometry. From [del-Rey-18c].

Fig. 4.22 Step stencil used for MIP.

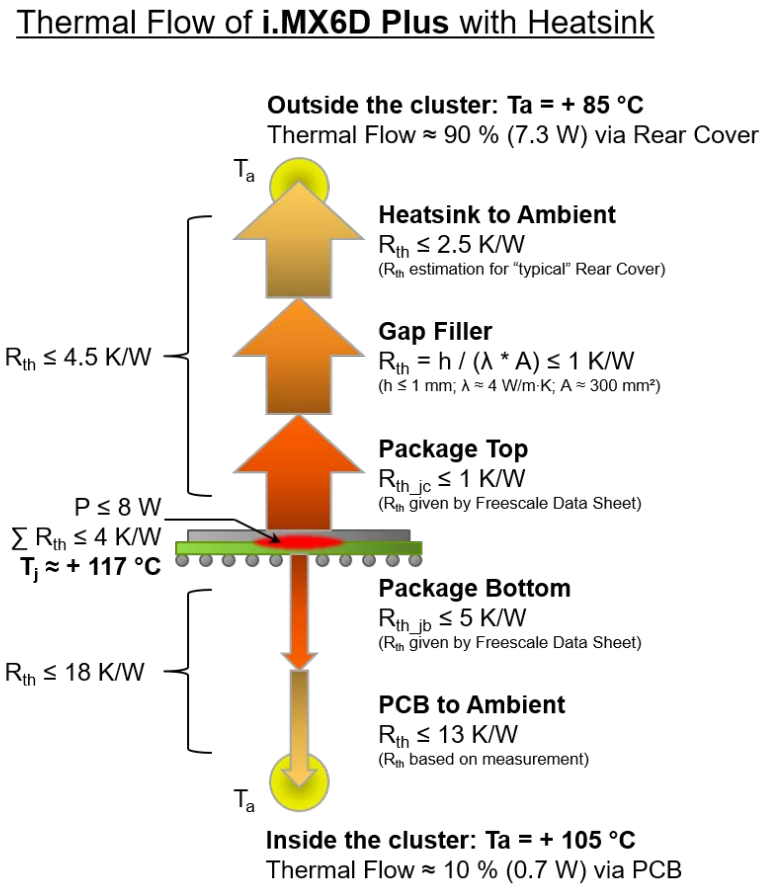


Fig. 4.23 i.MX6 thermal resistance calculation.

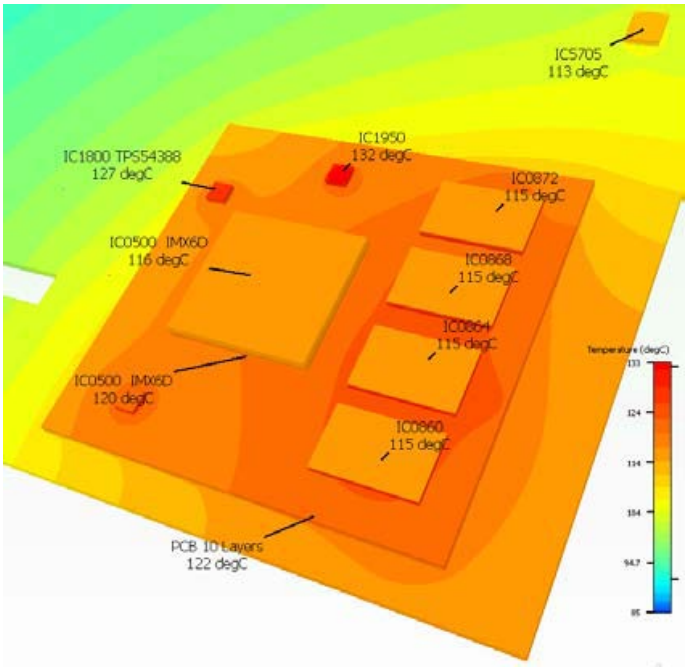


Fig. 4.24 MIP thermal simulation.

Lage	Lagenaufbau	Basisdicke	verpresste Dicke	Kupferverteilung	εr	Type	Beschreibung	Masken-Dicke	Farbe
					4,000	SolderMask	Liquid PhotoImageable Mask	0,025	Green
1		0,018	0,043	0,000		Copper	Copper Foil		
		0,132	0,119		4,180	2116	2116		
		0,201	0,181		4,280	7628	7628		
2		0,035	0,035	0,000					
	1,4654	0,710	0,710		4,200	Core	0.71mm		
3		0,035	0,035	0,000					
		0,201	0,181		4,280	7628	7628		
		0,132	0,119		4,180	2116	2116		
4		0,018	0,043	0,000		Copper	Copper Foil		
					4,000	SolderMask	Liquid PhotoImageable Mask	0,025	Green

Fig. 4.25 Four-layer standard PCB stackup used for FDC application board. From [MOS-09]

4.1.3.6 Test FDC Application Board Description

The test application board, depicted in Fig. 4.17, includes the automotive power supply solution, flash memories to store the application software, display connectors such as LVDS and RGB video buses, an encryption/immobilizer circuitry, and serial communications circuitry, such as CAN, LIN, UART, Ethernet, JTAG and USB. The last ones are provided for programming and debugging task.

Additionally, an automotive microcontroller is necessary in order to provide the startup

power-on sequence, and other functions such as gasoline level signal processing, and hazard telltales. All these features should fit into a 4-layer standard PCB stackup, like the one shown in Fig. 4.25 [MOS-09].

4.1.3.7 Testability

MiP should be designed with mass-production testability in mind. Fully exposed test points for in circuit test (ICT) have been added, along with a dedicated JTAG connector on MiP PCB, for standalone power-on verification.

4.2. Assembly Process and Test of a Module in Package Customized for the Automotive Environment

This Section describes the assembly process of an automotive fully digital instrument cluster (FDC) by using the MiP technology, specifically depicting the solder-paste-printed based bumping process due to its availability and cost-effectiveness [Arnold-16]. After manufacturing some prototypes, the corresponding results from a number of technical verifications are also presented.

4.2.1 Assembly Description and Set-Up

The flow to manufacture regular surface mount technology (SMT) consists of four main

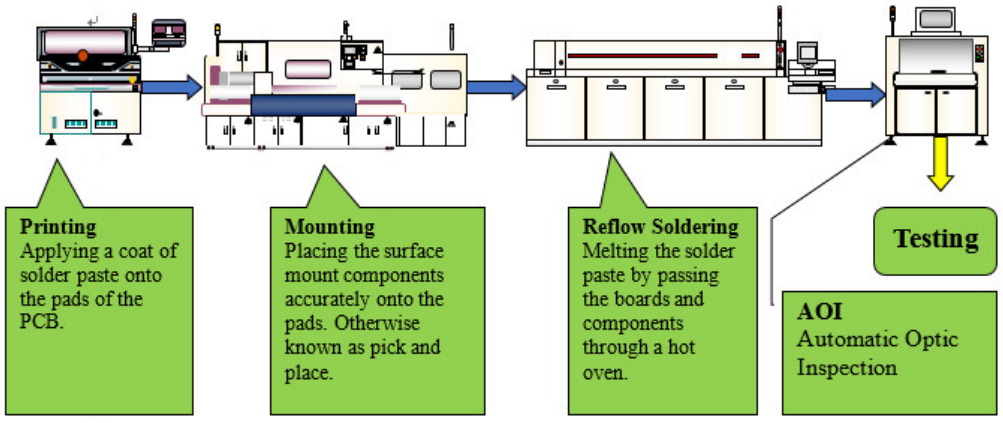


Fig. 4.26 Surface mount technology manufacturing steps. From [Seeed Tech.-17]

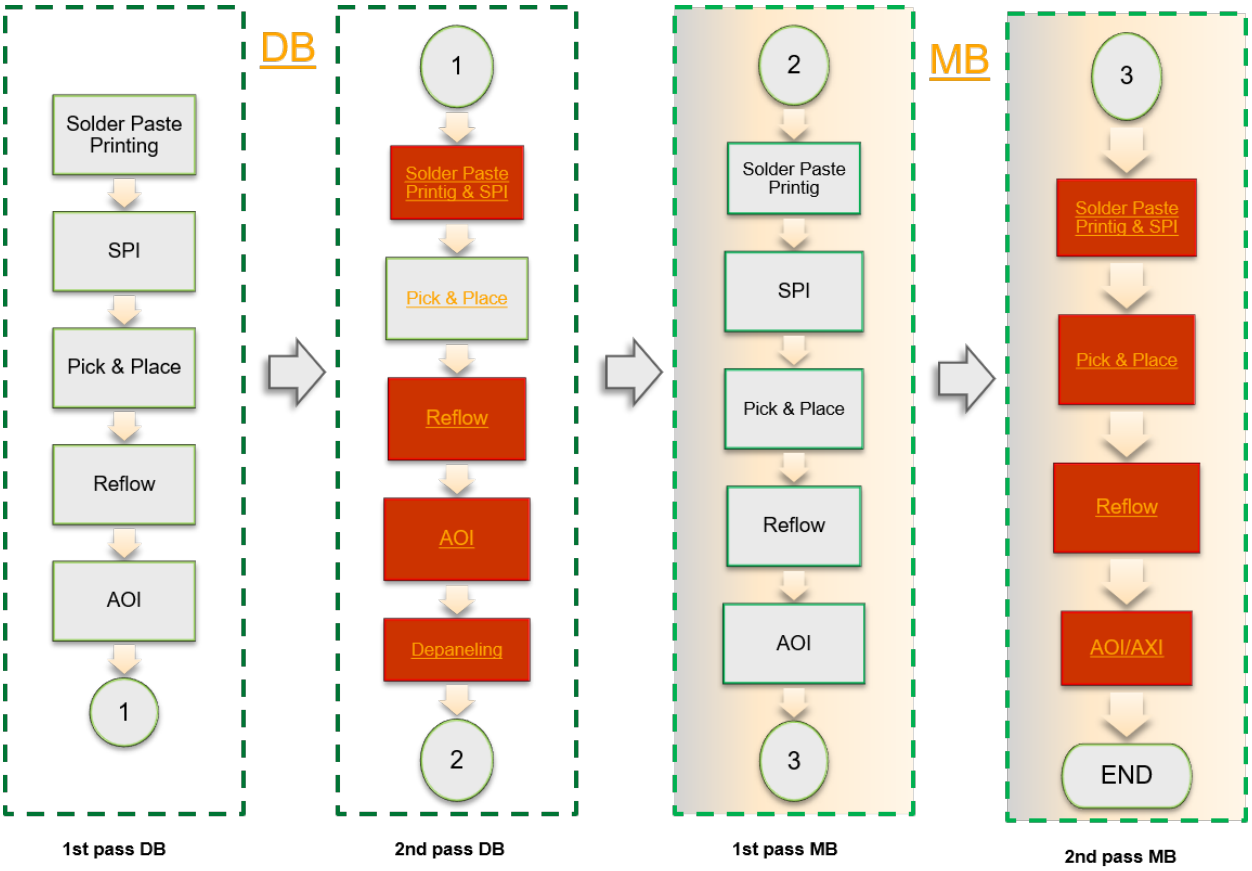


Fig. 4.27 Prototype assembly process.

steps: printing, mounting, reflow soldering, and testing, as depicted in Fig. 4.26 [Seeed Tech.-17]. In order to guarantee an error-free operation, there are additional stages for inspection between steps, such as solder paste inspection (SPI) after printing, automated optical inspections (AOI) during mounting, and automated X-ray inspections (AXI) after reflow.

The FDC prototype built in this work consists of a minimum computer system module in package (MiP) held onto a daughter board (DB) module, bonded to an automotive instrument cluster application board or mainboard (MB) through solder paste printed interconnects or bumps. For this reason, four different SMT processes are executed, one per PCB assembly surface, starting with the DB and then the MB, as shown in Fig. 4.27. Hereafter, the following machinery was used:

a) Solder paste transfer (SPT): [redacted]
b) SPT Inspection: [redacted]
c) Component placement: [redacted]
d) Reflow oven: Rehm, [redacted]
e) Solder joint inspection: [redacted]

TABLE 4.2. MAXIMUM AND MINIMUM INTERCONNECTS' HEIGHTS PER SIDE OF THE BOARD

Cross-section plane	Minimum		Maximum	
	Ball	Height (mm)	Ball	Height (mm)
A1	34	0.325	07	0.347
A2	39	0.294	03	0.326
A3	02	0.302	23	0.335
A4	04	0.314	35	0.345

4.2.2 Daughter Board Assembly Process

The main targets for the DB assembly are to create a 100% of solder bonding interconnects, with a consistent volume, no solder shorts or bridges and an excellent process capability index Cpk ≥ 1.67, which is a standard safety or critical parameter for a new process [NIST-13]. For the solder paste print set-up, the following parameters were applied:

a) Stencil supplier: [redacted]
b) Stencil type: [redacted]
c) Squeegee: [redacted]
d) Solder paste: [redacted]
e) Print speed: [redacted]
f) Print pressure: [redacted]
g) Separation speed: [redacted]
h) Separation distance: [redacted]

A solder paste printed DB is shown in Fig. 4.28. No insufficient or excess solder was found.

Fig. 4.28 Solder paste printed daughter board.

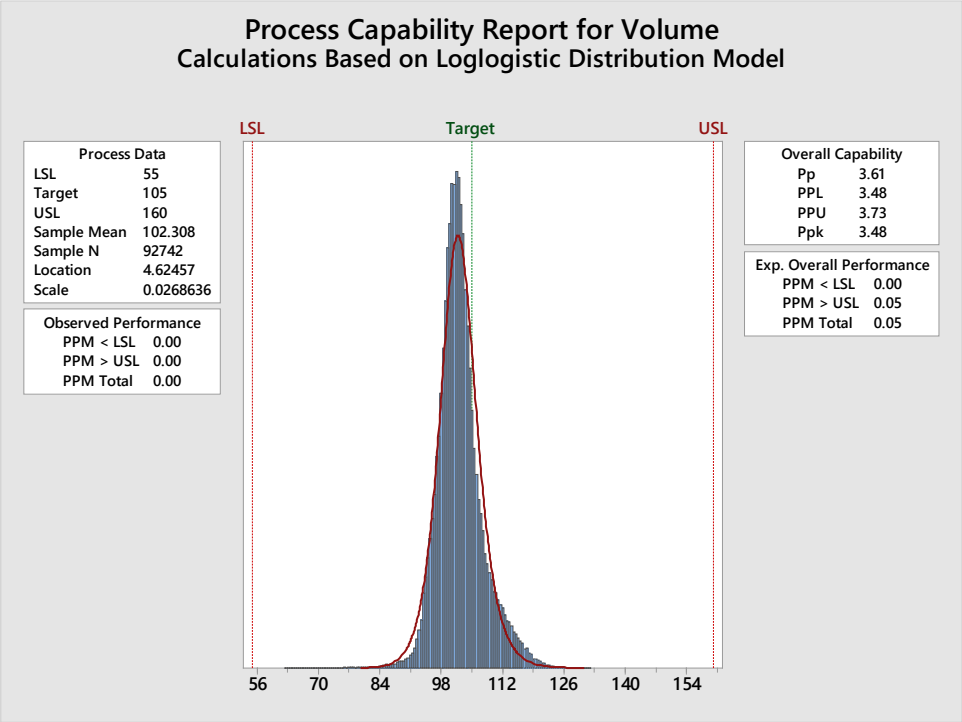


Fig. 4.29 Process capability index for the solder paste printed daughter board.

Fig. 4.30 Solder paste printed daughter board with surface mount components.

The solder paste printing process exhibited a reliable performance with a process performance index Ppk = 3.48 at the interconnect area, as shown in Fig. 4.29. For the surface mount component placement process no issues were observed. The resultant sample is shown in Fig. 4.30. Reflow profile from Fig. 4.31 was followed, according to the solder paste manufacturer recommendations. The resultant interconnects after reflow can be seen in Fig. 4.32.

After AOI inspection, no solder paste migration nor any other issue was observed. In fact, a bad board sample had to be created to assure failures detection before normal production, as shown in Fig. 4.33.

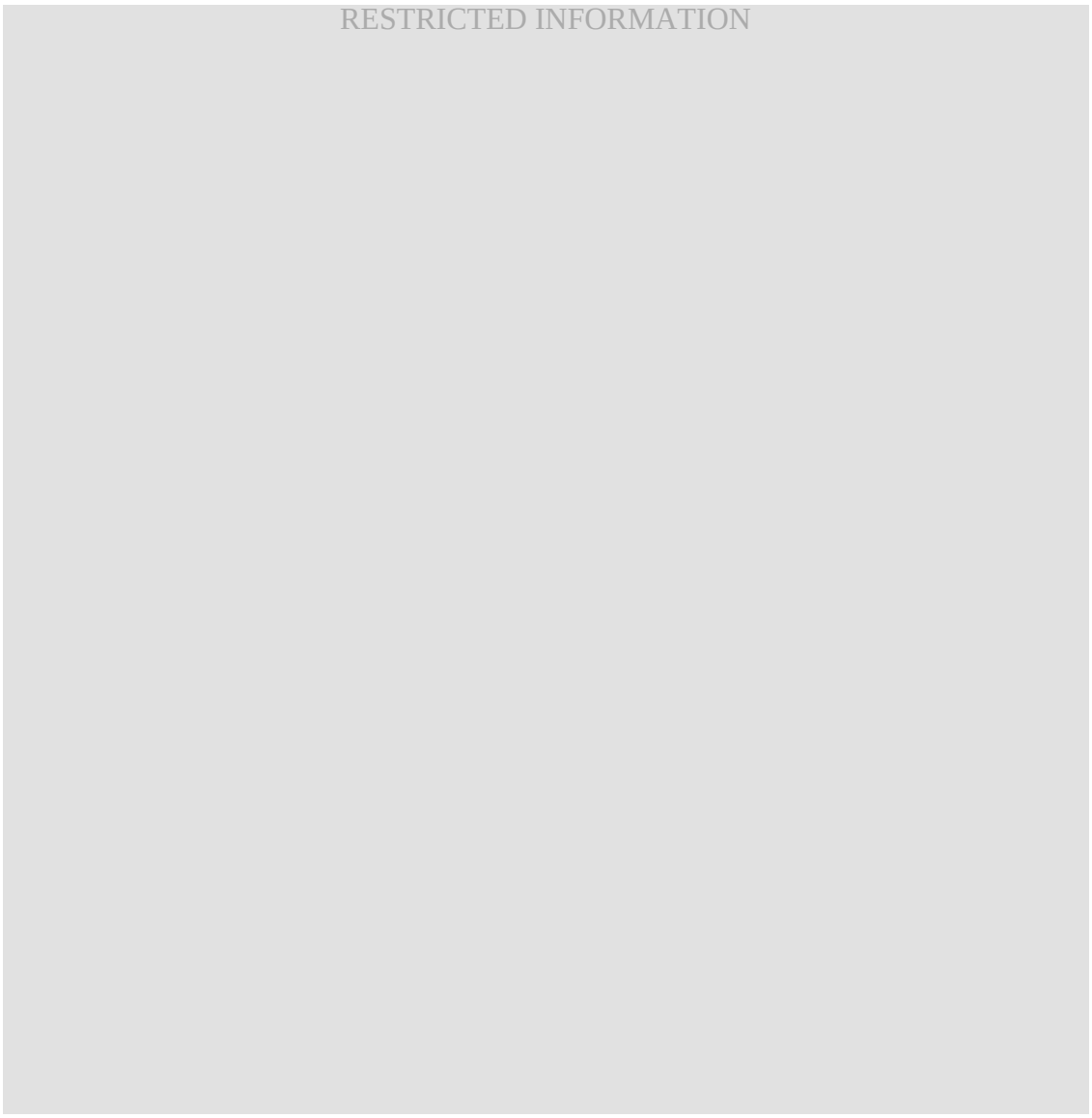


Fig. 4.31 Reflow profile of daughter board.

Fig. 4.32 Resultant daughter board interconnects after reflow.

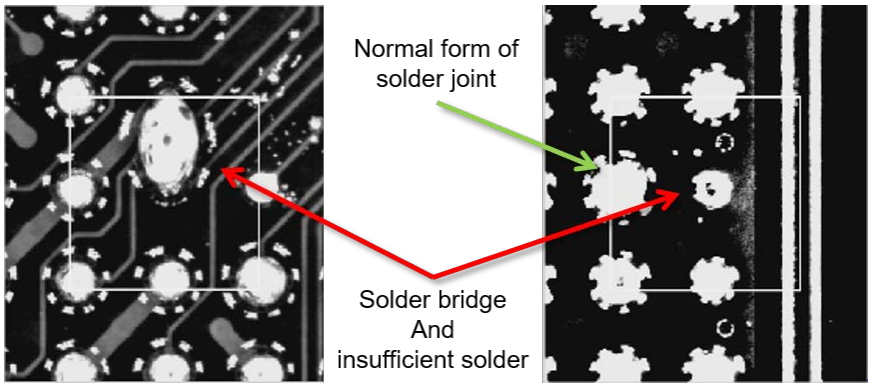


Fig. 4.33 Automatic optical inspection of daughter board.

4.2.3 Mother Board Assembly Process

As a standard cost saving methodology in automotive instrument clusters, the MB was panelized in a 2×1 array, as shown in Fig. 4.34. The assembly process is quite standard with the exception that the DB is a large IC package to be mounted, and picking location should be carefuly considered. This process step is standard. The following parameters were applied:

a) Stencil supplier: [redacted]
b) Stencil type: [redacted]
c) Squeegee: [redacted]
d) Solder paste: [redacted]
e) Print speed: [redacted]
f) Print pressure: [redacted]
g) Separation speed: [redacted]
h) Separation distance: [redacted]

For the solder paste print process, no issues were found. Handling of the populated and bumped DB's did not represent any major challenges at pick and place process, with the exception that the digital vision evaluation of the B2B interconnects requires advance lighting skills to adjust its contrast due to light reflections caused by large amounts of shinny flux residues. A special tray for picking up the DBs is needed for the pick and place machine, as shown in Fig. 4.35. DBs were picked up from processor's back, as depicted in Fig. 4.36. No issues were observed after this process. The resultant sample is shown in Fig. 4.37.

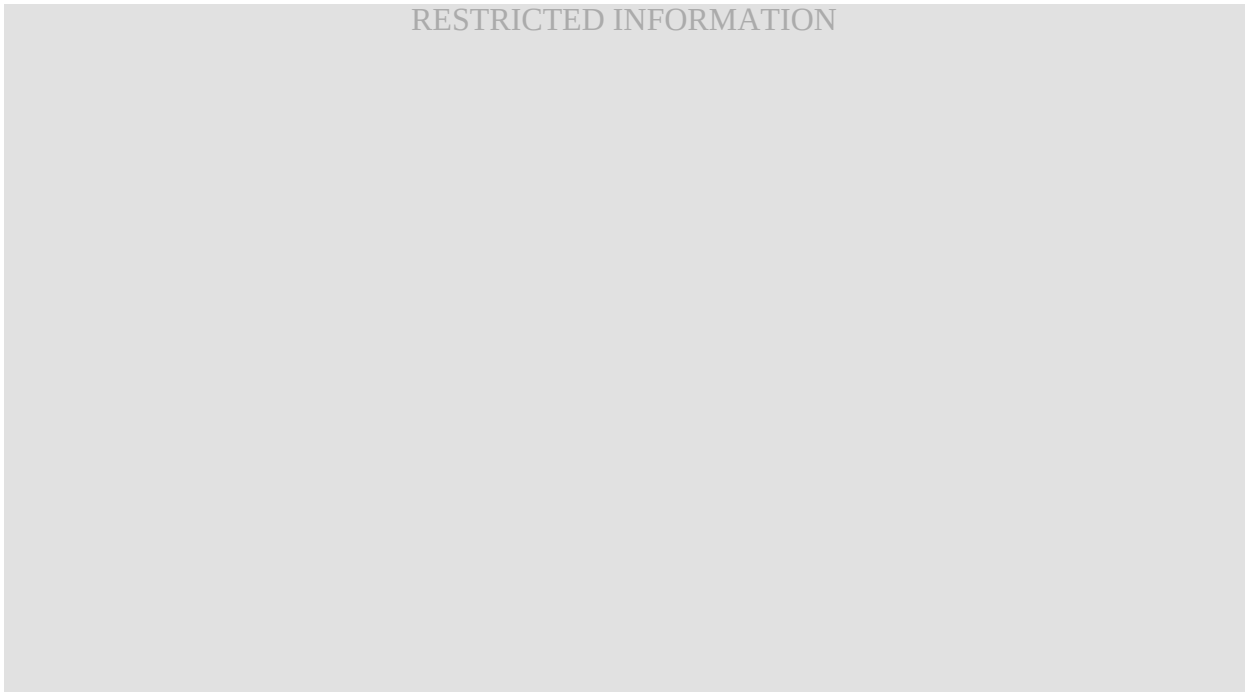


Fig. 4.34 Main board panel.

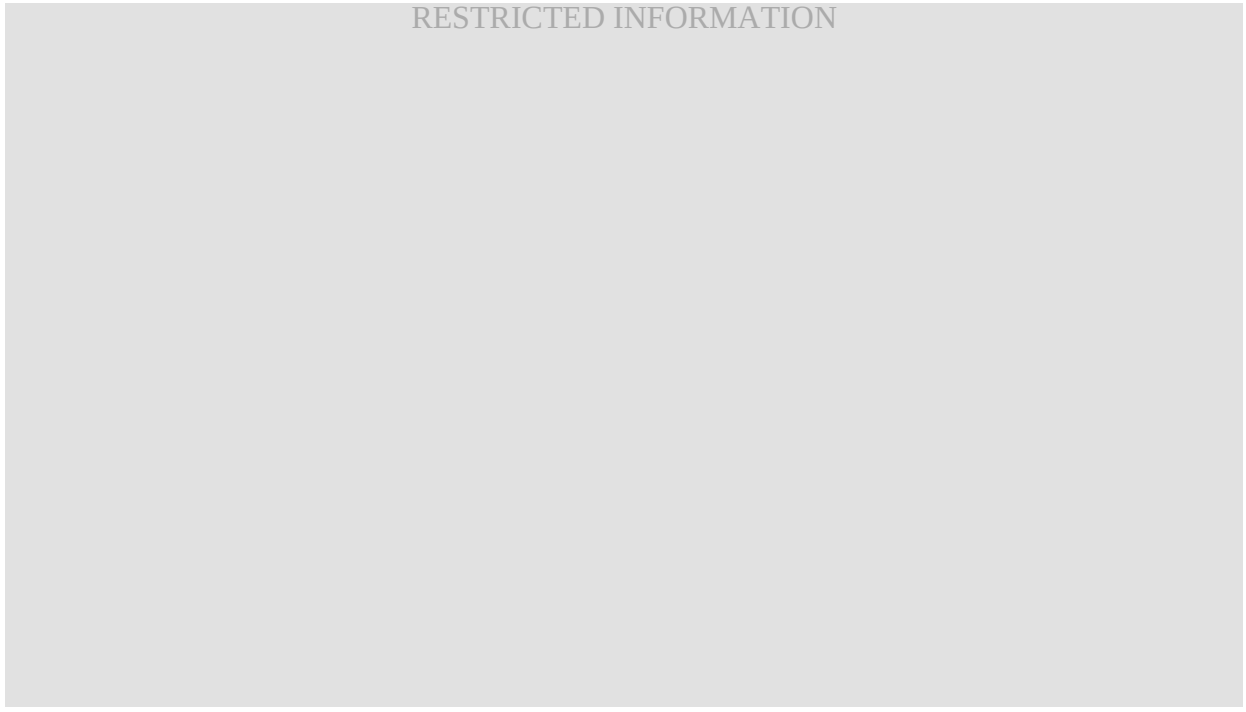


Fig. 4.35 Mounting tray for daughter boards.

Fig. 4.36 Daughter board being picked inside pick and place machine.

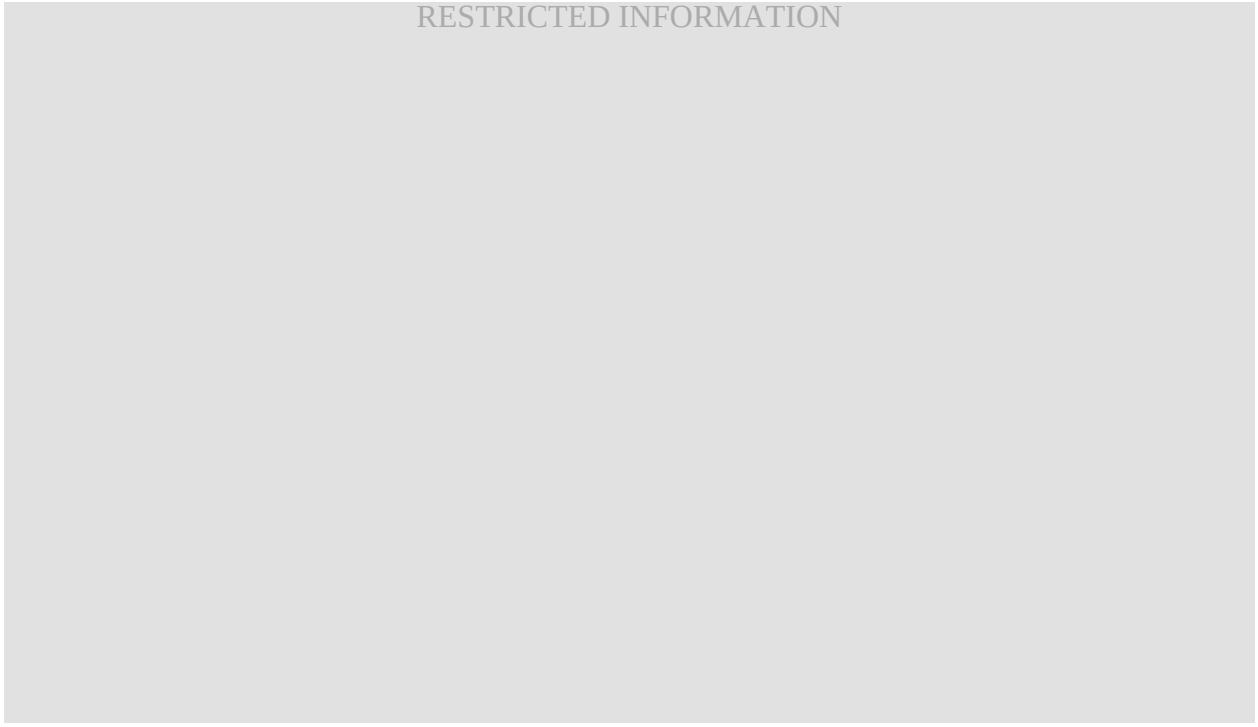


Fig. 4.37 Resultant main board panel before reflow process.

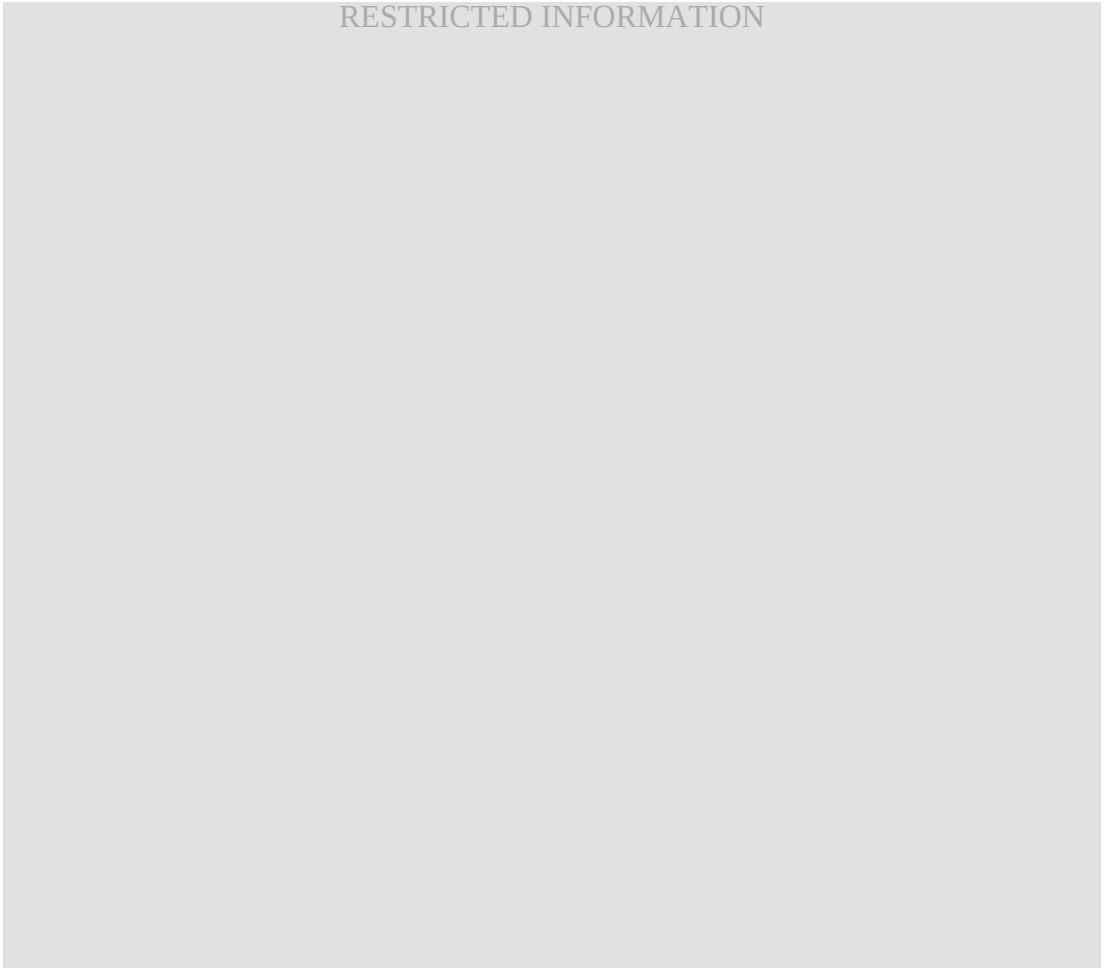


Fig. 4.38 Reflow profile of main board.

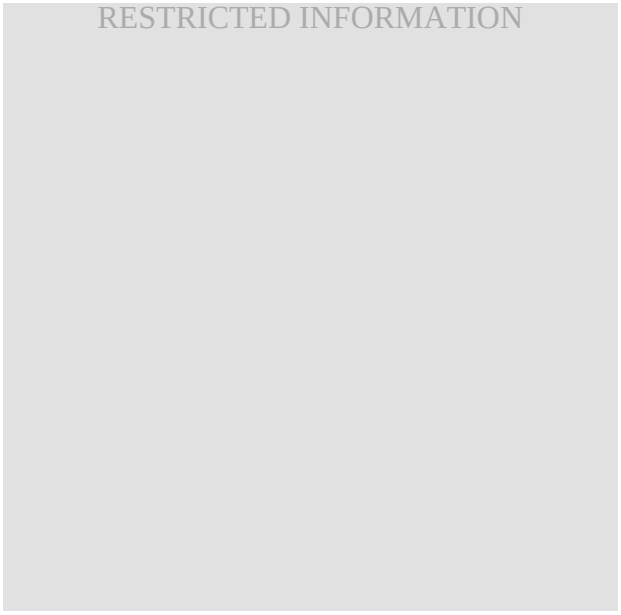


Fig. 4.39 Automated X-Ray inspection of daughter board assembled onto mother board.

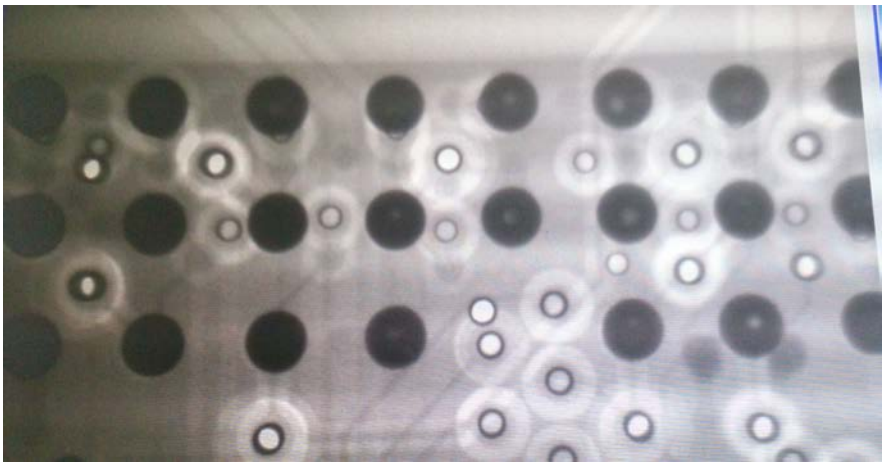


Fig. 4.40 Voids inside interconnects found in AXI inspection.

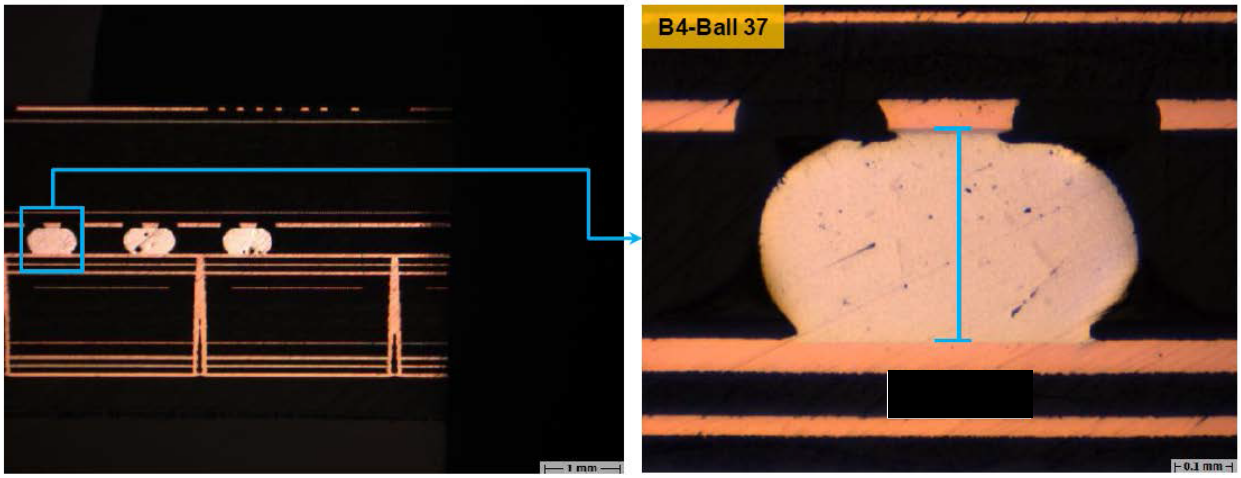
Subsequently, a reflow profile according to solder paste manufacturer recommendations was followed, as shown in Fig. 4.38. After reflow and cooling process, the B2B interconnection solder joints were reviewed by standard AXI methods and the process shows good solder performance, as shown in Fig. 4.39. The AXI results showed that most B2B interconnects had voids with an area smaller than 30% of the solder balls area, as shown in Fig. 4.40, being compliant with IPC standard IPC-7351B [IPC Sd IPC7351B]. No opens or bridges were observed by x-ray inspection.

4.2.4 Technical Verification

Interconnects' bonding quality, warpage, and electromechanical performance need to be analyzed after manufacturing the prototypes. Several tests were conducted such as cross sectioning, applying thermal shocks, analyzing warpage through a computerized tomography scan, and performing functional and electrical stress tests, as per automotive requirements.

4.2.4.1 Cross-Sectional Analysis

The first logic check is the size, shape, and mechanical attachment of the created interconnects. Hence, metallurgical cross-sectional analysis was conducted using the X-ray analysis as a guide. A sample is shown in Fig. 4.41, where it is seen that no opens, shorts or even cracks were found in the post-manufacturing cross-sectional analysis. A few voids were identified but their total added area was smaller than 30% of the ball area.



a) b)

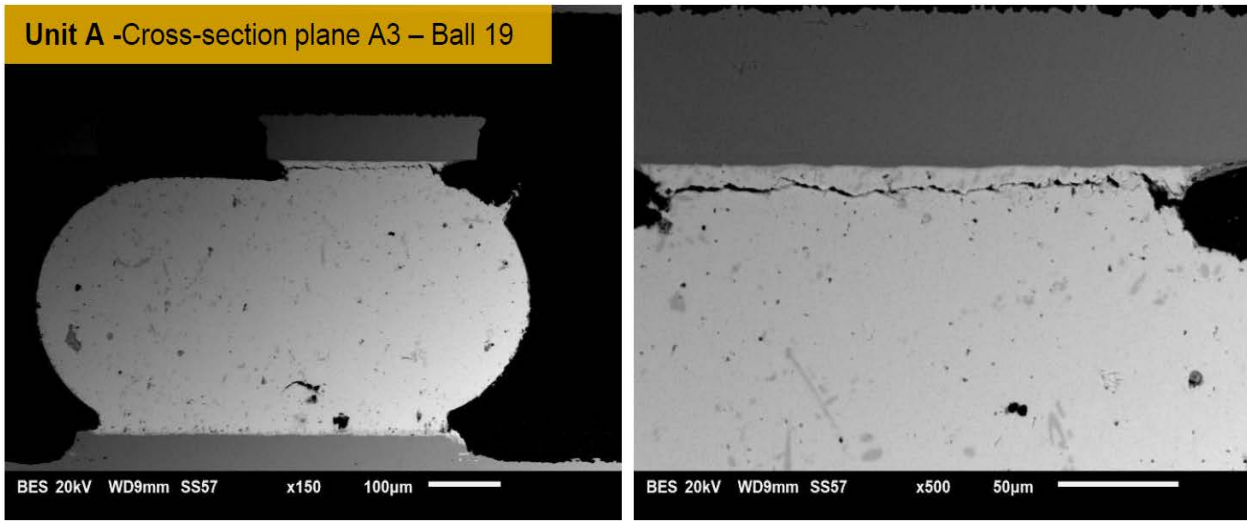
Fig. 4.41 Resultant interconnects in cross-sectional view: a) section of the interconnect, b) zoom of a vertical connection.

4.2.4.2 Thermal Shocks Test

This test exposes the design under test (DUT) to alternating low and high air temperatures to accelerate failures caused by repeated temperature variations during normal use conditions. The transition between temperature extremes occurs very rapidly during thermal shock testing, greater than 15 °C per minute [Delserro-15]. One cycle consists of [redacted] minutes cold, [redacted] seconds heating, [redacted] minutes hot, and [redacted] seconds cooling [Dengler-16].

Twelve DUTs were laid into a rapid temperature cycling (RTC) chamber, where the temperature changes between –40 °C and 125 °C. Four modules were removed for cross-sectional analysis after 250, 500, 750 and 1000 cycles, and the others are retention samples. Cross-sectional analysis' results were evaluated against IPC standard IPC-A-610F in a descending order from the highest cycling DUT until a success criterion was reached, which happened at [redacted] cycles. Analysis was performed starting with X-ray inspection, then cross section, then optical inspection. Results are summarized as follows:

a) Alignment (IPC section 8.3.12.1): solder ball offset does not violate minimum electrical clearance.
b) Solder ball clearance (IPC section 8.3.12.2): solder balls do not violate minimum electrical clearance.
c) Soldered connection (IPC section 8.3.12.3): no bridging observed, solder balls are not



a) b)

Fig. 4.42 Crack found in 1000 thermal cycles: a) complete interconnect, b) zoom of cracked region.

uniform in size and shape (process indicator), fractures were found in solder balls at 1000 cycles, as shown in Fig. 4.42. No fractures were found in solder balls at 750 cycles.

d) Voids (IPC section 8.3.12.4): voids found in less than 30% of total volume, according to X-ray inspection. Resultant interconnects are shown in Fig. 4.43.

Regarding the [redacted] cycles test, no solder defects were observed nor missing solder balls. Resultant solder ball heights are shown in Table 4.2, and the corresponding cross-section planes are depicted in Fig. 4.44.

4.2.4.3 Computerized Tomography

In order to evaluate warpage, a computerized tomography (CT) analysis was performed to the DUT. In fact, significant warpage happened. Nevertheless, no disconnections were found, which is unusual with a warpage amount of approximately 2.5 times the original height, as depicted in Fig. 4.45.

Due to the metallic alloy, stencil geometry, and process selected, a phenomenon that we called “the peanut interconnect” occurred, as shown in the CT scan imaging render in Fig. 4.46. Due to the deviation of the expected interconnect, we proceeded to generate an EM model in CST[21] of the peanut interconnect, as shown in Fig. 4.47, for its 3D full-wave EM analysis up to 20 GHz.

[21] CST Microwave Studio 2016, CST AG, Darmstadt, Germany, 2016.

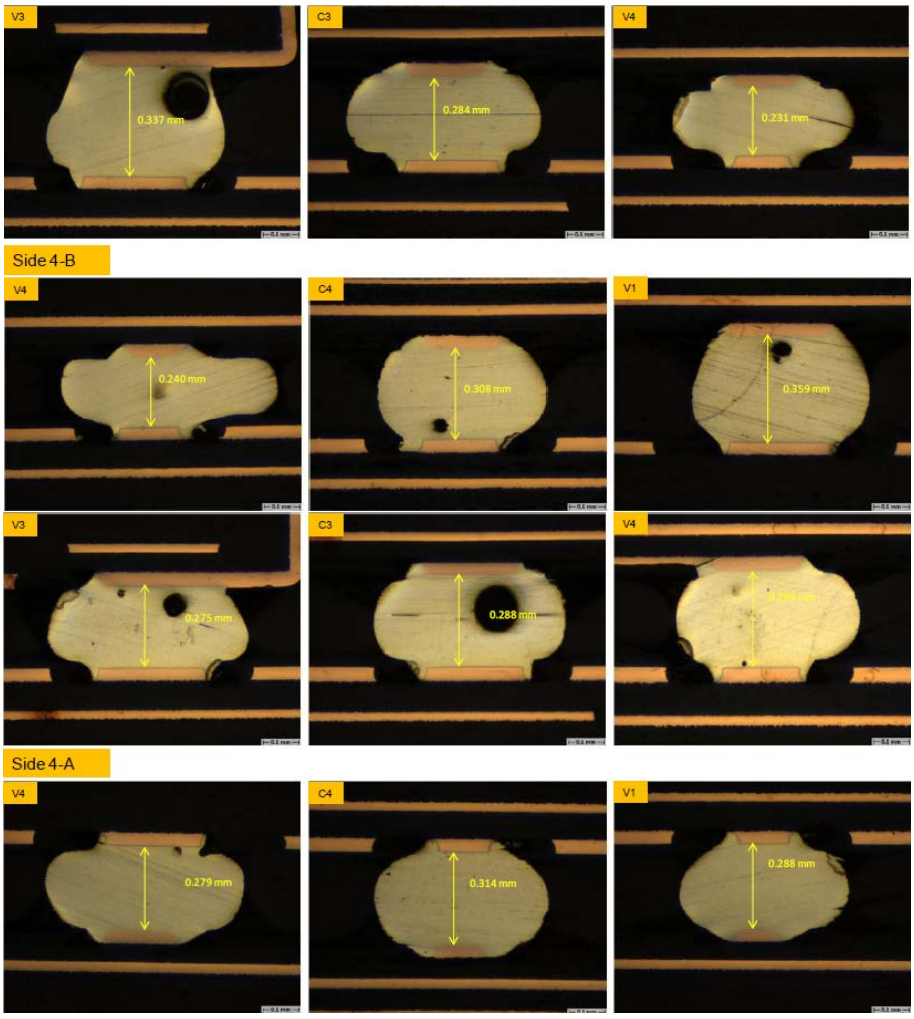


Fig. 4.43 Voids analysis.

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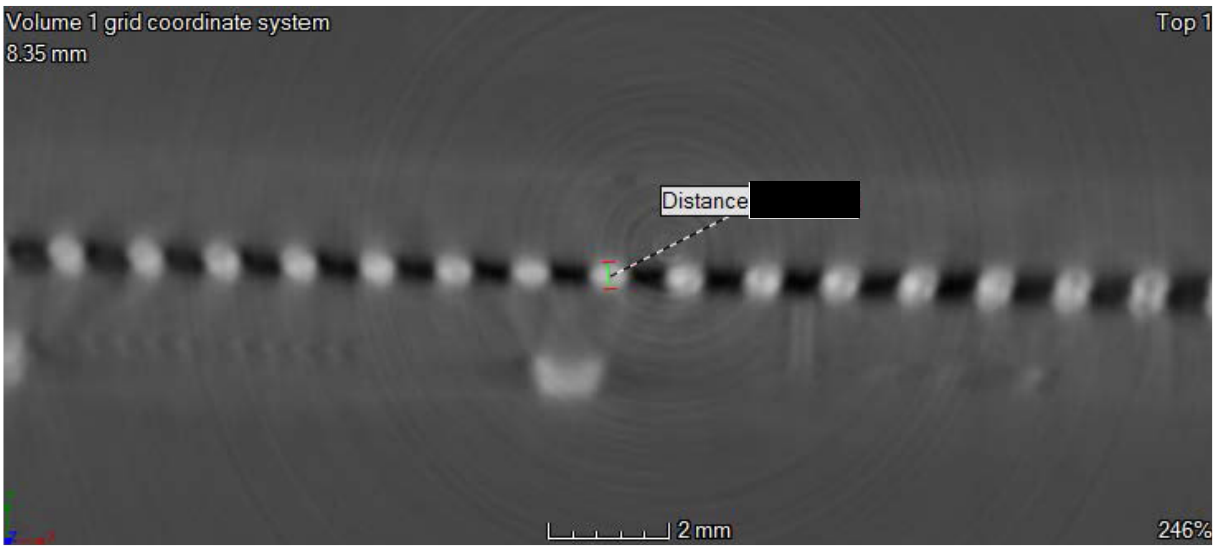
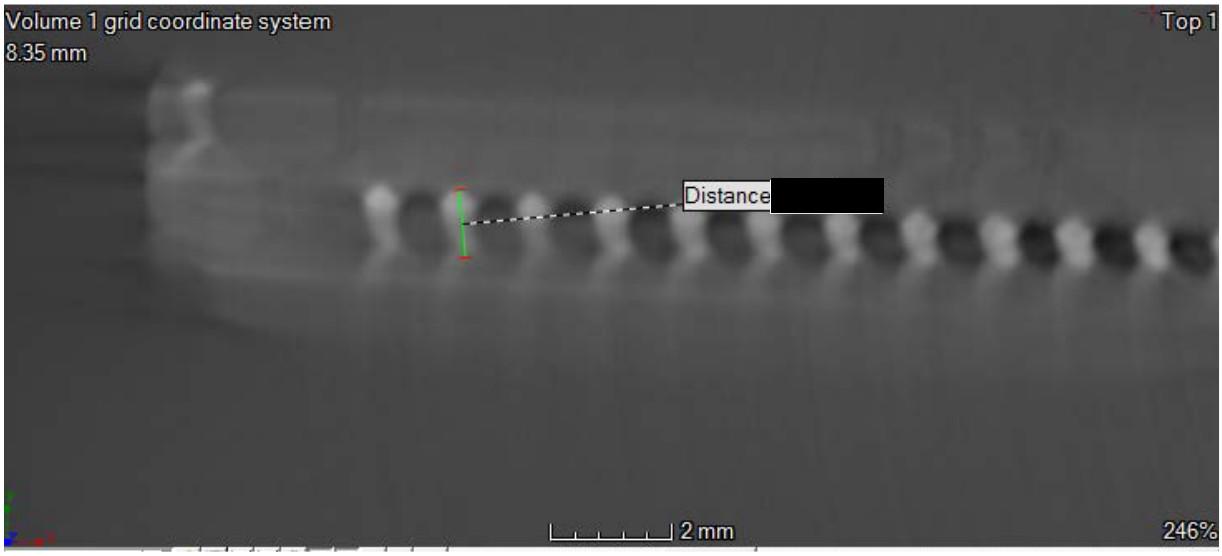
Fig. 4.44 Solder balls cross-section planes identification.



a)



b)

Fig. 4.45 Warpage ratio can be seen from: a) minimum interconnect height, b) maximum interconnect height.

Fig. 4.46 Solder balls cross-section planes identification.

Fig. 4.47 Peanut shaped interconnect EM model.

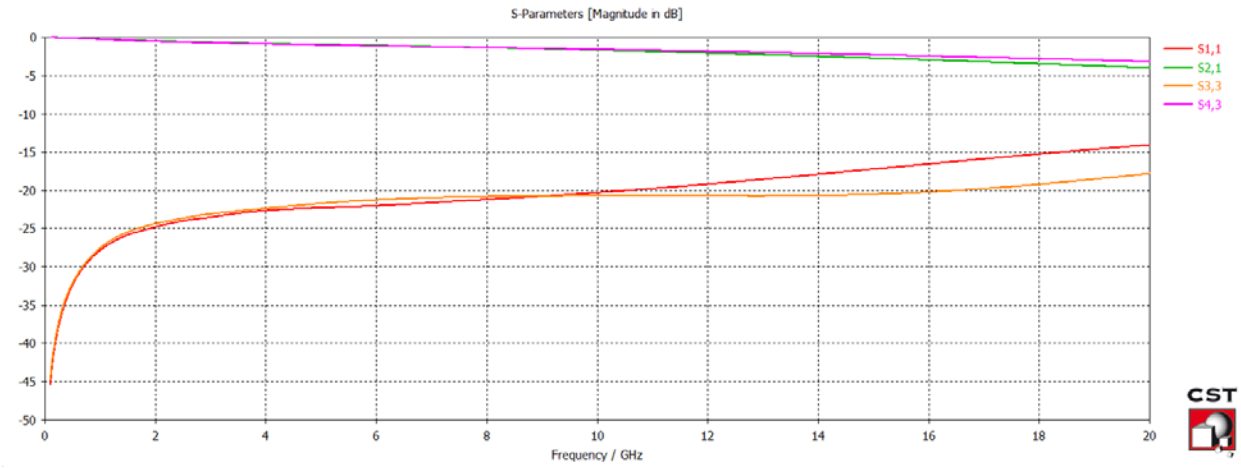


Fig. 4.48 Peanut interconnect S-parameter response.

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Fig. 4.49 EM model of a cluster of 6 peanut interconnects.

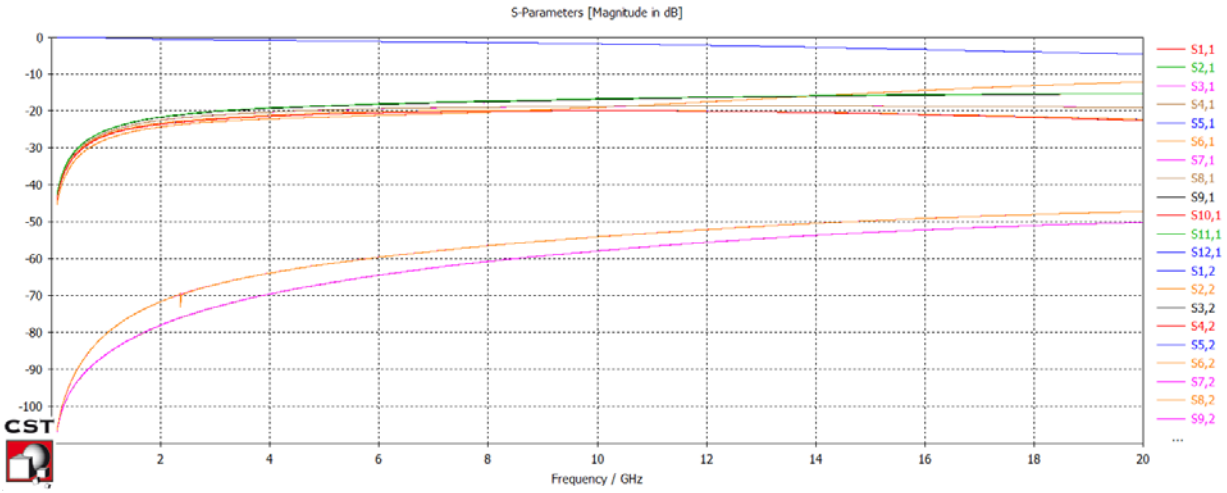

Fig. 4.50 S-parameters response of a cluster of 6 peanut interconnects.

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Fig. 4.51 DB standalone test straps.

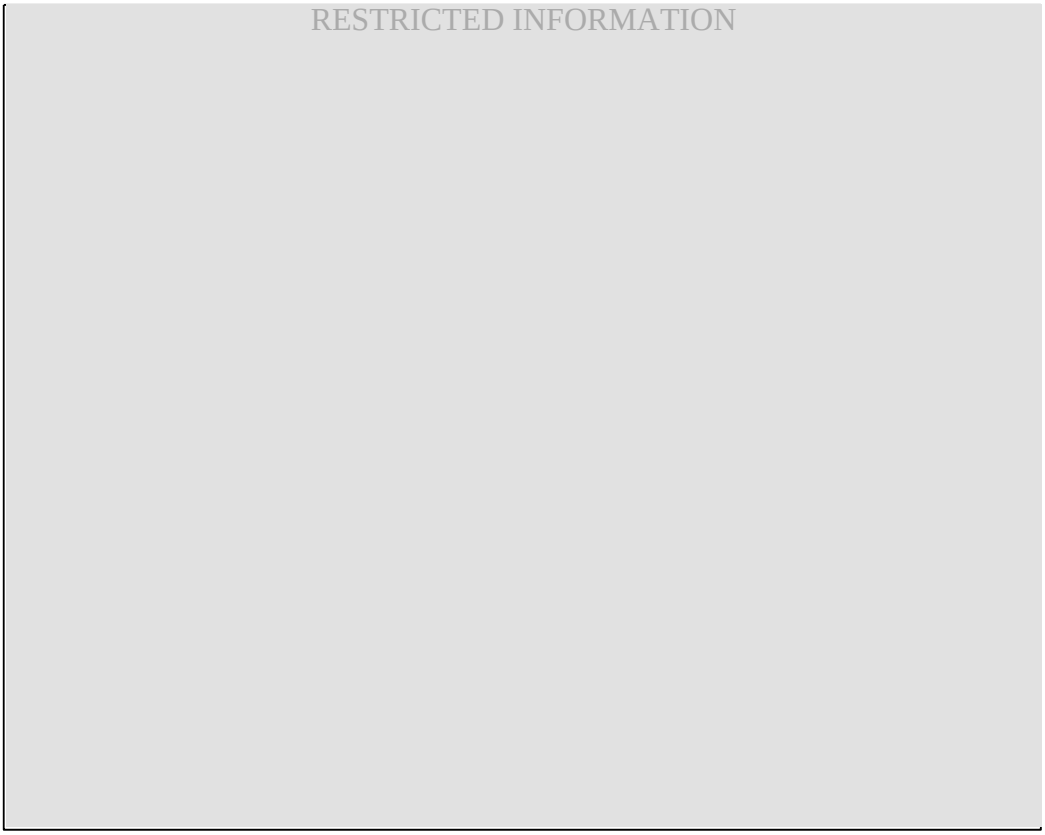


Fig. 4.52 Terminal data thrown by standalone MIP DB with functional test bootloader software.

The EM response of the peanut interconnect was not bad at all, especially up to 10 GHz, as confirmed in Fig. 4.48. To analyze crosstalk effects, a more comprehensive model was generated for a cluster of 6 peanut interconnects, as shown in Fig. 4.49, which allows evaluating the effects produced by the neighboring peanut interconnects. The results plotted in Fig. 4.50 show that there is no significant impact of the inclusion of peanut interconnects in frecuencies below 10 GHz.

4.2.4.4 Functional Tests

A functional test was performed to entirely assess the MiP prototype in a comprehensive way. First, the DB was tested standalone by manually wiring its required logic straps, as shown in Fig. 4.51, and by following the respective power-on sequence required by the processor vendor. Consequently, the processor was flashed with a bootloader which successfully ran without any rework, as shown in Fig. 4.52.

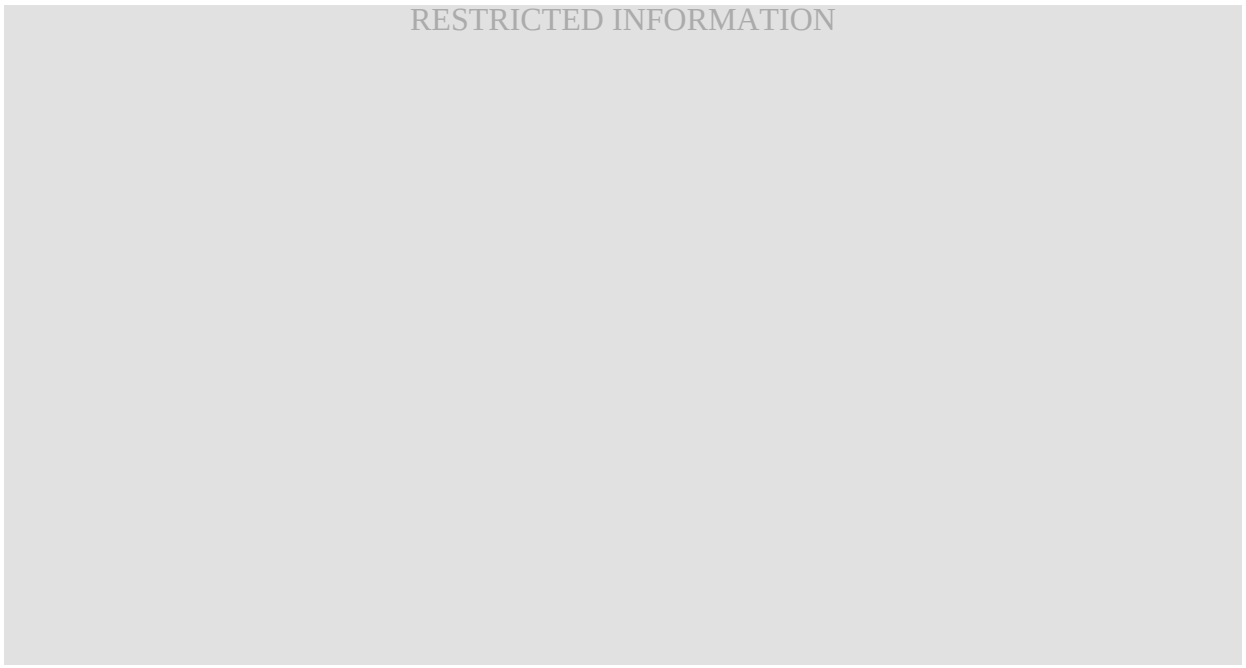


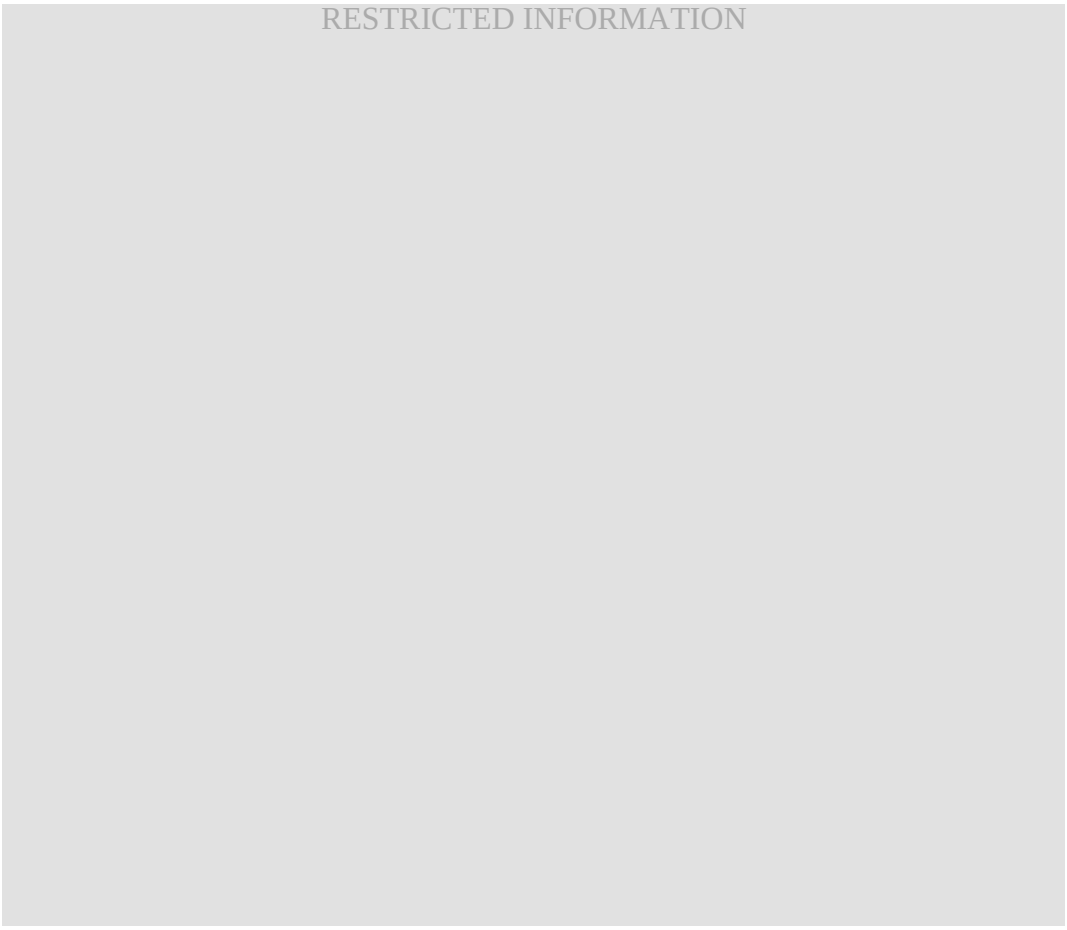
Fig. 4.53 Complete DUT running the application software.

Correspondingly, the full assembled MB + DB DUT was stressed with a special stress-test software, which ran all peripherals and memories successfully. The final DUT running its application software can be seen in Fig. 4.53.

4.3. Flexible Metallic Interconnect Envisioned for High Frequency Signal Transfer Amongst Two Printed Circuit Boards

This Chapter is a synthesized transcription of Mexican patent application MX/A/2018/003154 [del-Rey-18c], which is related with the electronics field in general; particularly related with printed circuit boards and their interconnects, specifically referring to flexible metallic interconnects for high-frequency signal transfer amongst two printed circuit boards. The background of the invention is presented, along with a brief portrayal of the prior art, the invention objectives, and a detailed description of the invention.

TABLE 4.3. GLOSSARY OF FIGURE NUMBERS



4.3.1 Background of the Invention

The interconnection of two printed circuit boards (PCBs) can be obtained by quite a few methods, such as the application of connectors and/or the application of fixation or bonding elements. The last ones are supposed to guarantee the direct contact of a landing or bonding pattern on external metal layers.

Conductive bonding elements involve either, the application of polymer structures with conductive particles meant to transport electricity, or the employment of preformed metal structures bonded by metal coalescence, such as soldered joints. The second ones are utilized in land grid array interconnect technology (LGA) and via-castellated post stamp packages [del-Rey-17c].

To name a few disadvantages of prior art, due to the nature of polymer-based conductive

Fig. 4.54 PCB cross-section, depicting the electronic components [redacted], according to the present invention. From [del-Rey-18c].

bonding elements, such as carbon printed interconnects, the high resistance of the whole structure limits the bandwidth to a few kilohertz. For metal-based bonding elements, such as the solder joints for LGA technology, the interconnects' density is limited by the joining package perimeter, restraining the number of signals to carry. In post-stamp or via castellated packaging interconnects, besides a low interconnection density presented due to the interconnect's thickness, the maximum frequency and bandwidth are limited due to the relatively high inductance and the interconnect size to wavelength ratio they present.

Additionally, preformed metal spheres used in ball grid array interconnects (BGA), even though they are widely used in the electronics industry with a mature manufacturing process, usually creates a precise undeformed interconnect due to their solid metal nature. This nature makes them prone to fractures and disconnections when subject to thermal shocks. Additionally, their assembly process associated to mass production impede the placement of SMD components adjacent to the preformed metal spheres, requiring higher cost PCB manufacturing processes to holistically compensate a digital high-speed design power integrity.

The summarized patent submission proposes RESTRICTED INFORMATION A search has been performed to determine the closest state-of-the-art.

Fig. 4.55 Conventional perspective views of top and bottom side of the interconnect PCB. From [del-Rey-18c].

4.3.1.1 Known Prior Art

United States (US) patent US3530231 from January 15th, 1969 submitted by Ralph F. Penoyer [Penoyer-69], deals with one of the problematics defined in the present invention. It involves the creation of unintentional short circuits between adjacent interconnects caused by the coexistence of liquid-state solder particles during a reflow manufacturing process. This happens due to the superficial tension inflected by the solder in liquid state above a plurality of conductive geometries, without an isolating coating, such as an epoxy paint or soldermask.

The referred patent solves this problem by generating transversal channels or grooves beside the interconnects' geometries, allowing solder excesses to flow through these channels. This is meant to avoid the migration of solder (or short circuits) to their adjacent interconnects during a solder reflow process.

Said document never reveals or suggest that solder conforms the main embodiment of the interconnect, as described by the proposed invention. For this reason, the amount of solder material is significantly bigger in our invention, in comparison to the described in the alleged document.

In the proposed invention, unintentional short circuits or solder bridges are solved with the aspect-ratio control and a proposed shape geometry, which parts from a circular base, plate or pad made of an electrical conductor over the dielectric substrate of a printed circuit board, and the creation of a tridimensional form similar to columns (columnoids), made of Sn & resin-core solder paste. Said geometry is interconnected by fixation with another plate or circular pad in a different printed circuit board substrate by a reflow manufacturing process. Due to the nature of the

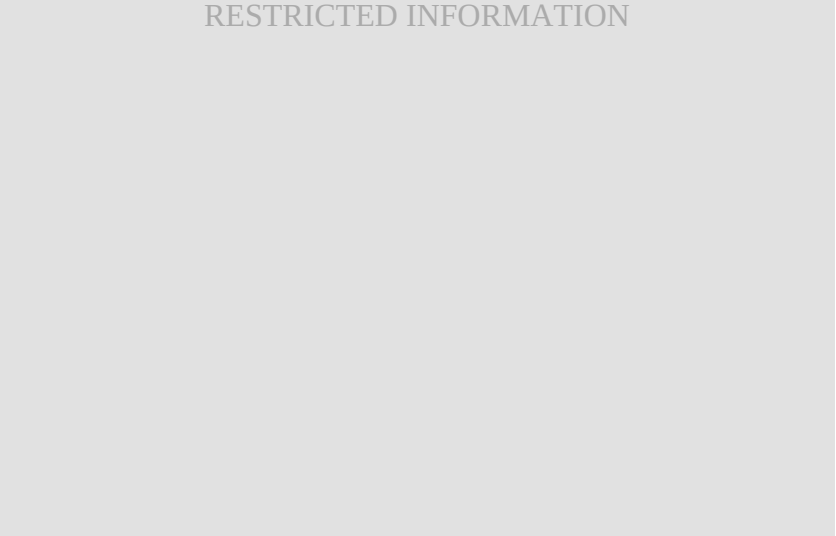


Fig. 4.56 Exploded diagram of the interconnect PCB. From [del-Rey-18c].

disclosed invention, it is impossible to groove transversal channels since the proposed interconnect is created vertically, in a manner totally opposed to the horizontal interconnect from US3530231.

Another relatable prior art document found is US patent US5029748A from March 15th, 1989, submitted by John H. Lauterbach and Leon T. Ritchie [Lauterbach-91]. This document describes a method to solder thru-hole mount technology pins (THMT) in a printed circuit board by reflowing preformed conductive elements previously placed over plated through holes, in a way that preformed elements melt and flow through said holes during reflow, integrating surface mount technology (SMT) with THMT technology in a single process. The proposed invention in this report does not refer or disclose any characteristic that includes, touch or solves the usage of THMT technology, since it relies only in the reflow process required by SMT technology. In fact, US5029748A does not suggest or proposes an object that is elaborated during the same solder paste printing process required by SMT technology as a fixation method, nevertheless it only refers to apply a preformed or pre-molded object.

Additionally, the proposed interconnect is small enough to allocate a significant number of interconnects with high frequency bandwidth due to its short length, as compared to the wavelength of current high-frequency digital signals intended to be transmitted, which in that aspect is similar to state-of-the-art ball grid array (BGA) technology. The main advantage of the present invention over BGA technology is that interconnects are formed during the PCB assembly, allowing the simultaneous placement of passive SMD components, meant to enhance the system response in higher frequencies, along with their reshape-ability in elevated temperatures.

a) b) c)

Fig. 4.57 Front views of the interconnect columnoids: a) elongated interconnect, b) regular interconnect, c) compressed interconnect. From [del-Rey-18c].

Moreover, due to the malleability of proposed metal alloy, the final joint is able to withstand a significant amount of mechanical and ambient stress without external fixation methods or processes, resulting in a cost reduction.

4.3.1.2 Invention Objectives

The proposed present invention targets to make flexible metallic interconnects available for the transfer of high frequency electric signals between two printed circuit boards. These interconnects present a number properties, as follows.

They present some degree of flexibility during a thermal event. For instance, they are able to elongate up to 2 times their original height without cracks, fractures or electrical disconnection. Additionally, they are able to withstand a compression of about 30% of their original height without bridging or making a short-circuit with another interconnect in its neighborhood.

They allow high densities and high speeds. Their geometry also allows the transfer of a high amount of high frequency signals, along with simultaneous placement of passive SMD components in parallel, which are needed to enhance the system's high-frequency response.

They are robust. They can reshape when exposed to elevated temperatures. Their construction consists in the coalescence or fusion of a malleable metallic alloy whose flexibility can guarantee the interconnect integrity without cracks against multiple thermal shocks in a temperature range of –40 °C to 105 °C.

They are cost-effective. They can be formed during the PCB assembly, and the final union is able to withstand a significant amount of mechanical and ambient stress without adding extra fixation materials or processes, resulting in a cost reduction.

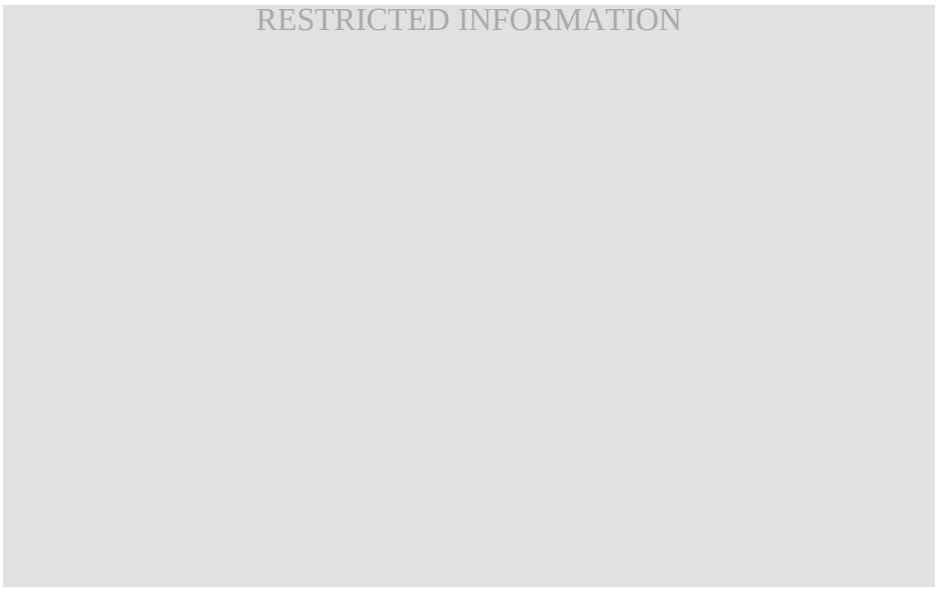


Fig. 4.58 Printed solderpaste columnoids. From [del-Rey-18c].

4.3.1.3 Brief Description of the Invention

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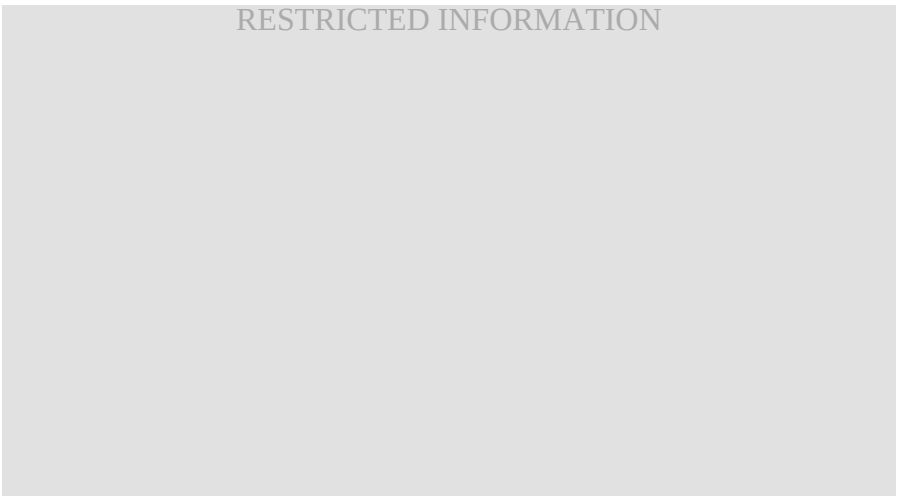

Fig. 4.59 Diagram of the printed solderpaste columnoids' geometry. From [del-Rey-18c].

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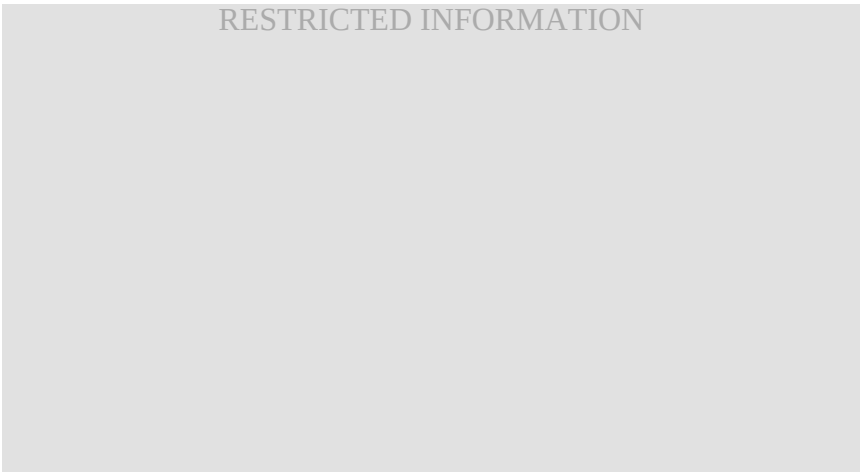

Fig. 4.60 Schematic diagram defining a high precision [redacted] and the land pattern geometry for SMD components to be mounted on a PCB. From [del-Rey-18c].

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Fig. 4.61 Top view of primary and secondary side of the interconnect PCB. From [del-Rey-18c].

Fig. 4.62 Diagram of the interconnection between the core PCB and a host PCB through [redacted] columnoids. From [del-Rey-18c].

4.4. Conclusions

In this Chapter is demonstrated how the Continental AG module in package (MiP) can reduce the gap between high-end mobile computing technology and automotive instruments in a cost-effective manner, by lowering the overall PCB materials' cost with the integration of high density and fine pitch components, such as a graphics processor, memory, and power supplies into an automotive oriented SiP-like package. The principal design constraints, along with a detailed design description that overcomes the problems related with bonding high-frequency interconnects between two PCBs have been portrayed in Section 4.1.

Consequently, after passing all the electromechanical and reliability tests, the MiP technology inclusion into a prototype proven to be a robust process suited for the automotive environment, as depicted in Section 4.2. The resulting peanut interconnect invention emerged as an unexpected feature which provides a competitive advantage to withstand a certain amount of warpage and still delivers a robust-enough product. Henceforth, a patent submission of it, has been presented as a cost-effective flexible metallic interconnect for high frequency signal transfer amongst two printed circuit boards, characterized by an array of small metallic columnoids or pillars.

In fact, it turns out that the closely related prior art found, along with the invention objectives and a wide-ranging set of thermal shock tests prove that the invention is original, useful and non-trivial, adequate and robust for high-speed low-cost automotive interconnects, setting the ground for future industrial exploitation.

General Conclusions

The costs associated with high performance PCBs is becoming an important challenge for the connected car environment, in which high performance computing is now shifting into the automotive industry. News about self-driving cars are becoming predominant these days, but the question of who is going to pay extra for the implicated features remains. Several approaches to speed up the time to market, reuse development resources, and standardize trims and variants are currently being applied by car manufacturers. From this context, the importance of the experimental cost reduction approaches performed in this work becomes apparent.

Different techniques for the IoT and mainly for the connected car environment were presented in this doctoral dissertation to bring the costs down of PCB interconnects. Such techniques included progressive impedance matching techniques through EM modeling and optimization, and the development of a novel, thermally robust, warpage tolerant, and cost-effective high-speed interconnect.

In Chapter 1, an unconventional coplanar differential PCB structure for impedance matching with a limited cost effective FR4 2-layer standard PCB is proposed, modeled, optimized, and validated. Its S-parameter responses along with the EMC emissions pre-scan results proven its adequacy and potential to enable more robust and cost-effective interconnects.

In Chapter 2, the current situation in the automotive electronics industry and the challenges in the requirements for the connected car were portrayed from an electrical engineering perspective. It was focused on the main PCB cost drivers and several cost reduction proposals that were evaluated and applied in subsequent chapters.

Chapter 3 addressed the most relevant cost optimization goals for advanced automotive electronics and benchmarked several board to board interconnects, obtaining the best balance between RF performance, high density, and warpage stability in the BGA geometries. Moreover, a detailed assessment on the common solder balling technologies for B2B and SiP applications identified that the best compelling processes for automotive SiPs and MiPs are stencil printing and the automated stencil balling.

Finally, Chapter 4 integrated the design and assembly of a MiP concept by using the stencil printing process described in Chapter 3. The successful electromechanical and reliability tests

proven its robustness for the automotive environment, which lead to the formalization of a Mexican Patent application to intellectually protect a novel, thermally robust, warpage tolerant, and cost-effective interconnect structure conceived in this doctoral dissertation work.

The proposed doctoral dissertation clearly indicates a number of research opportunities for the future. Further investigation with different EM-based optimization algorithms, considering different PCB materials, could be exercised in a future research. Another possible research work could be directed towards developing quasi-static equivalent circuit models (or even metamodels) of the patented novel interconnect, correlated against full-wave EM simulations and actual laboratory measurements. A third research line could be focused on developing multi-physics models for the proposed interconnect, to reproduce in a 3D multi-physics finite-element-based simulator the actual mechanical deformations experimentally found after applying thermal stress, and from here, elaborate on suitable numerical optimization methodologies.

Conclusiones Generales

Los costos asociados con PCBs de alto desempeño se están convirtiendo en un desafío importante para el entorno del automóvil conectado, en el que la informática de alto rendimiento se está trasladando a la industria del automóvil. Las noticias sobre los vehículos autónomos predominan hoy en día, sin embargo, la cuestión sobre quién pagará más por las características implicadas prevalece.

Actualmente, diversos enfoques para acelerar el tiempo de comercialización, reutilizar los recursos de desarrollo, y estandarizar las variantes de los vehículos están siendo aplicados por los fabricantes de automóviles. Desde este contexto, la importancia de los enfoques experimentales de reducción de costos realizados en este trabajo se vuelve evidente

En esta tesis doctoral se presentaron diferentes técnicas para el IoT y principalmente para el entorno del automóvil conectado, con el objetivo de reducir los costes de las interconexiones de PCB. Dichas técnicas incluyen metodologías progresivas de acoplamiento de impedancia a través de modelado EM y algoritmos de optimización, así como el desarrollo de una nueva interconexión rentable de alta velocidad, térmicamente robusta, y tolerante a la deformación.

En el Capítulo 1, se modela, optimiza y valida una estructura coplanar diferencial no convencional propuesta para el acoplamiento de impedancias en un PCB estándar de 2 capas basado en FR4. Sus respuestas de parámetros-S junto con los resultados de emisiones EMC demostraron su desempeño y potencial para lograr interconexiones más robustas y rentables.

En el Capítulo 2, se describe la situación actual en la industria de la electrónica automotriz y los desafíos para lograr los requerimientos del automóvil conectado, tratado desde la perspectiva de la ingeniería eléctrica. Se enfocó en los principales factores de costos en PCBs y se dieron propuestas de reducción de costos, las cuales han sido evaluadas y aplicadas en los capítulos subsecuentes.

El Capítulo 3 aborda los objetivos de optimización de costos más relevantes para la electrónica automotriz avanzada, asimismo se estableció una comparación de varias interconexiones de PCB a PCB (B2B), obteniendo el mejor equilibrio entre el desempeño de RF, una alta densidad de interconexiones y la estabilidad ante la deformación mecánica en las geometrías BGA. Además, una evaluación detallada de las tecnologías comunes de montado de

bolas de soldadura para aplicaciones B2B y SiP identificó que los procesos mejor adecuados para tecnologías SiP y MiP automotrices son la impresión de soldadura con plantilla, y el boleo automatizado con plantilla.

Finalmente, en el Capítulo 4 se integra el diseño y montaje de un prototipo de MiP utilizando el proceso de impresión de pasta de soldadura descrito en el Capítulo 3. Las exitosas pruebas electromecánicas y de confiabilidad demostraron su robustez para el entorno automotriz, lo que condujo a la formalización de una solicitud de patente mexicana para proteger intelectualmente una novedosa estructura de interconexión, rentable, térmicamente robusta, y tolerante a la deformación, concebida en este trabajo de tesis doctoral.

Esta tesis doctoral crea visiblemente una serie de nuevas oportunidades de investigación. Se podría investigar con mayor profundidad sobre diversos algoritmos de optimización basados en modelos EM, considerando diferentes sustratos y materiales de PCBs. Otro posible trabajo de investigación podría estar dirigido a desarrollar modelos de circuitos equivalentes cuasiestáticos (o incluso metamodelos) de la nueva interconexión patentada, correlacionada con simulaciones EM de onda completa y mediciones reales de laboratorio. Una tercera línea de investigación podría centrarse en el desarrollo de modelos multifísicos para la interconexión propuesta en este trabajo, a modo de reproducir en un simulador tridimensional de física de elementos finitos las deformaciones mecánicas reales encontradas experimentalmente después de aplicar el estrés térmico y, a partir de aquí, elaborar sobre metodologías de optimización numérica adecuadas.

Appendix

A. LIST OF INTERNAL RESEARCH REPORTS

1) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Impedance matching analysis of a low-cost PCB differential interconnect," Internal Report *PhDEngScITESO-14-05-R (CAECAS-14-05-R)*, ITESO, Tlaquepaque, Mexico, Aug. 2014.
2) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Impedance matching optimization of a low-cost PCB differential interconnect," Internal Report *PhDEngScITESO-14-18-R (CAECAS-14-12-R)*, ITESO, Tlaquepaque, Mexico, Dec. 2014.
3) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Precision awareness in measurements of PCB high speed interconnects," Internal Report *PhDEngScITESO-14-20-R (CAECAS-14-13-R)*, ITESO, Tlaquepaque, Mexico, Dec. 2014.
4) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Modeling of a low-cost PCB differential interconnect using several commercially available simulators," Internal Report *PhDEngScITESO-15-19-R (CAECAS-15-17-R)*, ITESO, Tlaquepaque, Mexico, Dec. 2015.
5) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Temperature effects in automotive-grade high speed interconnects," Internal Report *PhDEngScITESO-16-31-R (CAECAS-16-15-R)*, ITESO, Tlaquepaque, Mexico, Dec. 2016.
6) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Challenges in the connected car requirements from a hardware perspective to enable safer and competitive next-generation driver information systems," Internal Report *PhDEngScITESO-17-38-R (CAECAS-17-17-R)*, ITESO, Tlaquepaque, Mexico, Nov. 2017.
7) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Cost reduction approaches for systems requiring high speed high density printed circuit board interconnects," Internal Report *PhDEngScITESO-17-41-R (CAECAS-17-19-R)*, ITESO, Tlaquepaque, Mexico, Dec. 2017.
8) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Board to board interconnecting technologies related to the automotive electronics, as a cost optimization technique for the connected car," Internal Report *PhDEngScITESO-17-44-R (CAECAS-17-20-R)*, ITESO, Tlaquepaque, Mexico, Dec. 2017.
9) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Board to board technology concept study for the automotive electronics industry," Internal Report *PhDEngScITESO-17-46-R*

(CAECAS-17-21-R), ITESO, Tlaquepaque, Mexico, Dec. 2017.

10) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Solder ball technologies for system in package and board to board solutions for the automotive," Internal Report *PhDEngScITESO-18-02-R (CAECAS-18-01-R)*, ITESO, Tlaquepaque, Mexico, Mar. 2018.
11) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "MIP design: a system in package customized for the automotive environment," Internal Report *PhDEngScITESO-18-05-R (CAECAS-18-03-R)*, ITESO, Tlaquepaque, Mexico, Apr. 2018.
12) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "MIP assembly process: a system in package customized for the automotive environment," Internal Report *PhDEngScITESO-18-09-R (CAECAS-18-05-R)*, ITESO, Tlaquepaque, Mexico, Apr. 2018.
13) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Flexible metallic interconnect envisioned for high frequency signal transfer amongst two printed circuit boards," Internal Report *PhDEngScITESO-18-12-R (CAECAS-18-07-R)*, ITESO, Tlaquepaque, Mexico, May. 2018.

B. LIST OF PUBLICATIONS AND INTELECTUAL PROPERTY

B.1. Conference Papers

1) J. R. del-Rey, Z. Brito-Brito, J. E. Rayas-Sánchez, and N. Izquierdo, "Temperature effects in automotive-grade high speed interconnects," in *IEEE MTT-S Latin America Microwave Conf. (LAMC-2016)*, Puerto Vallarta, Mexico, Dec. 2016, pp. 1-4. (ISBN: 978-1-5090-4288-3; e-ISBN: 978-1-5090-4287-6; INSPEC: 16670767; DOI: 10.1109/LAMC.2016.7851273)
2) J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Impedance matching analysis and EMC validation of a low-cost PCB differential interconnect," in *IEEE Latin-American Test Symp. (LATS-2015)*, Puerto Vallarta, Mexico, Mar. 2015, pp. 1-5. (ISSN: 2373-0862; e-ISBN: 978-1-4673-6710-3; INSPEC: 15111168; DOI: 10.1109/LATW.2015.7102514).

B.2. Patents

1) J. R. del-Rey and Z. Brito-Brito, "*Interconexión metálica flexible para transferencia de señales eléctricas de alta frecuencia entre dos circuitos impresos*," Mexican Patent Application MX/A/2018/003154 (IMPI), March 14, 2018.

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Author Index

Subject Index

L

M

N

O

P

R

S

T

V

W