Post-silicon Receiver Equalization
Metamodeling by Artificial Neural Networks

Francisco E. Rangel-Patiño, José E. Rayas-Sánchez, Andres Viveros-Wacher, José L. Chávez-Hurtado, Edgar A. Vega-Ochoa, and Nagib Hakim

Abstract—As microprocessor design scales to the 10 nm technology and beyond, traditional pre- and post-silicon validation techniques are unsuitable to get a full system functional coverage. Physical complexity and extreme technology process variations severely limits the effectiveness and reliability of pre-silicon validation techniques. This scenario imposes the need of sophisticated post-silicon validation approaches to consider complex electromagnetic phenomena and large manufacturing fluctuations observed in actual physical platforms. One of the major challenges in electrical validation of high-speed input/output (HSIO) links in modern computer platforms lies in the physical layer (PHY) tuning process, where equalization techniques are used to cancel undesired effects induced by the channels. Current industrial practices for PHY tuning in HSIO links are very time consuming since they require massive lab measurements. An alternative is to use machine learning techniques to model the PHY, and then perform equalization using the resultant surrogate model. In this paper, a metamodeling approach based on neural networks is proposed to efficiently simulate the effects of a receiver equalizer PHY tuning settings. We use several design of experiments techniques to find a neural model capable of approximating the real system behavior without requiring a large amount of actual measurements. We evaluate the models performance by comparing with measured responses on a real server HSIO link.

Index Terms—artificial neural network, equalization, HSIO, metamodels, post-silicon validation, receiver, simulation, system margining.

I. INTRODUCTION

Technology scaling and advanced silicon packaging techniques are allowing high density integration. However, as process technologies scale down, traditional IC design methods are challenged by the problem of increased silicon process variation. Design-time optimization and post-silicon tuning are the techniques currently used to maximize the parametric yield based on statistical design for high-speed computer systems. Accurate simulations for design-time optimization techniques which exhaustively explore the design space are computationally very expensive given the complexity of the system involved [1].

On the other hand, adaptive tuning in analog design has been widely adopted to confront the silicon process variation. Tunable elements are proposed to adjust the analog circuit performance after chip fabrication [2], [3]. These tunable elements provide a way to reconfigure high-speed input/output (HSIO) links in post-silicon servers to mitigate the effects of system channels’ variability [4], as illustrated in Fig. 1. The adoption of circuit tuning, however, introduces new design challenges. A tunable circuit may contain a large number of control knobs for reconfiguration, and it is extremely expensive to repeatedly run a large number of highly accurate simulations over all process variations and environmental corners to validate a given design during pre-silicon validation [5], making necessary to perform tuning at post-silicon based on physical measurements.

Post-silicon tuning requires first to measure the circuit performance and then determine the optimal knobs set based on measurement results. Current industrial practices for post-silicon tuning in HSIO links are very time consuming since they are typically based on exhaustive testing requiring massive lab measurements [4], resulting in an extremely high cost. Therefore, the challenge is how to make the post-silicon circuit tuning inexpensive by significantly reducing the number of lab measurements.

Several methodologies have been proposed to address the aforementioned challenge. A method to do transmitter (Tx) equalization based on eye diagram analysis and direct optimization is proposed in [1]. In contrast, the problem of receiver (Rx) equalization is addressed in [4] by doing surrogate-based optimization using Kriging modeling. An extension of [4] is presented in [6] by developing several surrogate models to choose the most accurate one at the expense of increasing data collection time on the real system, and then perform numerical optimization of the PHY tuning Rx equalizer settings for a SATA Gen 3 channel topology.

In this paper, we explore the application of machine learning techniques to address the aforementioned challenge with emphasis on the modeling process. In contrast to [6], here we are not looking for a highly accurate surrogate model, but we are looking for a suitable coarse neural model by employing a frugal DoE method for data collection. This is done not only for SATA Gen3, but also for USB3 Superspeed Gen 1. The ultimate goal will be to use the resultant coarse neural model in a space mapping optimization approach [7], [8]. Also in contrast to [6], in this paper we provide an abbreviated review
on machine learning techniques as applied to post-silicon validation, as well as a detailed formulation on the ANN-based modeling and training technique employed, including the regularization scheme to control ANN generalization. More specifically, we propose a metamodeling approach, based on artificial neural networks (ANN), to efficiently synthesize the silicon equalizer circuitry of the Rx. The model is generated using a frugal set of training data exploiting several design of experiments (DoE) approaches to reduce the number of test cases. We evaluate the neural model performance by comparing with actual measured responses on an industrial server validation platform. First, a hardware mechanism provides automated measurements over multiple test cases. We then arrange the data collected to develop a learning procedure to predict the circuit behavior by an artificial neural network. This neural model can be later used for efficient circuit tuning at post-silicon validation. The proposed methodology is illustrated by the neural modeling of a silicon equalizer Rx circuitry of two current industrial HSIO channel topologies: USB3 Super-speed Gen 1 and SATA Gen 3.

The rest of this paper is organized as follows. In Section II, we provide a brief review on machine learning as applied to post-silicon validation. The ANN-based receiver modeling technique is presented in Section III. The system for experimental evaluation is described in Section IV. Results from the proposed modeling approach are compared to actual measured responses in Section V. The last section presents our conclusions.

II. MACHINE LEARNING IN POST-SILICON VALIDATION

Machine learning algorithms, a branch of artificial intelligence, build statistical models from examples, which are then used to make predictions when faced with cases not seen before. On the other hand, the goal of HSIO post-silicon validation is to understand and validate from physical examples the correct operation of the design, identify bugs, and determine the best settings to avoid any failure. Machine learning aims at a similar goal: learning from examples and identifying the structure in a system [9]. In addition, the large volume of data generated from typical post-silicon testing suggests the application of machine learning techniques to predict post-silicon behavior.

There has been recent research on machine learning applications to some areas of post-silicon validation. In [10], authors propose a trace signal simulation-based selection technique that exploits machine learning to efficiently identify a small set of key traceable signals, reducing the simulation cost. An algorithm that applies anomaly detection techniques is proposed in [9] for post-silicon bug diagnosis. Machine learning is applied in [11] to bug finding in post-silicon server power management. In [12], several neural models are developed to learn post-silicon unknown module-level behavior and diagnose localized design bugs.

It is seen that all the previously cited machine learning approaches to post-silicon validation have been focused on developing efficient and reliable techniques for diagnosis, failure detection, or bug identification. An assessment of several surrogate modeling and DoE techniques to identify the best approach for a HSIO link model and simulation is realized in [6]. From that assessment, polynomial-based surrogate modeling (PSM) combined with Sobol DoE with 150 samples was identified as the most accurate surrogate model [6]. While an accurate model is desirable for direct optimization, it can still be expensive since it requires a significant amount of lab measurements to develop. Additionally, the required time to evaluate and even to train any metamodel becomes, for practical purposes, insignificant as compared to the time required to collect the measurement data. On the other hand, it has been demonstrated [13], [14] that both ANN and polynomial functional surrogates perform better than SVM and Kriging surrogates in cases with a very limited amount of training data, while polynomial surrogates exhibit better performance than ANN only in cases with low-dimensionality and small regions of interest. Then, we propose a neural modeling approach to efficiently approximate the effects of a HSIO post-silicon receiver equalizer with a very reduced set of knobs. The resultant metamodel, obtained from the proposed inexpensive method, could later be used as a fast coarse model in a space mapping approach [7], [8] to find the optimal equalizer settings that maximize the actual HSIO performance.

Several other innovative approaches have been proposed to find out the optimal performance of the system in post-silicon validation. In [15], [16], and [5] a statistical framework, referred to as Bayesian model fusion (BMF), is proposed for post-silicon tuning. That methodology is based on the assumption that an early-stage (e.g. pre-silicon) model or data is already available. Then, a relatively small number of post-silicon measurements may be required by applying Bayesian...
inference, allowing the post-silicon cost of tuning to be substantially reduced. However, that BMF approach is not feasible in a post-silicon environment if not enough pre-silicon model information is available, as in our case. Similarly, in [17], a methodology for programming a reconfigurable RF receiver is proposed, showing a maximum efficiency of 27.5× speed-up as compared with the exhaustive search. In [18], a post-silicon tuning methodology is proposed based on a dynamic programming algorithm [19] combined with a fast Monte Carlo simulation flow for statistical analysis and discrete optimization. That method achieves 20× speed-up as compared with the exhaustive search. These methodologies allow very significant acceleration of the tuning time in post-silicon validation. However, it is unclear if they could be easily applied when dealing with a large number of circuit knobs, which is our case.

III. ANN-BASED RECEIVER METAMODELING

Metamodels are scalable parameterized mathematical models that emulate the component behavior over a user-defined design space. These techniques allow developing an approximation of a system response within a design region of interest, following a “black-box” approach. The problem of modeling in post-silicon validation can be mapped to a mathematical problem of function estimation in presence of noisy data points. The most popular estimators are neural networks and Kernel estimation. In [20], authors demonstrate the functional estimation capability of an artificial neural network (ANN).

ANNs are particularly suitable to approximate high-dimensional and highly nonlinear relationships, in contrast to more conventional methods such as numerical curve-fitting, empirical or analytical modeling, or response surface approximations [21]. ANNs have been used in many areas of applications, including RF and microwave circuits [22], EM-based design optimization [23], control process, telecommunications, biomedical, remote sensing, pattern recognition, and manufacturing, just to mention a few [24]. Recently, ANNs have been used for HSIO simulations, but they were focused to model the nonlinear relationships between channel parameters and system performance to speed up system simulations, as in [25] and [26]. In [27], authors proposed ANNs for eye diagram modeling based on simulations, and they use an adaptive sampling method for data collection process.

Once trained, ANN provides a fast way to perform a large number of I/O links and channel simulations that take into account the die-to-die process variations, board impedances, channel losses, add-in cards, end-point devices, and operating conditions [28]. ANN modeling involves two inter-related process: a) neural network model development - that includes selection of representative training data, network topology, and training algorithms; and b) neural model validation - the neural network model is tested and validated according to its model accuracy, and this could be very expensive in the post-silicon validation environment. An alternative to reduce the dimension of the learning set is to properly select the learning points by using DoE, to ensure adequate design space parameter coverage [29].
ANN Topology

Multilayer perceptrons are feedforward networks widely used as the preferred ANN topology. Since a 3-layer perceptron (3LP) is in principle sufficient for universal approximation [30], we use a 3LP to implement our neuromodel, with approximations [31], we use a 3LP to implement our neuromodel. With the 3LP, there is no need to fix the system at voltage/temperature (VT) nominal conditions and without changing the external device. Under these conditions, $\psi$ and $\delta$ remain constant. Therefore, the ANN model during training is treated as

$$ R_{L} = R_{S}(x, w) \quad (4) $$

The ANN performance during training is evaluated by computing the difference between ANN outputs and the targets for all the learning samples,

$$ E_{L}(w) = R_{LL}(x, w) - t_{L} \quad (5) $$

where $E_{L}$ is the learning error matrix.

Following [32], the problem of training the ANN is formulated as

$$ w = \arg \min_{w} |E_{L}(w)|_{F} \quad (6) $$

To control the generalization performance while solving (6), we use $T$ testing base points ($x_{T}$) not used during training. The scalar learning and testing errors are given by

$$ E_{L} = |R_{LT}(x_{L}, w) - R_{TL}|_{F} \quad (7) $$$$ E_{T} = |R_{TT}(x_{T}, w) - R_{TT}|_{F} \quad (8) $$

where $R_{LT}$ and $R_{TT}$ are the output matrices of the fine model and ANN model, respectively, at the $T$ testing base points, and $R_{LL}$ is the fine model response at the $L$ learning base points.

The 3LP is trained by using the Bayesian regularization [33] method available in MATLAB Neural Network Toolbox. The algorithm for training the ANN is shown in Fig. 3. We first define the learning ratio to split the pairs of inputs and targets into the learning and testing datasets. The learning process often begins by initializing the ANN weights with arbitrary values using a random number generator [34], however, in our case we use a decoupling network process with initial set of inputs and outputs to compute initial weighting factors $w_{0}$ and corresponding initial error $E_{0}$. Then, we start training the 3LP with just one hidden neuron ($h = 1$), and calculate the
corresponding learning and testing errors. We keep increasing the complexity of the ANN \((h)\) until the current testing error is larger than the previous one, and the current learning error is smaller than the current testing error, as in [32] (see Fig. 3).

IV. EXPERIMENTAL SYSTEM CONFIGURATION AND DoE APPROACHES

The system under test is a server post-silicon validation platform, comprised mainly of a CPU and a platform controller hub (PCH). The PCH is a family of Intel microchips which integrates a range of common I/O blocks required in many market segments, and these include USB [35], PCI Express [36], SATA [37], SD/SDIO/MMC, and Gigabit Ethernet MAC, as well as general embedded interfaces such as SPI, I2C, UART, and GPIO. The PCH also provides control data paths with the Intel CPU through direct media interface (DMI), as shown in Fig. 4. This figure also shows the automation mechanism to read the Rx eye diagram parameters (eye width and eye height). Within the PCH, our methodology was tested on two different HSIO links: USB3 Super-speed Gen 1 and SATA Gen 3.

The measurement system is based in the system margin validation (SMV) process [4], [38], which is a methodology to verify the signal integrity of a circuit board and assess how much margin is in the design relative to silicon characteristics and processes. The SMV methodology consists of measuring the Rx functional eye width and eye height by using on-die design for test (DFT) features until the eye opening has been shrunk to a point where the Rx detects errors or the system fails [6].

We employ three different DoE techniques to explore the desired solution space with a reduced number of test cases. For each test case, we use seven input variables that represent Rx knobs \((n = 7)\), which are settings used in three main Rx circuitry blocks (CTLE, VGA, and CDR), and then we retrieve the eye measurements from the system under test. The employed DoE techniques are: 1) Box Behnken (BB), which is type of second order response surface methodology (RSM)
performance is achieved with $h = 4$, yielding 7.98% of learning error and 6.75% of testing error. Thus, the metamodels are able to reach above 90% of accuracy for these initial sampling points.

The neural model response at $w^*$ and $h = 3$ for $e_w$ and $h = 4$ for $e_h$ from Sobol50 is compared in Fig. 7a and Fig. 7b, respectively, with the fine model (real measurements), by using 30 testing base points not used during training, in order to test the generalization performance. It is observed that the neural model effectively simulates the actual physical measurements with a total relative error of 1.7% for the $e_w$ response and 2.5% for the $e_h$ response. In other words, the ANN metamodel is able to predict margins with up to 95% of accuracy when using equalization values not used during the ANN training.

We obtained similar results for the case of USB3 Super-speed Gen 1, where we use ten input variables ($n = 10$) that represent the corresponding Rx knobs, which again are settings used in the three main Rx circuitry blocks. For the sake of brevity, we present only the final results in Fig. 8. It is seen that for USB, the resultant neural model also effectively simulates the fine model (physical platform), finding a total relative error of 6.7% for the $e_w$ response, as shown in Fig. 8a, and a 5.7% relative error for the $e_h$ response, as shown in Fig. 8b. This metamodel performance was achieved using also a Sobol50 DoE.

VI. CONCLUSIONS

We presented a metamodeling technique based on artificial neural networks to efficiently simulate the effects of the receiver equalization circuitry in industrial HSIO links. The neural model is trained using different DoE approaches to identify the best system response sampling strategy that yields an acceptable neural model with a very reduced set of learning and testing samples. The resultant neural model approximates with sufficiently accuracy the eye diagram of a real post-silicon HSIO validation platform. The proposed machine learning approach can be exploited to develop extremely efficient vehicles to drive fast PHY tuning in HSIO links.

REFERENCES


Comput.-Aided Design Integr. Circuits Syst., vol. 35, no. 8, pp. 1255-

Rayas-Sánchez, and N. Hakim, “System margining surrogate-based 
opimization in post-silicon validation.” IEEE Trans. Microwave 

K. Madsen and J. Søndergaard, “Space mapping: the state of the art,” 
2004.

aggressive space mapping algorithm over two decades of development 
and engineering applications,” IEEE Microwave Magazine, vol. 17, no. 4, 
p. 64-76, Apr. 2016.

[9] A. DeOrio, Q. Li, M. Burgess, and V. Bertacco, “Machine learning-
based anomaly detection for post-silicon bug diagnosis,” in Europe 
Conf. & Exhibition (DATE) in Design, Automation & Test, Grenoble, 
France, March 2013.

using machine learning techniques,” IEEE Trans. Very Large Scale 

server validation using machine learning,” Int. J. Applied Information 

learning: A machine learning paradigm for post silicon debug of 
RF/analog circuits,” in IEEE 32nd VLSI Test Symp. (VTS), Napa, CA, 
April 2014.

surrogate modeling of RF and microwave circuits in frequency domain 
exploiting the multinomial theorem,” IEEE Trans. Microwave Theory 

opimization of full-wave EM models by low-order low-dimension 
polynomial surrogate functions,” Int. J. Numerical Modelling: 
2017.


framework for efficient pre-silicon validation and post-silicon tuning of 
complex analog and mixed-signal circuits,” in IEEE/ACM Int. Conf. 

reconfigurable radio frequency (RF) receivers,” in 19th Asia and South 
Pacific Design Automation Conf. (ASP-DAC), Singapore, Singapore, 
Feb. 2014.


[19] D. Bertsekas, Dynamic Programming and Optimal Control, Belmont, 

generated regression neural networks (DD-GRNN) for function 
approximation," IEEE Trans. Neural Netw., vol. 18, no. 6, pp. 1683-
1696, Nov. 2007.

experiments: Kriging versus artificial neural network,” Qual. Reliab. 

[22] P. Zhang and K. C. Gupta, Neural Networks for RF and Microwave 


networks”, in Intel Design & Test Technology Conference (DTTC), 
Oregon, CA, Oct. 2015.

[26] M. Liu and J. H. Tsai, “USB3.1 silicon and channel design optimization 
using artificial neural network modeling”, in IEEE Electromagnetic 
Compatibility and Signal Integrity Symp., Santa Clara, CA, May. 2015.

prediction with improved adaptive sampling algorithm,” in Asian 

analysis and nonlinear modeling of high-speed interconnect systems,” 

opimization framework: A case study in aerospace design,” in 
Evolutionary Computation in Dynamic and Uncertain Environments. 
Studies in Computational Intelligence, S. Yang, YS. Ong, Y. Jin, Ed., 

networks are universal approximators,” Neural Networks, vol. 2, no. 5, 

[31] J. E. Rayas-Sánchez, Neural Space Mapping Methods for Modeling and 
Design of Microwave Circuits, Ph.D. Thesis, Dept. of Electrical and 

analysis and yield prediction of microwave circuits using linear-input 
network-output space mapping,” IEEE Trans. Microwave Theory Tech., 


[34] G. Thimm, and J. B. Ra, “High-order and multilayer perceptron 
initialization,” IEEE Trans. Neural Netw., vol. 8, no. 2, pp. 349-359, 


[36] PCI SIG Org. (2016), Peripheral Component Interconnect Express 3.1 

[37] SATA Org. (2016), Serial Advanced Technology Attachment 3.2 

[38] A. Viveros-Wacher et al, “SMV methodology enhancements for high 
speed IO links of SoCs,” in IEEE VLSI Test Symposium (VTS), Napa, 
CA, Apr. 2014, pp. 1-5.

[39] C. F. J. Wu and M. Hamada, Experiments: Planning, Analysis, and 

using sequential neural-network approximation and orthogonal array”, 
in IEEE PES Transmission and Distribution Conference & Exposition: 

[41] I. M. Sobol, “On the distribution of points in a cube and the 
approximate evaluation of integrals,” U.S.S.R. Computational 
Mathematics and Mathematical Physics, vol. 7, no. 4, pp. 86-112, 
1967.

Francisco Elias Rangel-Patío was born in Veracruz, Mexico in 1968. He received the 
B.Sc. degree in electronics engineering from the Universidad Veracruzana, Mexico, in 
1991, the Master degree in Electronics and Telecommunications Engineering from the 
CICESE Research Center, Mexico, in 1994 and the Master degree in Computer Sciences from 
the Tecnológico Nacional de México, Mexico, in 2002. He is currently pursuing the Ph.D. degree in 
electrical engineering sciences at the Department of Electronics, Systems, and Informatics, ITESO – The Jesuit University of Guadalajara, Mexico.

Since 2010, he is with Intel Corp. His current research interests include optimization methods, surrogate-based optimization, and neural network applications for Post-Silicon Validation.
José Ernesto Rayas-Sánchez received the B.Sc. degree in electronics engineering from ITESO, Guadalajara, Mexico, the Masters degree in electrical engineering from Monterrey Tec, Monterrey, Mexico, and the Ph.D. degree in electrical engineering from McMaster University, Ontario, Canada. He is a Profesor Numerario (hons.) with ITESO – The Jesuit University of Guadalajara, where he is Chair of the Doctoral Program in Engineering Sciences. He leads the Research Group on Computer-Aided Engineering of Circuits and Systems (CAECAS) at ITESO. His research focuses on computer-aided and knowledge-based modeling, design, and optimization of high-frequency electronic circuits and devices (including RF, microwave, and wireless circuits).


Since 2013, he is IEEE MTT-S Regional Coordinator for Latin America. He was the General Chair of the First IEEE MTT-S Int. Microwave Workshop Series in Region 9 (IMWS2009-R9) on Signal Integrity and High-Speed Interconnects (Guadalajara, Mexico, Feb. 2009). He was the General Chair of the First IEEE MTT-S Latin America Microwave Conference (LAMC-2016, Puerto Vallarta, Mexico, Dec. 2016).

Edgar Andrei Vega-Ochoa received his bachelor’s degree in electrical engineering in 1997 from ITCG (Technical Institute of Guzman City, Mexico) and his Master’s degree in Electrical Engineering in 2000 from CINVESTAV Research Center (Guadalajara, Mexico). Edgar is an analog validation engineer at Intel Corp., he began his career as a pre-silicon validation engineer and spent three years on the validation of SONET/SDH framers and mappers. Later, Edgar moved to the Electrical Validation group where he has led the validation on multiple high speed interfaces (parallel and serial) for different projects on client, server and device market-segments.

José Luis Chávez-Hurtado was born in Guadalajara, Mexico, in 1985. He received the B.Sc., the M.Sc., and Ph.D. degrees in electronics engineering from ITESO – The Jesuit University of Guadalajara, Mexico, in 2007, 2009 and 2017, respectively. He also received the Master’s degree in business and economics from the University of Guadalajara, Mexico, in 2012.

Since 2012, he has been an adjunct professor with the Mathematics Department, University of Guadalajara – Business School, Mexico. Since 2014, he has also been an adjunct professor with the Department of Electronics, Systems, and Informatics, ITESO – The Jesuit University of Guadalajara, Mexico. His research interests include optimization methods for modeling and design of microwave circuits, surrogate-based optimization, neural network applications, linear programming and nonlinear forecasting.

Nagib Hakim received his MS and Ph.D. degrees in electrical engineering from Columbia University in 1986 and 1992, respectively after which he joined Intel Corporation in Santa Clara, CA. He has conducted extensive development in the areas of technology modeling and design optimization, including statistical circuit modeling and optimization, SER prediction, and power/performance analysis. He applied these techniques to system-level modeling for electrical post-silicon validation. He is currently a Principal Engineer in the AI Product Group of Intel focusing on machine learning and deep learning algorithms and applications. He has published more than 40 papers in the CAD and validation areas, and holds one patent. He was a recipient of the Mahboob Khan Outstanding Industry Liaison Award in 2012.