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Maestría en Diseño Electrónico

REPORTE DE FORMACIÓN COMPLEMENTARIA EN ÁREA DE CONCENTRACIÓN EN DISEÑO ELECTRÓNICO DE ALTA FRECUENCIA

TRABAJO RECEPCIONAL que para obtener el **GRADO** de
MAESTRO EN DISEÑO ELECTRÓNICO
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1. Introducción

El presente reporte final del trabajo de grado, corresponde al área de concentración de "Diseño Electrónico de Alta Frecuencia" dentro de la Maestría de Diseño Electrónico. Las tres asignaturas que se cursaron para la realización de dicho reporte fueron las siguientes: "Diseño Electrónico en Alta Frecuencia", "Método de Simulación de Circuitos Electrónicos" y "Modelado y Diseño de Circuitos Basados en Optimización".

Este trabajo representa un resumen de los proyectos finales de las materias antes mencionadas. Para la materia de "Diseño Electrónico de Alta Frecuencia", se presentó el proyecto "Diseño de un filtro rechaza banda". En la materia de "Método de Simulación de Circuitos Electrónicos", como proyecto final se trabajó en el "Cálculo del *Anti Pad* para un *PCB* de alta velocidad". Y finalmente, para la asignatura de "Modelado y Diseño de Circuitos Basados en Optimización", se presentó como proyecto final el "Cálculo del *Anti Pad* para un *PCB* de alta velocidad utilizando método de optimización".

En el área de diseño de tarjetas electrónicas en Intel Guadalajara, existen 4 grupos de especialización: Diseño Electrónico, Análisis de Integridad de Señal, Diseño físico de *PCBs (Printed Circuit Boards*) y Diseño de *FPGAs* (*Field Programmable Gate Arrays*). De éstas 4 áreas mencionadas, a lo largo de mi carrera me he enfocado principalmente al campo de diseño electrónico, al diseño de *FPGAS* y conozco muy bien el tema de diseño de *PCBs*. Sin embargo, en la parte de Análisis de Integridad de Señal, no me había involucrado mucho profesionalmente.

En el área de integridad de señal, principalmente se llevan a cabo las simulaciones de las nuevas topologías e interfaces, para saber si la propuesta de diseño, cumple con las velocidades y las restricciones de las nuevas tecnologías. En éste campo, se utilizan herramientas muy sofisticadas para realizar dichos análisis. Ésa fue la principal razón de elegir éste dominio como mi área de concentración, para poder conocer mejor las herramientas que se utilizan, entender los estudios y los requerimientos que ellos tienen, y saber interpretar toda la información y resultados que se genera con sus estudios.

De ésta manera, estaría cerrando el eslabón que me haría falta en mi grupo de desarrollo, para conocer de buena manera, las 4 áreas de enfoque y así adquirir el conocimiento necesario para ser mejor profesionista

2. Resumen de los proyectos realizados

2.1. Diseño de Filtro Rechaza Banda

El primer proyecto final consistió en el diseño de un filtro rechaza banda que cumpla con las siguientes especificaciones:

- Frecuencia central: 3.4 GHz
- Ancho de banda fraccional: 5%
- Orden del filtro: 3
- Tipo de respuesta: 0.1dB *Chebyshev*
- Impedancia: = 50Ω
- El circuito será fabricado en una microcinta usando el siguiente substrato:
  - Rogers RO4003
  - h = 0.81 mm
  - Revestimiento de 0.5oz
  - Er = 3.55

2.1.1 Teoría

Un filtro es una red de dos puertos usado para controlar la respuesta en frecuencia a cierto punto en un sistema de RF o de micro ondas, permitiendo la transmisión de frecuencias dentro de la banda de paso del filtro y atenuando en la banda de rechazo del filtro. Las típicas respuestas de frecuencia son: pasa bajas, pasa altas, pasa bandas y rechaza bandas. Las aplicaciones pueden ser encontradas en virtualmente cualquier tipo de comunicación RF, micro ondas, radar o equipos de medición y prueba.

2.1.2 Metodología

La metodología utilizada para resolver el diseño del filtro, se resume básicamente en los siguientes puntos:

1. Obtener los valores de g
2. Calcular los valores teóricos de Xi/Zo
3. Calcular el ancho de la traza y los valores de λ
4. Diseñar el resonador de forma L
5. Simular para obtener los valores de Xi/Zo
6. Simular para completar el filtro rechaza bandas en APLAC
7. Simular el filtro usando la herramienta Sonnet

2.1.3 Resultados de simulación usando la herramienta APLAC

El filtro rechaza bandas consiste de un resonador en forma de L, de orden 3. Los parámetros que se obtuvieron fueron los siguientes:

- W = 1.78 mm
- H = 0.81 mm
- 5H = 4.05 mm
- λ/4 = 13.14 mm
- S1 = 0.2518 mm
- S2 = 0.2125 mm
- S3 = 0.2518 mm.

Después de simular el diseño, los valores de frecuencia obtenidas fueron las siguientes:

- F0 = 3.386 GHz, F1 = 3.315 GHz, F2 = 3.465 GHz

Con base en los resultados se calculó el FBW, el cual fue muy cercano al requerimiento del 5% y el F0 de 3.3846%, también fue muy cercano al requerimiento de 3.4 GHz.

2.1.4 Resultados de simulación usando la herramienta SONNET

Con los mismos parámetros usados en la herramienta de APLAC, se creó un diseño con la herramienta de SONNET, sin embargo, los resultados fueron un poco diferentes, los cuales se muestran a continuación:

- F0 = 3.5025 GHz
- F1 = 3.366 GHz
- F2 = 3.639 GHz
- FBW = 7.79 %

Debido a ello, los valores de S fueron modificados para obtener un valor de FBW más cercano al 5%. Después de varios intentos, los valores S obtenidos fueron: S1 = 0.3512 mm, S2 = 0.3138 mm y S3 = 0.3512 mm. Los valores de frecuencia fueron:

- F0 = 3.512 GHz
- F1 = 3.416 GHz
- F2 = 3.608 GHz
- FBW = 5.4 %

2.1.5 Conclusiones

De los resultados obtenidos se puede concluir que debido a que la herramienta de APLAC es mucho más rápida que SONNET, APLAC se puede utilizar para obtener los valores semilla que serán alimentados a SONNET, ahorrando con esto mucho tiempo de simulación. Los valores obtenidos fueron muy cercanos al requerimiento, lo cual demostró que el proceso fue el adecuado. Solo es cosa de más tiempo de simulación para obtener el FBW del 5%.

Como parte del proyecto se evaluó a la herramienta Qucs, y se demostró que obtuvo resultados muy similares a APLAC. La ventaja de Qucs es que es una herramienta libre, y ésta puede ser usada en versión completa por el estudiante, desde la comodidad de su casa. Se demostró que es una excelente opción, y es muy fácil de usar.

2.2. Cálculo del *Anti Pad* para un *PCB* de alta velocidad

El segundo proyecto final consistió en el cálculo del *Anti Pad* para un *PCB* de alta velocidad. En los diseños que contienen señales de alta velocidad, es muy común ejecutar simulaciones para asegurar que la integridad de la señal es la adecuada. En éste caso, se llevaron a cabo simulaciones utilizando la herramienta de *HFSS (High Frequency Structural Simulation)*, para asegurarse que una de las trayectorias de la señales de alta velocidad, cumpliera con la impedancia controlada de 50 ohms.

Un elemento clave que afecta la impedancia son las capacitancias parásitas de la vía, por ello la importancia de simular, para encontrar el valor correcto del diámetro del *Anti Pad* en los planos de tierra, para mantener las capacitancias parásitas lo más bajo posible, ya que la capacitancia parásita de la vía está afectando la impedancia de la trayectoria de la señal.

Ahora bien, también la inductancia es un elemento clave que influye en el cálculo de la impedancia, sin embargo, para el alcance de éste proyecto se ignoró su influencia, debido a que se consideró que se encontraba bajo control, gracias al uso de 7 vias de tierra que rodeaban la vía de señal.

2.2.1 Especificaciones del diseño

Para las especificaciones de diseño se definió el *stackup* del *PCB* a ser usado, para que sea capaz de transmitir las señales de alta velocidad. Dicho *stackup* fue proporcionado por el fabricante del *PCB*. El material utilizado es el Megtron6 que es un material de baja pérdidas.

Usando el *stackup* del *PCB* como referencia se creó el modelo del *PCB* para la herramienta *HFSS*. Otro requerimiento fue utilizar el modelo del conector SAMTEC que fue entregado por la propia compañía fabricante del conector. Dicho modelo ya contenía las características necesarias para ser utilizado en la simulación con la herramienta *HFSS*. El modelo del *PCB* creado fue conectado al modelo del conector. Ambos modelos forman el modelo completo para la simulación. La impedancia de la trayectoria a simular debe de ser de 50 ohms ± 5%.

2.2.2 Modelos *HFSS*

En el *stackup* del *PCB* se presentan dos tipos de vías: Una vía *through hole* que va de la capa 1-6 y un micro vía que va de la capa 1-2, y de la capa 5-6. Por lo tanto se crearon dos modelos de vías. En un modelo se simularon la vía *through hole* y en el según modelo, se simularon la micro vías. Las descripciones gráficas de los modelos se pueden observar en el apéndice 2.

2.2.3 Resultados de la simulación: Vía *through hole*

Una vez que los modelos en *HFSS* fueron creados, se corrieron varias simulaciones para encontrar los valores adecuados del *Anti Pad.* La herramienta *HFSS* fue preparada para entregar la impedancia terminal TDR.

Debido a que el tamaño del pad del conector es diferente del tamaño del pad de la vía, dos diferentes *Anti Pad* fueron utilizados: *Anti Pad1* y *Anti Pad2.* El *Anti Pad1* es usado en el plano de tierra 1 y el *Anti Pad2* es usado en los planes de tierra 3, 4 y 6

De los resultados de la simulación los mejores valores obtenidos fueron del diámetro de *Anti Pad1*=60 mils y para el *Anti Pad2*=28 mils, con los cuales se obtuvieron una impedancia máxima de 53.56 ohms y una mínima de 44.06 ohms. Aunque los resultados obtenidos están un poco fuera de especificación, los valores están muy cercanos a los valores esperados, y por lo tanto se consideran valores aceptables.

2.2.4 Resultados de la simulación: Micro Vía

En el caso del micro vía, mejores resultados se obtuvieron. Los mejores resultados se obtuvieron para un *Anti Pad1*= 45 mils y *Anti Pad2*= 50 mils. El valor máximo de la impedancia obtenida fue de 51.26 ohms y el valor mínimo de la impedancia fue de 46.98 ohms. Ambos valores están muy cercanos a la especificación de 50 ohms ± 5%. Las gráficas de los resultados se pueden observar en el apéndice 2.

2.2.5 Conclusiones

Fue muy interesante trabajar en una herramienta en la que se integraron los modelos del fabricante del conector y de nuestro *PCB*, integrar ambos modelos y ejecutar simulaciones para obtener valores más cercanos a la realidad de los valores del *Anti Pad1 y 2*.

Varias simulaciones fueron ejecutadas para el modelo de *through hole*, sin embargo no se pudieron obtener valores que cumplieran 100% con la especificación. A pesar de ello, después de preguntar a varios expertos al parecer esto no es muy inusual. Al final de cuentas, la idea es estar más cerca al estado ideal, aunque algunas veces no puede ser logrado, pero son aproximaciones muy certeras.

2.3. Cálculo del *Anti Pad* para un *PCB* de alta velocidad utilizando métodos de optimización

En el tercer proyecto final consistió en utilizar métodos de optimización para resolver el problema del segundo proyecto final, es decir, el cálculo del *Anti Pad* para un *PCB* de alta velocidad. Anteriormente, las simulaciones fueron ejecutadas sin utilizar ningún método de optimización. Los valores de *Anti Pad* fueron cambiados en forma manual.

En éste caso el objetivo fue utilizar los mismos modelos *HFSS*, pero ahora se utilizaron métodos de optimización para calcular los valores de *Anti Pad*, en lugar de cambiarlos en forma manual.

2.3.1 Métodos de optimización

La tecnología de optimización ha sido adoptada rápidamente en la mayoría de las industrias. La idea es entregar mejores diseños en menos tiempo comparado con los métodos manuales. Una de las principales barreras tiene que ver con escoger el algoritmo adecuado de optimización.

Para el desarrollo de éste proyecto se utilizó el método de optimización llamado *Nelder-Mead*. En éste método los valores de *Anti-Pad* fueron alimentadas como las entradas al modelo de

optimización y las salidas finales fueron los valores de *Anti Pad* optimizados para tener los valores de impedancia entre ciertos valores.

2.3.2 Especificaciones del diseño

Para las especificaciones de diseño se definió el *stackup* del *PCB* a ser usado, para que sea capaz de transmitir las señales de alta velocidad. Dicho *stackup* fue proporcionado por el fabricante del *PCB*. El material utilizado es el Megtron6 que es un material de baja pérdidas.

Usando el *stackup* del PCB como referencia se creó el modelo del *PCB* para la herramienta *HFSS*. Otro requerimiento fue utilizar el modelo del conector SAMTEC que fue entregado por la propia compañía fabricante del conector. Dicho modelo ya contenía las características necesarias para ser utilizado en la simulación con la herramienta *HFSS*. El modelo del *PCB* creado fue conectado al modelo del conector. Ambos modelos forman el modelo completo para la simulación. La impedancia de la trayectoria a simular debe de ser de 50 ohm ± 5%.

2.3.3 Modelos *HFSS*

En el *stackup* del PCB se presentan dos tipos de vías: Una vía *through hole* que va de la capa 1-6 y un micro vía que va de la capa 1-2, y de la capa 5-6. Por lo tanto se crearon dos modelos de vías. En un modelo se simularon la vía *through hole* y en el según modelo, se simularon la micro vías. Las descripciones gráficas de los modelos se pueden observar en el apéndice 3.

2.3.4 Modelo de optimización: MATLAB driver

Una vez que el modelo *HFSS* ha sido creado, éste fue usado como base para crear el manejador de Matlab. La función clave fue el grabar un *script* en la herramienta de HFSS. Éste *script* contiene todas las operaciones que se necesitan ejecutar en el modelo HFSS para poder ejecutar las simulaciones con diferentes valores de *Anti Pad*, y esto fue grabado en un archivo.

El proceso para crear el manejador de Matlab se describe en el apéndice 3.

Todas las actividades del *script* se grabaron en un archivo .vbs de tal forma que cada vez que éste archivo es ejecutado, todas las actividades contenidas en dicho archivo, son ejecutadas

automáticamente. El único cambio que es ejecutado en el *script* es reemplazar los valores de *Anti Pad* por variables, para que ésas puedan ser modificadas automáticamente.

2.3.5 Parámetros fijos, variables de optimización y valores de inicio

Debido a que las simulaciones ya habían sido ejecutadas in *HFSS* pero sin ningún método de optimización, los valores de *Anti Pad* se modificaban en forma manual, y ésos eran los únicos elementos que se modificaban. Por lo tanto, los variables para optimización que fueron tomados son *Anti Pad1* (para la parte de arriba de la tarjeta) y *Anti Pad2* (para las capas internas de la tarjeta y la capa inferior). Por lo tanto, los valores iniciales que se definieron fueron basados en las simulaciones del proyecto anterior los cuales son *Anti Pad1* = 46 mils y *Anti Pad2* = 52 mils.

El resto de los elementos del diseño fueron considerados como parámetros fijos.

2.3.6 Resultados de la simulación usando Matlab

Una vez que el modelo de optimización fue ejecutado, varias iteraciones fueron ejecutadas para encontrar los valores correctos. De los resultados, la máxima impedancia obtenida fue 55.51 ohm con un diámetro de *Anti Pad1* de 59.51 mils, y una impedancia 46.65 ohm con el *Anti Pad2* diámetro de 32.5 mils. Esto fue con una tolerancia del 15%. Los resultados son muy cercanos a los obtenidos en forma manual, pero ahora más rápido y eficiente.

2.3.7 Conclusiones

Uno de los elementos claves del proyecto fue la creación del manejador para Matlab. La idea inicial era usar uno que ya existía, pero debido a que no funcionaba adecuadamente, se decidió en crear uno nuevo con base a la información dada en clase. El nuevo driver funcionó adecuadamente.

Fue muy interesante ver cómo aplicar los métodos de optimización en una herramienta tan complicada como *HFSS* y ver como los resultados fueron los esperados ahorran mucho tiempo respecto al proceso manual

3. Conclusiones

Dentro del área de concentración de Diseño Electrónico de Alta Frecuencia, los tres proyectos finales son aplicables completamente al tipo de análisis de integridad de señal que se lleva a cabo en los centros de desarrollo de Intel.

En el primer proyecto, se aprendieron herramientas de simulación como APLAC, SONNET y por mi cuenta estudié Qucs. Estas herramientas han sido de mucha ayuda, para realizar simulaciones en diferentes diseños que se han realizado dentro de la empresa.

Para el segundo proyecto, se trabajó con *HFSS* integrando modelos de simulación y ejecutando simulaciones para análisis de integridad de señal. Éste tipo de simulaciones es muy común en mi grupo de trabajo, pero yo no había estado familiarizado con ellas. Gracias a ésta clase, pude entender bastante al grupo de integridad de señal y el porqué del tipo de trabajo que están realizando.

Para el tercer proyecto, fue muy interesante utilizar los métodos de optimización, Matlab y *HFSS*. Juntas las tres herramientas entregaron resultados increíbles. Además, estos métodos de optimización pueden ser utilizados en diferentes áreas de diseño. Serán de mucha utilidad en un futuro.

Las tres materias me han proporcionado conocimientos que son altamente aplicados en mi grupo de desarrollo dentro de Intel, y principalmente para el área de integridad de señal.

Gracias al conocimiento adquirido en estos cursos y a su aplicación en proyectos reales en el desarrollo tecnológico en Intel, he podido entender cómo se llevan a cabo las simulaciones de las nuevas topologías e interfaces, para saber si se cumple con las velocidades y las restricciones de las nuevas tecnologías. Para mí ahora es familiar el uso de las herramientas que se utilizan para realizar dichos análisis. Ahora entiendo los conceptos, términos, información que se utiliza en mi área de trabajo, del tal forma que ahora puedo interpretar toda la información y resultados que se generan.

Como lo mencioné en la introducción del trabajo, la realización de estos proyectos me ha ayudado a cerrar el eslabón que me hacía falta para conocer todo lo que se realiza en mi grupo de desarrollo en Intel.

Apéndices

1. BAND STOP FILTER DESIGN

1. Introduction

1.1 Problem Statement

Design a Band-Stop filter with the following specifications:

- Center frequency: 3.4 GHz
- Fractional Bandwidth: 5%
- Filter order: 3
- Type of frequency response: 0.1dB Chebyshev
- Reference impedance = 50Ω
- The Circuit will be fabricated in microstrip using the following substrate:
    - Rogers RO4003
        - h = 0.81 mm
        - cladding of 0.5oz
        - Er = 3.55
        - www.rogers-corp.com

1.2 Deliverables

The deliverables for the project are:

- Simulate the filter using APLAC
- Obtain the layout and then simulate the circuit layout using SONNET in order to observe any deviation from the circuit simulations performed with APLAC
- Modify the layout if necessary to match the specifications.

2. Theoretical Analysis

2.1 Theoretical Background

A filter is a two-port network used to control the frequency response at a certain point in an RF or microwave system by providing transmission at frequencies within the passband of the filter and attenuation in the stopband filter. Typical frequency responses include low-pass, high-pass, band-pass, and band-reject characteristics. Applications can be found in virtually any type of RF or microwave communication, radar, or test and measurement.

There are two general methods for filter design: The image parameter method and the insertion loss method. The image parameter method of filter design was developed in the late 1930s and was useful for low-frequency filters in radio and telephony. Today, most microwave filter design is done with sophisticated computer-aided design (CAD) packages based on the insertion loss method.

Filters designed using the image parameter method consist of a cascade of simpler two-port filter sections to provide the desired cutoff frequencies and attenuation characteristics but do not allow the specification of a particular frequency response over the complete operating range. Thus, although the procedure is relatively simple, the design of filters by the image parameter method often must be iterated many times to achieve the desired results.

The method utilized on this filter design was the insertion loss method, which uses network synthesis techniques to design filters with a completely specified frequency response. The design is simplified by beginning with low-pass filter prototypes that are normalized in terms of impedance and frequency. Transformations are then applied to convert the prototype designs to the desired frequency range and impedance level.

2.2 Methodology

The methodology utilized to solve this filter design was the one explained at class, which is the next one:

1- To obtain the g's values
2- To calculate the Xi/Zo theoretical values
3- Trace width and λ calculations
4- L shape resonator design
5- Simulation to obtain Xi/Zo values
6- To simulate the complete band-stop filter in APLAC
7- To simulate the filter design using the Sonnet tool

2.3 Design Development

The design of the filter was obtained by following the proposed methodology:

2.3.1 Obtaining the g's values

Based on the design requirements, since the design filter order is 3 and the type of response must be a 0.1 dB Chebyshev, the g's values were obtained from the table 2.1 below. The table was obtained from the "Microstrip Filters for RF/Microwave Applications" book.

n	g_1	g_2	g_3	g_4	g_5	g_6	g_7	g_8	g_9	g_{10}
1	0.3052	1.0								
2	0.8431	0.6220	1.3554							
3	1.0316	1.1474	1.0316	1.0						
4	1.1088	1.3062	1.7704	0.8181	1.3554					
5	1.1468	1.3712	1.9750	1.3712	1.1468	1.0				
6	1.1681	1.4040	2.0562	1.5171	1.9029	0.8618	1.3554			
7	1.1812	1.4228	2.0967	1.5734	2.0967	1.4228	1.1812	1.0		
8	1.1898	1.4346	2.1199	1.6010	2.1700	1.5641	1.9445	0.8778	1.3554	
9	1.1957	1.4426	2.1346	1.6167	2.2054	1.6167	2.1346	1.4426	1.1957	1.0

Table 2.1 Element Values for pass band ripple 0.1 dB

From the table 2.1, the g's values were obtained for a filter order n=3:

g0 = 1.0
g1 = 1.0316
g2 = 1.1474
g3 = 1.0316
g4 = 1.0

2.3.2 Xi/Zo theoretical values calculations

Using the g's values obtained on the 2.3.1 section, the Xi/Zo values were calculated in the following way:

$$x_i = Zo\,(\frac{Zu}{Zo})^2 \frac{g_o}{g_i\,\Omega_c\,FBW} \qquad \text{For i =1 to n}$$

$$\frac{x_i}{Z_o} = (\frac{Zu}{Zo})^2 \frac{g_o}{g_i\,\Omega_c\,FBW}$$

Since Zu = Zo = 50 Ω, the equation can be reduced to:

$$\frac{x_i}{Z_o} = \frac{g_o}{g_i\,\Omega_c\,FBW}$$

Since Ωc = Wc = 1, the equation can be reduced to:

$$\frac{x_i}{Z_o} = \frac{g_o}{g_i\,FBW}$$

Since design filter order n=3, we will calculate three values for xi/Zo:
For i =1:

$$\frac{x_1}{Z_o} = \frac{g_o}{g_1(0.05)} = \frac{1}{(1.0316)(0.05)} = 19.38$$

For i =2:

$$\frac{x_2}{Z_o} = \frac{g_o}{g_2(0.05)} = \frac{1}{(1.1474)(0.05)} = 17.43$$

For i =3:

$$\frac{x_3}{Z_o} = \frac{g_o}{g_3(0.05)} = \frac{1}{(1.0316)(0.05)} = 19.38$$

2.3.3 Trace width and λ calculations

The trace width was calculated based on the problem specifications:

- H=0.81 mm
- Impedance = 50 Ω
- Er = 3.55
- Cladding of 0.5oz (From Rogers R04003 datasheet Thickness = 17 um)

With the previous specifications and using the PCB Microstrip impedance calculator from EE Web Electrical Engineering Community, the trace width was calculated to match the 50 Ω impedance.

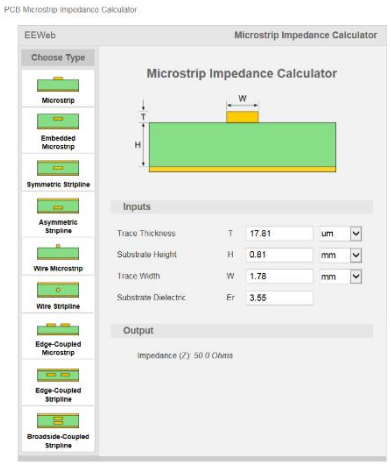


Figure 2.2 PCB Microstrip impedance calculator

The trace width calculated was 1.78 mm.

Knowing the trace width value, the λ value is calculated using the center frequency of 3.4 GHz:

$$\lambda = \frac{V_p}{f}$$

$$V_p = \frac{c}{\sqrt{Ee}}$$

$$\lambda = \frac{c}{f\sqrt{Ee}}$$

$$Ee = \frac{Er + 1}{2} + \frac{Er - 1}{2\sqrt{1 + (10H/W)}}$$

$$Ee = \frac{3.55 + 1}{2} + \frac{3.55 - 1}{2\sqrt{1 + (\frac{10(0.81)}{1.78})}} = 2.275 + 0.5411 = 2.8161$$

$$\lambda = \frac{0.3\ Gm/s}{3.4\ GHz\ \sqrt{2.8161}} = 0.0525\ m = 52.5\ mm$$

$$\frac{\lambda}{2} = 26.28\ mm$$

$$\frac{\lambda}{4} = 13.14\ mm$$

2.3.4 L shape resonator design

Based on the parameters obtained in the previous section, the L shape resonator was designed:

- W = 1.78 mm
- H = 0.81 mm
- 5H = 4.05 mm
- λ/4 = 13.14 mm
- S was the variable that was modified to obtain the x/Zo values

The L shape resonator parameters were based on the following figure

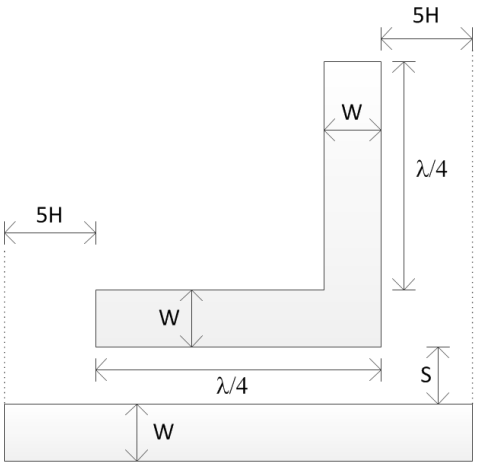


Figure 2.3: L shape resonator design parameters

The design was captured and simulated in APLAC tool, like described below:

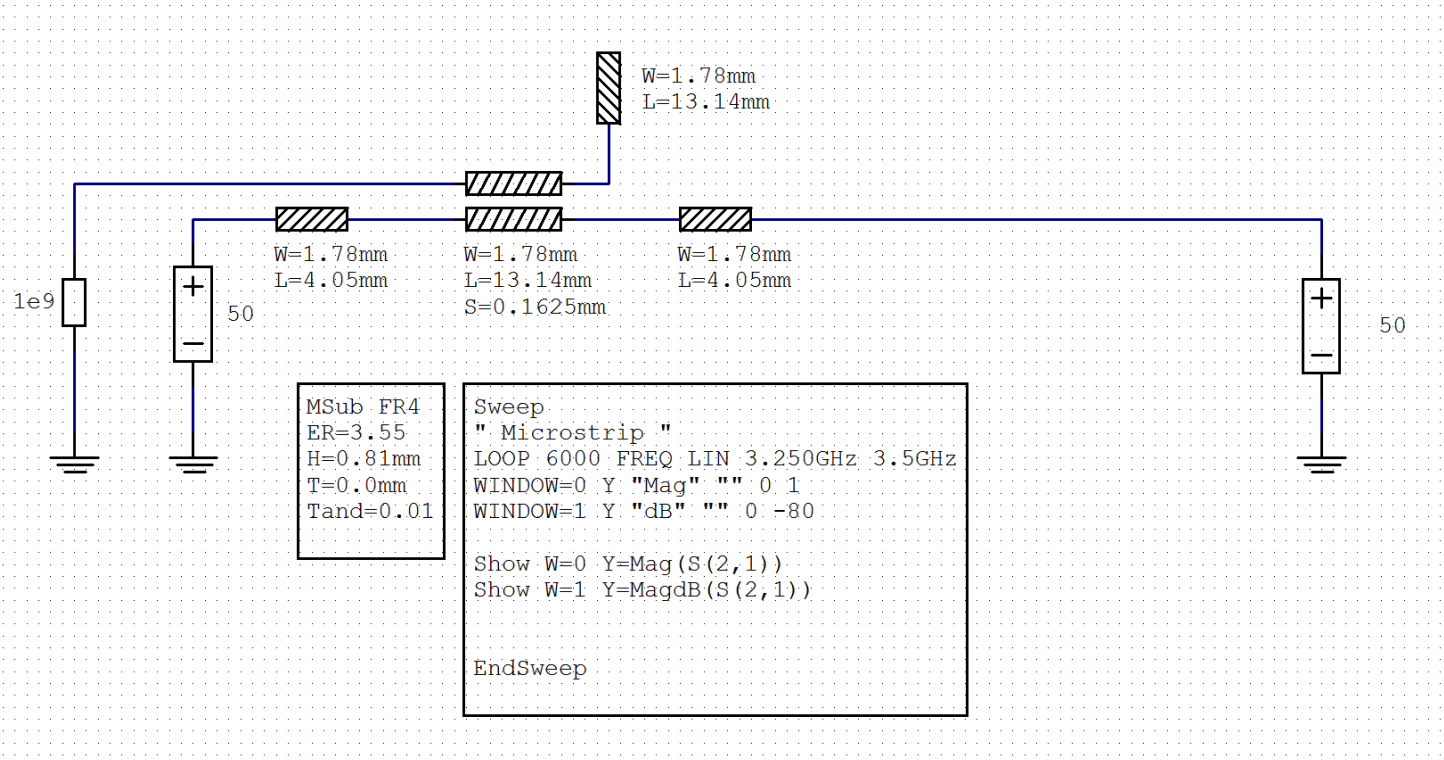


Figure 2.4: L shape resonator design in APLAC

2.3.5 Simulation to obtain Xi/Zo values

Once the Xi/Zo theoretical values were obtained and the W and λ values were calculated, the next step in the methodology is to obtain Xi/Zo simulated values using the APLAC tool, that match as close of possible the Xi/Zo theoretical values.

To obtain the Xi/Zo simulated values, the L shape resonator with λ/2 length is simulated for a specific S value, and the frequencies F0, F1 and F2 are obtained. From those frequencies values, and using the following formula, the x/Zo parameter is obtained:

$$\frac{x}{Z_o} = \frac{f_o}{2\Delta f_{3dB}} = \frac{f_o}{2(f_2 - f_1)}$$

S value is changed and new values of Xi/Zo are obtained. The process is repeated until the X/Zo value is closer to the Xi/Zo theoretical values.

The frequencies values of F0, F1 and F2, are obtained from the S21 response, as described below. F1 and F2 are measured at the -3 dB level.

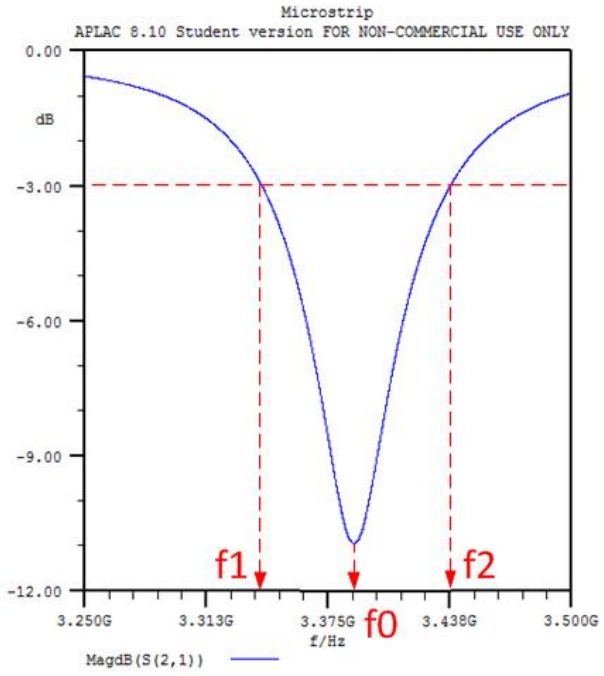


Figure 2.4: S21 response obtained for a specific S value

After several simulations were performed for different S values, the following values were obtained:

S (mm)	f0 (GHz)	f2 (GHz)	f1 (GHz)	x/Zo
0.000000025	3.368	3.767	3.021	2.257373
0.000025	3.379	3.652	3.138	3.286965
0.00025	3.383	3.606	3.187	4.036993
0.0025	3.388	3.556	3.239	5.343849
0.025	3.392	3.504	3.29	7.925234
0.1	3.391	3.463	3.324	12.19784
0.15	3.39	3.45	3.333	14.48718
0.2	3.389	3.44	3.34	16.945
0.2125	3.388	3.438	3.341	17.46392
0.225	3.388	3.436	3.342	18.02128
0.25	3.387	3.432	3.344	19.24432
0.25125	3.387	3.432	3.344	19.24432
0.251875	3.387	3.432	3.345	19.46552
0.2525	3.387	3.432	3.345	19.46552
0.255	3.387	3.431	3.345	19.69186
0.26	3.387	3.43	3.345	19.92353
0.3	3.386	3.425	3.348	21.98701

Figure 2.5: Simulations values obtained

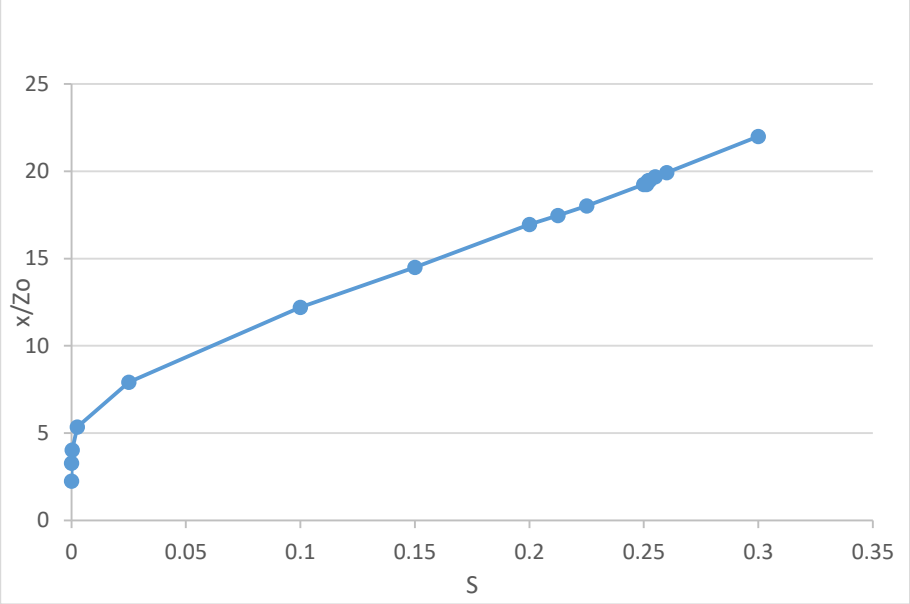


Figure 2.6: Graphic of the simulations values obtained

Since the theoretical values for x/Zo are 17.43 and 19.38, the closer values obtained from Figure 2.5 are 17.46 and 19.46 that corresponds to an S value of 0.2125 mm and 0.2518 mm respectively.

Those S values are the ones that will be used in the filter.

3 Band Stop Filter APLAC Simulations Results

The Band Stop Filter consists of 3 L shape resonators (Filter Order =3). In previous section were obtained the different parameters that correspond to the xi/Zo theoretical values. The schematic and the parameters obtained for the filter are described below.

- W = 1.78 mm
- H = 0.81 mm
- 5H = 4.05 mm
- λ/4 = 13.14 mm
- S1 = 0.2518 mm
- S2 = 0.2125 mm
- S3 = 0.2518 mm

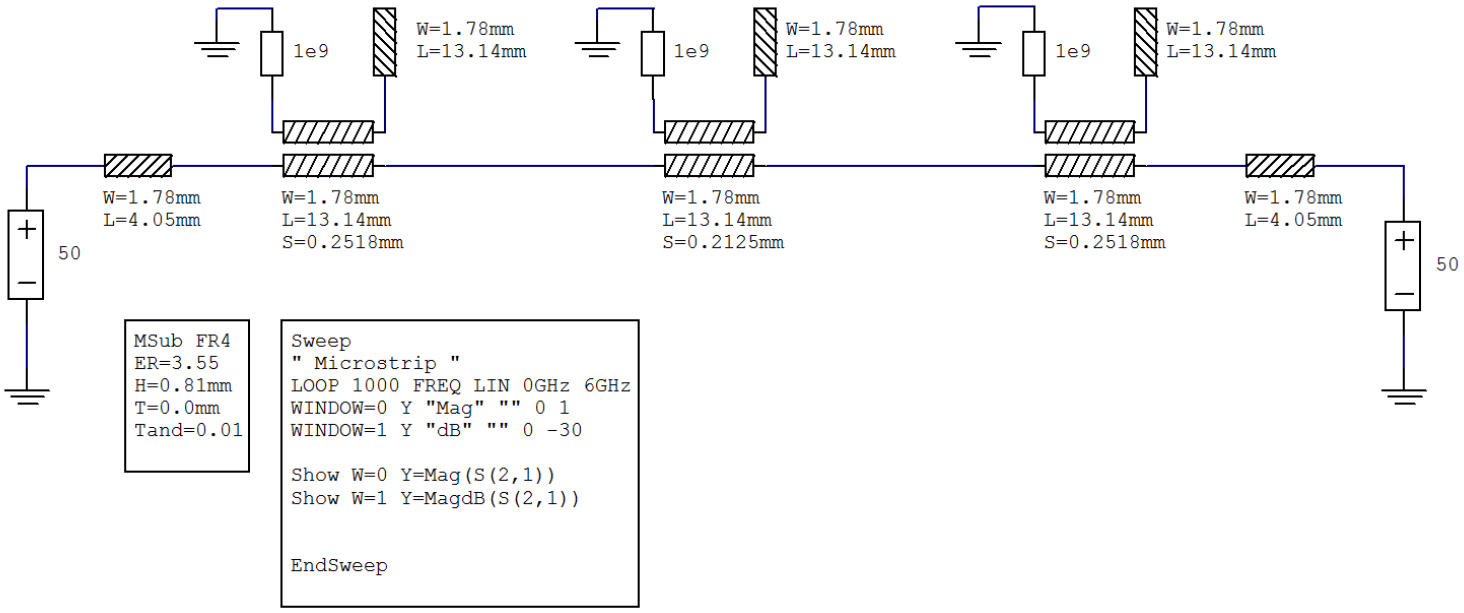


Figure 3.1: Band Stop Filter schematic in APLAC

After simulating this design, the following waveform was obtained:

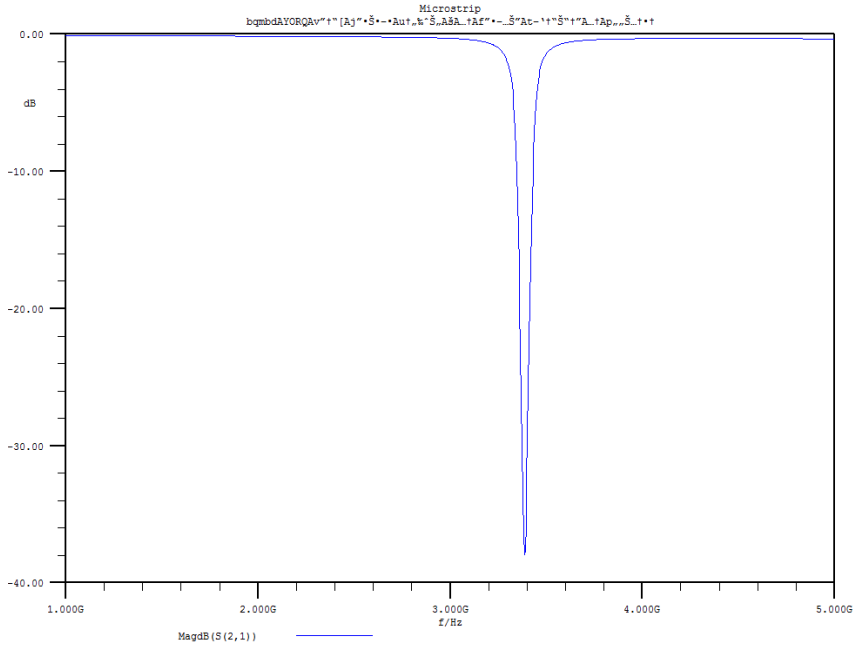


Figure 3.2: Band Stop Filter simulation results in APLAC

The values of the frequencies obtained from this waveform are:

- F0 = 3.386 GHz
- F2 = 3.465 GHz
- F1 = 3.315 GHz

Based on this results, the FBW was calculated using the following formulas:

$$FBW = \frac{f_2 - f_1}{f_0}$$

$$f_0 = \frac{f_1 + f_2}{2}$$

$$FBW = 4.42\ \%$$

FBW was very close to the requirement of 5% and the F0 of 3.3846 GHz was very close to the 3.4 GHz requirement

4 Band Stop Filter SONNET Simulations Results

With the same parameters than in APLAC tool, a design was created for the SONNET tool. The parameters were the next ones:

- W = 1.78 mm
- H = 0.81 mm
- 5H = 4.05 mm
- λ/4 = 13.14 mm
- S1 = 0.2518 mm
- S2 = 0.2125 mm
- S3 = 0.2518 mm

However, the results were not like the APLAC tool. The results were:

The results obtained from the simulation were:

- F0 = 3.5025 GHz
- F2 = 3.639 GHz
- F1 = 3.366 GHz
- FBW = 7.79 %

The values of the S were modified to get a FBW value closer to 5%. After several tries, the values of S to get a FBW closer to the specification were:

- S1 = 0.3512 mm
- S2 = 0.3138 mm
- S3 = 0.3512 mm

And the frequency values obtained were:

- F0 = 3.512 GHz
- F2 = 3.608 GHz
- F1 = 3.416 GHz
- FBW = 5.4 %

The Sonnet diagram utilized and waveform obtained are below:

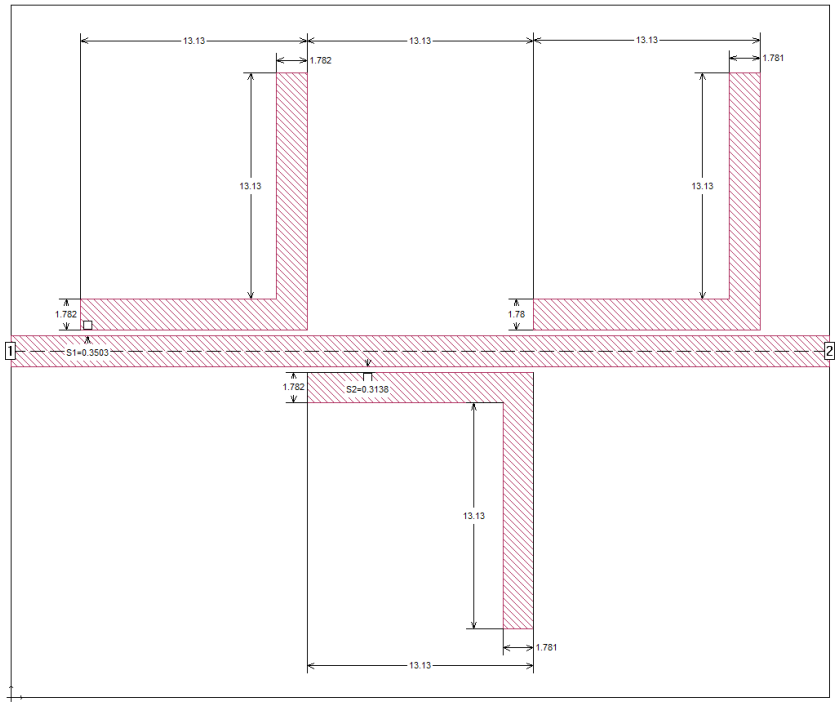


Figure 4.1: Band Stop Filter model in SONNET

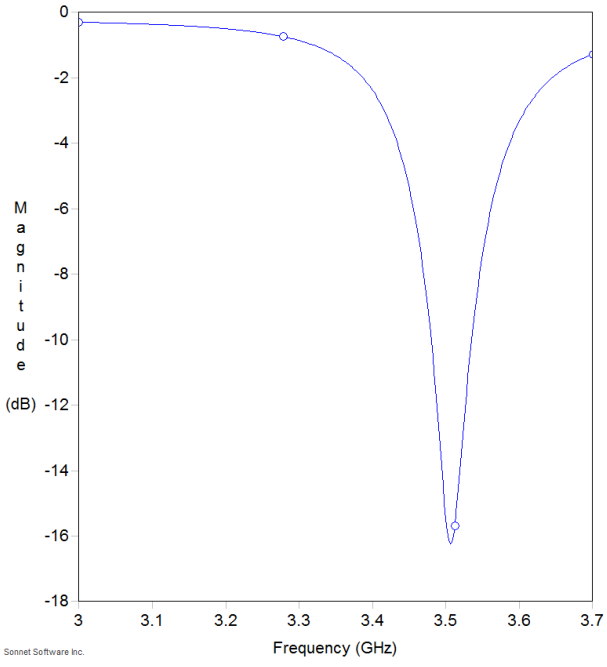


Figure 4.2: Band Stop Filter simulation results in SONNET

5 Band Stop Filter using Qucs tool

Due to both tools (APLAC and SONNET) need to be used at the ITESO laboratory, to be able to run simulations with the 3 resonators, I investigated another tool that could be used at home, and I found the Qucs tool, which is free (http://qucs.sourceforge.net/).

Qucs stands for Quite Universal Circuit Simulator, and it is a simulator very similar to APLAC tool.

Qucs is an integrated circuit simulator which means you are able to setup a circuit with a graphical user interface (GUI) and simulate the large-signal, small-signal and noise behavior of the circuit. After that simulation has finished you can view the simulation results on a presentation page or window.

The Qucs GUI is well advanced and allows setting up schematics and presenting simulation results in various types of diagrams. DC, AC, S-parameter, noise and transient analysis is possible, mathematical equations and use of a sub circuit hierarchy (with parameterized sub circuits) are available. Qucs can also import existing SPICE models for use in your simulations.

The APLAC schematic was converted to the Qucs environment, and the circuit looks like this:

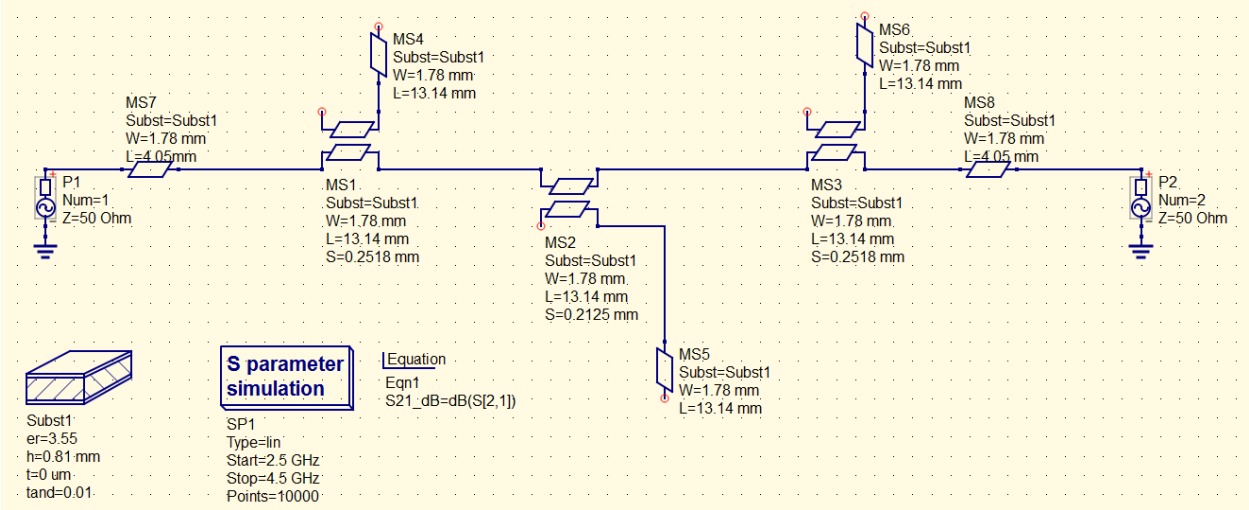


Figure 5.1: Band Stop Filter schematic in Qucs

As we can see in the figure 5.1, the circuit is very similar to APLAC. After it was simulated, the waveform obtained was the next one:

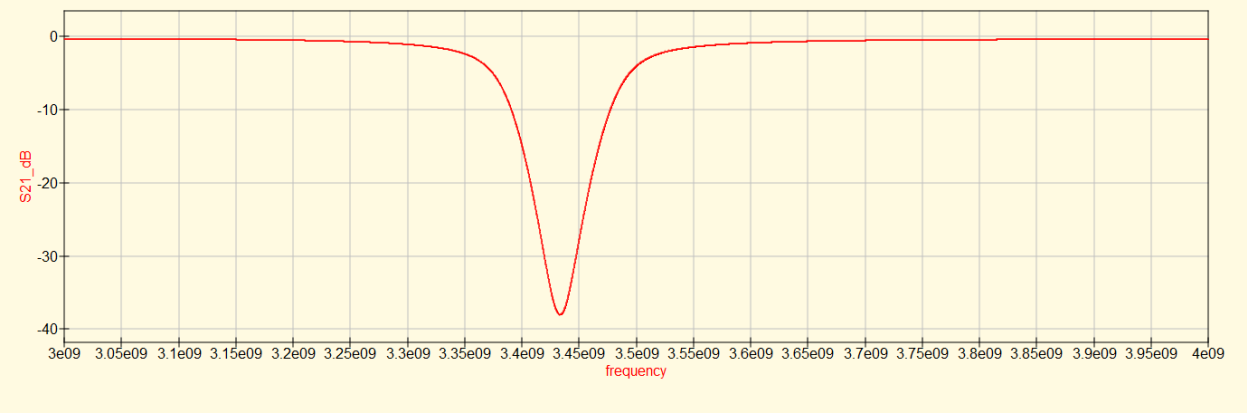


Figure 5.2: Band Stop Filter simulation results in Qucs

The values of the frequencies obtained from this waveform are:

- F0 = 3.386 GHz (APLAC) vs 3.43 GHz (Qucs)
- F2 = 3.465 GHz (APLAC) vs 3.51 GHz (Qucs)
- F1 = 3.315 GHz (APLAC) vs 3.36 GHz (Qucs)
- FBW = 4.42% (APLAC) vs 4.3% (Qucs)

As we can see, the results are very similar. Therefore, since Qucs is the complete version and it is free, it can be a very good option when a simulator APLAC like is needed.

6 Conclusions

From the results obtained what we can conclude is that, we used the APLAC tool to get the approximated values for S (seed values). Since APLAC tool is faster than SONNET, APLAC helped saving a lot of time to work with several interactions. Once the seed values were obtained (S1 = 0.2518mm, S2=0.2125 mm, S3 = 0.2518 mm) the first approximation of the filter was obtained. In this case, F0 = 3.386 GHz and FBW = 4.42%. Then, using those values as a seed, the SONNET simulations were performed, and after several tries, the values obtained were F0 = 3.512 GHz and FBW = 5.4%. As we can see, even though FBW is very close to 5%, which is the requirement, the F0 value is a little bit higher (3.512 GHz) in reference with the requirement (3.4 GHz).

Here the next step is to start modifying the values of S and L of the filter, until getting the F0 and FBW requested. It can take some time to get the values, therefore the exercise was concluded here, since the right process to perform the design has been proven and is just a matter of time, to get to the required values.

The filter was successfully designed following the procedure explained in class. The requirements were followed as expected.

Qucs tool presented results very similar than the APLAC tool, therefore, it can be used for future generations in class, to be able to work from home.

6 Bibliography

- Microwave Engineering. David M. Pozar; 2012 John Wiley & Sons, Inc.
- Microstrip Filters for RF/Microwave Applications. Jia-Sheng Hong, M. J. Lancaster; 2001 John Wiley & Sons, Inc.
- Rogers RO4003 Datasheet: www.rogers-corp.com
- PCB Microstrip impedance calculator from EE Web Electrical Engineering Community (http://www.eeweb.com/toolbox/microstrip-impedance)
- Qucs tool (http://qucs.sourceforge.net/)

2. ANTI PAD CALCULATION FOR A HIGH SPEED PCB

1 Introduction

In the design of PCBs that contains high speed signals, is very common to perform signal integrity simulations in certain areas of the design (the most critical ones), using tools like HFSS (High Frequency Structural Simulation) from ANSYS. In the case of this project, there was a need to design a board to perform electrical validation of one of the chips designed by Intel. The board include in its design a Samtec connector bulls eye type, like the one depicted in the figure 1.1

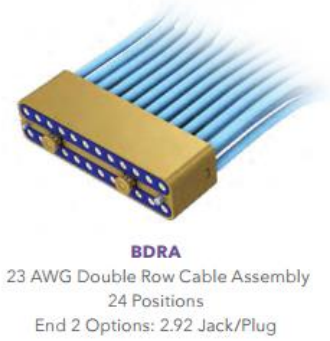


Figure 1.1 Samtec connector (bulls eye type).

The Samtec connector goes to the CPU via single ended lines with a controlled impedance of 50 ohms, and this was the part of the design that was simulated, which corresponds to the path: Samtec connector – connector pad - via – via pad - trace, which is described in the figure 1.2.

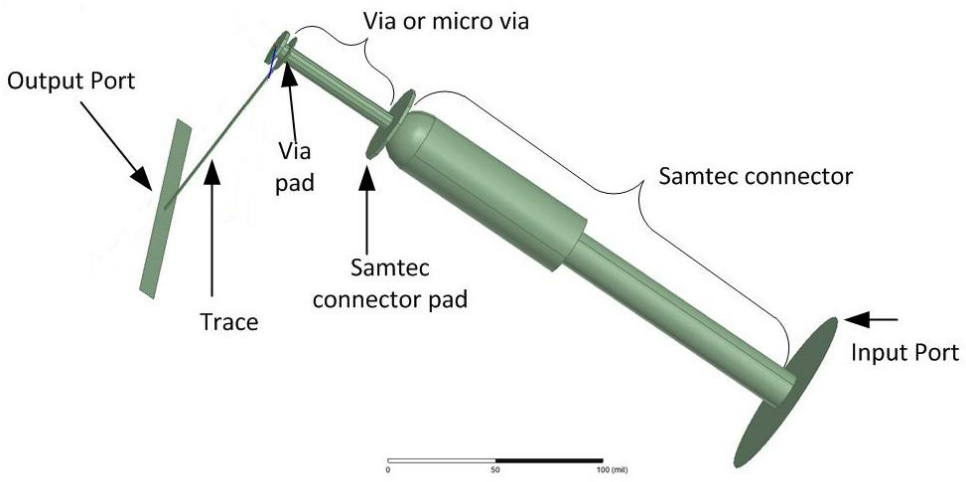


Figure 1.2 Path simulated: Samtec – Via - Trace

It is very important for the design, to maintain as much as possible the 50 ohms impedance in the path. One key element that is affecting the impedance is the parasitic capacitance of via, hence the importance to perform the simulations, to find the right value of the

anti-pad diameter in the ground planes, to maintain that parasitic capacitance very low. The anti-pad is described in the figure 1.3.

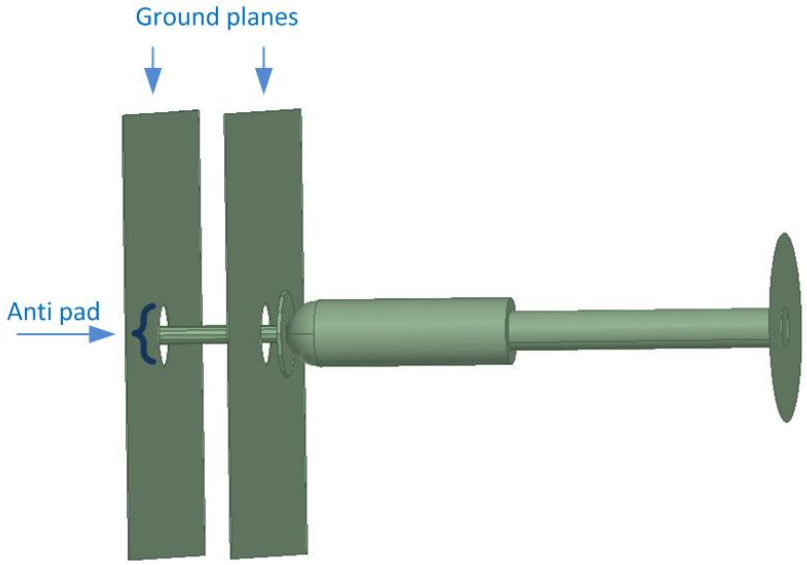


Figure 1.3 Anti pads in the ground planes

The present report contains the following elements:

- Theory to describe why is important to reduce the parasitic capacitance of the via
- Specifications of the PCB:
  - Board stack up
  - SAMTEC connector model
- Results of the models created in HFSS
  - Through hole via
  - Micro via
- Simulation results for through hole via and micro via
- And finally, the conclusions

2 Theory

In the design of PCB boards that include higher speed frequencies, it is very important to take into account the parasitic elements that are intrinsic in the physical design. In this project, the parasitic capacitance of via is affecting the impedance of the complete signal path.

For the impedance equation, various forms exist depending on whether we are examining plane wave impedance, circuit impedance, and the like. For wire, or a PCB trace, the following equation is used:

$$Z = R + jX_L + \frac{1}{jX_C} = R + jwL + \frac{1}{jwC} \qquad (2.1)$$

where $X_L = 2\pi fL$ (the component in the equation that relates only to wires or PCB traces) [1]

$$X_C = \frac{1}{2\pi f C} \qquad (2.2)$$

$$w = 2\pi f_C \qquad (2.3)$$

As we can see in the equation 2.1, the capacitance is a key factor in the calculation of the impedance, that in the case of this project, the capacitance of the via was key for the calculation of the impedance for the complete path, which is formed by the SAMTEC connector, the via and the PCB trace, as described in the figure 2.1.

Every via has parasitic capacitance to ground. Vias being physically small structures, they behave very much like lumped circuit elements. We can predict, within an order of magnitude, the amount of parasitic capacitance for a via: [2]

$$C = \frac{1.41 \varepsilon r \, T D_1}{D_2 - D_1} \qquad (2.4)$$

Where D2 = diameter of clearance hole in ground plane(s), in.
D1 = diameter of pad surrounding via, in.
T = thickness of printed circuit board, in.
εr = relative electric permeability of circuit board material
C = parasitic via capacitance, pF

When the pad size approaches the clearance hole diameter, pads pick up a lot more capacitance. If your ground clearance holes must remain small to maintain ground continuity, shrink or eliminate the pads on ground layers. For trace routing vias, it doesn't matter if you get some breakout on the plane layers. [2]

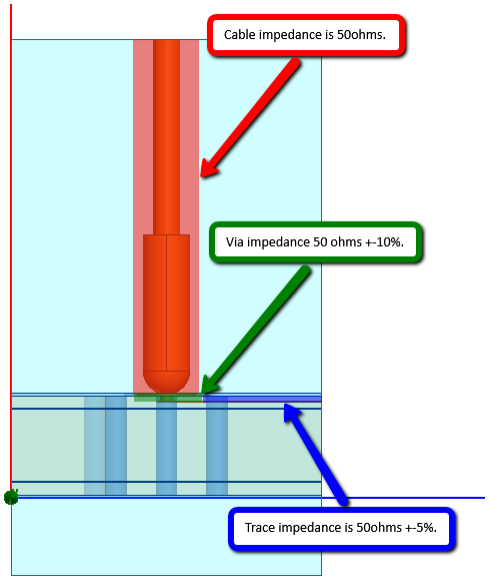


Figure 2.1 Impedance of the cable, via and trace

The primary effect of via capacitance is that it slows down, or degrades, the rising edge of digital signals.

If we must make many pad capacitance predictions, it is recommended to use electromagnetic field modeling software, since these packages can (with enough computer resources) accurately model the inductance and capacitance of three-dimensional structures. [2]

In the development of this project, the PCB simulation that was used was HFSS.

As we can see in the equation 2.1, also the inductance is a key element that influence the calculation of the impedance, however, in this project was considered to be in control, because of the use of 7 ground vias that surrounds the via signal, following the recommendation of the Samtec connector designer. In this way, the influence of the inductance is kept in control. Those ground vias can be observed in the figure 2.2.

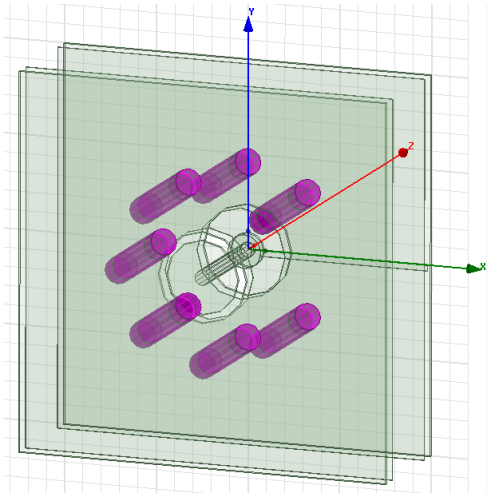


Figure 2.2 Ground vias surrounding the via signal

3 Project Development

3.1 Design Specifications

The PCB board with the following stack up has to be used, it was part of the requirement, to be able to design a board to transmit the high speed signals. This stack up was provided by the PCB manufacturer vendor. The PCB material is low loss (Megtron6).

			Customer Stack-up	OPCM Stack-up Information							
Layer		Cu Weight	Thickness (mils)	Proposed Thickness (mils)	Structure	Via	Assume copper density	Ref	Diffential 100ohm +/- 10%		Diffential 100ohm +/- 10%	
									Target LW/SP	Finished LW/SP	Target LW/SP	Finished LW/SP
	Soldermask		0.50	0.50								
L1	Top	1/3oz+Plating	1.80	1.80			75%					
	Prepreg		3.60	3.60	1078RC72			L1 & L3		3.4/4.6		3.8/8.2
L2	Signal	Hoz	0.60	0.60			25%					
	Core		4	4	4mil core							
L3	GND	Hoz	0.60	0.60			75%					
	Prepreg		8.90	10.00	2116RC56 * 2							
	Core		26	26	26mil dummy core							
	Prepreg		8.90	10.00	2116RC56 * 2							
L4	GND	Hoz	0.60	0.60			75%					
	Core		4	4	4mil core							
L5	Signal	Hoz	0.60	0.60			25%	L4 & L6		3.4/4.6		3.8/8.2
	Prepreg		3.60	3.60	1078RC72							
L6	Bottom	1/3oz+Plating	1.80	1.80			75%					
	Soldermask		0.50	0.50								
Finished Thickness (mils)				68.20								

Figure 3.1 Stack up defined by the PCB Manufacturer

Using the stack up described in the figure 3.1 as a reference, the PCB model was created at the HFSS tool.

Another requirement was to use the SAMTEC connector model provided by the SAMTEC Company. The connector model contains all the characteristics needed to properly simulate the connector. The PCB model created was connected to the SAMTEC connector model, forming the complete model used in the HFSS simulations. The PCB and the Samtec connector can be seen in the Figure 3.2 and 3.3 respectively.

The requirement of the path impedance, is that it must be 50 ohms ± 5%.

Figure 3.2 PCB and Samtec connector

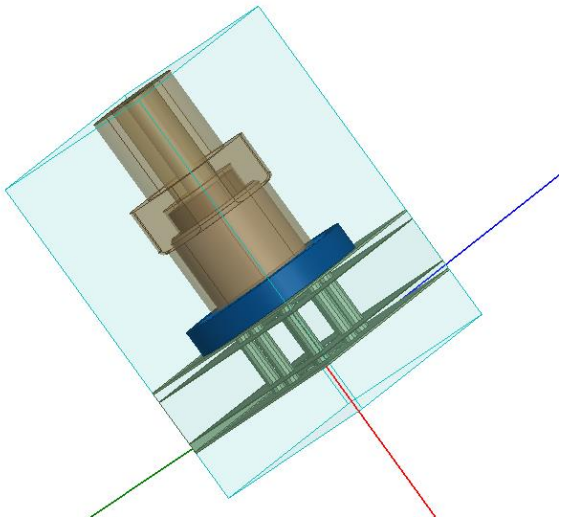


Figure 3.3 PCB and Samtec connector assembled

3.2 HFSS models

As we can see in the stack up described in the figure 3.1, there are two types of vias: A through hole via going from layer 1 thru 6, and micro vias going from layers 1 thru 2, and 5 thru 6. Therefore two models were created. In one model we simulated the through hole via, and in the second model we simulated the micro vias.

3.2.1 HFSS model with the through hole via

The following pictures represents how the through hole via model was created. At the left hand picture, the pads, connector, via and trace are highlighted. Then, at the right hand picture, can be observed the PCB with the 7 via grounds, with the 4 ground layers.

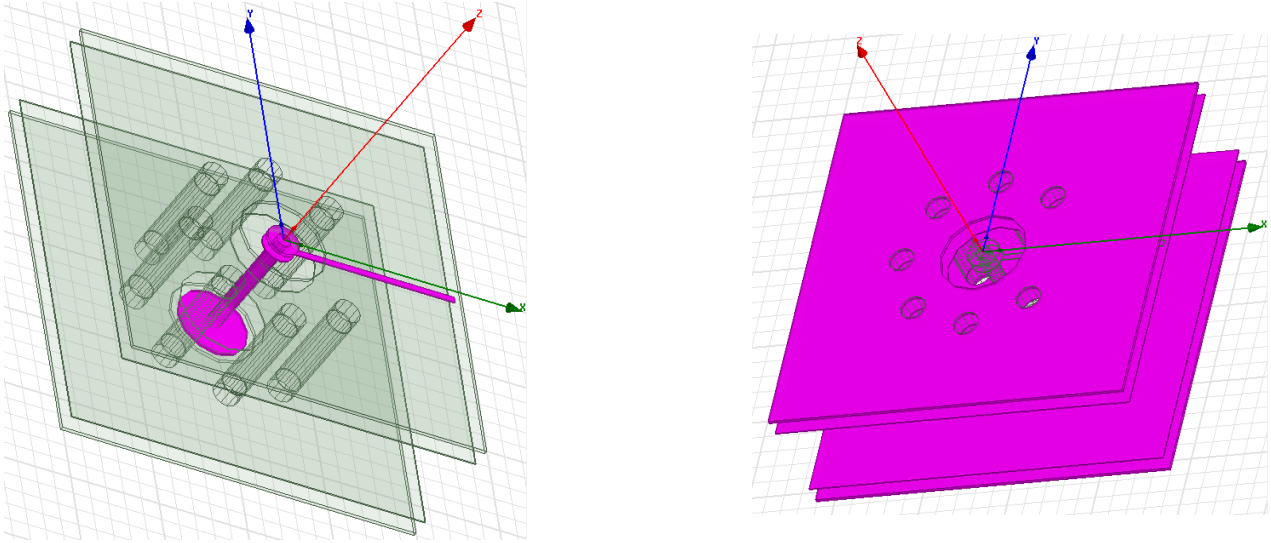


Figure 3.4 HFSS model for the through hole via

3.2.2 HFSS model with the micro via

The following pictures represents how the micro via model was created. At the left hand picture, the pads, connector, via and trace are highlighted. Then, at the right hand picture, can be observed the PCB with the 7 via grounds, with the 4 ground layers.

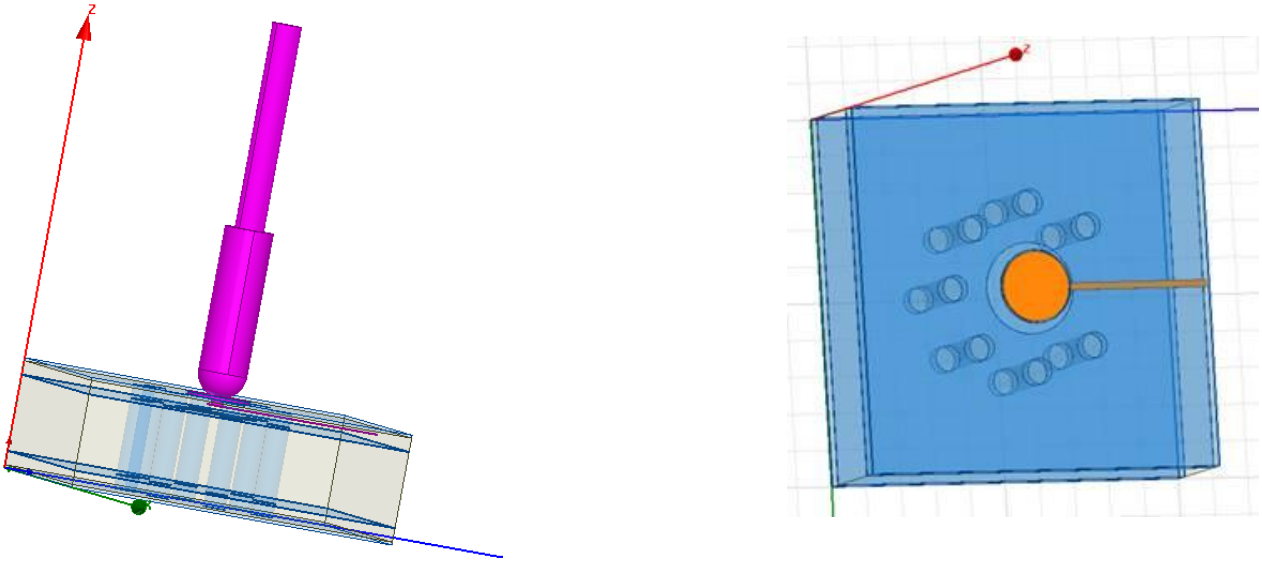


Figure 3.5 HFSS model for the micro via

3.3 Simulation results

Once the models were created, several simulations were performed to find the right values of the anti- pads. The tool was setup and the report was defined to obtain a Terminal TDR impedance. Those are the reports that will be presented in the graphs. The setup for the simulation is described below.

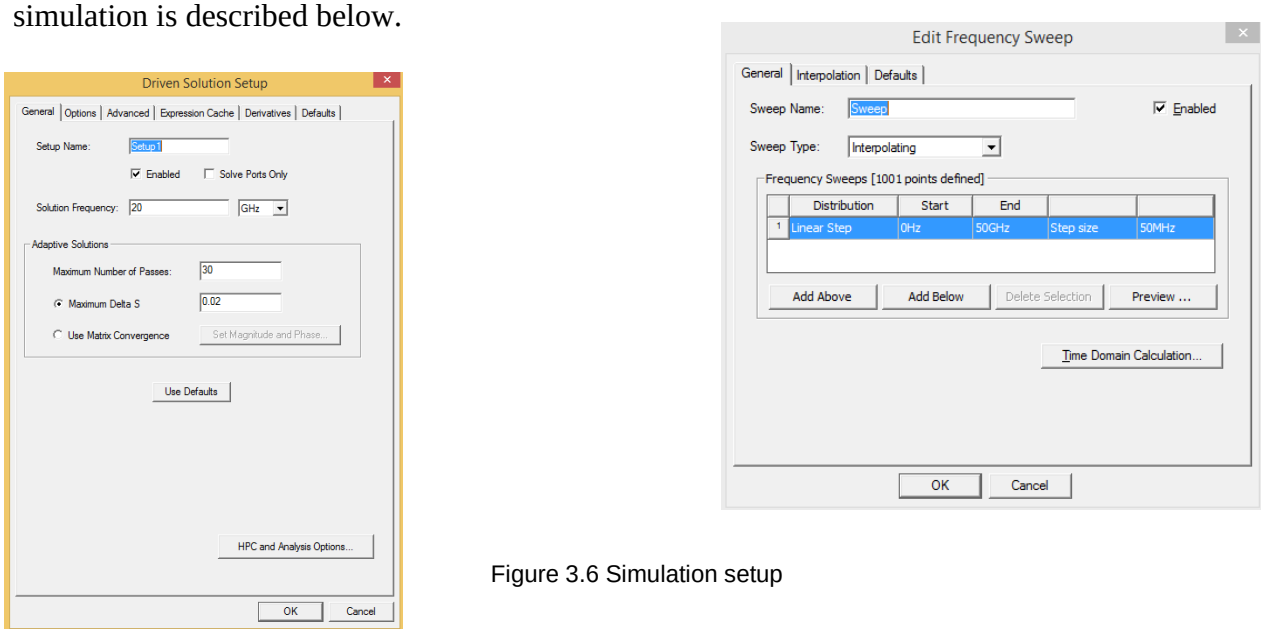


Figure 3.6 Simulation setup

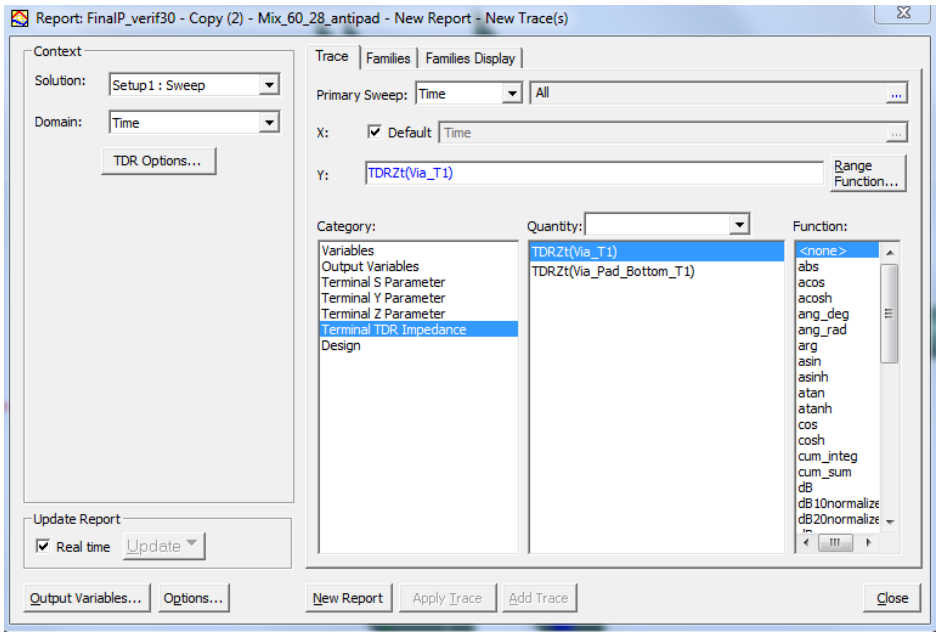


Figure 3.7 HFSS report setup

Now, since the size of the pad of the connector is different than the size of the pad of via, there are two anti-pad values that need to be modified. The figure 3.7 describe the 2 different anti-pads that were used. There is an anti-pad 1 that is used in ground layer 1 and an anti-pad2 that is used in ground layers 3,4 and 6.

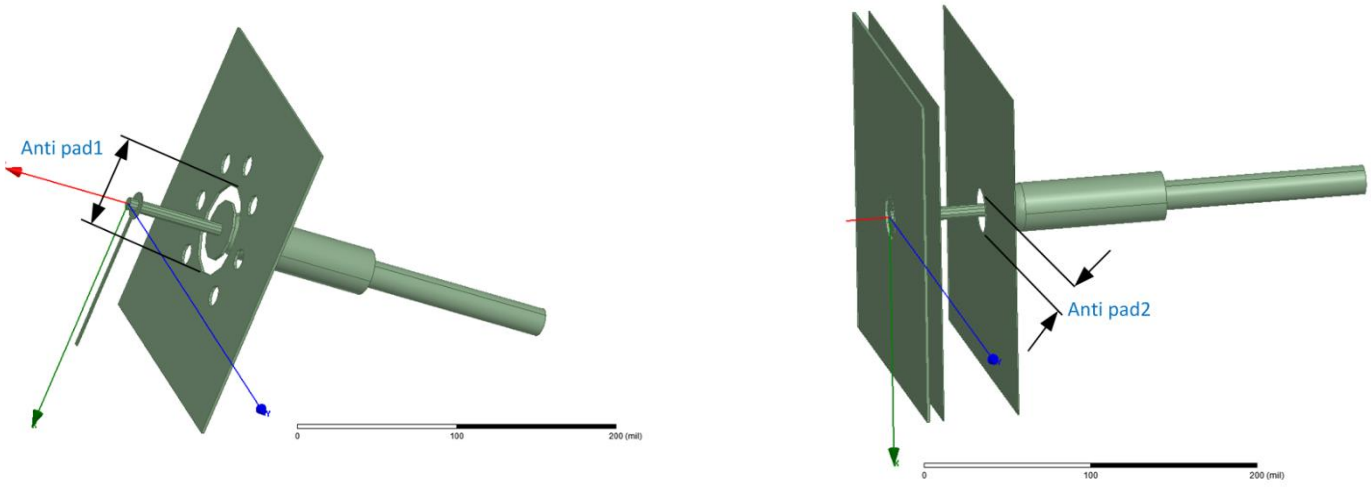


Figure 3.8 Anti-pad1 and Anti-pad2 definition

3.3.1 Through hole via results

The simulation results were divided in two parts. In the first part, the simulations were performed using the value of the anti-pad1 = antipad2, trying to find a common solution for both anti-pads to facilitate the PCB design work. The values of the anti-pad that were used, started at 40 mils and finished at 56 mils. However, the values of the impedance did not comply with the requirement of 50 ohms ± 5%. Those results can be observed in the Figure 3.8 below. The best value was obtained with an anti-pad diameter of 46.5 mils, but in some cases, the impedance was above 60 ohms. These results can be observed in the figure 3.8.

In the second part of the experiment, several values of anti-pad1 and anti-pad2 were tested, and the best value was obtained with anti-pad1 diameter = 60 mils and anti-pad2 diameter = 28 mils. In this case, the maximum impedance obtained was 53.56 ohms and the minimum was 44.06 ohms. Even though, is still out of specification, its values are really close to the expected values, and therefore it is acceptable. The results can be observed in the figure 3.9.

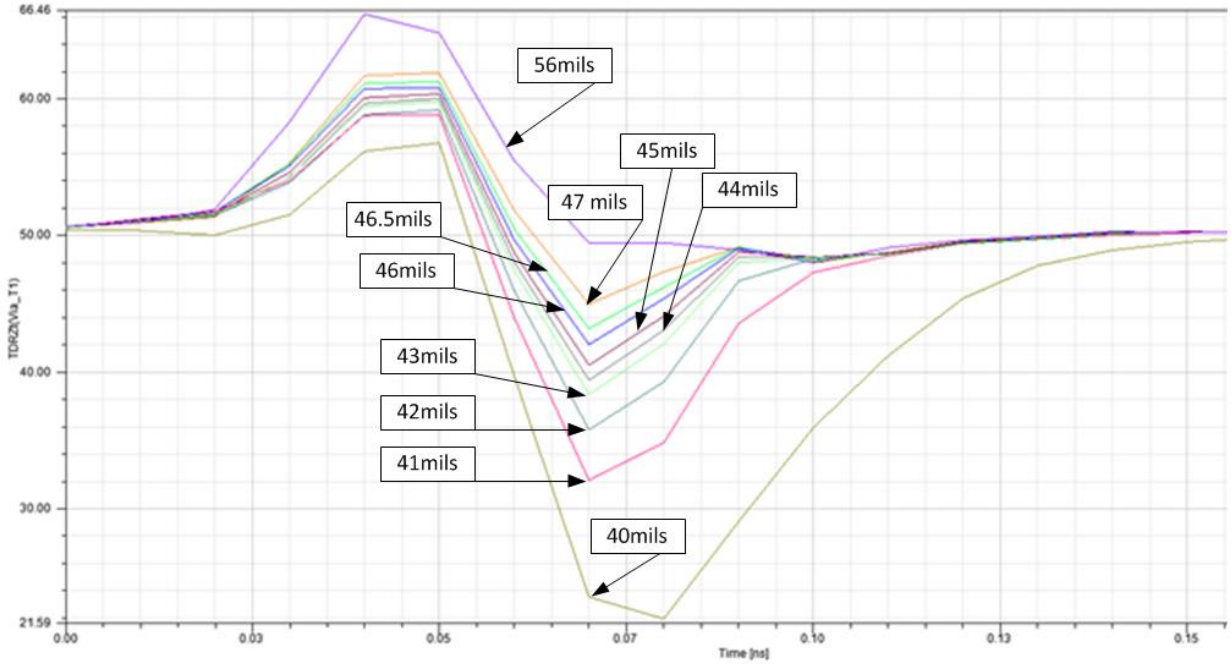


Figure 3.9. Through hole via results with Anti-pad1 diameter = Anti-pad2 diameter

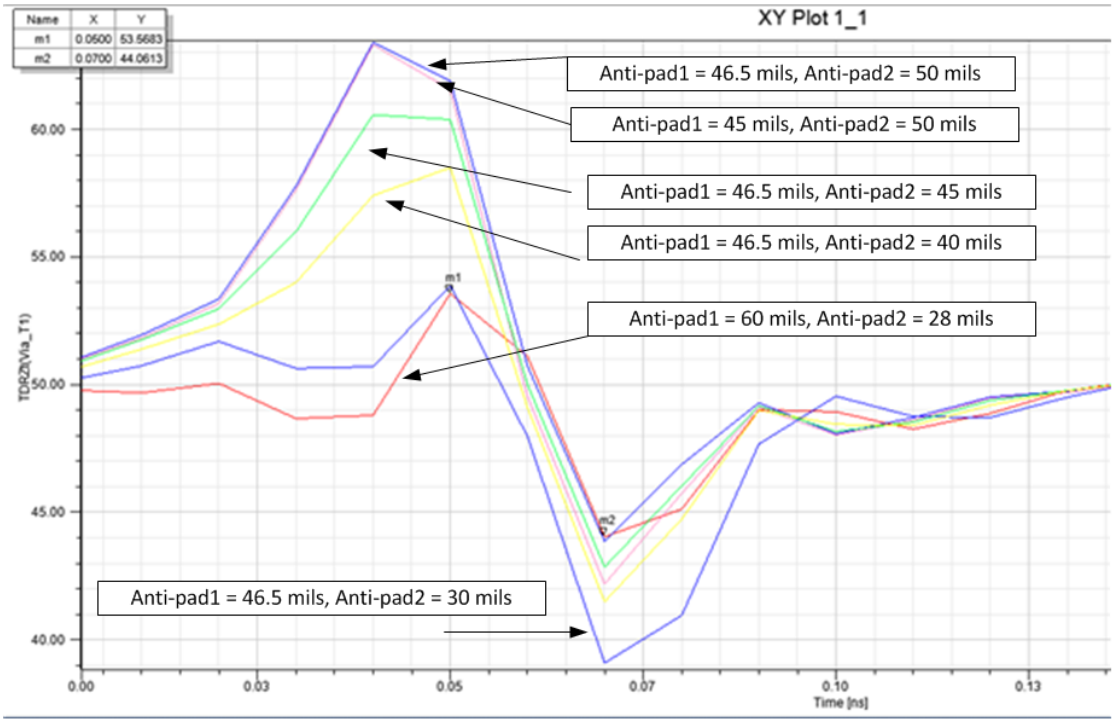


Figure 3.10. Through hole via results with Anti-pad1diameter different than Anti-pad2 diameter

3.3.2 Micro via results

In the case of the micro-via, better results were obtained. The best result was obtained with anti-pad1 diameter = 45 mils and anti-pad2 diameter = 50 mils. The results can be observed in the figure 3.10.

The maximum impedance value obtained was 51.26 ohms and the minimum impedance value obtained was 46.98 ohms. Both values comply with the specification of 50 ohms ± 5%. Those can be observed in the figure 3.11.

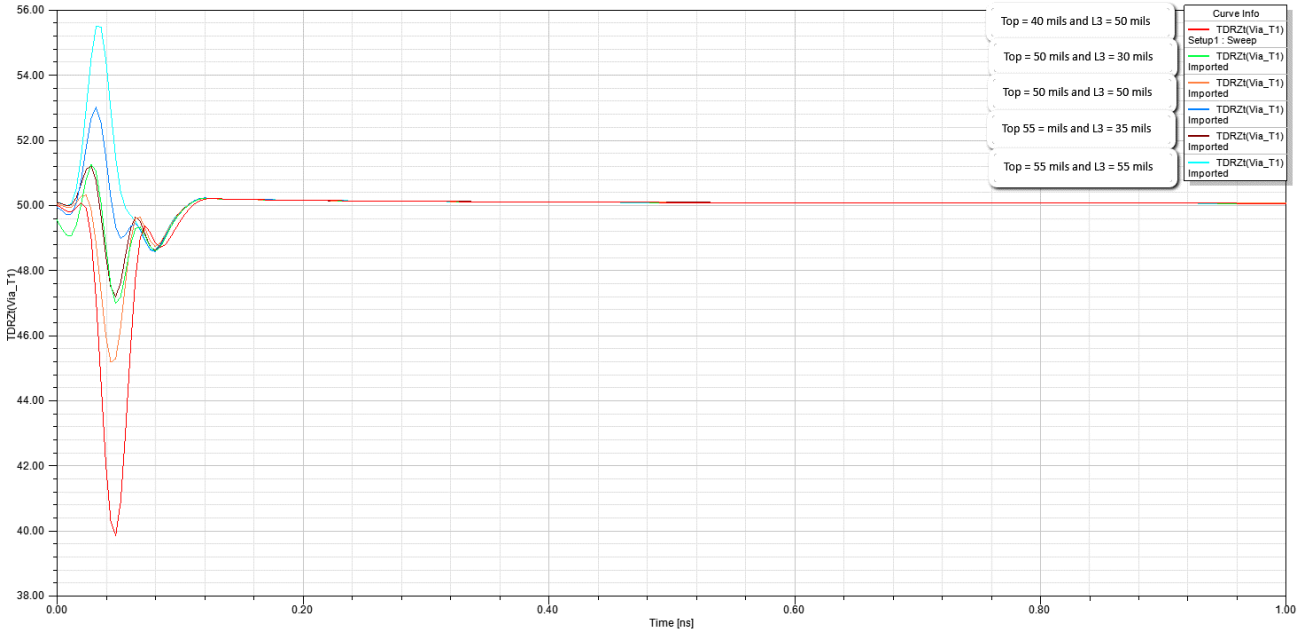


Figure 3.11 micro via results

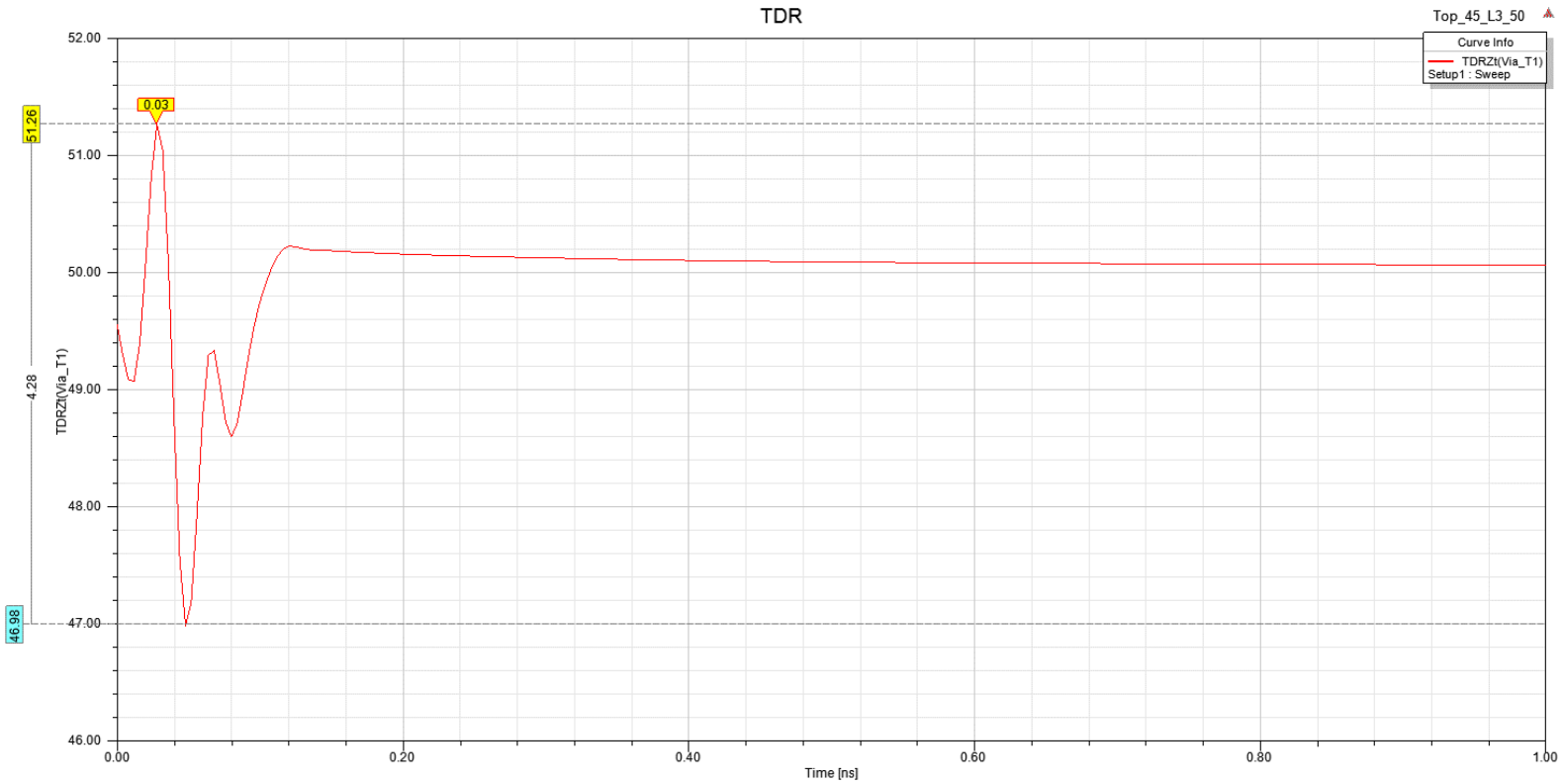


Figure 3.12 Micro via best result value.

4 Conclusions

It was very interesting to work in a tool where we were able to implement our own PCB model and then integrate it with a model provided by a connector manufacturer. In this way, the simulations performed for our designs, will be closer to the reality, and we take advantage of the work performed by the connector manufacturer.

Several simulation were performed for the through hole via model, but we were not able to comply 100% with the specification, although it was very close. However, looks like this is not unusual. At the end, the idea is to be as close as possible to the ideal state, even though sometimes cannot be implemented in this way. However, it is a very good approximation.

Even though this tool was not reviewed in class, the basics and the elements for the Sonnet tool, helped a lot to understand easily this tool. The main ideas were clear, the rest is was just a matter of playing with the tool.

It was very nice to work in a project that Signal Integrity Engineers normally does. In this way, we got a better understanding of the work that they develop.

5 Bibliography

[1] Mark I. Montrose, “EMC and Printer Circuit Board”, Wiley, 1999, pp 34.

[2] Howard Johnson, Martin Graham, “High-Speed Digital Design”, Prentice Hall, 1993, pp 257.

3. ANTI PAD CALCULATION FOR A HIGH SPEED PCB USING OPTIMIZATION METHODS

1. Introduction

In the design of PCBs that contains high speed signals, is very common to perform signal integrity simulations in certain areas of the design (the most critical ones), using tools like HFSS (High Frequency Structural Simulation) from ANSYS. In the case of this project, there was a need to design a board to perform electrical validation of one of the chips designed by Intel. The board include in its design a Samtec connector bulls eye type, like the one depicted in the figure 1.1

Figure 3.1 Samtec connector (bulls eye type).

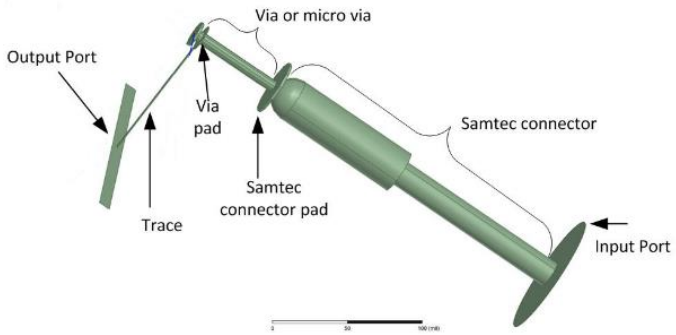


Figure 4.2 Path simulated: Samtec – Via - Trace

The Samtec connector goes to the CPU via single ended lines with a controlled impedance of 50 ohms, and this was the part of the design that was simulated, which corresponds to the path: Samtec connector - connector pad – via - via pad - trace, which is described in the figure 1.2.

It is very important for the design, to maintain as much as possible the 50 ohms impedance in the path. One key element that is affecting the impedance is the parasitic capacitance of via, hence the importance to perform the simulations, to find the right value of the anti-pad diameter in the ground planes, to maintain that parasitic capacitance very low. The anti-pad is described in the figure 1.3.

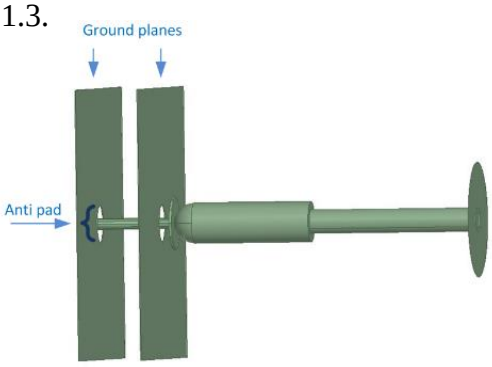


Figure 5.3 Anti-pads in the ground planes

In the previous project [1], this simulation was already performed without using any optimization method. The simulation was done by changing manually the anti-pads values of the vias in the HFSS tool, but in this case, the objective was to use the same HFSS model, but now using an optimization method to calculate the anti-pad values, instead of changing them manually.

The present report contains the following elements:

- Theory to describe why is important to reduce the parasitic capacitance of the via and why the importance of optimization methods
- Design specifications for the project
- HFSS model description
- Elements of the optimization model
- Simulation results of the models created in HFSS using Matlab: Through hole via
- And finally, the conclusions.

2. Theory

2.1 Parasitic elements in a PCB

In the design of PCB boards that include higher speed frequencies, it is very important to take into account the parasitic elements that are intrinsic in the physical design. In this project, the parasitic capacitance of via is affecting the impedance of the complete signal path.

For the impedance equation, various forms exist depending on whether we are examining plane wave impedance, circuit impedance, and the like. For wire, or a PCB trace, the following equation is used:

$$Z = R + jX_L + \frac{1}{jX_C} = R + jwL + \frac{1}{jwC} \qquad (2.1)$$

where $X_L = 2\pi fL$ (the component in the equation that relates only to wires or PCB traces) [2]

$$X_C = \frac{1}{2\pi fC} \qquad (2.2)$$

$$w = 2\pi f_C \qquad (2.3)$$

A better model for a PCB trace is the use of a transmission line, but for simplicity, the equation 2.1 was considered, even though is valid only in a very limited range of operation conditions.

As we can see in the equation 2.1, the capacitance is a key factor in the calculation of the impedance, that in the case of this project, the capacitance of the via was key for the calculation of the impedance for the complete path, which is formed by the SAMTEC connector, the via and the PCB trace, as described in the figure 2.1.

Every via has parasitic capacitance to ground. Vias being physically small structures, they behave very much like lumped circuit elements. We can predict, within an order of magnitude, the amount of parasitic capacitance for via: [3]

$$C = \frac{1.41\varepsilon r\, TD_1}{D_2 - D_1} \qquad (2.4)$$

Where D2 = diameter of clearance hole in ground plane(s), in.

D1 = diameter of pad surrounding via, in.

T = thickness of printed circuit board, in.
εr = relative electric permeability of circuit board material
C = parasitic via capacitance, pF

When the pad size approaches the clearance hole diameter, pads pick up a lot more capacitance. If your ground clearance holes must remain small to maintain ground continuity, shrink or eliminate the pads on ground layers. For trace routing vias, it doesn't matter if you get some breakout on the plane layers. [3]

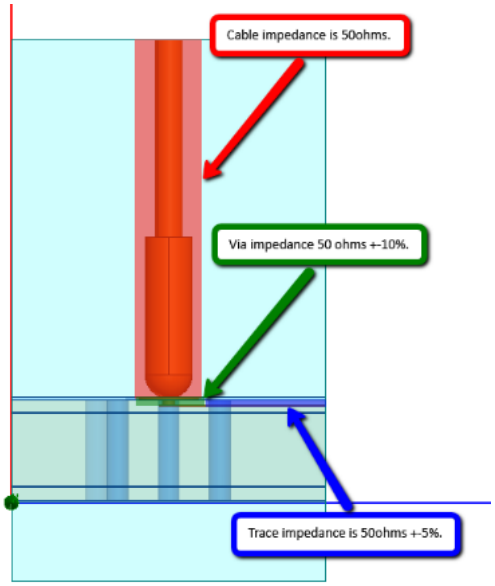


Figure 6.1 Impedance of the cable, via and trace. signal

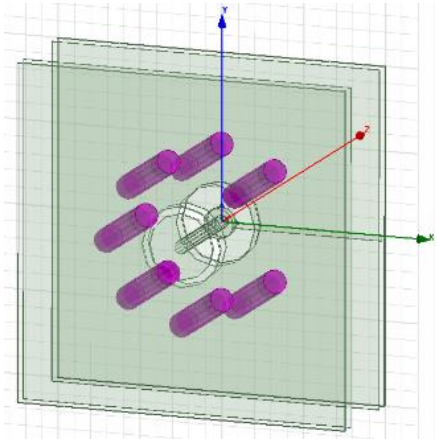


Figure 7.2 Ground vias surrounding the via

The primary effect of via capacitance is that it slows down, or degrades, the rising edge of digital signals.

If many pad capacitance predictions are needed, it is recommended to use electromagnetic field modeling software, since these packages can (with enough computer resources) accurately model the inductance and capacitance of three-dimensional structures. [3]

In the development of this project, the PCB simulation that was used was HFSS.

As we can see in the equation 2.1, also the inductance is a key element that influence the calculation of the impedance, however, in this project was considered to be in control, because of the use of 7 ground vias that surrounds the via signal, following the recommendation of the Samtec connector designer. In this way, the influence of the inductance is kept in control. Those ground vias can be observed in the figure 2.2.

2.2 Optimization methods

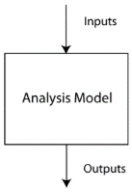
Automated design optimization technology is rapidly being adopted by engineers in nearly all major industries. The potential for delivering better designs in less time compared to manual optimization approaches makes automated design optimization very attractive from both a technical and a business point of view. However, one of the main barriers to widespread usage

of design optimization in industry is the difficulty of choosing an appropriate optimization search algorithm for a given problem. [5]

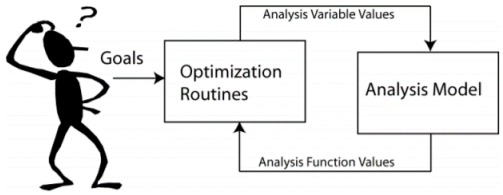
It is well known that all search methods have at least some limitations. For example, some methods work effectively only when it is possible to accurately compute gradients of the solution with respect to the variables. Some methods work only for continuous or discrete variables (but not both), or for a relatively small number of variables. And some methods require a relatively large number of design evaluations to be performed in order to find an optimal solution. There is no single method or algorithm that works best on all or even a broad class of problems. In order to choose the best method for a given problem, one must first understand the type of design space that is being searched. The design space for a given problem is defined by the types of responses and by the number, types and ranges of the design variables. [5]

For the development of this project the Nelder-Mead optimization method was used.

A model requires some inputs in order to make calculations. Analysis models require inputs—analysis variables— and compute outputs—analysis functions. [4]



The designer specifies a set of inputs, evaluates the model, and examines the outputs. Suppose, in some respect, the outputs are not satisfactory. Using intuition and experience, the designer proposes a new set of inputs which he or she feels will result in a better set of outputs. The model is evaluated again. This process may be repeated many times. The computer is now used to both evaluate the model and search for a better design. [4]



For this project, the anti-pad values were considered as the inputs to the optimization model and the final outputs were the anti-pad values optimized to have the impedance between certain values.

3 Project Development

3.1 Design Specifications

The PCB board with the following stack up has to be used, it was part of the requirement, to be able to design a board to transmit the high speed signals. This stack up was provided by the PCB manufacturer vendor. The PCB material is low loss (Megtron6).

			Customer Stack-up	OPCM Stack-up Information					Diffential 100ohm +/- 10%		Diffential 100ohm +/- 10%	
Layer		Cu Weight	Thickness (mils)	Proposed Thickness (mils)	Structure	Via	Assume copper density	Ref	Target LW/SP	Finished LW/SP	Target LW/SP	Finished LW/SP
	Soldermask		0.50	0.50								
L1	Top	1/3oz+Plating	1.80	1.80			75%					
	Prepreg		3.60	3.60	1078RC72			L1 & L3		3.4/4.6		3.8/8.2
L2	Signal	Hoz	0.60	0.60			25%					
	Core		4	4	4mil core							
L3	GND	Hoz	0.60	0.60			75%					
	Prepreg		8.90	10.00	2116RC56 * 2							
	Core		26	26	26mil dummy core							
	Prepreg		8.90	10.00	2116RC56 * 2							
L4	GND	Hoz	0.60	0.60			75%					
	Core		4	4	4mil core							
L5	Signal	Hoz	0.60	0.60			25%	L4 & L6		3.4/4.6		3.8/8.2
	Prepreg		3.60	3.60	1078RC72							
L6	Bottom	1/3oz+Plating	1.80	1.80			75%					
	Soldermask		0.50	0.50								
Finished Thickness (mils)				68.20								

Figure 3.1 Stack up defined by the PCB Manufacturer

Using the stack up described in the figure 3.1 as a reference, the PCB model was created at the HFSS tool. Another requirement was to use the SAMTEC connector model provided by the SAMTEC Company. The connector model contains all the characteristics needed to properly simulate the connector. The PCB model created was connected to the SAMTEC connector model, forming the complete model used in the HFSS simulations. The PCB and the Samtec connector can be seen in the Figure 3.2.

The requirement of the path impedance, is that it must be 50 ohms ± 15%.

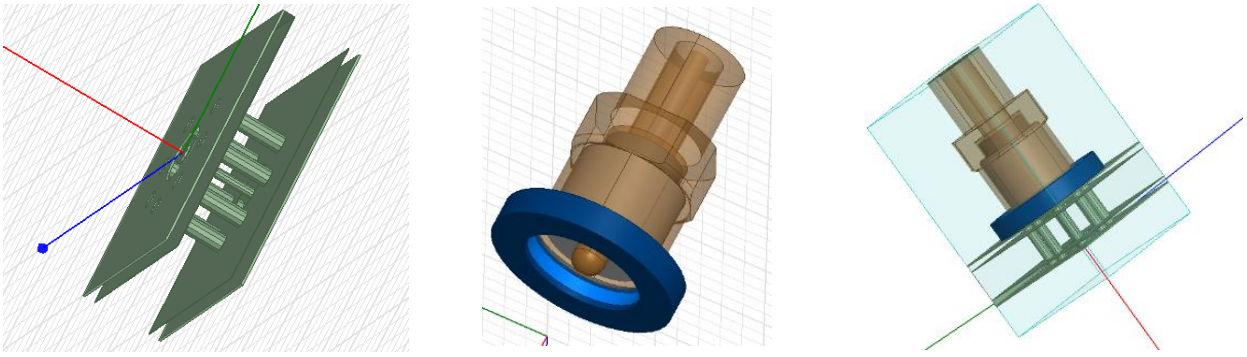


Figure 3.2 PCB, Samtec connector and PCB assembled with Samtec connector

3.2 HFSS model with through hole via

As we can see in the stack up described in the figure 3.1, there are two types of vias: A through hole via going from layer 1 thru 6, and micro vias going from layers 1 thru 2, and 5 thru 6. Therefore two models were created, however, for the development of this project, only the through hole via was used.

The following pictures represents how the through hole via model was created. At the left hand picture, the pads, connector, via and trace are highlighted. Then, at the right hand picture, can be observed the PCB with the 7 via grounds, with the 4 ground layers.

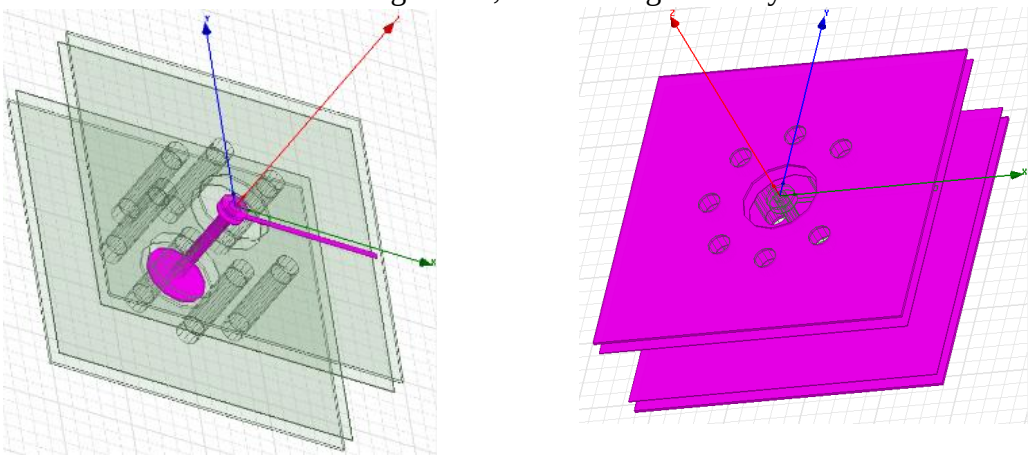


Figure 3.3 HFSS model for the through hole via.

3.3 Optimization model

3.3.1 MATLAB driver

Once the HFSS model was created, it was used as a base to create the Matlab driver. The key function that was used to develop the driver, was the recording of a script at the HFSS tool. This script would contain all the operations that need to be performed at the HFSS model to perform the simulations with different anti-pad values, and those were saved at a script file.

To create the driver, at the tools menu of the HFSS tool, a "record script to file" was initiated, and then the following activities were performed:

- The HFSS model was opened
- The active design was defined
- The 3-D modeler was opened and the anti-pad values were modified
- The project was saved
- The simulation was started (AnalizeAll)
- A report was created and the results were sent to a .csv file
- The project was closed

All previous activities were recorded at a .vbs file (visual basic script). Every time this script is performed again, all the activities would be performed. The .vbs file can be seen at the Appendix 6.1.

This was the script that was used to create the Matlab driver. The only change that was performed, was to replace the values of the anti-pads by variables that could be modified. The Matlab driver can be seen at the Appendix 6.2 (antipad_HFSS_driver.m file).

3.3.2 Fixed parameters, optimization variables and starting points

Since this simulation was already performed in HFSS but without any optimization method [1], at that moment, the anti-pad sizes were changed manually by the user, and those were the only elements modified, therefore, that was the initial approach taken. The optimization variables for this design are anti-pad 1 (the top side of the board) and the anti-pad 2 (internal and bottom layers). The optimization algorithm starting point was defined based on the simulations performed for the first project, and the seed selected was: Anti-pad 1 = 46mils; Anti-pad2 = 52 mils. The figure 3.4 describe the 2 different anti-pads that were used, the Anti-pad 1 was used in ground layer 1 and the Anti-pad2 was used in ground layers 3, 4 and 6.

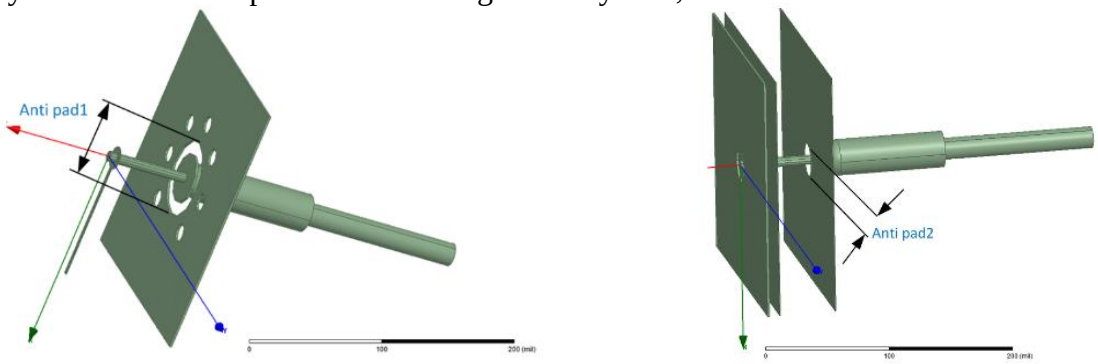


Figure 3.4 Anti-pad1 and Anti-pad2 definition

The rest of the elements of the design were considered fixed parameters. Those parameters are stack-up, frequency design (the high speed simulating in this project works at 20GHz), shielding vias (ground) around the singled ended trace, via size, trace width, impedance trace of 50 ohms and the SAMTEC connector model provided by SAMTEC company.

3.3.3 Design specifications for the optimization model

The design specifications for the model are the next ones:

$|Z_{max}| < 50\ \Omega$ + tolerance for all frequencies

$|Z_{min}| > 50\ \Omega$ - tolerance for all frequencies

The tolerances used on the analysis were 5%, 10%, 15% and 20%. Different values were evaluated, to find the best solution.

3.3.4 Formulation of the Optimization Problem

The optimization problem can be formulated in the following way:

$x^* = \arg\min_x \max \{\ldots.ek(x)\ldots.\}$

subject to

38 mils > x(1) > 20 mils

38 mils > x(2) > 10 mils

where the k-th error function is given by:

$$ek(x) = \begin{cases} 1 - \frac{Z\_min(x)}{Z\_lb+eps} & \text{for } Z\_min < Z\_lb \\ \frac{Zmax(x)}{Z\_ub+eps} - 1 & \text{for } Z\_max > Z\_ub \end{cases}$$

where Z_ub = 50Ω + tolerance, Z_lb = 50Ω – tolerance. Tolerance values were 5%, 10%, 15% and 20% and eps = 1e-3. The x values are restricted due to the physical constraints of the design.

The implementation of the objective function, can be analyzed at the Appendix 6.3 (antipad_HFSS_OF.m file). The implementation of the main optimization function, can be analyzed at the Appendix 6.4 (antipad_HFSS_opt.m file). In this case, the Nelder Mead optimization method (fminsearch) was used.

For the plotting of the results the following Matlab programs were created: antipad_HFSS_plot.m and marks_for_specs_antipad.m, which can be analyzed at the Appendix 6.5

3.4 Simulation results using Matlab

Once the optimization was run, several iterations were performed to find the right values of the anti- pads. The results are the following:

Tolerance: 15% (57.5 ohms - 42.5 ohms)					
antipad 1 (mils)	antipad 2 (mils)	Zmax (ohms)	Zmin (ohms)	Maxerror	Duration (min)
46	52	64.36	43.64	0.1193	21.46
48.3	52	64.12	45.51	0.1151	17.57
46	54.6	67.75	43.85	0.1435	17.33
48.3	49.4	63.11	45.24	0.0976	20.71
49.45	46.8	61.47	45.13	0.069	18.22
51.75	46.8	61.42	46.14	0.0683	18.32
54.62	44.2	60.5	46.011	0.05	17.94
55.77	39	58.54	44.42	0.0181	19.45
59.51	32.5	55.51	42.65	0	

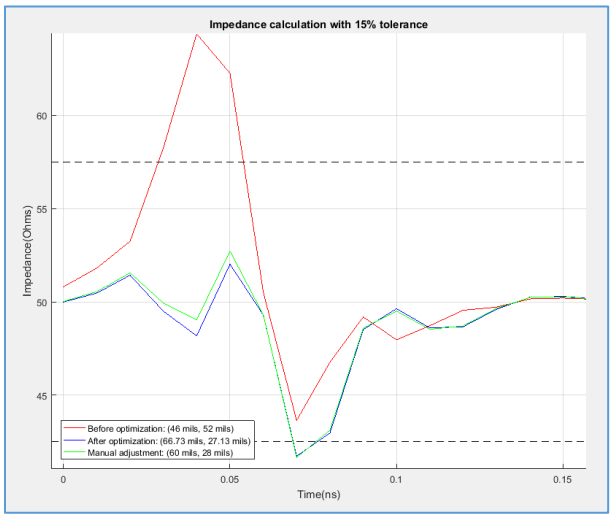


Figure 3.5 Simulation results using the optimization method

From the results, the maximum impedance of 55.51Ω was obtained with an anti-pad1 diameter of 59.51 mils and the minimum impedance of 42.65Ω was obtained with the anti-pad2 diameter of 32.5 mils. Those results were obtained with a tolerance of 15%. As it can be seen in the graphs, the results are very close to the ones obtained with manual adjustment in the previous project [1].

4 Conclusions

One of the key elements of the project was the development of the Matlab driver for the HFSS tool. Even though at the beginning the plan was to use an existing driver, after several experimentation with no good results, it was decided to develop a new driver. All the homework experience and class notes, were key for the development of the driver for a tool with few experience of its use. The driver worked very well.

Another important thing was the definition of the objective function. A bad definition led us to wrong results, but by observing the error behavior it was easy to fix the issue. Therefore it was demonstrated how important is to have a deep understanding of the optimization model to be able to quickly find the solution to the problems.

In order to implement these size of anti-pad in a PCB is going to be necessary to round the anti-pad because the anti-pad sizing can not be set to decimal numbers due to tolerance fabrication process will dismiss it.

It was very exciting to apply optimization methods in a real work project. It will be the base to be used in the future in the design center, to take advantage of the acknowledgement acquired.

5 Bibliography

[1] Galindo-De La Torre, “Anti pad calculation for a High Speed PCB”, Método de Simulación de Circuitos Electrónicos, 2016, ITESO.

[2] Mark I. Montrose, “EMC and Printer Circuit Board”, Wiley, 1999, pp 34.

[3] Howard Johnson, Martin Graham, “High-Speed Digital Design”, Prentice Hall, 1993, pp 257.

[4] Alan R. Parkinson, “Optimization Methods for Engineering Design”, Brigham Young University 2013 pp 3, 6 and 7.

[5] Red Cedar Technology, “How to Select the right optimization method for your problem”, WP-1022 Rev.05.08, East Lansing, MI, USA, pp 1.

6 Appendix

6.1 .vbs file generated by HFSS

```
' ----------------------------------------------
' Script Recorded by ANSYS Electronics Desktop Version 2016.0.0
' 22:58:31  May 04, 2017
' ----------------------------------------------
Dim oAnsoftApp
Dim oDesktop
Dim oProject
Dim oDesign
Dim oEditor
Dim oModule
Set oAnsoftApp = CreateObject("Ansoft.ElectronicsDesktop")
Set oDesktop = oAnsoftApp.GetAppDesktop()
oDesktop.RestoreWindow
oDesktop.OpenProject "C:/JDLTA/HFSS/antipad_hfss.aedt"
Set oProject = oDesktop.SetActiveProject("antipad_hfss")
Set oDesign = oProject.SetActiveDesign("Mix_45_50_antipad")
Set oEditor = oDesign.SetActiveEditor("3D Modeler")
oEditor.ChangeProperty Array("NAME:AllTabs", Array("NAME:Geometry3DCmdTab", Array("NAME:PropServers",  _
  "AntiPad:CreateRegularPolyhedron:1"), Array("NAME:ChangedProps", Array("NAME:Start Position", "X:=",  _
  "23mil", "Y:=", "0mil", "Z:=", "0mil"))))
oEditor.ChangeProperty Array("NAME:AllTabs", Array("NAME:Geometry3DCmdTab", Array("NAME:PropServers",  _
  "antipad2:CreateRegularPolyhedron:1"), Array("NAME:ChangedProps", Array("NAME:Start Position", "X:=",  _
  "26mil", "Y:=", "0mil", "Z:=", "0mil"))))
oProject.Save
oDesign.AnalyzeAll
Set oModule = oDesign.GetModule("ReportSetup")
oModule.CreateReport "XY Plot 1", "Terminal Solution Data", "Rectangular Plot",  _
  "Setup1 : Sweep", Array("Domain:=", "Time", "HoldTime:=", 1, "RiseTime:=",  _
  2E-011, "StepTime:=", 0, "Step:=", true, "WindowWidth:=", 1, "WindowType:=", 4, "KaiserParameter:=",  _
  1, "MaximumTime:=", 0), Array("Time:=", Array("All"), "MS_w:=", Array("Nominal"), "H:=", Array( _
  "Nominal"), "ap2:=", Array("Nominal"), "ap21:=", Array("Nominal")), Array("X Component:=",  _
  "Time", "Y Component:=", Array("TDRZt(Via_T1)")), Array()
oModule.ExportToFile "XY Plot 1", "C:/JDLTA/HFSS/antipad_hfss_results.csv"
oProject.Save
oProject.Save
oDesktop.CloseProject "antipad_hfss"
```

6.2 antipad_HFSS_driver.m

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Driving HFSS driver from Matlab                                              %
%                                                                              %
% This function drives the antipad_hffss.aedt project from Matlab and          %
% returns the simulation results in vectors t and Z.                           %
%                                                                              %
% Usage: [t, Z] = antipad_HFSS(Xo)                                             %
%   Xo(1): antipad1 value (mils)                                               %
%   Xo(2): antipad2 value (mils)                                               %
%   t: time (ns)                                                               %
%   Z: Impedance value(ohms)                                                   %
%                                                                              %
% Functions required: None.                                                    %
%                                                                              %
% AGV/JDLTA May, 2017                                                          %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function [t, Z] = antipad_HFSS_driver(Xo)
    antipad1 = Xo(1);
    antipad2 = Xo(2);
    ss{1}  = ' Dim oAnsoftApp ';
    ss{2}  = ' Dim oDesktop   ';
    ss{3}  = ' Dim oProject   ';
    ss{4}  = ' Dim oDesign    ';
    ss{5}  = ' Dim oEditor    ';
    ss{6}  = ' Dim oModule     ';
    ss{7}  = ' Set oAnsoftApp = CreateObject("Ansoft.ElectronicsDesktop")';
    ss{8}  = ' Set oDesktop = oAnsoftApp.GetAppDesktop()';
    ss{9}  = ' oDesktop.RestoreWindow';
    ss{10} = ' oDesktop.OpenProject "C:/JDLTA/HFSS/antipad hfss.aedt"';
    ss{11} = ' Set oProject = oDesktop.SetActiveProject("antipad_hfss")';
    ss{12} = ' Set oDesign = oProject.SetActiveDesign("Mix_45_50_antipad")';
    ss{13} = ' Set oEditor = oDesign.SetActiveEditor("3D Modeler")';
    ss{14} = ' oEditor.ChangeProperty Array("NAME:AllTabs", Array("NAME:Geometry3DCmdTab", Array("NAME:PropServers",  _';
    ss{15} = '   "AntiPad:CreateRegularPolyhedron:1"), Array("NAME:ChangedProps", Array("NAME:Start Position", "X:=",  _';
    ss{16} = ['   "' mat2str(antipad1) '  mil", "Y:=", "0mil", "Z:=", "0mil"))))'];
    ss{17} = ' oEditor.ChangeProperty Array("NAME:AllTabs", Array("NAME:Geometry3DCmdTab", Array("NAME:PropServers",  _';
    ss{18} = '   "antipad2:CreateRegularPolyhedron:1"), Array("NAME:ChangedProps", Array("NAME:Start Position", "X:=",  _';
    ss{19} = ['   "' mat2str(antipad2) ' mil", "Y:=", "0mil", "Z:=", "0mil"))))'];
    ss{20} = ' oProject.Save';
    ss{21} = ' oDesign.AnalyzeAll';
    ss{22} = ' Set oModule = oDesign.GetModule("ReportSetup")';
    ss{23} = ' oModule.CreateReport "XY Plot 1", "Terminal Solution Data", "Rectangular Plot",  _';
    ss{24} = '   "Setup1 : Sweep", Array("Domain:=", "Time", "HoldTime:=", 1, "RiseTime:=",  _';
    ss{25} = '   2E-011, "StepTime:=", 0, "Step:=", true, "WindowWidth:=", 1, "WindowType:=", 4, "KaiserParameter:=",  _';
    ss{26} = '   1, "MaximumTime:=", 0), Array("Time:=", Array("All"), "MS_w:=", Array("Nominal"), "H:=", Array( _';
    ss{27} = '   "Nominal"), "ap2:=", Array("Nominal"), "ap21:=", Array("Nominal")), Array("X Component:=",  _';
    ss{28} = '   "Time", "Y Component:=", Array("TDRZt(Via_T1)")), Array()';
    ss{29} = ' oModule.ExportToFile "XY Plot 1", "C:/JDLTA/HFSS/antipad_hfss_results.csv"';
    ss{30} = ' oProject.Save';
    ss{31} = ' oDesktop.CloseProject "antipad_hfss"';

```

```
    % Save HFSS Script as a .vbs file in matlab working directory
    CircuitFileName = 'antipad_hfss_m.vbs';
    ckt_file = str2mat(ss);
    [rows,columns] = size(ckt_file);
    fid = fopen(CircuitFileName,'w+');          % File identifier opened.
    for i = 1:rows
    fprintf(fid, '%s', ckt_file(i,:));          % Save each row of ckt_file.
    fprintf(fid, '%s\r\n', '');
    end
    fclose(fid); % File identifier closed.

    % Run HFSS tool
    system(CircuitFileName);

    % Reading HFSS Output File
    RespZ = csvread('C:\JDLTA\HFSS\antipad_hfss_results.csv',1,0);
    t = RespZ(:,1);                 % Time value
    Z = RespZ(:,2);                 % Impedance value
    % Erase Data Files
    delete C:\JDLTA\HFSS\antipad_hfss_results.csv;
end
```

6.3 antipad_HFSS_OF.m

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Objective function of the hfss antipad program                                  %
%                                                                                 %
% AGV/JDLTA April, 2017                                                           %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
function MaxError = antipad_HFSS_OF(Xo)
    %%% Initialization
    ti = clock;
%   Z_ub = 60;              % Maximum impedance tolerance (50 ohms + 20%)
%   Z_lb = 40;              % Minimum impedance tolerance (50 ohms - 20%)
%   Z_ub = 57.5;            % Maximum impedance tolerance (50 ohms + 15%)
%   Z_lb = 42.5;            % Minimum impedance tolerance (50 ohms - 15%)
    Z_ub = 55;              % Maximum impedance tolerance (50 ohms + 10%)
    Z_lb = 45;              % Minimum impedance tolerance (50 ohms - 10%)
%   Z_ub = 52.5;            % Maximum impedance tolerance (50 ohms + 5%)
%   Z_lb = 47.5;            % Minimum impedance tolerance (50 ohms - 5%)
    eps = 1e-03;
    max_radio_apd   = 38;   % Maximum radio for antipad 1 & 2 allowed
    min_radio_apd_1 = 20;   % Minimum radio for antipad 1 allowed
    min_radio_apd_2 = 10;   % Minimum radio for antipad 2 allowed

    %%% Antipad1 evaluations to know if it has valid values
    if (Xo(1) < max_radio_apd) && (Xo(1) > min_radio_apd_1)
        antipad1_valid = 1;         % antipad1 value is valid
    else
        antipad1_valid = 0;         % antipad1 value is not valid
    end

    %%% Antipad2 evaluations to know if it has valid values
    if (Xo(2) < max_radio_apd) && (Xo(2) > min_radio_apd_2)
        antipad2_valid = 1;         % antipad2 value is valid
    else
        antipad2_valid = 0;         % antipad2 value is not valid
    end

    %%% MaxError calculation
    if (antipad1_valid && antipad2_valid) == 1
        % Antipad values are valid
        % Obtaining response from the HFSS tool
        [t,Z] = antipad_HFSS_driver(Xo);
        Z_max = max(Z);                 % Zmax value
        Z_min = min(Z);                 % Zmin value
        % MaxError calculation
        if (Z_max > Z_ub)
            % The bigger error is at Zmax value
            MaxError = ( Z_max/(Z_ub+eps) ) - 1;
        elseif (Z_min < Z_lb)
            % The bigger error is at Zmin value
            MaxError = 1 - (Z_min/(Z_lb+eps));
        else
```

```
            % A solution has been found
            Error_1 = Z_ub - Z_max;
            Error_2 = Z_min - Z_lb;
            if (Error_1 > Error_2)
                MaxError = Error_1;
            else
                MaxError = Error_2;
            end
            fprintf('The value of antipad 1 is: %d \n',Xo(1)*2);
            fprintf('The value of antipad 2 is: %d \n',Xo(2)*2);
            fprintf('The maximum impedance value is: %d \n',Z_max);
            fprintf('The minimum impedance value is: %d \n',Z_min);
            fprintf('The MaxError value is: %d \n',MaxError);
            fprintf('\n');
        end
        % A solution has not been found, fminsearch will continue
        fprintf('The value of antipad 1 is: %d \n',Xo(1)*2);
        fprintf('The value of antipad 2 is: %d \n',Xo(2)*2);
        fprintf('The maximum impedance value is: %d \n',Z_max);
        fprintf('The minimum impedance value is: %d \n',Z_min);
        fprintf('The MaxError value is: %d \n',MaxError);
    else
        % Antipad values are not valid
        MaxError = 1;
        fprintf('The value of antipad 1 is: %d \n',Xo(1)*2);
        fprintf('The value of antipad 2 is: %d \n',Xo(2)*2);
        fprintf('No impedance was calculated. \n');
        fprintf('The MaxError value is: %d \n',MaxError);
    end

    %%% Stopping the clock for time calculation
    tf = clock;
    SimulationTime = etime(tf,ti);
    disp(['Partial sim time = ' mat2str(SimulationTime/60,5) ' minutes']);
    fprintf('\n');
end
```

6.4 antipad_HFSS_opt.m

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Main optimization program for the antipad calculation                          %
%                                                                                %
% AGV/JDLTA May, 2017                                                            %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clc;
ti_opt = clock;
disp(['Simulation starting time = ' mat2str(ti_opt/60,5) ' minutes']);
fprintf('\n');

%%% Seed values for the optimization variables
Xo=[23 26]; % Opt variables (antipad radio): [antipad1 antipad2]

%%% Applying the optimization method - fminsearch
options = optimset('MaxFunEvals',1000,'MaxIter',100,'TolX',1e-1);
[Xopt,FunVal,EF,output]=fminsearch('antipad_HFSS_OF',Xo,options);
f=FunVal;
iter=output.iterations;

fprintf('The number of iterations is: %d\n',iter);
fprintf('The function value at the solution is: %d\n',f);
fprintf('The value of the exit flag (EF) is: %d\n',EF);

fprintf('\n');
tf_opt = clock;
SimulationTime_opt = etime(tf_opt,ti_opt);
disp(['Total sim time = ' mat2str(SimulationTime_opt/60,5) ' minutes']);
```

6.5 Matlab files for plotting

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Main optimization program for plotting                                      %
%                                                                             %
% AGV/JDLTA May, 2017                                                         %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clc;
clear all;

% %%% Starting the clock for time calculation
% ti = clock;
%
% %%% Saving good data
% % Xo=[23 26];          % Seed values (antipad radio): [antipad1 antipad2]
% % Xo=[31.05 15.6];     % Antipad radio values with 20% tolerance
% % Xo=[29.755 16.25];   % Antipad radio values with 15% tolerance
% % Xo=[33.15 13.565];   % Antipad radio values with 5% tolerance
% Xo=[30 14];            % Antipad radio values - FIrst project
% [t, Z] = antipad_HFSS_driver(Xo);
% Z_max = max(Z);                % Zmax value
% fprintf('The maximum impedance is: %d \n',Z_max);
%
% %%% Stopping the clock for time calculation
% tf = clock;
% SimulationTime = etime(tf,ti);
% disp(['Total sim time = ' mat2str(SimulationTime/60,5) ' minutes']);

% Reading HFSS Output File
RespZ1 = csvread('C:\JDLTA\HFSS\antipad_hfss_results_23_26.csv',1,0);
t1 = RespZ1(:,1);                % Time value
Z1 = RespZ1(:,2);                % Impedance value

figure;
grid on;
hold on;

% RespZ2 = csvread('C:\JDLTA\HFSS\antipad_hfss_results_31_15.csv',1,0);
% RespZ2 = csvread('C:\JDLTA\HFSS\antipad_hfss_results_29_16.csv',1,0);
% RespZ2 = csvread('C:\JDLTA\HFSS\antipad_hfss_results_27_19.csv',1,0);
RespZ2 = csvread('C:\JDLTA\HFSS\antipad_hfss_results_33_13.csv',1,0);
t2 = RespZ2(:,1);                % Time value
Z2 = RespZ2(:,2);                % Impedance value


RespZ3 = csvread('C:\JDLTA\HFSS\antipad_hfss_results_30_14.csv',1,0);
t3 = RespZ3(:,1);                % Time value
Z3 = RespZ3(:,2);                % Impedance value

plot(t1,Z1,'r');
plot(t2,Z2,'b');
plot(t3,Z3,'g');

xlabel('Time(ns)'); ylabel('Impedance(Ohms)');
title('Impedance calculation with 15% tolerance');
marks_for_specs_antipad();

legend('Before optimization: (46 mils, 52 mils)',...
       'After optimization: (66.73 mils, 27.13 mils)',...
       'Manual adjustment: (60 mils, 28 mils)',...
       'Location','southwest');
```

```
function marks_for_specs_antipad()
    % Plotting the top specification:
      xh1 = [-5 10];
%     yh1 = [52.5 52.5 ];                    % 50 Ohms + 5%
%     yh1 = [55 55 ];                        % 50 Ohms + 10%
      yh1 = [57.5 57.5 ];                    % 50 Ohms + 15%
%     yh1 = [60 60 ];                        % 50 Ohms + 20%
      plot (xh1,yh1,'--k','linewidth',1);

    % Plotting the top specification:
%     yh2 = [47.5 47.5 ];                    % 50 Ohms - 5%
%     yh2 = [45 45 ];                        % 50 Ohms - 10%
      yh2 = [42.5 42.5 ];                    % 50 Ohms - 15%
%     yh2 = [40 40 ];                        % 50 Ohms - 20%
      plot (xh1,yh2,'--k','linewidth',1);
end
```