Instituto Tecnológico y de Estudios Superiores de Occidente

Reconocimiento de validez oficial de estudios de nivel superior según acuerdo secretarial 15018, publicado en el Diario Oficial de la Federación del 29 de noviembre de 1976.

Departamento de Electrónica, Sistemas e Informática

Maestría en Diseño Electrónico

Design of a 12-bit Sigma Delta ADC in 45 nm CMOS technology

TESIS que para obtener el **GRADO** de
MAESTRO EN DISEÑO ELECTRÓNICO

Presenta: **MARIO ANDRÉS JIMÉNEZ GONZÁLEZ**

Director **DR. ESTEBAN MARTÍNEZ GUERRERO**
Codirector: **DR. CUAUHTÉMOC R. AGUILERA GALICIA**

Tlaquepaque, Jalisco. 3 de noviembre de 2024.

To my parents, Bety González and Adrián Jiménez, for their unconditional love, constant support, and for instilling in me the values that have guided me throughout this journey, and for always encouraging me to strive for self-improvement. Your trust in me has been the driving force behind overcoming every obstacle.

To my wife, Mayra, for her patience, understanding, and for being my partner in this adventure. Thank you for your love, for believing in me, and for supporting me unconditionally through every step of this long journey.

To my siblings, Gustavo and Sandy, for being my source of inspiration and for always standing by my side during the most challenging moments of my life.

To my advisors, Esteban and Cuauhtémoc, for their invaluable guidance, endless patience, knowledge, and for sharing their expertise with me. Your mentorship has been essential to the completion of this work.

To Infineon, for believing in my potential and motivating me to finalize this chapter of my life by being surrounded by very talented colleagues.

Abstract

This thesis presents a 12-bit ΣΔ ADC design on 45 nm CMOS technology for MEMS sensor applications. The design was performed using Virtuoso Cadence tools. The circuit is composed by a first-order ΣΔ Modulator, a CIC filter, and a Decimator. The first-order ΣΔ Modulator having an oversampling ratio K=128 is developed implementing the switched-capacitor technique. The first-order ΣΔ Modulator is composed by an integrator, a comparator, and a 1-bit DAC. Simulation results show how the Modulator changes the output transitions frequency depending on the input voltage value, being K=128 the best tradeoff between the number of modulations and circuit complexity. The physical design of this block is fully customized. For the digital filter and decimator blocks, a third-order Cascaded Integrator Comb (CIC) filter is developed as a Verilog macro model to test and measure the transient and spectral response of the ADC, as well as its main Figures of Merit.

List of acronyms and abbreviations

ADC. Analog to Digital Converter

APR. Automatic Place and Route

CIC. Cascaded Integrator-Comb

CMOS. Complementary Metal-Oxide-Semiconductor

DAC. Digital to Analog Converter

DNL. Differential Nonlinearity

DR. Dynamic Range

ENOB. Effective Number of Bits

FFT: Fast Fourier Transform

FIR. Finite Impulse Filter

FOM. Figure of Merit

FSR. Full-Scale Range

GBW. Gain Bandwidth

IC. Integrated Circuit

IIR. Infinite Impulse Filter

INL. Integral Nonlinearity

MEMS. Micro-Electro-Mechanical Systems

MOS. Metal-Oxide-Semiconductor

MSB. Most Significative Bit

LPF. Low Pass Filter

LSB. Least Significative Bit

OTA. Operational Transconductance Amplifier

OSR. Oversampling Ratio

PSD: Power Spectral Density

RTL. Register Transfer Level

SC. Switched-Capacitor

SFDR. Spurious Free Dynamic Range

SINAD. Signal-to-Noise and Distortion Ratio

SNR. Signal-to-Noise Ratio

SQNR. Signal-to-Quantization-Noise Ratio

SR. Slew Rate

TG. Transmission Gate

VLSI. Very Large-Scale Integration

ΣΔ. Sigma-Delta

Contents

List of Tables

List of Figures

Introduction

Analog-to-digital converters (ADCs) play a vital role in modern electronics by converting continuous analog signals into discrete digital representations. This process allows for digital processing, storage, and manipulation of various signals, such as audio, video, sensor data, etc.

One prominent type of ADC is the sigma-delta (ΣΔ) converter, known for its high resolution and noise performance. ΣΔ converters employ a technique called oversampling, which involves sampling the analog signal at a much higher rate than the Nyquist-Shannon sampling theorem dictates. By oversampling, ΣΔ converters can achieve increased resolution and enhanced noise shaping.

The working principle of a ΣΔ converter involves a modulator and a digital filter. The modulator, a ΣΔ modulator, samples the analog signal at a high frequency and produces a stream of 1-bit digital data, commonly referred to as a bitstream. The digital filter then processes the bitstream, employing complex algorithms that reconstruct the original analog signal with high precision.

Oversampling converters provide several advantages. Firstly, the oversampling technique enables the converter to push the quantization noise to higher frequencies, reducing its impact on the desired band. This noise shaping property allows for increased dynamic range and improved signal-to-noise ratio.

Moreover, oversampling converters can achieve higher resolutions without the need for expensive, power-hungry, or precision components. By sacrificing sampling speed, oversampling converters can provide precise measurements even with lower-resolution analog-to-digital conversion.

ΣΔ converters find applications in various fields, including audio and video processing, telecommunications, and sensor interfaces [1]. They are particularly useful in situations where high-resolution conversion and noise immunity are critical, such as audio digital-to-analog converters (DACs) for high-fidelity audio reproduction or in medical devices for precise signal acquisition [2].

The ΣΔ converter presented in this document is designed on 45 nm CMOS technology.

In chapter one, the basics and fundamentals of ADCs are revisited, including an overview of both dynamic and static main specifications. Nyquist-rate ADCs and oversampling ADCs, such as ΣΔ ADCs, are reviewed.

Chapter two provides a detailed description of each block of the ΣΔ ADC. The design procedure for each block is presented in terms of specifications; numerous time-domain simulations are presented to validate the fulfillment of specifications of each block.

In chapter three, the CIC filter architecture and its components are introduced. Detailed description of the system macro model, implementation, and testing of each block are provided.

Chapter four integrates and tests the ΣΔ modulator with the CIC filter. The procedure and testbench are described, to measure the main ADC FoMs and its transient response.

In chapter five, the physical design of each block of the ΣΔ modulator is presented. Future work, including ADC improvements, VLSI implementation of the CIC Filter, and a general floorplan for the sigma delta ADC, is proposed.

The focus of this work is to put into practice all the micro-electronics techniques seen on the master's degree at ITESO University by developing this mixed-signal converter circuit.

This work presents several significant contributions, each addressing crucial aspects of the project. Firstly, it focuses on the meticulous design and implementation of a 12-bit Sigma-Delta

Converter, aiming to achieve high precision and reliability. Subsequently, extensive performance evaluation and analysis are conducted to assess the effectiveness and accuracy of the converter design. Additionally, efforts are directed towards circuit optimization and enhancing power efficiency to ensure optimal functionality and energy usage. Furthermore, the integration of the converter on 45 nm CMOS technology is explored, leveraging the advantages of this advanced fabrication process. Lastly, practical applications and implications of the developed converter are considered, aiming to extend its utility across various domains and industries, thus emphasizing its significance in advancing signal processing and measurement technologies.

While 45 nm is not the technology with highest density nowadays, and as there are plenty of ADCs with higher bitrate and performance, this dissertation makes several significant contributions to the academic environment and to the industry as some high-volume ICs are still manufactured on 45 nm technology.

1. Fundamental of ADCs

In this chapter, we will review the data conversion basics by describing what is a signal, the analog to digital data conversion process, their pros and cons, their tradeoffs most important Figures of Merit (FoMs). We'll also skim over some oversampling data converters and ΣΔ architectures.

1.1. Signal Digitization

Analog and digital signals

In the real world, analog signals such as sound, light, temperature, motion, force, etc. follow a continuous sequence with values that vary smoothly over time. However, for signal processing, this format of signals is not convenient but the digital one. This is the reason why in almost any electronic system a front-end a digitization scheme is added.

Digital signals are depicted as a series of discrete values, where the signal is divided into sequences based on the time intervals or sampling rate.

Analog to digital converter

An analog-to-digital converter (also known as ADC) converts an analog signal at the input, either voltage or current, and delivers a digital signal at its output. An ADC represented as a black box is depicted in Fig. 1-1. On the left side of the ADC, a sinusoidal signal represents the analog input, while on the right side the ADC delivers the digital outputs in this case, in a 3-bit word, for a 3-bit ADC.

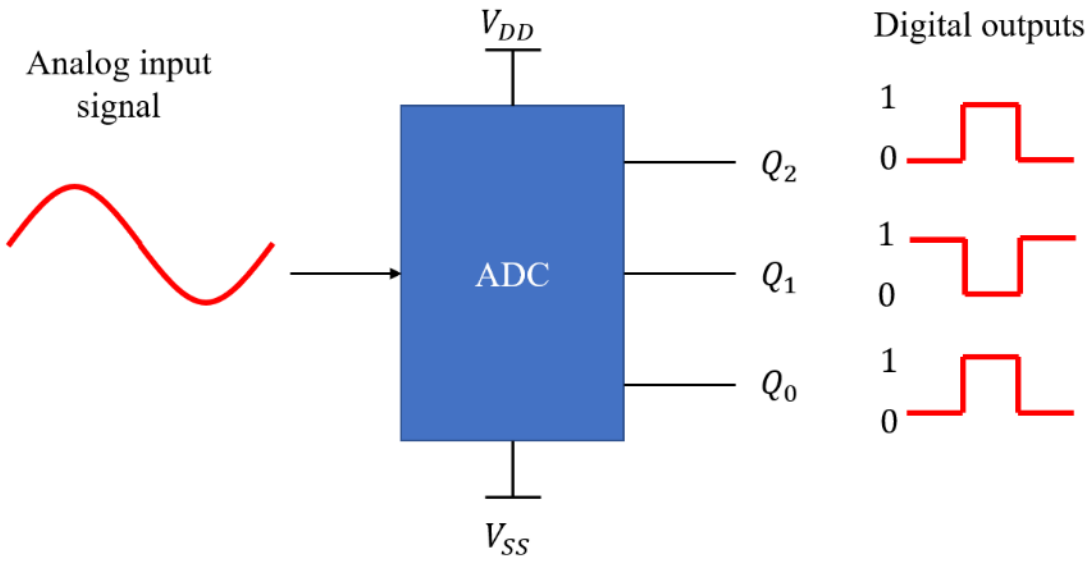

Fig. 1-1. A 3-bit ADC viewed as a black box [3].

Fig. 1-2 presents another abstraction level an ADC. From left to right, we have in the input of the ADC the analog signal which we want to digitize. Within the ADC the signal is first sampled, giving as a result, a discrete signal, which has stopped to be continuous in time. The quantization block receives the discrete signal and delivers a quantized signal as a result, which the main feature is that the signal amplitude is translated into digital words. Lastly, the Encode block receives the quantized signal and delivers a digital signal in a bitstream format.

Later, every block will be described deeply.

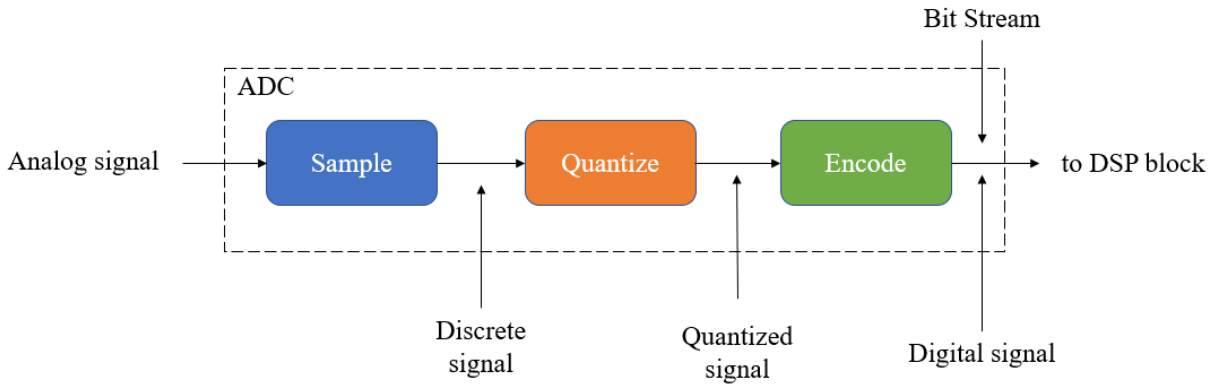

Fig. 1-2. ADC main blocks for data acquisition systems.

Sampling process

A discrete-time signal $x[n]$ is developed by uniformly sampling a continuous-time signal $x_a(t)$ as depicted in Fig. 1-3:

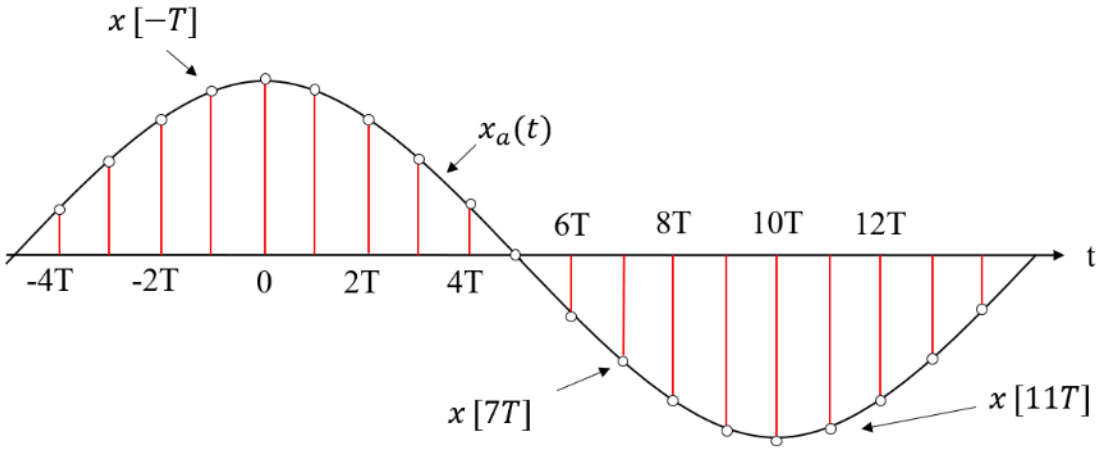

Fig. 1-3. Discrete-time sequence (in red) is generated by sampling the continuous-time signal $x_a(t)(black)$ [4].

According to the Nyquist-Shannon sampling theorem, to digitize an analog signal and transmit it by an electrical medium over long distances and be able to recover it at the far end with the highest possible fidelity, it is required that the analog signal be sampled (F_s) at least twice its maximum frequency (f_m).

$$F_s \geq 2f_m \tag{1.1}$$

Quantization

After having sampled a continuous-time signal, the resulting discrete-time signal values still are into a continuous space(infinite). Thus, is necessary to assign a value to them into a discrete space(finite) through quantization $Q[x(n)]$. It is important highlight that this process is a not invertible process.

The resulting quantized values depends on the number of quantization levels (L), quantization step (q) and the Dynamic Range (DR) of the signal ($V_{pp} = 2V_p$).

V_{pp} is defined as the peak-to-peak voltage of a signal, calculated as the difference between the positive ($+V_p$). and negative amplitudes (- V_p) of a waveform.

$$q = \frac{x_{max} - x_{min}}{L}$$

Where x_{max} and x_{min} are the upper and lower values of the quantized step.

A more graphical explanation of how related the L levels with the quantization step are, is shown in Fig. 1-4.

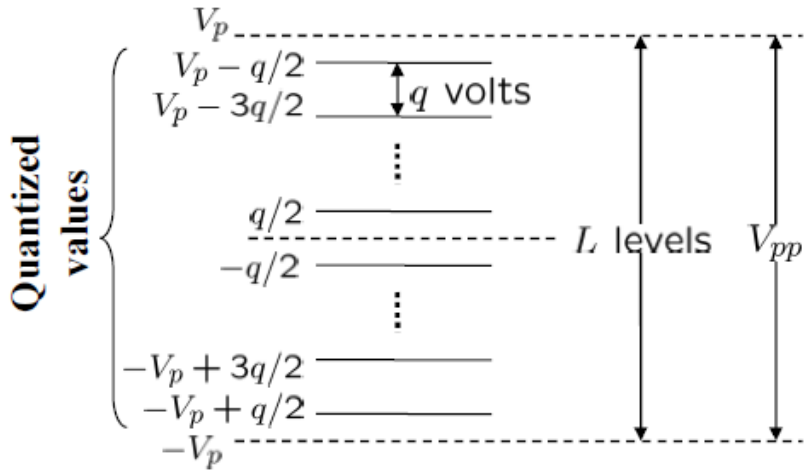

Fig. 1-4. Signal Quantization Levels in terms of the dynamic range of the signal and quantization step q [5].

As it can be noted from Fig. 1-4, the inverse relationship between the quantization step and the signal fidelity, as bigger the quantization q step is, the more information of the analog signal is lost, thus a low value of q is desirable. However, in practice, L can't be infinite, and the designer task is to find the appropriate values that satisfy the specifications of data conversion.

Let's illustrate this with an example, we need to digitize a sinusoidal signal using $q = 3$. It can be seen in Fig. 1-5 that the step size might be remarkably big for some applications, but the benefit of this could be an ultra-low power converter. That could be attractive in some applications where high accuracy is not a priority, but power consumption.

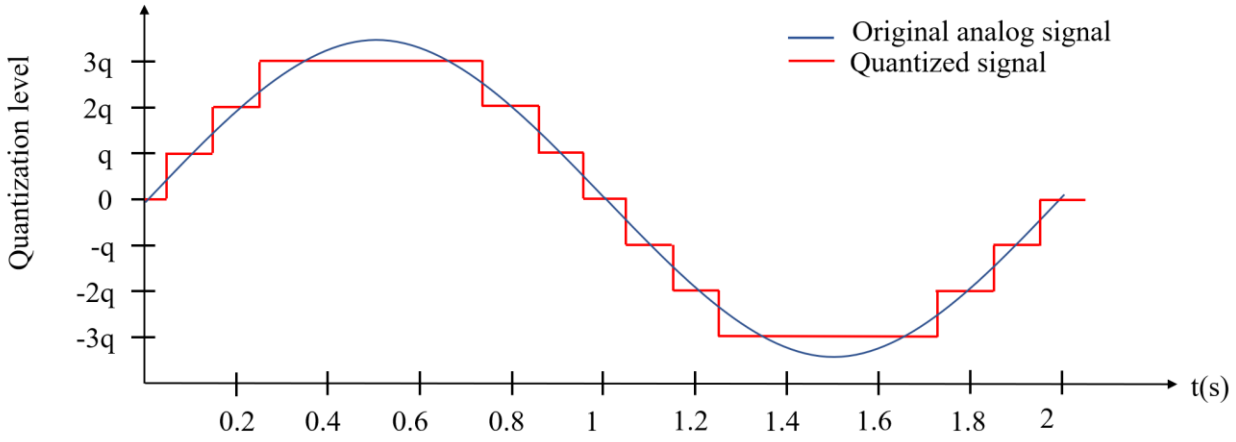

Fig. 1-5. Sinusoidal analog signal quantized with q = 3 [6].

Codification

After having quantized the samples, now a binary code must be assigned to them. The resulting serial sequence made with ones and zeros is known as Pulse-code modulation (PCM) sequence.

Every sample is codified with the same bit number (word length B) which is determined by:

$$k = log_2(\mathrm{B}) \tag{1.2}$$

Let's take again the example from Fig. 1-5. Here, the samples are taken in fixed intervals of time, but what happens when we take a sample that is out of these intervals and out of the quantization steps? And how is determined the output PCM sequence according to the quantized sample?

To have a more graphical approach, Fig. 1-6 depicts the same sinusoidal signal with $q = 3$, but here the samples are taken in non-fixed intervals. It can be seen how the quantized sample is being truncated or rounded up from the natural sample value to the closest code number.

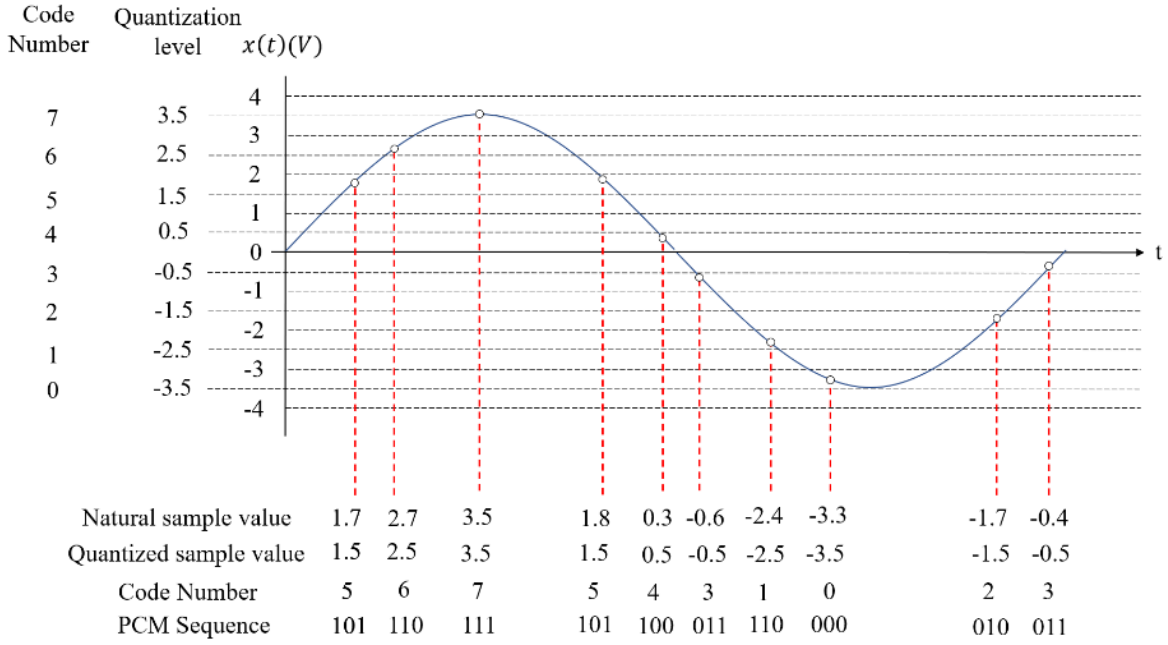

Fig. 1-6. Sinusoidal analog signal coded to a 3-bit Digital signal [7].

1.2. Static ADC specifications

In this section we define the main parameter of data converters that typically are used to define the performance of a converter.

Quantization error (Qe)

It is defined as the difference between the analog input signal and the digital output signal generated by the ADC.

$$Q_e = V_{in} - V_{quantized} \tag{1.3}$$

Where $V_{quantized}$ can be obtained as:

$$V_{quantized} = D * \frac{V_{ref}}{2^N} \tag{1.4}$$

Here V_{ref} is the voltage reference of the converter, N is the number of bits of resolution of the ADC, and D is the output code value in decimal.

Gain error

Defined as the slope error that interpolates the transfer function steps. Ideally, the value of slope "m" we want is 1. Nevertheless, when the gain error is present, the slope gets modified, and then we define the gain error as the deviation between the actual slope and the ideal slope (see Fig. 1-7).

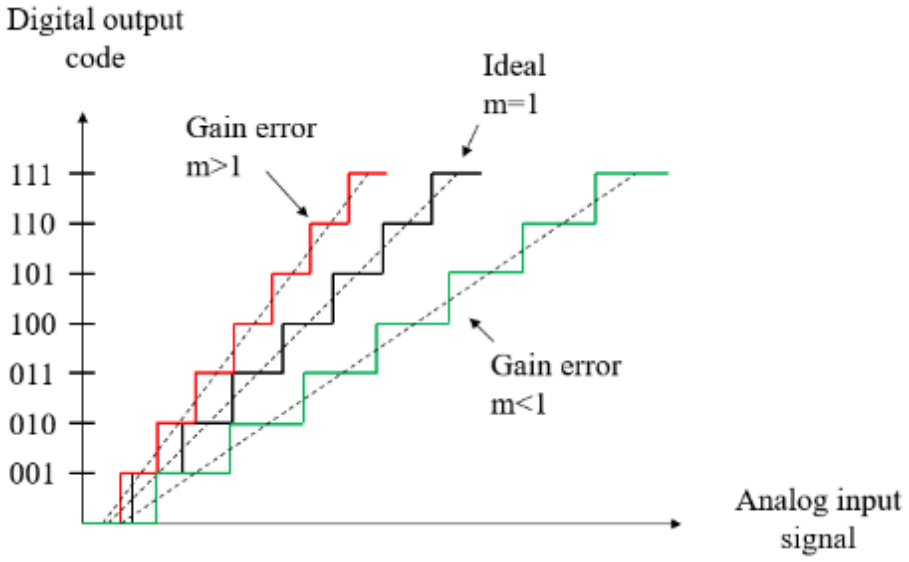

Fig 1-7. Gain error for a 3-bit ADC. [8]

Offset error

It is defined as the output value when the input is zero. Offset error impacts the transfer function, causing all steps to shift equally (see Fig. 1-8).

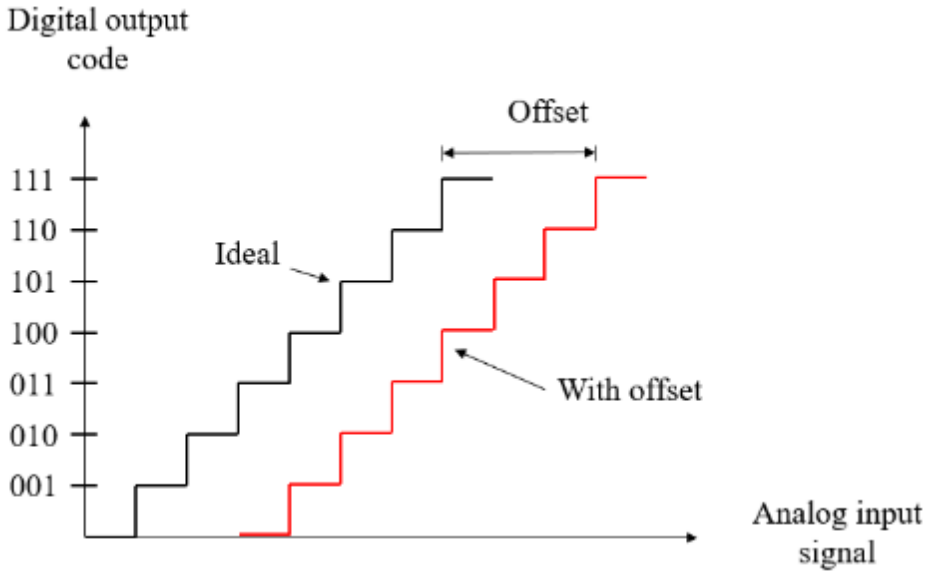

Fig. 1-8. Offset error for a 3-bit ADC [9].

Differential Nonlinearity (DNL)

Defined as a fraction of the LSB value between the actual transfer function and the perfect transfer function of the converter (see Fig. 1-9).

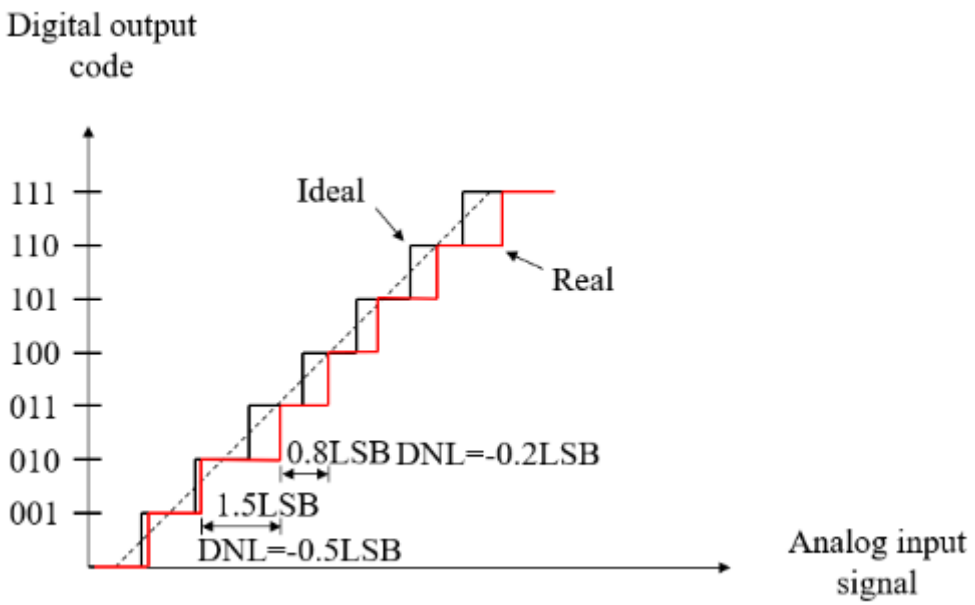

Fig. 1-9. DNL for a 3-bit ADC [10].

Integral Nonlinearity (INL)

It is defined as the maximum deviation between the converter's transfer function and the straight line connecting the first and last digital output codes of the converter (see Fig. 1-10).

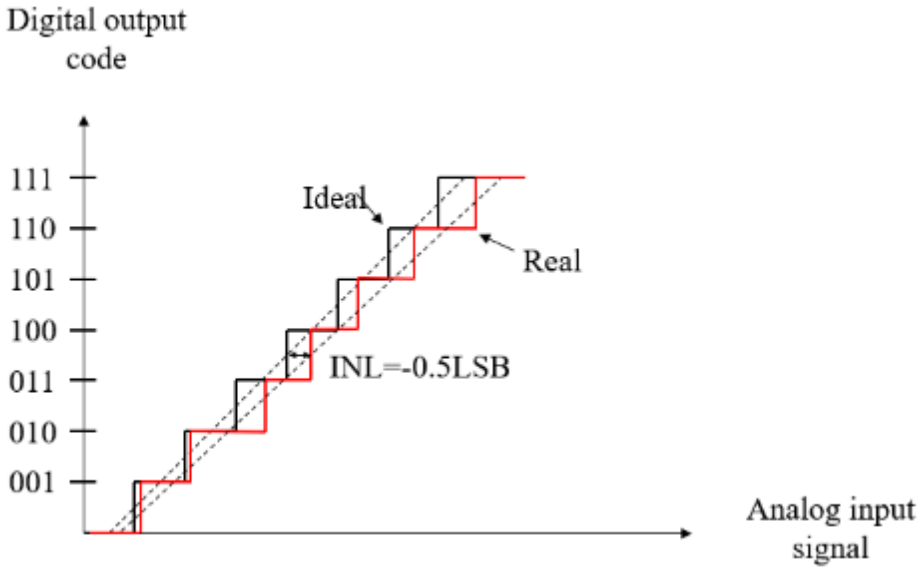

Fig. 1-10. INL for a 3-bit ADC [10].

Resolution

It is defined as the smallest input voltage increment within the Full-Scale Range (FSR) that results in a change to the digital output.

$$Resolution = \frac{V_{ref}}{2^N} \tag{1.5}$$

1.3. Dynamic ADC specifications

Dynamic Range (DR)

Defined as the range between the noise floor of a device and its specified maximum output level. In other words, this is the range of signal amplitudes that the ADC can resolve.

$$DR = 20 \log (2^N - 1) \tag{1.6}$$

Spurious Free Dynamic Range (SFDR)

It describes the ratio between the amplitude of the fundamental frequency and the amplitude of the strongest harmonic.

$$SFDR = 20 \log \left(\frac{Amplitude\ of\ Fundamental(RMS)}{Amplitude\ of\ Largest\ Spur(RMS)} \right) \tag{1.7}$$

Signal-to-Noise Ratio (SNR)

Represents the ratio of the highest RMS value of the input signal to the RMS noise value of the converter. It is typically expressed in dB and calculated as:

$$SNR = 20\log\left(\frac{V_{Signal}(max)}{V_{Noise}}\right) \tag{1.8}$$

Signal-to-Noise and Distortion Ratio (SINAD)

Defined as the ratio of the RMS signal amplitude to the root-sum-square (RSS) of all other spectral components, including harmonics, but excluding the DC component. Typically, this parameter is plotted for frequencies above the Nyquist frequency to assess performance in undersampling scenarios [11]. This specification can be known as SNDR too.

$$SINAD = 20\log\left(\frac{V_{Signal}(max)}{V_{Noise} + V_{Distortion}}\right) \tag{1.9}$$

Signal-to-Quantization-Noise Ratio (SQNR)

Defined as the ratio of the input signal power, to the quantization noise power [12].

$$SQNR = 10\ log\frac{P_{sig}}{P_{NQ}} = 6.0206\ N + 1.7609\ dB \tag{1.10}$$

It can be seen in equation (1.10), that every bit added (N) results in +6 dB to the SQNR.

Effective Number of Bits (ENOB)

It reflects the converter's accuracy based on the input frequency and the selected sampling rate. This is determined by substituting the measured Signal-to-Noise and Distortion (SINAD) value into the equation for the Signal-to-Noise Ratio (SNR) of an ideal ADC, then solving for N (the number of bits).

$$ENOB = \frac{SINAD - 1.76\ dB}{6.02}(bits) \tag{1.11}$$

Power consumption (P)

Defined as the total power that drains the ADC from a determined voltage power supply, in a steady state. It is measured in Watts (W).

An ADC will usually require two separate power supplies: analog and digital. While the analog voltage supply (A_{VDD}) powers the conversion block, the digital voltage supply (D_{VDD}) is used for the device's digital communications, then, the total average power consumption is defined as:

$$P_{total} = P_{AVDD} + P_{DVDD} \tag{1.12}$$

$$P_{AVDD} = A_{VDD} * I_{AVDD} \tag{1.13}$$

The current drawn from A_{VDD} source (I_{AVDD}) is usually found in the device data sheet based on the sampling rate (F_s). If I_{AVDD} is not specified, the equation (1.14) can be used to find it [13].

$$I_{AVDD} = (I_{AVDD}@1MHz) * \frac{F_s}{1\ MHz} \tag{1.14}$$

On the other hand, P_{DVDD} is a function of D_{VDD} and I_{DVDD},

$$P_{DVDD} = A_{VDD} * I_{DVDD} \tag{1.15}$$

I_{DVDD} depends on the frequency of stage changes to the digital output signal (f_{D_out}) and the load capacitance of the digital output line (C_{D_out}) [13],

$$I_{DVDD} = D_{VDD} * f_{D\_out} * C_{D\_out} \tag{1.16}$$

Slew rate (SR)

Indicates the highest rate of change an ADC's input signal can undergo without introducing errors in the digital output.

$$V_p = \frac{SR}{2 * \pi * f} \tag{1.17}$$

$$SR > 2 * \pi * f * V_p \tag{1.18}$$

Where f is the frequency of the output signal, and V_p is the peak voltage of the output signal.

Sampling rate

It refers to the number of samples collected per unit of time from a continuous signal in order to create a discrete signal during the analog-to-digital conversion process.

1.4. ADC architectures

Nowadays, the wide variety of markets has led to more spec-demandant ADCs, in which the balance between resolution and sampling rate are crucial, determining the ADC architecture of the desired application.

If we categorize these architectures according to their operating sampling rate, we get two major categories:

Nyquist-Rate ADCs: Includes all ADCs where the sampling rate is only slightly higher than the Nyquist rate. In Fig. 1-11 is depicted the typical high-level block diagram of these converters. In contrast to Fig. 1-2 previously seen, the Sample block is now split in the Anti-aliasing and the S/H (Sample and Hold) blocks.

Most of these converters can't achieve an ENOB above 15-bit [14]. Just to mention some ADCs techniques of conversion within this category, the Flash, Pipeline, and Successive approximation ADCs.

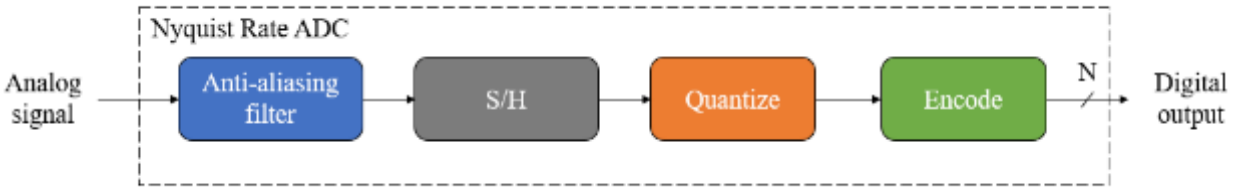

Fig. 1-11. Block Diagram structure of a typical Nyquist Rate ADC [15].

Oversampling ADCs: It refers to all ADCs that have a far high sampling rate above the signal bandwidth. In Fig. 1-12 is depicted the high-level block diagram of these converters. Main difference with the Nyquist Rate ADC is that the ΣΔ modulator acts as the Anti-aliasing filter, the sampling and quantize blocks due to its operation principle. The encoding is accomplished by applying a digital filter at the output.

The oversampling ADC is capable of achieving significantly higher resolution compared to converters operating at the Nyquist rate. The ΣΔ modulator is the most popular architecture under this classification, being so the architecture that this work will focus on.

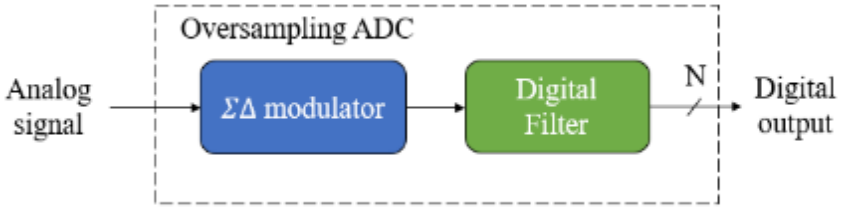

Fig. 1-12. Block Diagram structure of an Oversampling Rate ADC [15].

1.5. ΣΔ ADC basics

While a Nyquist-Rate ADC produces a quantization noise in terms of the quantized step, up to half of the ADC sampling rate $F_s/2$ (depicted in Fig. 1-13), an oversampling ADC features a narrow quantization noise but spreads far above $F_s/2$. It comprehends up to K* $F_s/2$, where K is the oversampling factor.

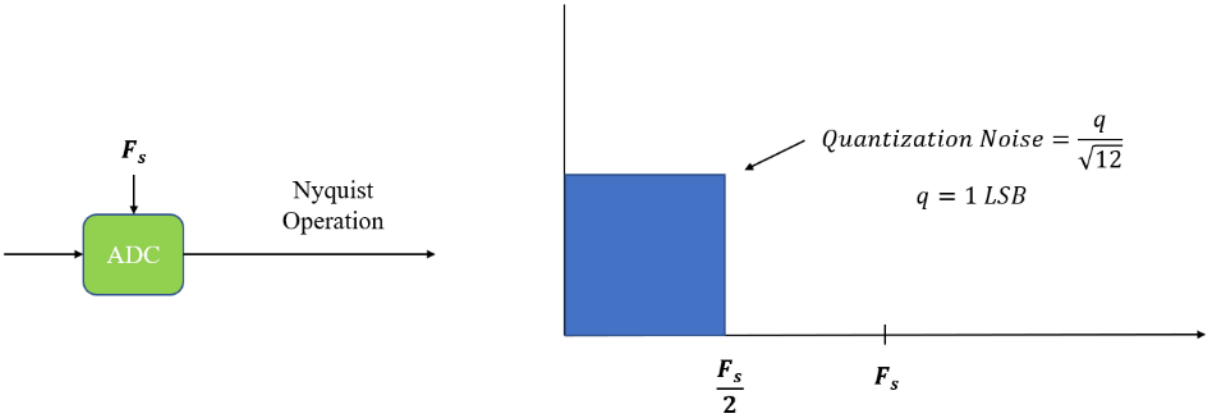

Fig. 1-13. Nyquist-rate ADC Quantization Noise [16].

The key technique here is using a Low Pass Filter (LPF) with a cutoff frequency of $F_s/2$ to filter out high-frequency quantization noise (depicted in Fig. 1-14). This is an advantage of oversampling ADC. But there's an additional feature that is still missing to fully complete the ΣΔ modulator and that is noise shaping.

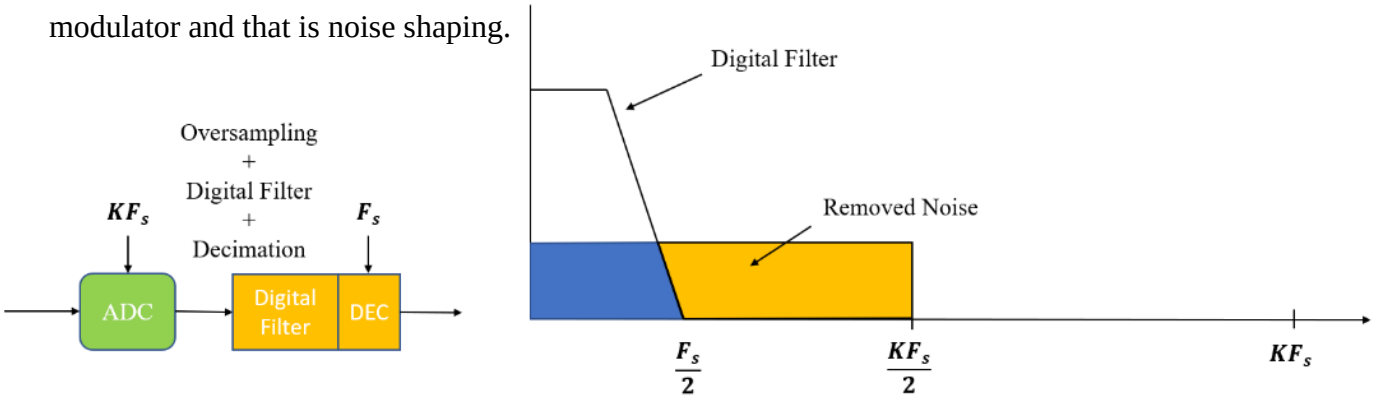

Fig. 1-14. Oversampling ADC Quantization Noise [16].

Until Fig. 1-14, quantization noise was spread uniformly across the frequency axis.

But what if this noise is "shaped" so that the majority of it lies beyond the $F_s/2$ frequency, meaning that after applying the LPF we got minimum remaining quantization noise? This phenomenon is depicted in Fig. 1-15, resulting in a much less quantization noise in comparison with a Nyquist-rate ADC.

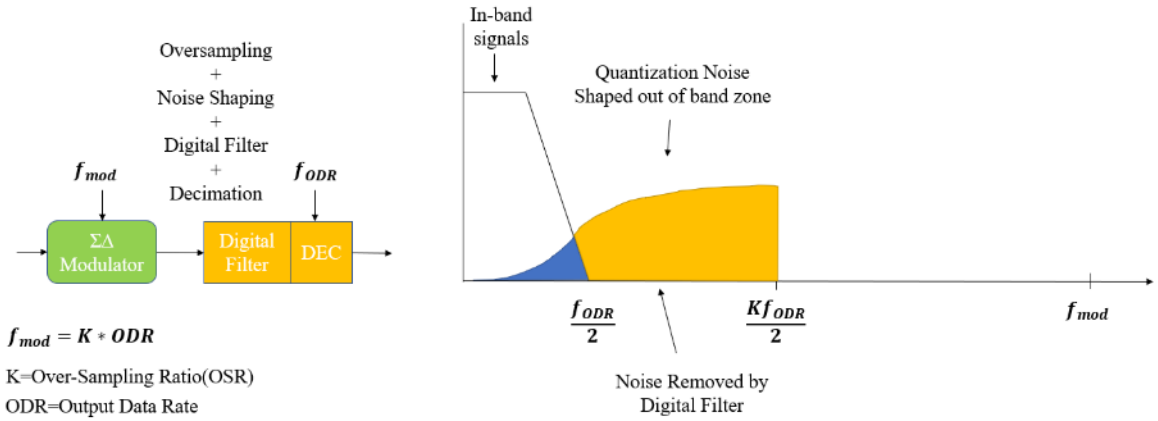

Fig. 1-15. ΣΔ ADC Quantization Noise [16].

The distribution of the quantization noise is determined by the order of the ΣΔ modulator.

While first-order ΣΔ modulator results in a far higher improvement in comparison to a normal oversampling ADC, a second-order ΣΔ modulator, as depicted in Fig. 1-15, removes even more noise out of the band zone [17].

The decimator block, which is at the end of the processing chain (yellow block of Figure 1-15), has the task of resampling the filtered output at a lower rate to eliminate any redundant signal data that could have been introduced by the oversampling process.

In Fig. 1-15, the digital filter and the decimator blocks are encapsulated in a single block because they are often combined to increase computational efficiency, but it is dependent on the Digital Filter that was implemented. For example, when using a finite impulse response (FIR) filter, which typically produces one output for each input sample, it is more efficient to calculate the filter outputs at a reduced decimation rate.

On the contrary, if an infinite impulse filter (IIR) is implemented, as it implements feedback resulting in immediate results used, is not possible to implement a decimation process inherently to the filter. Also, there are even ΣΔ ADCs architectures that implement the filtering in two or more stages, combining IIR and FIR filters, where the decimation is usually done just at the end of the FIR filter, or if the filter consists of FIR filters only, the decimation is split between the stages.

The selection of FIR or IIR filters depends on a variety of tradeoffs of stability, phase characteristics, design complexity but also determine the built-in “pipeline” delay, which is also

known as latency. As these filters can be quite large (up to several hundred taps), delay can become an issue depending on the application.

A first order ΣΔ Modulator block depicted in Fig. 1-12 is translated to its equivalent closed-loop circuit as shown in Fig. 1-16:

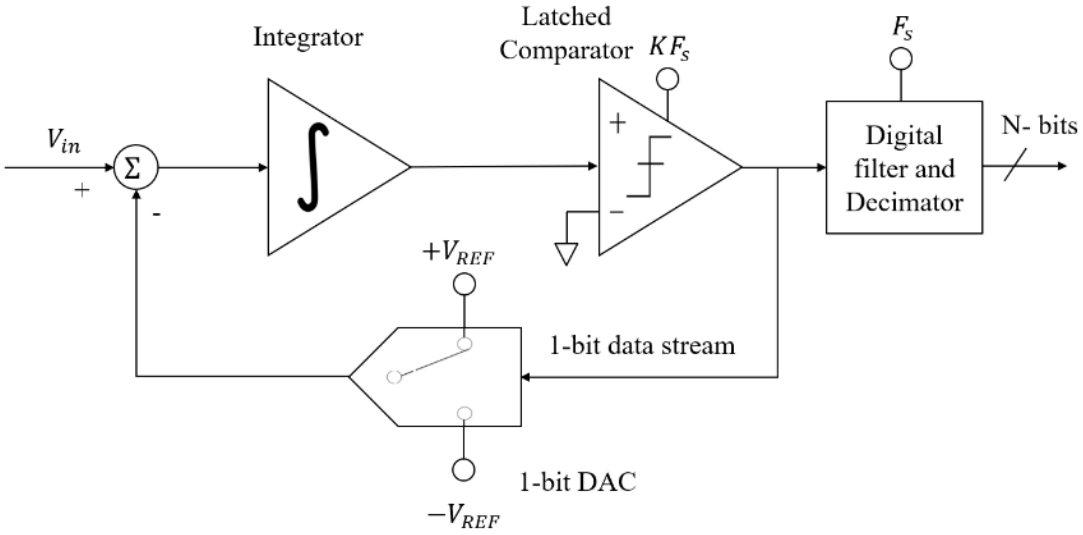

Fig. 1-16. First-order ΣΔ ADC Closed-Loop System Block Diagram [18].

The negative feedback system in Fig. 1-16 of a first-order ΣΔ Modulator, is compound in the direct branch first by an Integrator and a Latched Comparator, while on the feedback branch only the 1-bit DAC.

The integrator has a ramping up/down behavior in presence of a DC input. It can be implemented through the switched-capacitor (SC) technique. This will be deeply described in the next chapter.

The comparator's function is to compare the voltages at its two inputs and produce a two-state logic output. If the voltage at the non-inverting input is greater than that at the inverting input, the output will be a logic "1." Otherwise, the output will be a logic "0."

At the output of the comparator begins the negative feedback branch with a 1-bit DAC module, which main function is to translate the stream of logic “1” and “0” to fixed positive and negative values that are next subtracted from the input signal. The negative feedback loop will

drive the average DC voltage at the DAC output to match V_{in}, meaning the DAC's average output must equal V_{in}. This average is regulated by the "ones density" in the comparator's output.

As the input signal approaches $+V_{REF}$, the proportion of "1"s in the serial bit stream increases, while the number of "0"s decreases. Conversely, when the input signal moves towards $-V_{REF}$, the number of "0"s rises, and the "1"s decrease. A meaningful result is only obtained when a large number of samples are averaged.

The output of this loop connects to the Digital Filter + Decimation blocks, which function was previously discussed.

ΣΔ ADCs can be viewed as voltage-to-frequency converters with an integrated counter. By counting the number of logic "1"s in the output over a sufficient number of samples, the counter will represent the digital value of the input signal.

1.6. Higher-order ΣΔ ADC

There are multiple ways of achieving higher-order ΣΔ Modulators by taking the structure of a first order ΣΔ Modulator, and by re-arranging some of their blocks. The most popular topology involves adding a second integrator into the direct branch and modifying the 1-bit DAC output of the feedback branch. At this time, the output of the 1-bit DAC is subtracted to both the input signal and the output of the first integrator as depicted on Fig. 1-17.

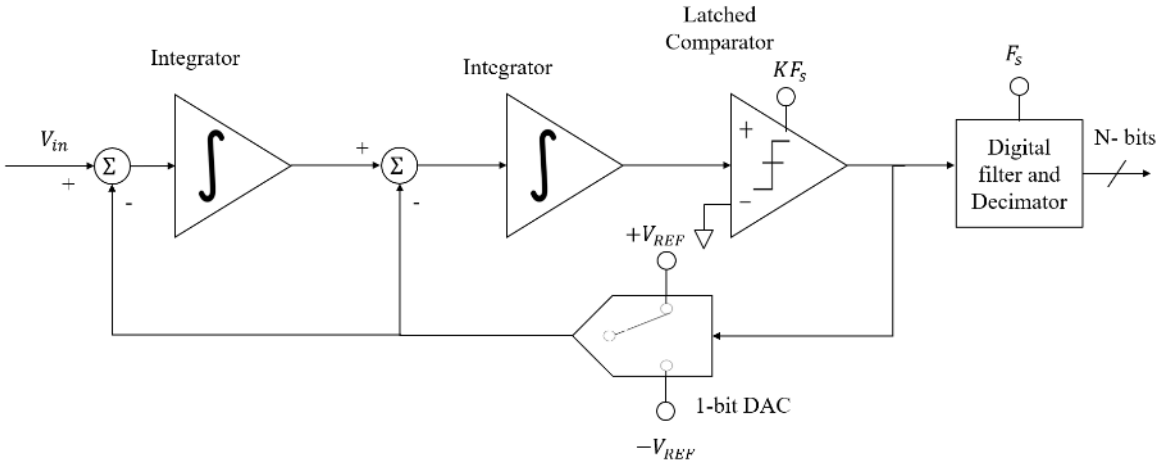

Fig. 1-17 Second-Order ΣΔ ADC Closed-Loop System Block Diagram [19].

Among the benefits of higher-order modulator loops are achieving a wide dynamic range and higher resolution than a first-order ΣΔ Modulator. Noise removed by the digital filter is higher, but the tradeoff is that the stability is not guaranteed under all input conditions.

On previous sections, a wide variety of specifications and ADC classifications were reviewed, but it is a task of the designer to choose between the pros and cons of them according to the specific application. In this work, an ADC is requested for a MEMS inertial sensor, thus some of the critical specifications for this application are resolution, ENOB, dynamic range, sampling frequency, SNR, power consumption, linearity, and Gain/Offset errors, as this ADC is intended to be integrated to a portable device [20] [21] [22] [23] [24].

2. The ΣΔ Modulator

2.1. Problem statement

An analog output from an inertial MEMs sensor must be digitized with 12-bit resolution. The analog output peak-to-peak voltage (V_{pp}) is 200 mV, it has a frequency $f = 4\ kHz$, and it is mounted over an offset voltage of 500 mV $(V_{DD} / 2)$.

A first order ΣΔ ADC was selected as they can achieve a high amount of output bits for low bandwidth requirements. A very low P_D is critical as is intended for battery-powered devices.

This converter also needs to meet certain static and dynamic FOMs. Depending on the OSR of the modulator it can achieve an SNR starting from 40 dB with an oversampling ratio K = 64, up to 80 dB or more with and K > 512 [25] [26].

There are reported works of first order ΣΔ Modulators with a THD of -69 dB while maintaining power consumption P_D of 114 µW [27].

In terms of resolution and ENOB, it is reported a range of 8 to 10 bits, depending on the blocks being ideal or transistor level [25] [26] [27].

The parameters in Table 1 were set as target FoMs for this work.

Table 1. Target ΣΔ ADC Figures of Merit.

FoM	*Value*
Signal-to-Noise Ratio (SNR)	60 dB
Total Harmonic Distortion (THD)	-69 dB
Max power consumption P_D	114 µW
Effective Number of Bits (ENOB)	8

2.2. Blocks of first order modulator

In the Section 1.5 (ΣΔ ADC basics), the ΣΔ Modulator blocks were briefly described; however, this chapter intends to analyze them more in detail and explore the effects, drawbacks, and trade-offs of choosing between one circuit implementation and another.

2.2.1 Switched-capacitor circuits.

Switched-capacitor (SC) circuits are implemented in this work as these operate in discrete-time, which results convenient in an analog-to-digital converter.

The switched-capacitor technique consists of using a capacitor between a series of switches to form a filter. It works by moving charges inside and out of the capacitors when the switches are open and closed.

The most popular SC circuit is to obtain an equivalent resistor by switching a capacitor between two switches [28], but this basic topology can carry high parasitic capacitances.

However, there are topologies that mitigate parasitic capacitances by evenly dividing them at the input terminals, thus the clock feedthrough and charge injection are minimized, resulting in an unaffected capacitance [28].

There are times when the signal in question to be filtered requires having the full excursion or closest from 0 to V_{DD}, where implementing the switches with only one MOS device runs the risk of not being able to comply it. To avoid this problem, transmission gates (TG) are preferred.

A TG is an arrangement of an NMOS and a PMOS transistors connected in parallel [29].

2.2.2 The integrator

The integrator block in the ΣΔ Modulator was implemented through the SC technique (see Fig. 2-1.

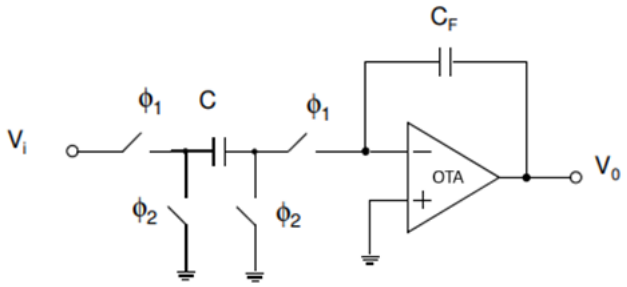

Fig. 2-1. Switched-capacitor Inverter Integrator [28].

$$\frac{V_o}{V_i}(s) = -\left(\frac{1}{sRC}\right) \tag{2.1}$$

$$\frac{V_o}{V_i}(z) = -\frac{1}{T_{CLK}\left(\frac{C_F}{C}\right)}\frac{1}{1-z^{-1}} \tag{2.2}$$

2.2.3 The OTA

The amplifier depicted in Fig. 2-1 is implemented with an Operational Transconductance Amplifier (OTA), which we will enter in detail.

An OTA combines the functionality of an op-amp with a transconductance amplifier with the finality to convert voltage signals into current signals.

There are basic implementations of OTA's with NMOS and PMOS transistors (e.g. simple OTA, telescopic OTA, etc. [30]), which achieves low gain, but as this works requires a high gain, a self-cascode OTA is implemented. This OTA takes the simple OTA implementation of [30] as a baseline but implements the self-cascode structure (see Fig. 2-2) to every MOS transistor to increase its output resistance, thus increasing the voltage gain.

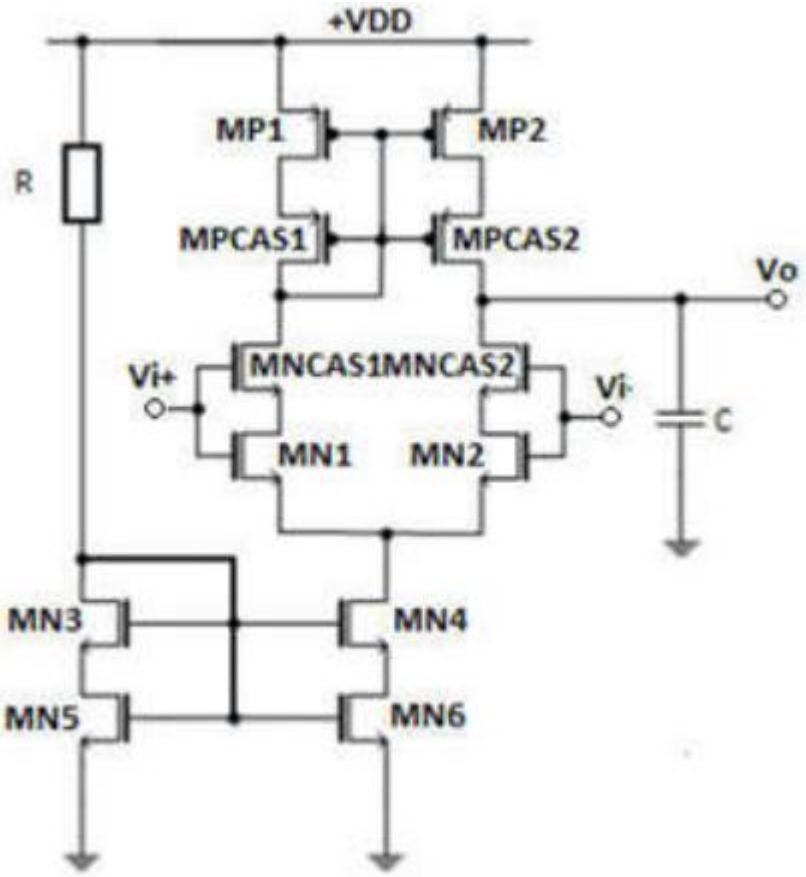

Fig. 2-2. Self-cascode OTA [31].

In Fig. 2-2, MOSFETs with subfix "CAS" perform the cascode effect, where they are sized to boost their output resistance.

Branch currents of the OTA are the following:

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{I_B}{2} \tag{2.3}$$

Where I_B is the bias current flowing through transistors MN4 and MN6.

Maximum I_B of the OTA can be calculated from P_{Dmax} , Gain-Bandwidth product (GBW), and Slew Rate (SR) specifications.

$$I_{Bmax} = \frac{P_{Dmax}}{V_{DD}} \tag{2.4}$$

Another useful relationship of I_B in terms of g_m and V_{Dsat} is the following:

$$I_B = g_m * V_{Dsat} \tag{2.5}$$

g_m is obtained from GBW specification.

$$GBW = \frac{g_m}{C_L} \tag{2.6}$$

DC voltage Gain and Gain-Bandwidth product can be calculated in terms of g_m and R_O:

$$A_v = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \cong g_m * R_O \tag{2.7}$$

The output resistance of the self-cascode OTA can be determined as follows:

$$R_o = \frac{A_v}{g_m} = g_{m1} * r_{o1} * r_{oCAS1} \tag{2.8}$$

Where $g_{m1} * r_{oCAS1}$ is called the cascode gain.

R_o can be also determined by:

$$R_o = (m-1) * r_{o1} \tag{2.9}$$

Where *m* can be set as the multiplicity parameter of the MOS transistor.

And g_m in terms of K_n, $\left(\frac{W}{L}\right)$ and I_D as:

$$g_m = \sqrt{2 * I_D * K_n \left(\frac{W}{L}\right)} \tag{2.10}$$

Where:

$$V_{Dsat} = V_{GS} - V_T \tag{2.11}$$

Also I_B can be defined in terms of the SR specification:

$$SR_+ = \frac{I_B}{C_L} \tag{2.12}$$

The DC voltage V_{OCM} in terms of V_{DD} and V_{Dsat} of transistor M3 is:

$$V_{OCM} = V_{DD} - |V_{TH3}| - \sqrt{\frac{I_B}{K_p * \left(\frac{W}{L}\right)_P}} \tag{2.13}$$

Solving for $\left(\frac{W}{L}\right)_P$ from equation (2.13),

$$\left(\frac{W}{L}\right)_P = \frac{I_B}{K_p(V_{DD} - V_{OCM} - |V_{TH3}|)^2} \tag{2.14}$$

The size ratio of NMOS transistors $\left(\frac{W}{L}\right)_N$ calculation by knowing g_m and I_B, that is,

$$\left(\frac{W}{L}\right)_N = \frac{{g_m}^2}{K_n * I_B} \tag{2.15}$$

Using $L_N = L_P = 2 * L_{min}$. And $\left(\frac{W}{L}\right)_P$ from equation (2.14) and $\left(\frac{W}{L}\right)_N$ from equation (2.15):

$$W_{N1} = W_{N2} = \left(\frac{W}{L}\right)_N * L_N \tag{2.16}$$

$$W_{P1} = W_{P2} = \left(\frac{W}{L}\right)_P * L_P \tag{2.17}$$

Current mirror I_o can be described as:

$$I_o = \frac{1}{2} K_n \left(\frac{W}{L}\right)_{N3} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \tag{2.18}$$

Where:

$$V_{GS} = V_{Dsat} + V_T \tag{2.19}$$

Then equation (2.18) can be rewritten as:

$$I_o = \frac{1}{2} K_n \left(\frac{W}{L}\right)_{N3} (V_{Dsat})^2 (1 + \lambda V_{DS2}) \tag{2.20}$$

Solving for $\left(\frac{W}{L}\right)_{N3}$ we get,

$$\left(\frac{W}{L}\right)_{N3} = \frac{2I_o}{K_n (V_{Dsat})^2 (1 + \lambda V_{DS2})} \tag{2.21}$$

R_{REF} calculation for the reference branch of the current mirror is:

$$R_{REF} = \frac{V_{DD} - V_{GS3} - V_{GS5}}{I_{REF}} \tag{2.22}$$

Solving for V_{GS} from equation (2.18):

$$V_{GS} = \sqrt{\frac{2 * I_o}{K_n * \left(\frac{W}{L}\right)_N}} + V_T \tag{2.23}$$

2.2.4 The comparator

A CMOS design comparator, especially in data converter applications, must meet several key specifications to ensure optimal performance; the main ones are response speed, accuracy, and power consumption.

Response speed for data converter applications: the response speed of a comparator is critical. It must be fast enough to keep up with the input signal and allow accurate data conversion. The intrinsic response speed of the comparator depends mainly on the size of the input transistors since they define the transconductance g_m and parasitics components. Other parameters such as the capacitive load can also affect the response speed of the comparator.

Accuracy: the accuracy of the comparator is essential to ensure accurate data conversion. The topology of the comparator should have small hysteresis and low offset voltage dispersion to minimize reading errors.

Power consumption: In any integrated circuit, minimizing power consumption is essential, particularly for portable or low-power applications. The power consumption of a comparator circuit is influenced by the bias current, supply voltage, and the circuit's response speed.

The comparator in this design uses a two-stage OTA topology (Fig. 2-3) because it offers advantages such as high open-loop voltage gain, large output swing, and fast response speed.

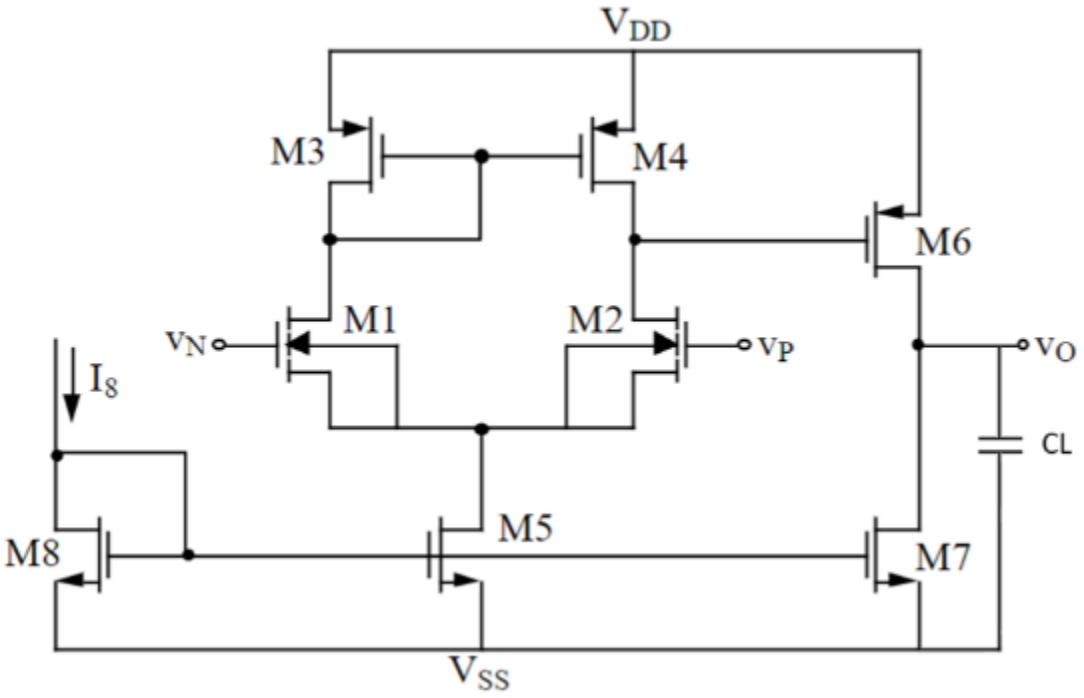

Fig. 2-3. Two-stage comparator schematic [32].

The CMOS comparator response can be characterized using several parameters, including the transconductance of the transistors, parasitic capacitances, and charge and discharge currents. A commonly used equation to define response speed in general terms is the following:

$$response\ speed = \frac{1}{2\pi f_{BW}} \tag{2.24}$$

Where f_{BW} is the bandwidth frequency of the comparator.

$$f_{BW} = \frac{1}{2\pi R_O C_O} \tag{2.25}$$

Here R_O and C_O represent the output resistance and the output capacitance of the OTA, respectively.

The Slew ratio SR of the OTA is defined as:

$$SR = \frac{I_5}{C_L} \tag{2.26}$$

Where I_5 is the current through transistor M5, and C_L the load capacitance.

Similar to a digital circuit, the comparator's power consumption consists of both static and dynamic power.

Static power is defined by equation (2.27)

$$P_{static} = V_{DD} I_{bias} \tag{2.27}$$

Where V_{DD} is the voltage supply of the comparator, and I_{bias} is the current flowing through I_5.

Dynamic power is given by equation (2.28)

$$P_{dynamic} = f_{clk} C_L V_{DD}^2 \alpha \tag{2.28}$$

C_L represents the load capacitance, f_{clk} is the clock frequency at which the output switches, and α is the switching activity factor, defined as the likelihood of the circuit node transitioning from logic "0" to logic "1". Switching power is only consumed during these transitions.

2.2.5 The 1-bit DAC

A 1-bit DAC converts a single-bit (0 or 1) digital signal into an analog signal. Its simplest structure involves a switch controlled by the input bit. Although 1-bit DACs may not offer the same precision as multi-bit DACs, they are useful in applications where speed and simplicity are more important than precision, such as in the sigma-delta modulator. According to Fig. 1-17, the input bit of the DAC is generated by the comparator. The DAC topology used in this design is composed by an inverter followed by two TGs switches (see Fig. 2-4). The reference voltages $+V_{REF}$ and $-V_{REF}$ are selected to satisfy the output voltage, and they are constrained to be between V_{DD} and GND. TG switches are preferred to allow the output to have a higher voltage swing.

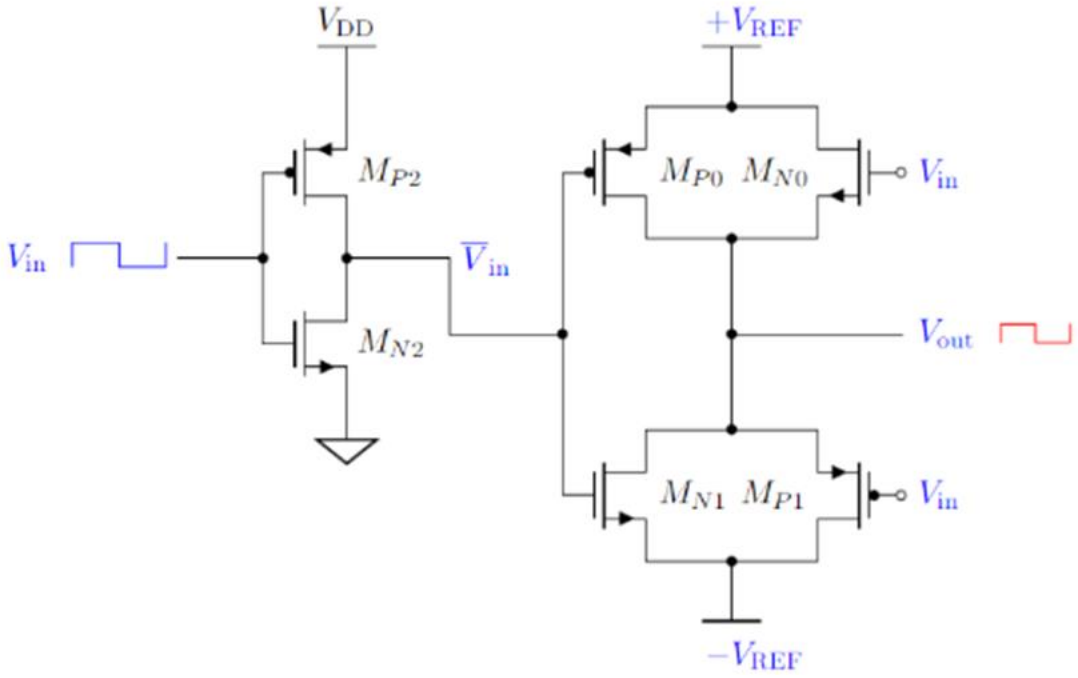

Fig. 2-4. 1-bit DAC comparator schematic [33].

2.2.6 The non-overlapped clock signals generator

A non-overlapped phase clock is commonly used in any SC circuit; thus, the control switches are not closed simultaneously (see Fig. 2-5).

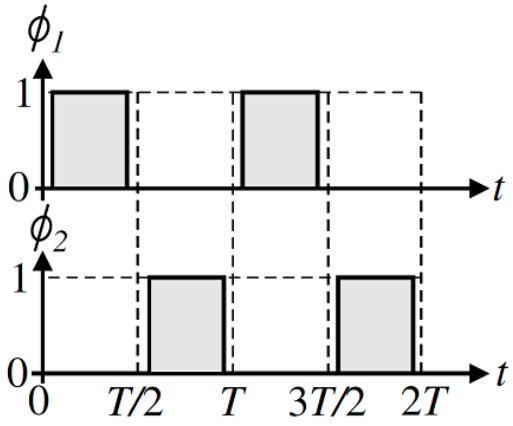

Fig. 2-5. Non-overlapped Phases clock [34].

Non-overlapped clock must be generated from a single clock source,

as is shown in Fig. 2-6.

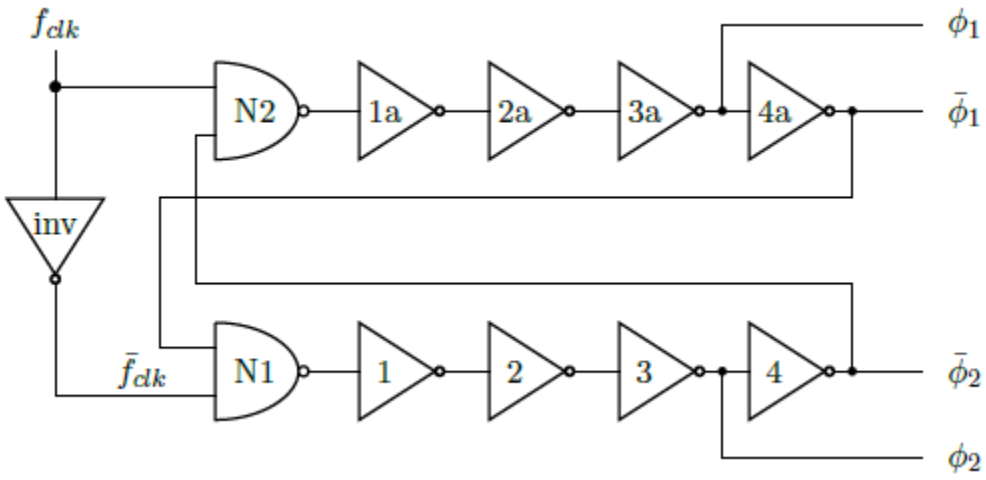

Fig. 2-6. Non-overlapped clock signals circuit generator [35].

Circuit in Fig. 2-6 considers complimentary clock phases $\overline{\phi_1}$ and $\overline{\phi_2}$, as they are required by the $\overline{EN}$ pins of the TG to correctly operate in the SC integrator (Fig. 2-1).

Typical non-overlapped clock signals are depicted in Fig. 2-7.

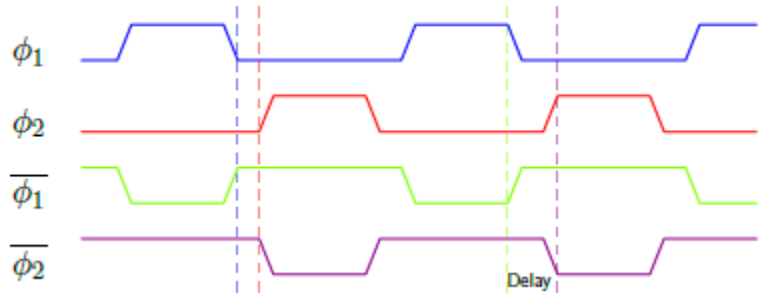

Fig. 2-7. Timing diagram of the resulting non-overlapped clock signals [35].

The transistor implementation of the inverter cell is depicted in Fig. 2-8, it is made by a single NMOS in the low side and a PMOS in high side configuration, with a common gate (Fig. 2-8 a). NAND Gates N_1 and N_2 of Fig. 2-6 are built by two PMOS on the high side and two NMOS on the low side, see Fig. 2-8 b.

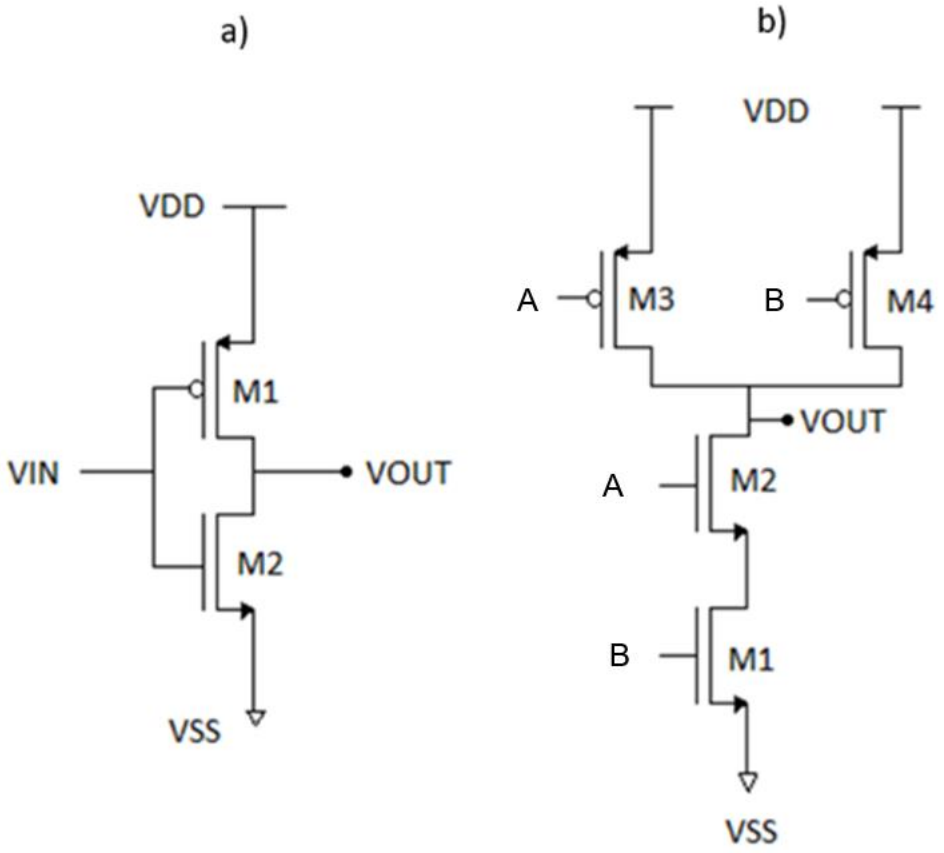

Fig. 2-8. Building blocks of non-overlapped clocks signal generator. a) Inverter cell and b) NAND cell [36].

2.3. Design of a first-order modulator

In this section, the design of each block of the modulator is described, that is the sizing of the MOS transistors of each schematic is also illustrated.

Disclaimer: The design was started in CMOS technology of 130 nm, however, due to changes in the CMOS design technologies available at ITESO, the design had to be migrated into CMOS technology of 45 nm. This migration was achieved by scaling parameters between the technologies (e.g. C_{OX}, V_{DSAT}, V_{TO}, etc), thus obtaining a new W/L for the MOS as starting point, and then fine-tuning into the simulator was made [37].

Table 2 summarizes the parameters of 130 nm and 45 nm CMOS technologies.

Table 2. 130 nm and 45 nm technology parameters [50].

Parameter	*130 nm technology*	*45 nm technology*
Supply voltage V_{DD}	1.2 V	1.1 V
Oxide capacitance C_{OX}	12.8e-15 F/μm^2	14.58e-15 F/μm^2
NMOS Mobility μ_N	450 cm^2/V*s	670 cm^2/V*s
PMOS Mobility μ_P	100 cm^2/V*s	250 cm^2/V*s
NMOS Threshold voltage V_{TON}	0.4 V	0.36 V
PMOS Threshold voltage V_{TOP}	-0.4 V	-0.3 V
Saturation voltage V_{DSAT}	180e-3 V	180e-3 V
I_{bias}	50e-6 A	50e-6 A

2.3.1 Design specifications

Table *3.* Modulator design specifications.

Parameter	*Value*
Input signal frequency	4 kHz
Input signal Amplitude	200 mV V_{pp}
Input offset voltage	0.5 V
Oversampling ratio K	128
Oversampling frequency	1.024 MHz

2.3.2 The input stage of the integrator

The implemented integrator is an enhanced SC circuit. The switches are implemented with TG to have the highest excursion as possible.

To minimize glitches, W/L ratios of transistors in TG switches were appropriately sized and 0.5 pF grounding capacitors (C_6 *and* C_7) were added between the center SC capacitor (see Fig. 2-9).

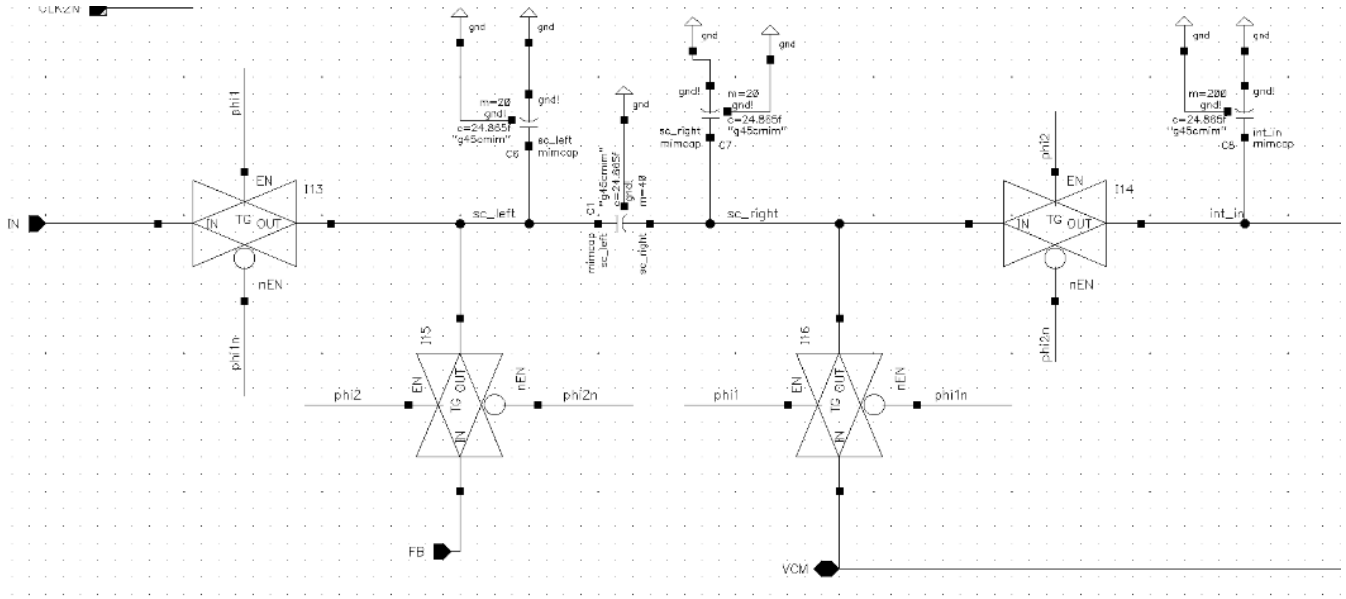

Fig. 2-9. SC circuit with TG for the integrator block.

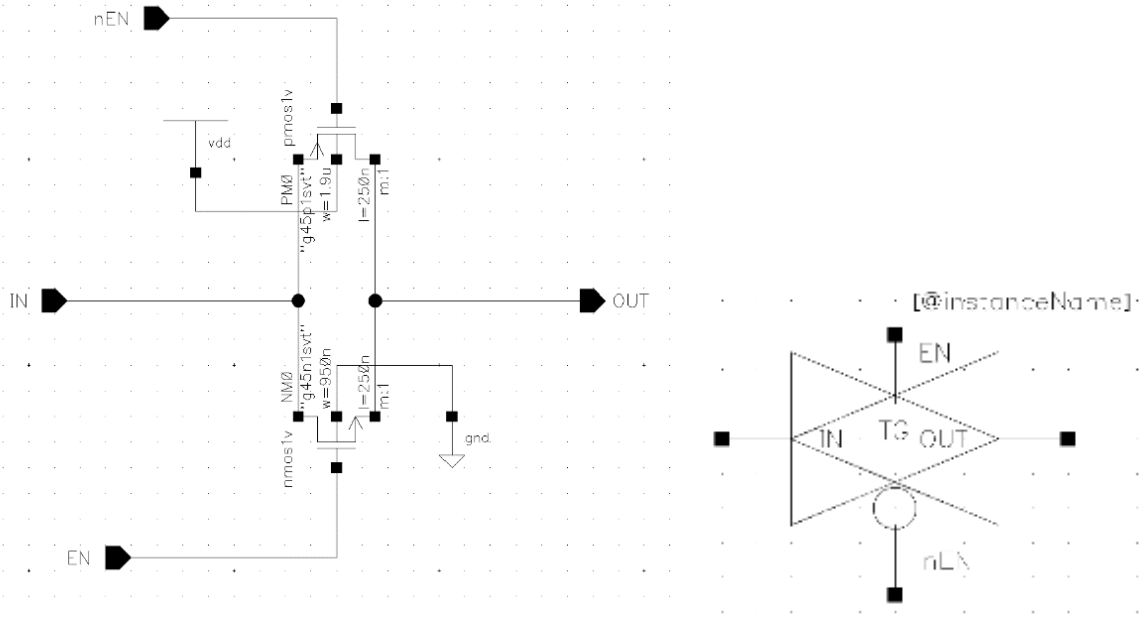

Fig. 2-10. TG schematic(left) and symbol(right).

Fig. 2-9 depicts the integrator SC circuit, implemented with TG for the switches. W/L of PMOS was twice of the NMOS, which is proportional to their mobility.

The SC circuit was built with TGs and tested in open loop with the FB pin tied to GND to verify if the SC circuit could sample adequately a sine wave as input signal (See Fig. 2-11).

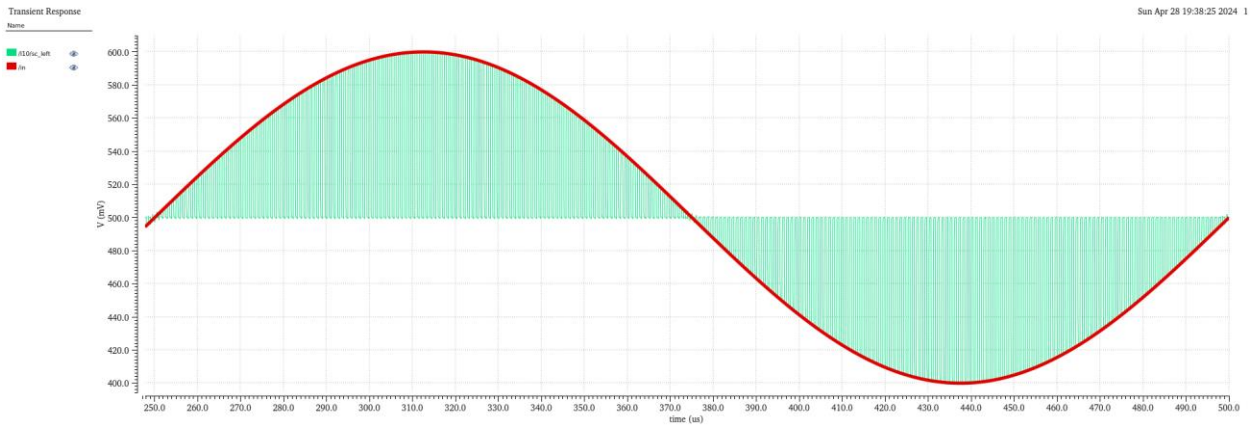

Fig. 2-11. SC circuit response sampling half a sine wave signal with 200 mV peak-peak magnitude, 4 kHz frequency. $F_s = 1.024\ MHz$.

Table 4. W/L size of TG switches in CMOS 45 nm.

Transistor	$\frac{W}{L}(\mu m)$
NMOS	0.95/0.25
PMOS	1.9/0.25

The input sine signal (red signal) depicted on Fig. 2-11 is mounted with an offset of 0.5 V ($V_{DD}/2$). The SC circuit of the modulator samples all the area beneath the sine signal down to the offset voltage (green signal).

2.3.3 The two-stage self-cascode OTA

A two-stage OTA was designed to obtain a high gain with a fair GBW. The first stage was a self-cascode OTA with the design parameters specified in Table 5 and Table 6 (using process parameters of CMOS 130 nm technology).

Table 5. Design specification for the self-cascode OTA stage for 130 nm CMOS.

Parameter	*Value*
V_{DD}	$1.2\ V$
V_{ICM}	$0.5 * V_{DD}$
V_{OCM}	$0.5 * V_{DD}$
P_{Dmax}	$100\ \mu W$
K_n	$200\ \mu A/V^2$
$A_{VDC}(dB)$	$40\ dB$
SR	$10\ V/\mu s$
GBW	$10\ MHz$
C_L	$1\ pF$
V_{TN}	$0.35\ V$

P_{Dmax} specification on Table 5 was selected to tackle problem statement of section 2.1 to fit consumption on portable devices. The first stage of the OTA was selected to have this $A_{VDC}(dB)$ as the V_{pp} of the input signal is quite low. GBW was selected to have 10 MHz to enable the modulator to have an oversampling ratio (K) up to 512. A SR up to 10 V/us enables fast transitions in the input waveform, e.g. a square signal.

Table 6. Design specification for OTA's current mirror.

Parameter	*Value*
$I_{ref} = I_B$	$12.57\ \mu A$
V_{dsat}	$200\ mV$
$I_o = \frac{1}{2} I_{ref}$	$6.2832\ \mu A$
λ	0.1
V_{th}	$0.35\ V$

I_{Bmax} calculation by knowing P_{Dmax} specification on equation (2.4).

$$I_{Bmax} = \frac{100\ \mu W}{1.2\ V} = 83.33\ uA$$

Solving for g_m from equation (2.5) and substituting C_L from Table 5,

$$g_m = 2\ (3.1416 * 10\ MHz) * (1\ pF)$$

$$g_m = 62.83\ \mu S$$

By substituting $A_{VDC}(dB)$ from Table 5 and solving with:

$$A_V = 10^{\frac{40\ dB}{20}} = 100$$

Substituting A_V in equation (2.6) and solving for R_O,

$$R_O = \frac{100}{62.83\ \mu S}$$

$$R_O = 1.592\ M\Omega$$

Where $g_{m1} * r_{oCAS}$ is the cascode gain. Thus:

$$A_{v-selfcascode} = g_{m1} * r_{oCAS} = 62.83\ \mu s * 159.2\ k\Omega = 10$$

By substituting values on equation (2.8) and solving for m:

$$m = \frac{1.592\ M\Omega}{159.2\ k\Omega} + 1 = 11$$

I_B calculation by knowing the GBW specification (implicitly through g_m)

By substituting $V_{Dsat} = 200\ mV$ in equation (2.5):

$$I_B = 62.83\ \mu S * 200\ mV$$

$$I_B = 12.566\ \mu A$$

Isolating I_B from equation (2.14) and substituting SR from Table 5:

$$I_B = 1\ pF * 10\ V/\mu s$$

$$I_B = 10\ uA$$

$I_B = 12.56\ \mu A$ is the bias current that allow us to fulfill the three specifications the GBW of 10 MHz, minimum SR of 10 V/µs and power consumption less than 100 µW. Next, this current value will be used to determine the appropriate transistor sizes.

From equation (2.14) and values in Table 5, we get $\left(\frac{W}{L}\right)_P$:

$$\left(\frac{W}{L}\right)_P = \frac{12.566\ \mu A}{(35\ \mu A/V^2)(1.2\ V - 0.792\ V - 0.2\ V)^2}$$

$$\left(\frac{\mathrm{W}}{\mathrm{L}}\right)_{\mathrm{P}} = 8.3$$

Similarly, from equation (2.19), we get for $\left(\frac{W}{L}\right)_N$:

$$\left(\frac{W}{L}\right)_N = \frac{62.83\ uS^2}{200\ \mu A/V^2 * 12.566\ \mu A}$$

$$\left(\frac{\mathrm{W}}{\mathrm{L}}\right)_{\mathrm{N}} = 1.5708$$

By considering $L_N = L_P$ = 2∗ L_{min} = 2*120 nm = 0.24 µm, and solving for equation (2.16) and (2.17), the widths of gates can be calculated as follows.

$$W_{N1} = W_{N2} = \left(\frac{W}{L}\right)_N * L_N = (1.5708)(0.24\ \mu m) = 0.377\ \mu m$$

$$W_{P1} = W_{P2} = \left(\frac{W}{L}\right)_P * L_P = (8.3)(0.24\ \mu m) = 1.992\ \mu m$$

For the proper sizing of the self-cascode transistors, the multiplicity *m* obtained together with the W_N *and* W_P, dimensions on the cascode MOSFETs are:

$$W_{NCAS} = m * W_N = 11 * 0.377\ \mu m = 4.147\ \mu m \quad (2.29)$$

$$W_{PCAS} = m * W_P = 11 * 1.992\ \mu m = 21.912\ \mu m \quad (2.30)$$

With the OTA's current mirror specifications in Table 6, and from equation (2.18),

$$\left(\frac{W}{L}\right)_{N3} = \frac{12.5664\ \mu A}{(200\ \mu A/V^2)(200\ mV)^2(1.055)}$$

$$\left(\frac{W}{L}\right)_{N3} = \left(\frac{W}{L}\right)_{N4} = 8.5$$

By solving equation (2.21) for V_{GS3} and V_{GS5},

$$V_{GS3} = \sqrt{\frac{2 * 12.57\ \mu A}{200\ \mu/V^2 * 14.58}} + 0.35\ V = 0.442\ V$$

$$V_{GS5} = \sqrt{\frac{2 * 12.57\ \mu A}{200\ \mu/V^2 * 1.4166}} + 0.35\ V = 0.657\ V$$

By replacing V_{GS3} and V_{GS5} in equation (2.22):

$$R = \frac{1.2\ V - 0.442\ V - 0.657\ V}{12.57\ \mu A} = 8.035\ k\Omega$$

For the second OTA stage, a common-source configuration was implemented to increase the total gain of the OTA by using a PMOS cascode arrangement.

Total OTA gain is obtained by multiplying the first self-cascode OTA by the common-source stage gains.

$$A_{total} = A_{V-OTA} * A_{V-CS} \tag{2.31}$$

By using the self-cascode technique for the common-source stage, A_{V-CS} is also determined by the equation (2.7):

$$A_{V-FC} = g_{m-selfcascode} * R_{o-selfcascode} = 62.83\ \mu S * 159.2\ k\Omega = 10 \tag{2.32}$$

Final gain A_{total} is obtained by substituting A_{V-FC} from equation (2.32) and from A_{V-OTA} from equation (2.31) in equation (2.33).

$$A_{total} = 10 * 100 = 1000 = 60\ dB \tag{2.33}$$

This design was done in 130 nm CMOS technology, then it was migrated to 45 nm by using the technology parameters of Table 2, and after fine-tuned the design in the simulator, the following OTA schematic fulfilled the design parameters (Fig. 2-12):

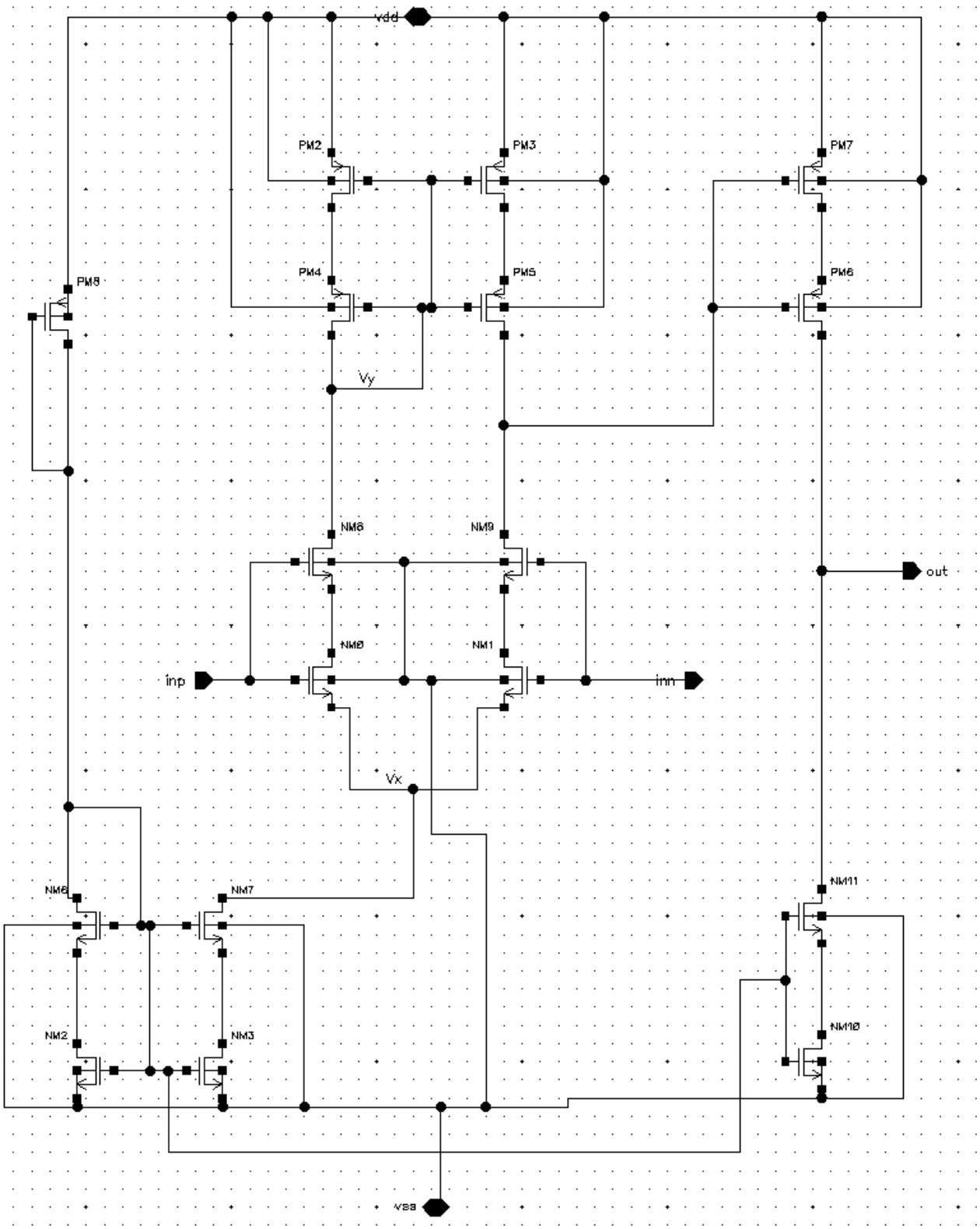

Fig. 2-12. Two-stage self-cascode OTA schematic.

In Fig. 2-12 the resistor obtained through equation (2.26) was replaced by PMOS PM8, which is connected as a diode, to reduce layout area.

$$R = r_{ds} = \frac{1}{K_p \left(\frac{W}{L}\right)(V_{GS} - V_T)}$$

V_{GS} for PM8 = 450 mV.

Table 7 summarizes the final sizing of the OTA transistors.

Table 7. Two-stage self-cascode transistors sizing of 45 nm CMOS.

Transistor	$\frac{W}{L}(\mu m)$	Multiplicity *"m"*
NM0, NM1	1.5/0.25	1
NM8, NM9	15/0.25	1
PM2, PM3, PM8	3/0.25	1
PM4, PM5	30/0.25	1
PM7	10/1	1
PM6	16/1	6
NM2, NM3, NM10	1/0.25	1
NM6, NM7, NM11	10/0.25	1

The AC response for the designed OTA is depicted on Fig. 2-13.

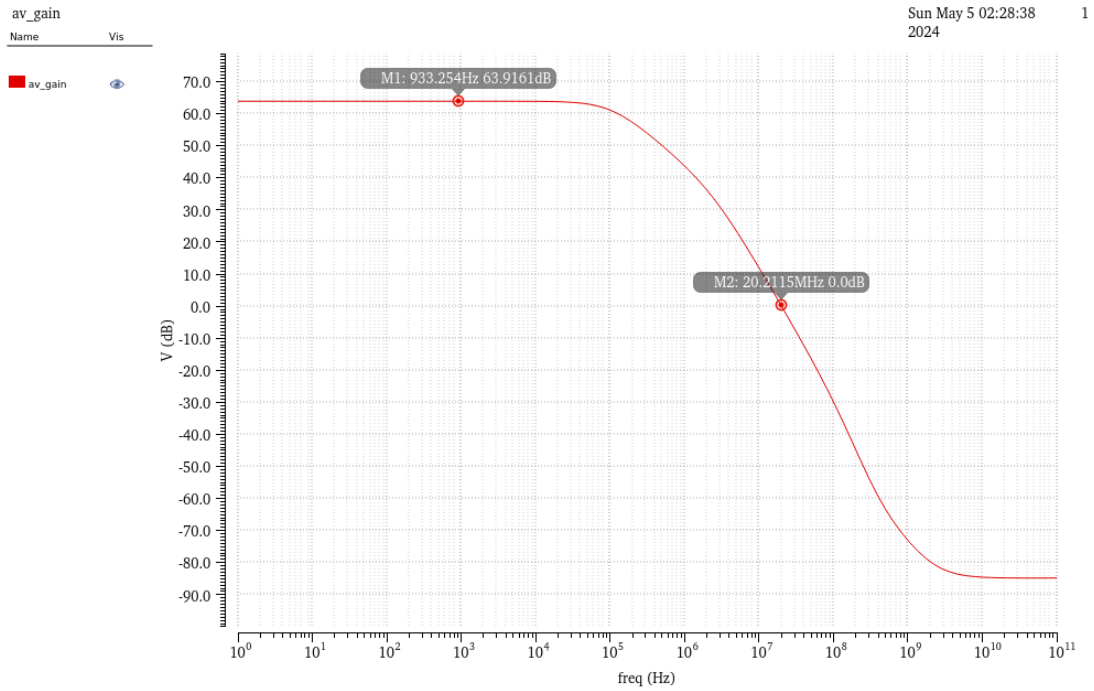

Fig. 2-13. Frequency response of Two-stage self-cascode OTA.

It can be appreciated that the $A_{VDC}(dB)$ gain in the frequency response of Fig. 2-13 is 63.91 dB, which fulfills the specification on equation (2.50). The GBW, which is measured at unity gain (0 dB), is 20.21 MHz, which also fulfills the specification on Table 5.

2.3.4 The SC integrator

The SC integrator comprehends the SC circuit of section 2.3.2 followed by the two-stage self-cascode OTA of section 2.3.3. The schematic is depicted on Fig. 2-14.

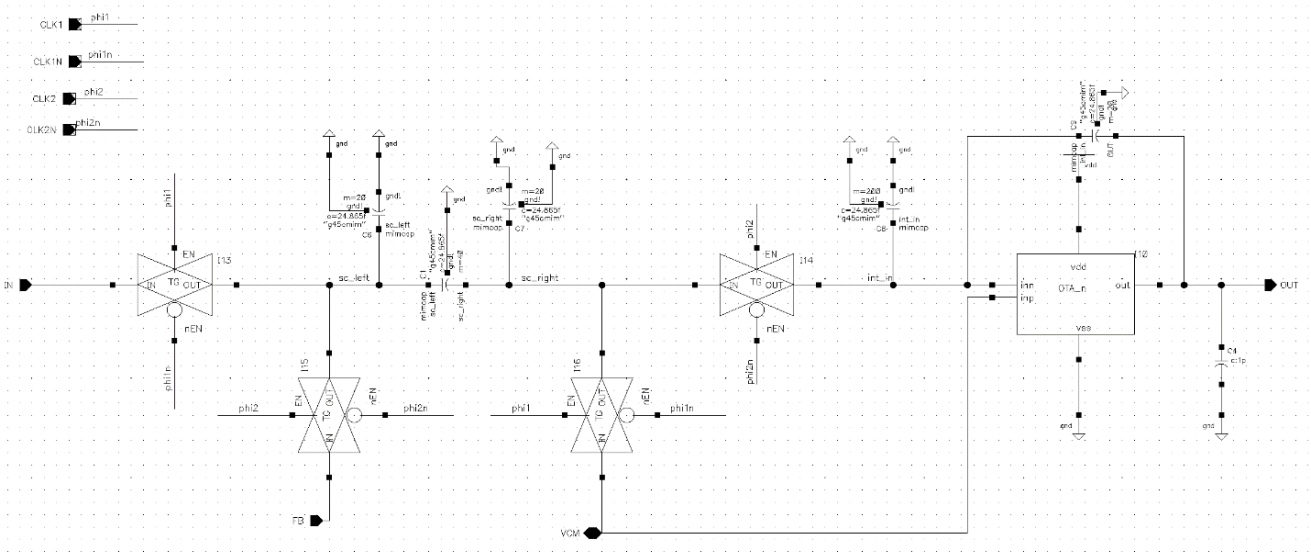

Fig. 2-14. SC Integrator schematic.

The SC Integrator was tested under the same conditions of the SC circuit on Fig. 2-9, where the circuit has an offset voltage of 0.5 V in open loop, with the FB pin tied to GND.

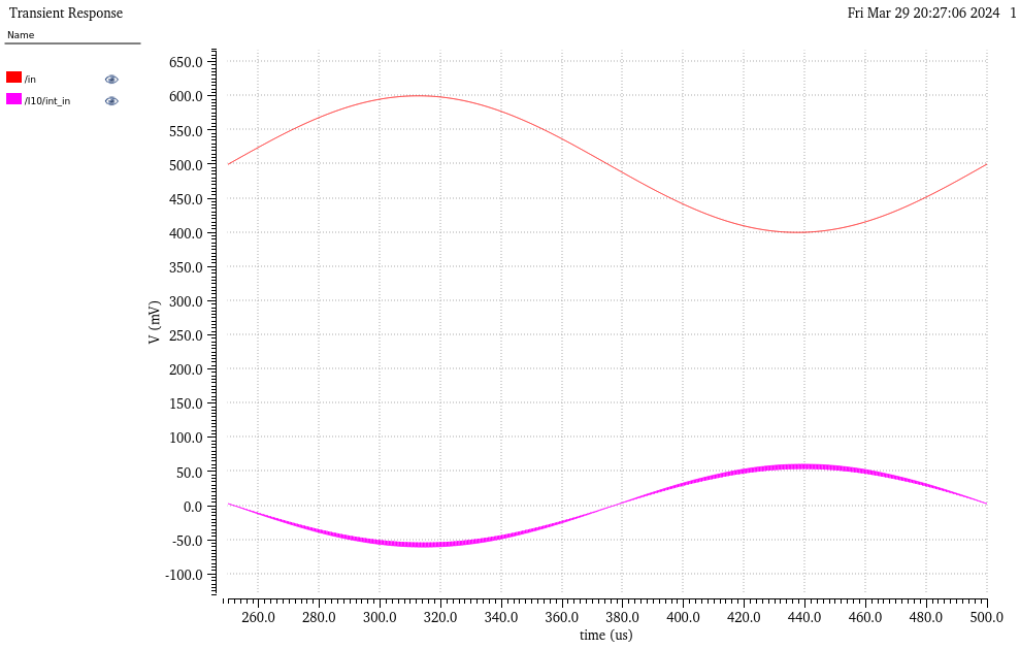

Fig. 2-15. SC Integrator response sampling a sine wave signal with 200 mV peak-peak magnitude, 4 kHz frequency.

In Fig. 2-15 it can be observed how the SC Integrator output has a sine wave output with the same frequency but with a 180° phase difference from the input, thus performing the integrator operation. Additionally, the magnitude has decreased by a half to 100 mV V_{pp}, and the offset has been eliminated. The integrator operation also induces some noise, by thickening the signal in both positive and negative cycles.

2.3.5 The comparator

As the two-stage comparator explored on section 2.2.4 is a simple OTA with an inverter on the second stage, the same NMOS and PMOS dimensions used on the self-cascode OTA were used as starting point, but without the cascode configuration.

The schematic of the comparator is shown in Fig. 2-16.

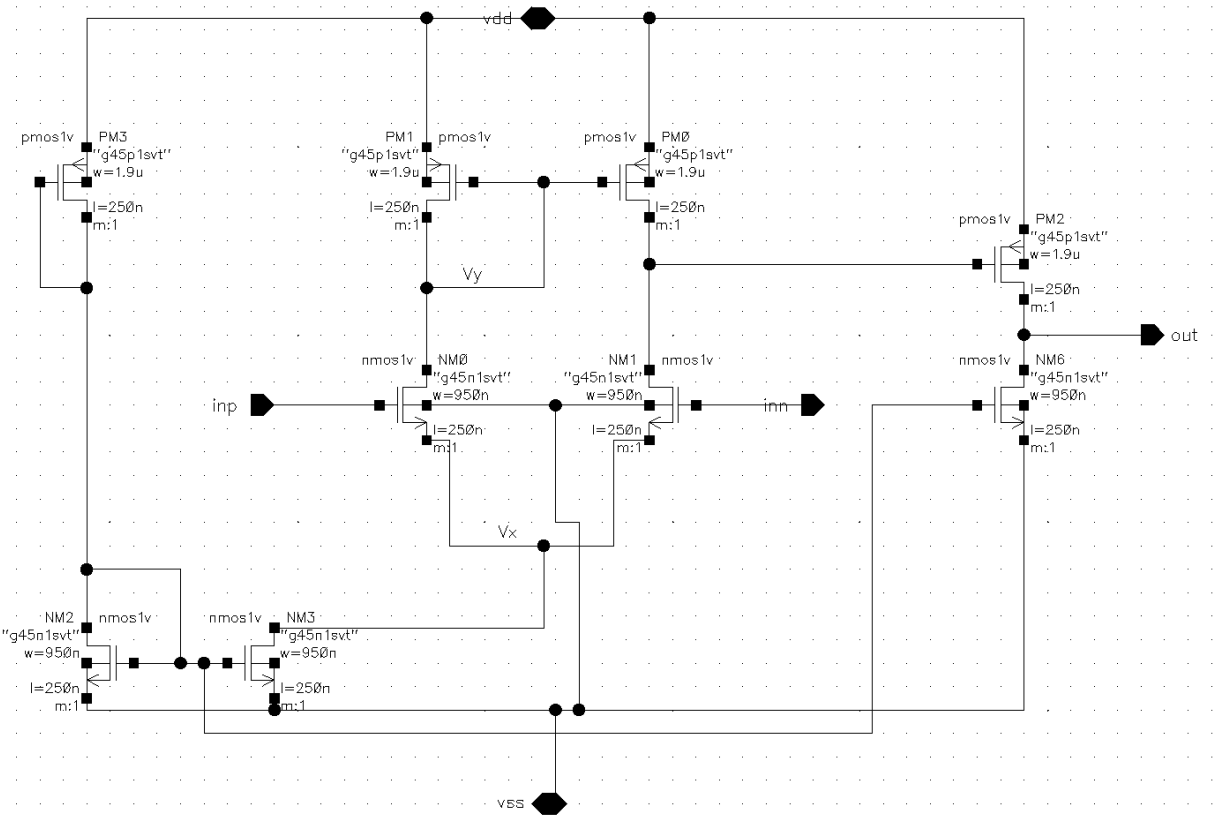

Fig. 2-16. Comparator schematic.

Table 8 summarizes sizing of the comparator transistors.

Table 8. Comparator transistors sizing of 45 nm CMOS.

Transistor	$\frac{W}{L}(\mu m)$
NM0, NM1	0.95/0.25
PM0, PM1, PM2, PM3	1.9/0.25
NM2, NM3, NM6	0.95/0.25

The comparator was tested with the negative input pin tied to V_{CM} = 0.5 V which is V_{ref}, and the positive input pin to a sinusoidal wave with 4 kHz frequency and 1 V_{PP} mounted with an offset voltage of 0.5 V. The output of the comparator is depicted on Fig. 2-17.

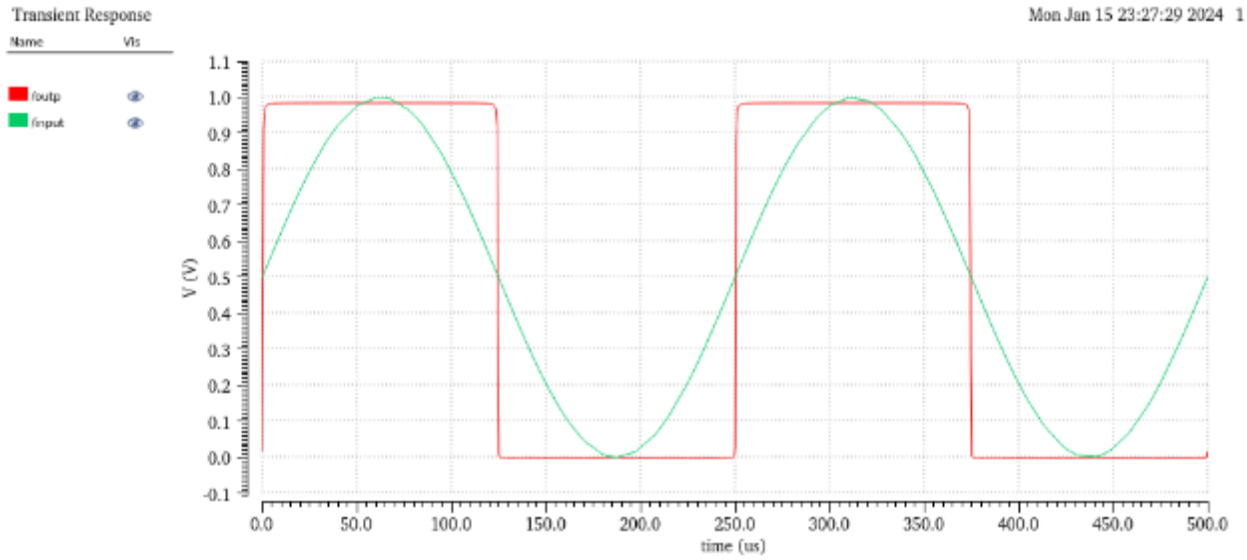

Fig. 2-17. Comparator response comparing a sine wave signal with 1 V peak-peak magnitude, 4 kHz frequency to V_{CM} = 0.5 V.

In Fig. 2-17 the comparator is demonstrating an expected behavior as the output (red square wave) is toggling states as soon as the input sine wave (green wave) gets to 0.5 V, which is the reference that the comparator is monitoring on the negative pin.

2.3.6 The 1-bit DAC

The 1-bit DAC was implemented as shown in section 2.2.5. Its schematic is depicted on Fig. 2-18. The same TG transistors sizing of the SC circuit in Table 4 was reused in this block.

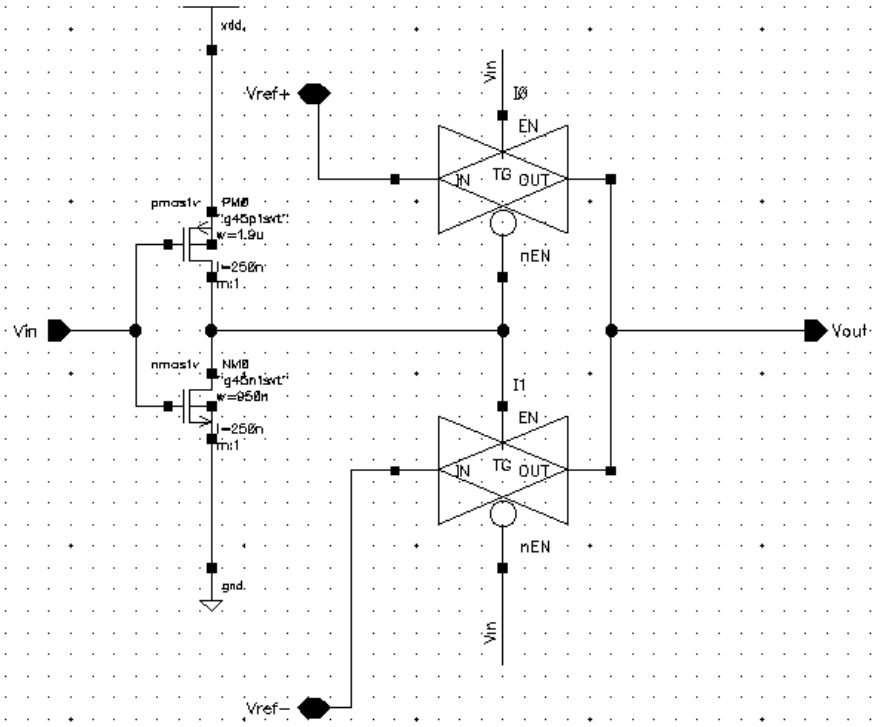

Fig. 2-18. 1-bit DAC schematic.

The 1-bit DAC was tested with a square wave as input with 1 V magnitude, but with $V_{ref+} = 600$ mV and $V_{ref-} = 400$ mV to test its response as voltage translator.

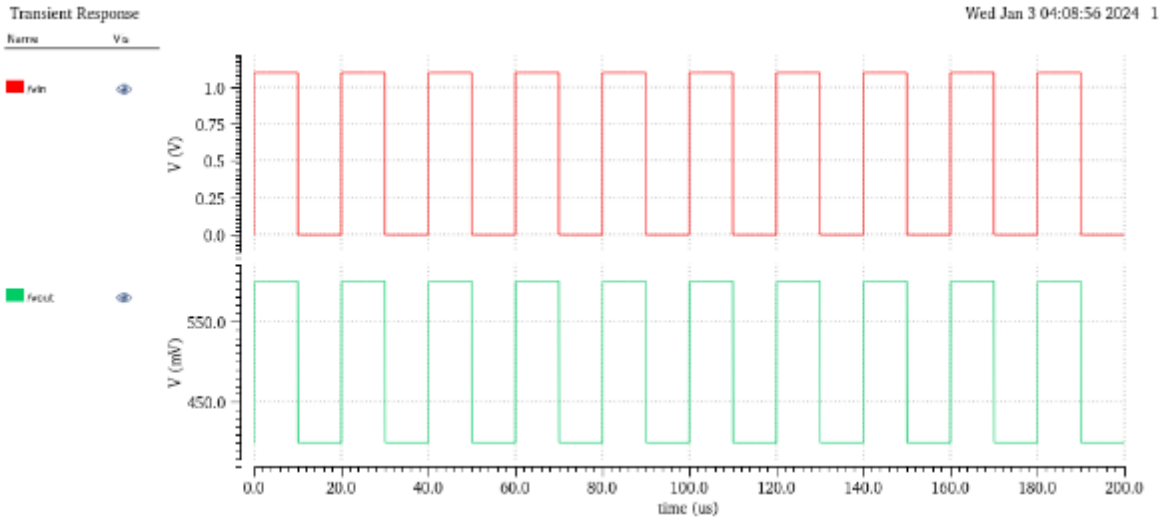

Fig. 2-19. 1-bit DAC response. Input is a square wave with V_{PP} = 1 V with 50 kHz frequency. V_{REF+} = 600 mV and V_{REF-} = 400 mV.

In Fig. 2-19, it is evident that the output signal from the 1-bit DAC shares the same square waveform and frequency as the input signal, but the output signal has a $V_{p+} = 600$ mV and $V_{p-} = 400$ mV, which are the reference voltages previously set.

2.3.7 The non-overlapped clocks signal generator

The propagation delay time of basic CMOS inverter is directly related to the W_p/W_n relation of the implemented MOSFET. A study presented in [38] demonstrated that the higher is this relationship, higher is the propagation delay time (Fig. 2-20).

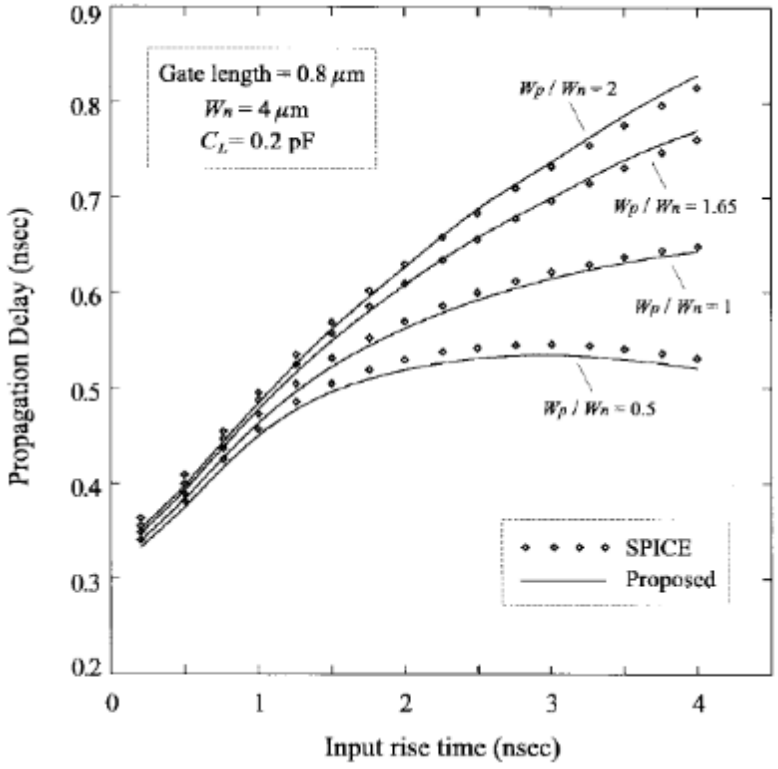

Fig. 2-20. Propagation delay time of an inverter for different W_p/W_n values. [38]

For example, using a $W_p/W_n = 0.5$, the propagation delay time is 1.6 times lower than an implementation with $W_p/W_n = 2$ (Fig. 2-20).

The delay reduction in $W_p/W_n = 0.5$ is caused by the asymmetry in the inverter circuit, which creates a logic threshold voltage sufficiently lower than $V_{DD}/2$, where the delay is measured.

According to [38], it is possible to control the overlap in the clock signals of Fig. 2-5, by appropriately sizing the W sizes of the transistors.

The topology described in section 2.2.3 (The OTA) was implemented with transistors, with the only change that an extra inverter was added at the output as the immediate signal after the delay chain had a noticeable overshoot while changing state. The "Delay Chain" block of I150 and I151 of the schematic in Fig. 2-21 contains 16 inverters connected as ring oscillators, which generates the non-overlapping time between the generated clocks.

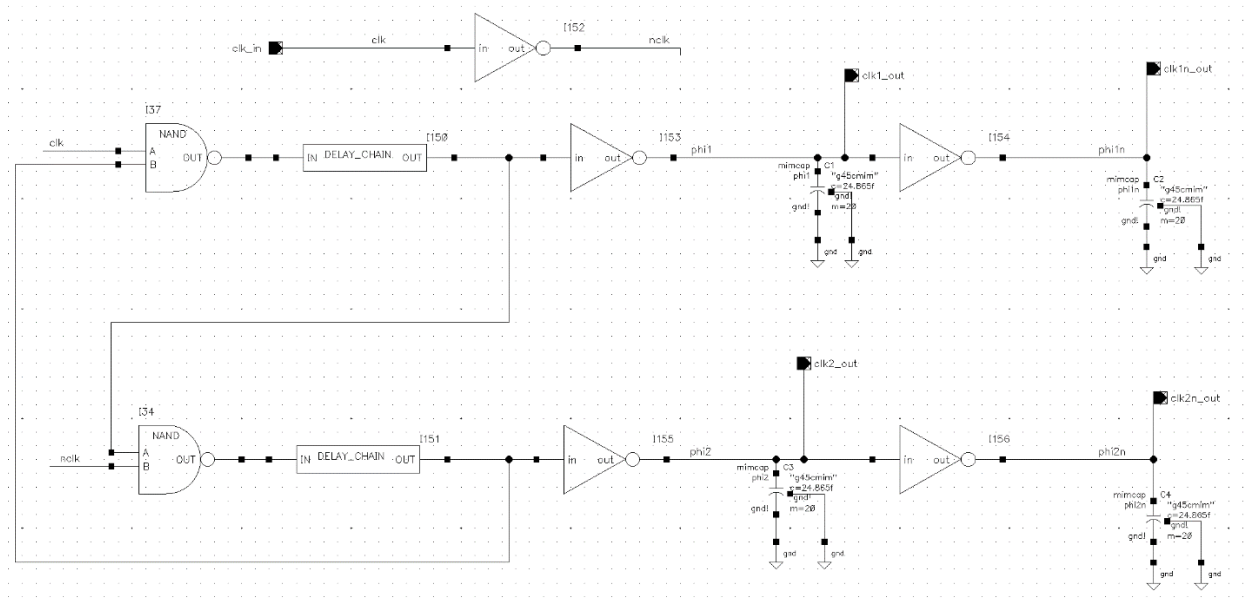

Fig. 2-21. Non-overlapped clocks generator schematic.

The ratio W_p/W_n of inverter cell of the non-overlapped clock generator was defined according to results shown in Fig 2-20, several W_p/W_n were tested with the intention to select an appropriate W_p/W_n that could generate an acceptable grade of non-overlapping between the generated clocks, but also to not oversize the circuit and use unnecessary chip area.

The generated clocks are depicted in Fig. 2-22 to Fig. 2-25. The blue and red clocks are the "clk1_out" and "clk2_out" from the schematic in Fig. 2-21. The blue and magenta curves are the complimentary clocks mainly used for the TG's.

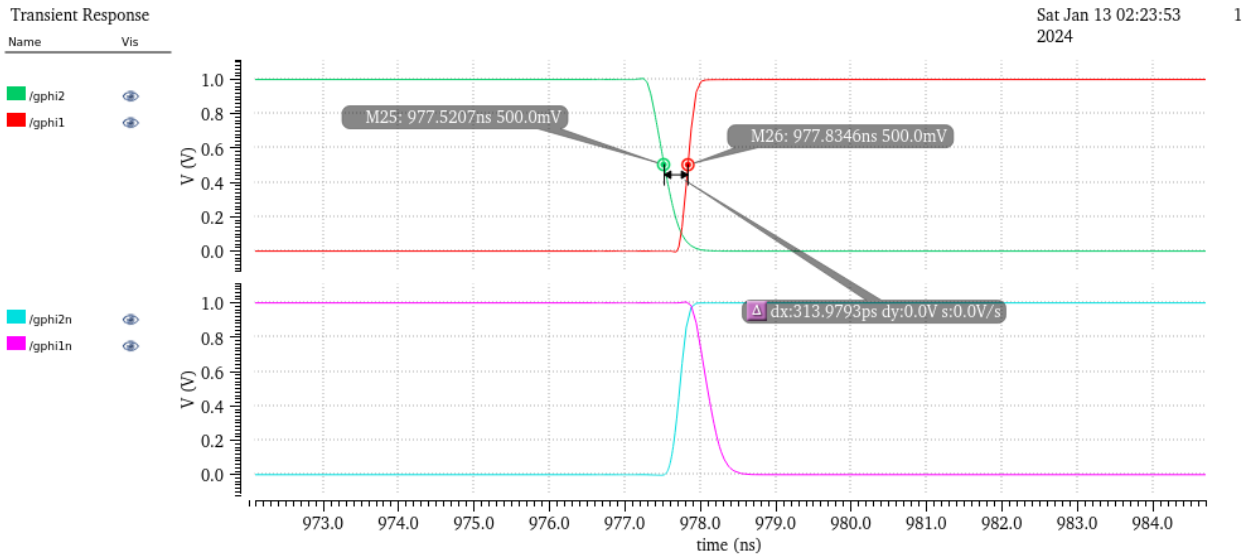

Fig. 2-22. Non-overlapped clocks generated with a square wave input with V_{PP} = 1 V and 1.024 MHz frequency. $W_p/W_n = 1$.

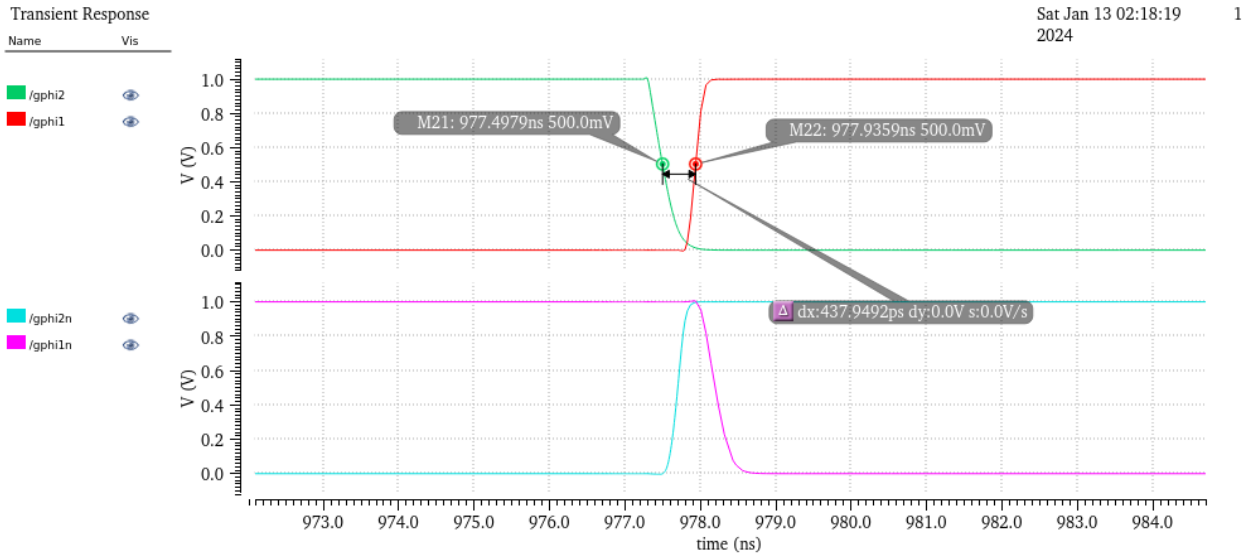

Fig. 2-23. Non-overlapped clocks generated with a square wave input with V_{PP} = 1 V and 1.024 MHz frequency. $W_p/W_n = 4$.

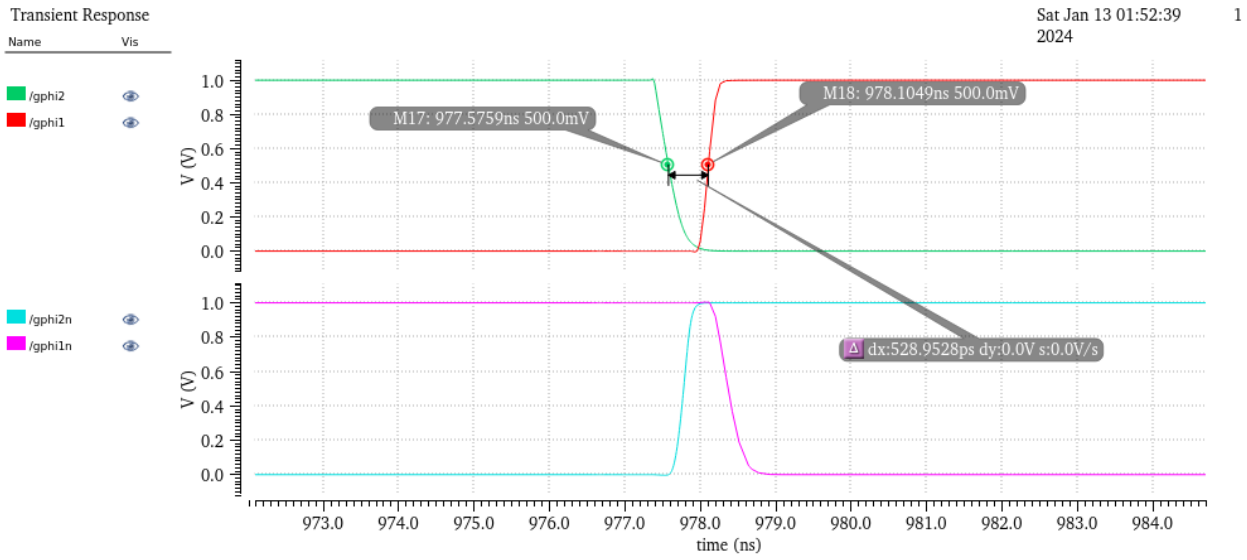

Fig. 2-24. Non-overlapped clocks generated with a square wave input with V_{PP} = 1 V and 1.024 MHz frequency. $W_p/W_n = 6$.

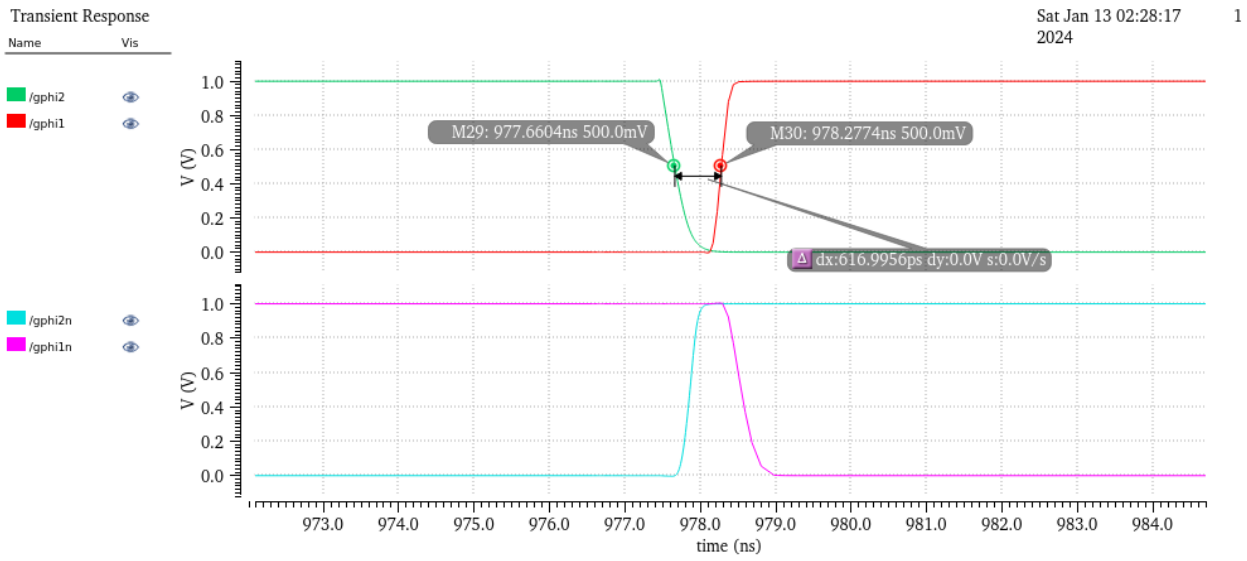

Fig. 2-25. Non-overlapped clocks generated with a square wave input with V_{PP} = 1 V and 1.024 MHz frequency. $W_p/W_n = 8$.

.

Table 9. Comparison of the W_p/W_n transistors relation and the generated propagation delay.

W_p/W_n	Propagation delay
1	313.97 ps
2	348.04 ps
4	437.94 ps
6	528.95 ps
8	616.99 ps

After analyzing Figs. 2-22 to 2-25 and its generated propagation delays of Table 9, $W_p/W_n = 6$ was chosen as it had the best ratio between the generated delay and the non-overlapping of the clock signals when toggling to a low state, whereas with a $W_p/W_n \leq 4$, the clock signals were still overlapping when toggling to a low state. In the other hand, $W_p/W_n = 8$ had unnecessarily too much propagation delay.

The inverters I152, I153, I154, I155 and I156 had a different sizing as they act as buffers to strengthen the generated clocks signals.

The NAND logic gates implemented in I34 and I37 have the schematic depicted in Fig. 2-26.

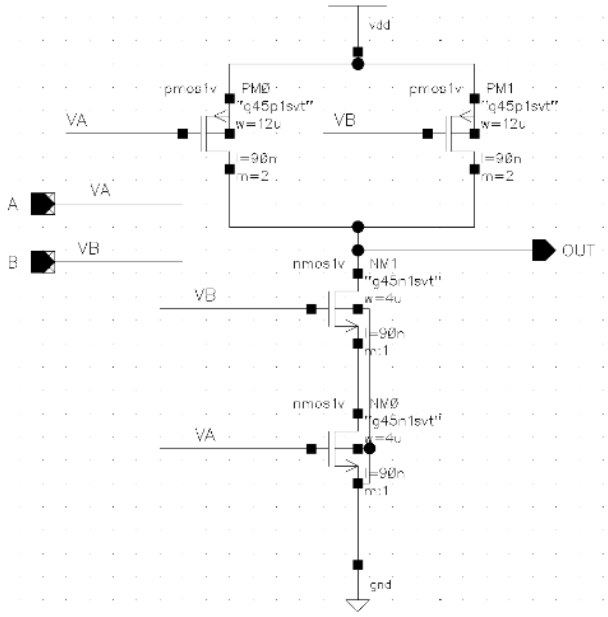

Fig. 2-26. NAND logic gate schematic.

The final transistors dimensions implemented on the non-overlapping clocks generator are shown in Table 10.

Table 10. Non-overlapped clocks generator transistors sizing of 45 nm CMOS.

Transistor	$\frac{W}{L}$ (μm)	Multiplicity "m"
NM_{NAND}	4/0.09	1
PM_{NAND}	12/0.09	2
NM_{INV}	12/0.09	1
PM_{INV}	36/0.09	1
NM_{DELAY}	2/0.09	1
PM_{DELAY}	12/0.09	1

2.4. Simulation results of first order modulator

After having designed the major internal blocks of the modulator, they were put in a closed loop system and was tested under different oversampling ratios *K*. Fig. 2-27 depicts how the SC Integrator and the Comparator are connected in the direct loop, and how the 1-bit DAC is connected in the feedback loop. The DAC and Comparator schematics were replaced by the symbols shown in Fig. 2-27.

This block receives the non-overlapped clocks designed in section 2.3.7 (The non-overlapped clocks signal generator), and the offset voltage of 0.5 V, which is the voltage that the input sine wave is mounted on, and V_{REF+} = 600 mV and V_{REF-} = 400 mV, which are the max and min amplitude values of the input sine wave for the feedback input of the SC Integrator. The schematic of the modulator can be depicted in Fig. 2-27 and its symbol on Fig. 2-28.

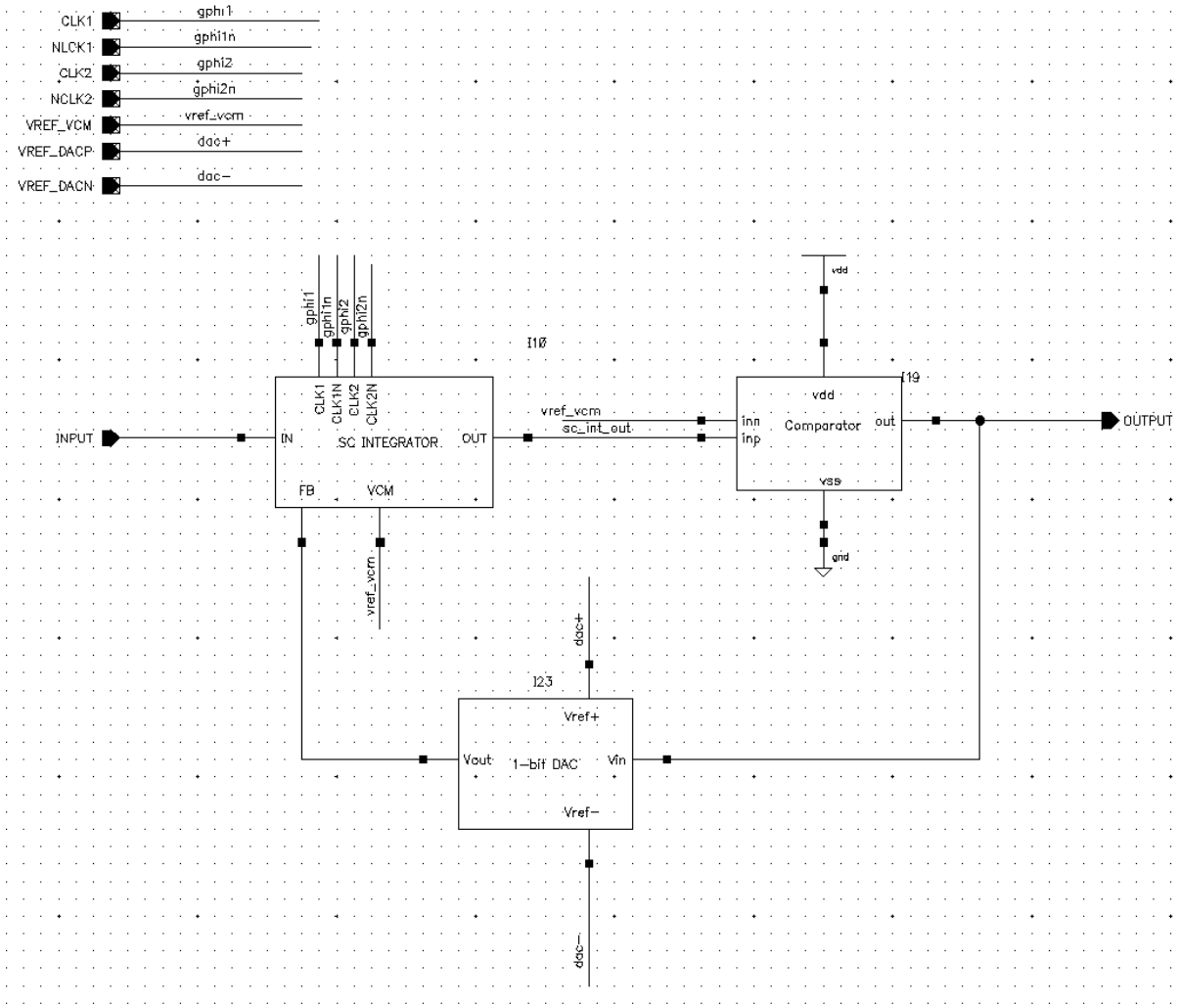

Fig. 2-27. First order ΣΔ modulator schematic.

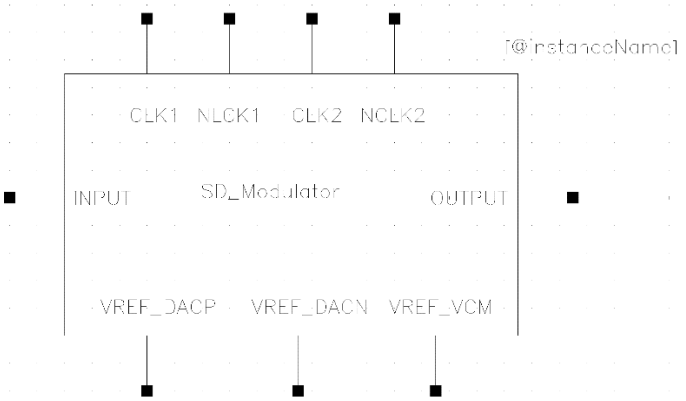

Fig. 2-28. First ΣΔ modulator symbol.

The closed loop system was tested with different oversampling ratios K, where:

$$K = \frac{F_s}{f_n} = \frac{F_s}{2 * f_{in}} \tag{2.34}$$

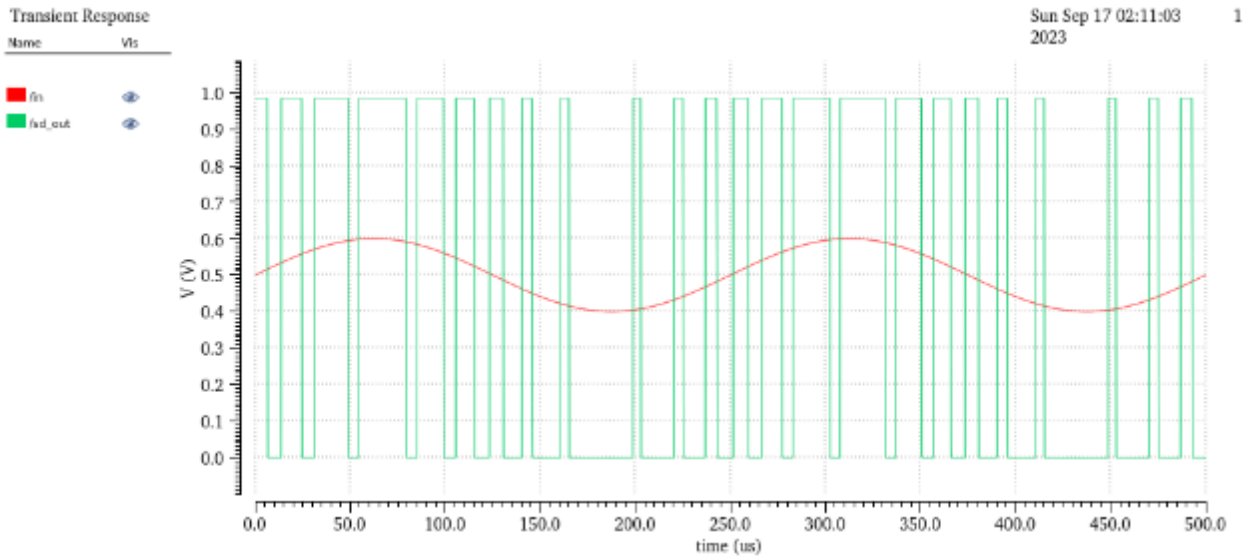

Fig. 2-29. First order ΣΔ modulator response for the first 2T. $f_{in} = 4\ kHz,\ F_s = 512\ kHz$ *, K = 64.*

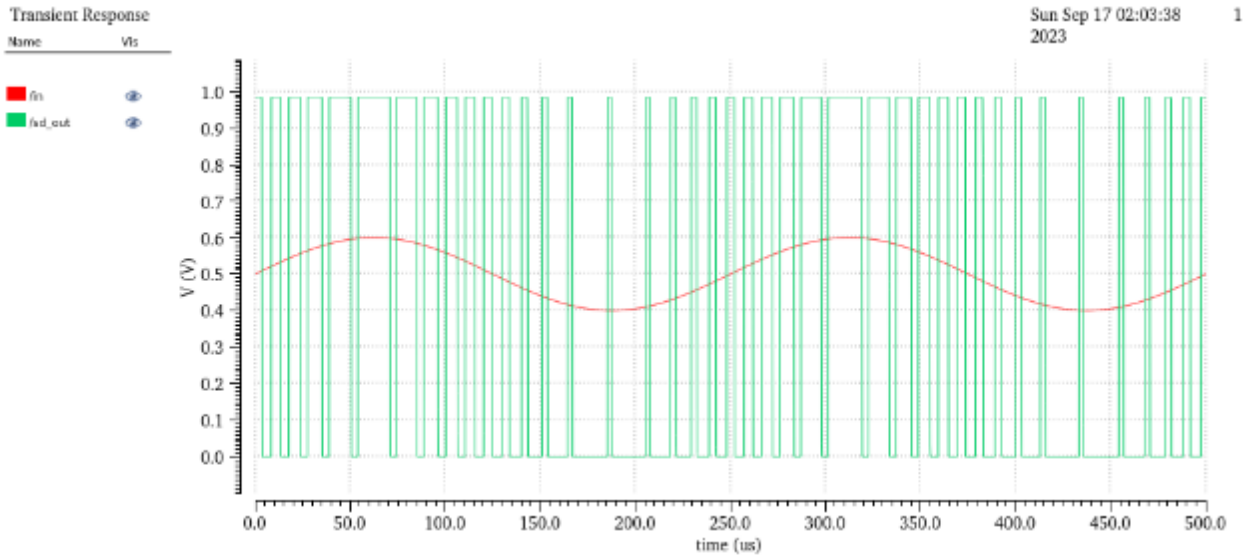

Fig. 2-30. First order ΣΔ modulator response for the first 2T. $f_{in} = 4\ kHz,\ F_s = 1.024\ MHz$ *, K = 128.*

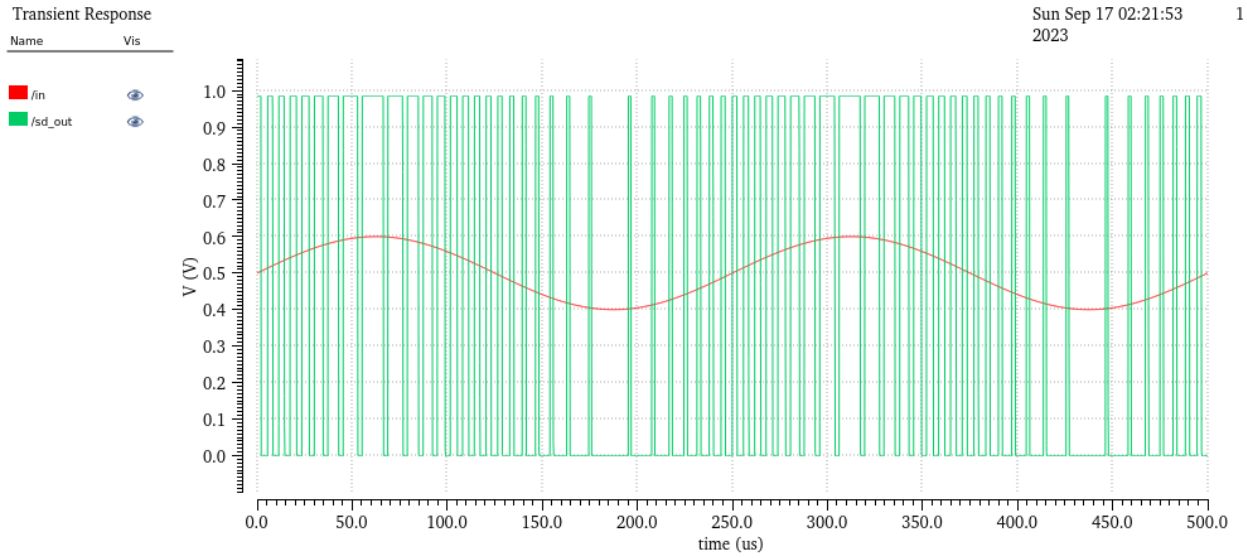

Fig. 2-31. First order ΣΔ modulator response for the first 2T. $f_{in} = 4\ kHz,\ F_s = 2.048\ MHz$ *,* $K = 256$.

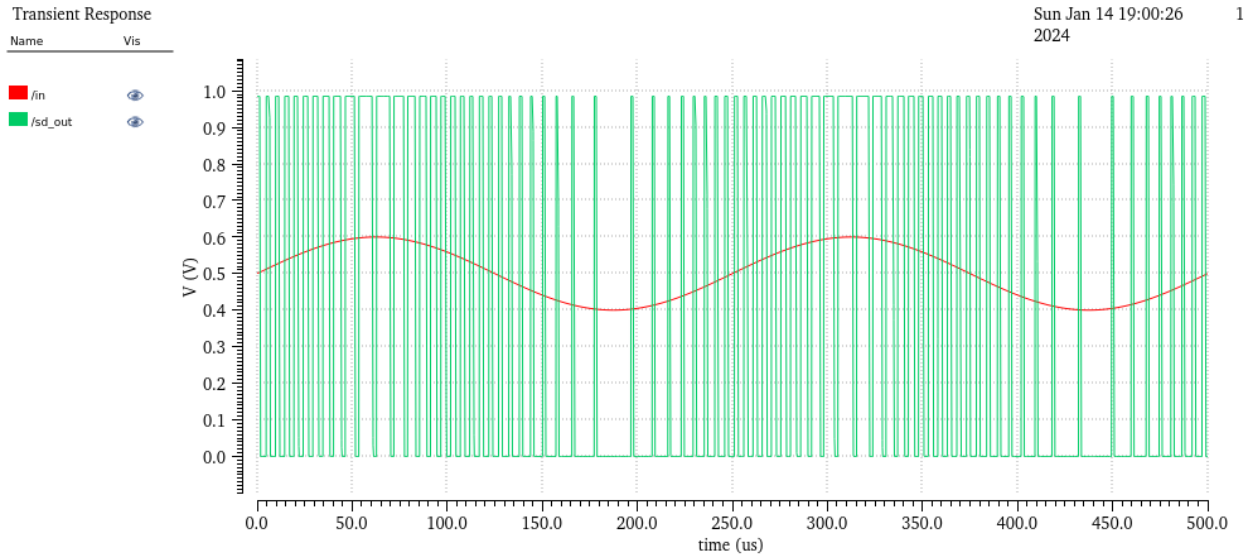

Fig. 2-32. First order ΣΔ modulator response for the first 2T. $f_{in} = 4\ kHz,\ F_s = 4.096\ MHz$ *,* $K = 512$.

After analyzing ΣΔ modulator response Figs. 2-29 to 2-32, it was noted that with K = 256 and K = 512 there wasn't a major difference in modulation, just brief extra transitions on the high side of the sine wave but wouldn't justify implementing an oversampling frequency $F_s = 4.096\ MHz$.

On the other hand, with a K = 64 it was noted that as the transitions are very few, it could lack some information for the Decimation filter.

A very high K increases dramatically the bit-length of the Decimation filter, (which will be discussed in the next section), thus K = 128 was chosen as it has the best tradeoff between the amount of modulation transitions throughout the sine wave, and it has a fair oversample frequency F_s that won't overcomplex the decimation filter.

3. The Decimator Filter

Due to the significant quantization noise caused by the high oversampling frequency of the ΣΔ modulator discussed in the previous chapter, it is necessary to reduce this noise by "decimating" the output. Decimation involves resampling the filtered output at a lower rate (down sampling) to eliminate any redundant signal information introduced during oversampling.

In practice, this process usually involves applying a low-pass filter to the signal followed by downsampling to reduce its effective sampling rate. A simple form of decimation is achieved through an averaging circuit or alternatively using a sync filter. One common implementation method is through an accumulate and dump circuit, which serves as both a sync filter and a digital low-pass filter. Cascading multiple decimation stages can improve stop-band attenuation, although this increases bandwidth limitations.

A widely used filter type for decimation is the Cascaded Integrator-Comb (CIC) filter.

3.1. CIC Decimation Filter Overview

The CIC filter is composed of integrator and differentiator stages that carry out digital low-pass filtering and decimation functions.

This filter offers cost-effective hardware implementation as it only utilizes full adders and delay elements, while maintaining superior filtering characteristics.

The CIC filter first functions as an averaging filter and then finishes with the decimation operation. A simple view of the CIC filter is depicted in Fig. 3-1.

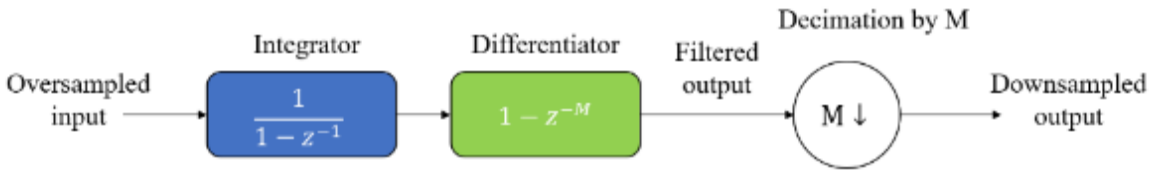

Fig. 3-1. First order CIC Filter Block Diagram [39].

The most common way to implement a first order CIC filter is shown in Fig. 3-1. Main issue with this implementation is that the differentiator block will need *"M"* delay elements (registers), which will dramatically increase with the oversampling ratio as well as the number of registers required to store data, thus being a constrain in higher order filters and higher oversampling rates.

One simple way to overcome this is by moving the Decimator operation just between the Integrator and Differentiator blocks as depicted in Fig. 3-2. With this change, a clock divider circuitry will generate a new clock M-times slower than the oversampling clock, on the output of the integrator stage. This operation will decrease the delay buffer depth of the differentiator and thereby a reduction in the power consumption as it will operate at a down sampled clock frequency.

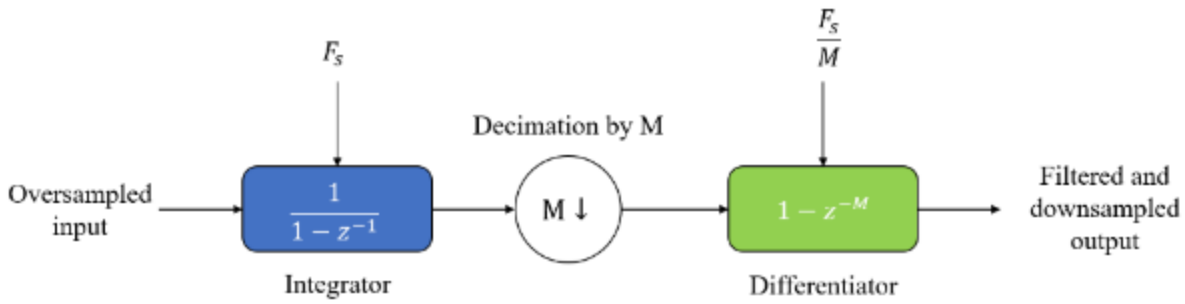

Fig. 3-2. Modified First order CIC Filter Block Diagram [39].

An integrator is a single-pole IIR filter with a feedback coefficient of one, functioning as an accumulator. The transfer function of the integrator in the z-plane is represented in the following equation.

$$H_I(z) = \frac{1}{1 - z^{-1}} \tag{3.1}$$

The frequency response of the integrator acts as a low-pass filter, having a very high gain at low frequencies and DC. Magnitude response can be depicted in Fig. 3.3 (red plot). The resulting spectrum has a very high magnitude at high frequencies but dramatically decreases as the frequency increases.

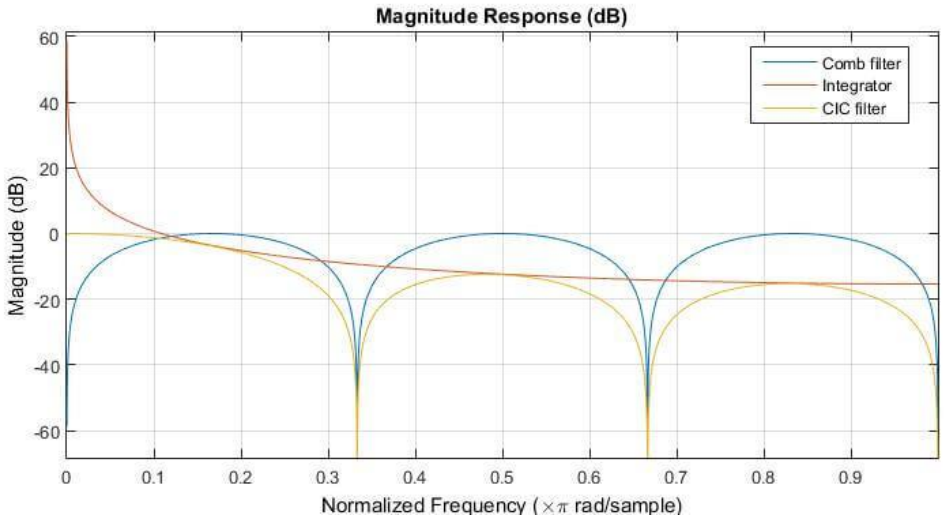

Fig. 3-3. Magnitude response of a comb-filter(blue), integrator(red) and CIC filter(yellow) [40].

The time-domain form of equation (3.1) is expressed in equation (3.2). According to equation (3.2), the integrator works by summing the current input with the previous output.

$$y[n] = y[n-1] + x[n] \tag{3.2}$$

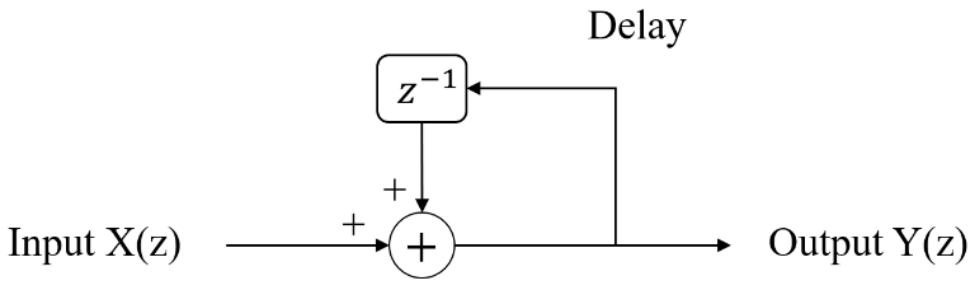

Fig. 3-4. Digital integrator block diagram [41].

The differentiator, also known as a comb filter, is an odd-symmetric FIR filter. Its transfer function is provided in equation (3.3).

$$H_C(z) = 1 - z^{-MN} \tag{3.3}$$

In equation (3.3), M is the oversampling ratio, and N is a design parameter known as the differential delay. N can be any positive integer, but it is usually limited to 1 or 2.

The frequency response of the differentiator acts as a high pass structure to attenuate infinite DC components and pass high frequencies. The differentiator magnitude response also depicted in Fig. 3.3 (blue plot). The resulting spectrum gets divided into N-number of peaks, separated by deep notches resembling a hair comb, that's why is often called comb-filter.

The time-domain representation of equation (3.3) is presented in equation (3.4).

$$y[n] = x[n] - x[n - M] \tag{3.4}$$

In equation (3.4), x[n] represents the current input, y[n] denotes the current output, and x[n - M] is the input delayed by M instants, where M is the decimation ratio. The role of the differentiator is to calculate the difference between the current input and the previous input.

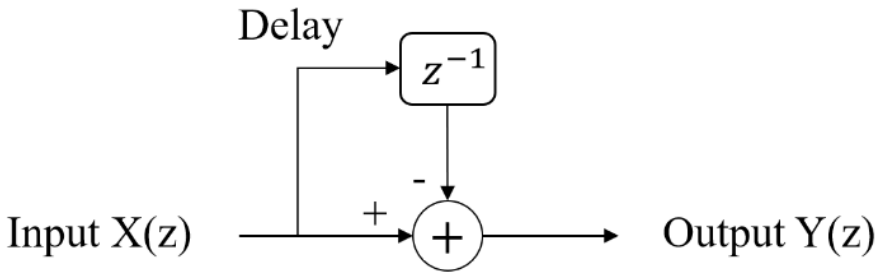

Fig. 3-5. Digital differentiator block diagram [41].

Derived of equations 3.1 and 3.3, the magnitude response of the CIC filter in Fig. 3-2 can be expressed as:

$$H(z) = \left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^{L} \tag{3.5}$$

Here, M represents the decimation ratio, and L denotes the filter's order.

The frequency response of the CIC filter results from the combined effect of the integrator and comb filter stages. The magnitude response can be depicted in Fig. 3-3 (yellow). The

resulting spectrum is the same N-number of peaks of the comb-filter, with the effect of the low-pass filter on the DC and high-frequencies, attenuating the magnitude of the peaks as the frequency increases.

3.1.1 Third Order CIC filter

Higher-order CIC filters are created by symmetrically cascading multiple digital integrators and differentiators. This multistage design enables most of the filter hardware to function at a reduced clock frequency and offers lower hardware complexity compared to a single-stage decimator.

A third order CIC filter is explored for this work. A basic block diagram is depicted in Fig. 3-6.

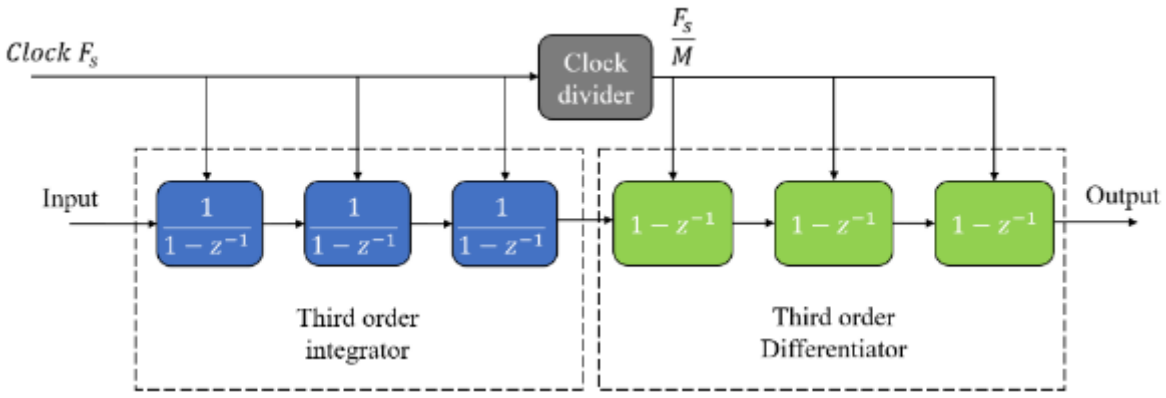

Fig. 3-6. Basic third order CIC filter with cascaded integrator and differentiator filters [42].

The word width (W) required to prevent overflow during runtime is estimated using equation (3.6) [43].

$$W = (1Sign\ bit) + (\text{Number of input bits}) + (\text{Order of the filter})\log_2(\text{M}) \qquad (3.6)$$

For this work, the output of the ΣΔ modulator is a 1-bit modulated output, the CIC Filter is a third order filter, and the decimation ratio M = 16. By replacing values on equation (3.6):

$$W = 1 + 1 + 3\log_2(16) = 14$$

To increase the bus size coming from the ΣΔ Modulator up to 14 bits, the integrators stage is preceded with a coder circuit. This block replicates the 1-bit modulation to each one of the 14 bits of the bus (see Fig. 3-7).

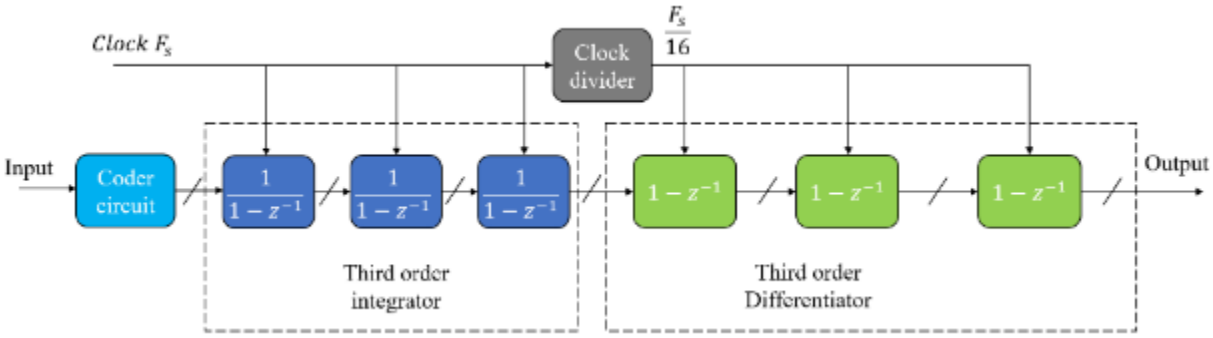

Fig. 3-7. Third order CIC filter with multibit output [42].

3.2. Integrator filter implementation

The digital integrator block (Fig. 3-4) was implemented in Verilog, Fig 3-8 shows its RTL (Register-transfer level) view:

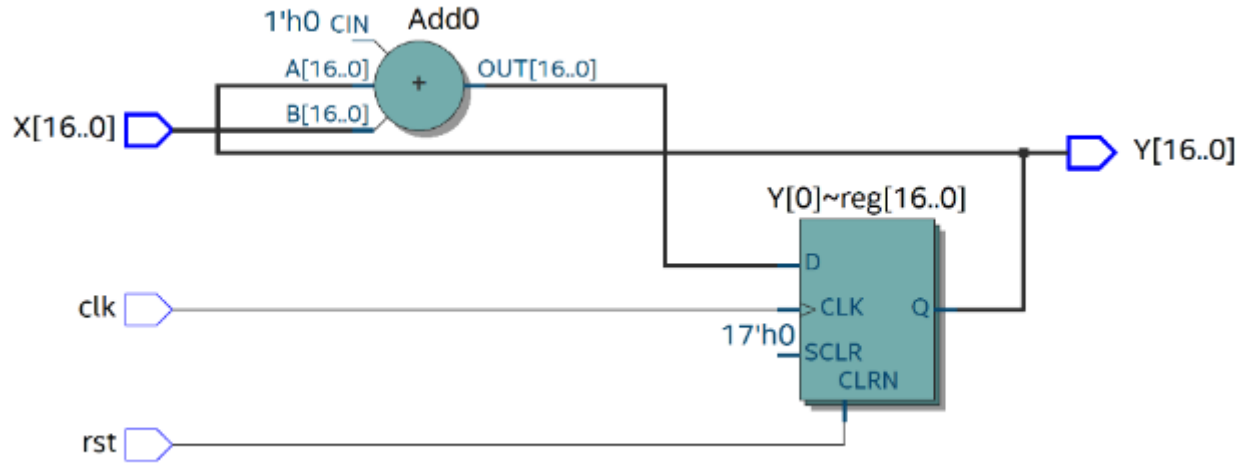

Fig. 3-8. Digital-Integrator filter RTL view.

In Fig. 3-8, the input X is directly connected to one input of an adder, while the other input of the adder is the system's output Y, which is also connected to the output of a register. This register introduces a delay to the adder's output based on the input clock.

This feedback branch of the output being delayed by the register corresponds to the delay of Fig. 3-4.

The Digital Integrator was simulated in Modelsim with a 4-bit word length and several values to the input to analyze its behavior.

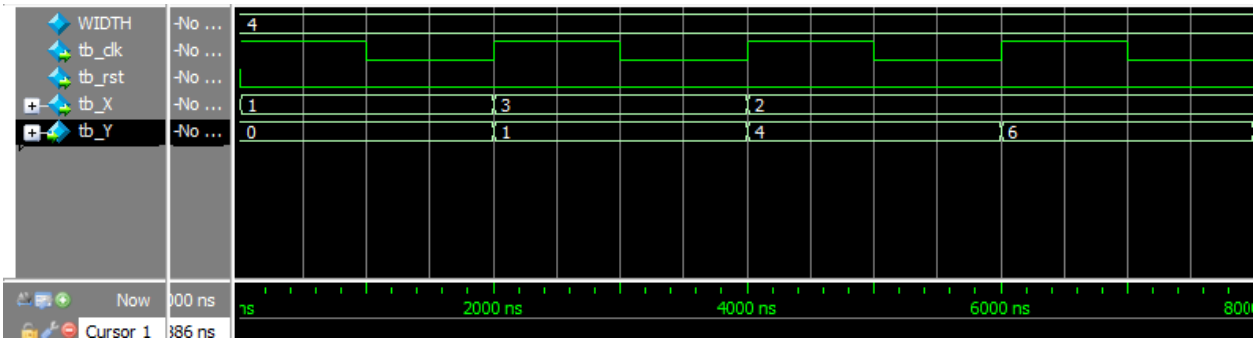

Fig. 3-9. Digital-Integrator output.

In Fig. 3-9, the Digital Integrator output can be observed under 4 clock edge transitions. In the first transition, the *rst* pin is first kept positive to reset all circuitry to prevent false past logic states.

After *rst* assertion, Y has an output of 0 and X was loaded with a value of 1 Decimal. In the second clock-rising edge, Y has the previous value of X, 0. Also in this second clock edge, X is now loaded with a 3 Decimal.

In the third clock edge, it is now observed how Y acts as an accumulator, as it now has a value of 4, which is the sum of Y's previous value (1), with the second clock edge X value (3).

In the last clock edge, X remained with 2 to verify that Y accumulates it on the fourth clock edge.

3.3. Differentiator filter implementation

The RTL view of the Digital Differentiator filter can be seen in Fig. 3-10.

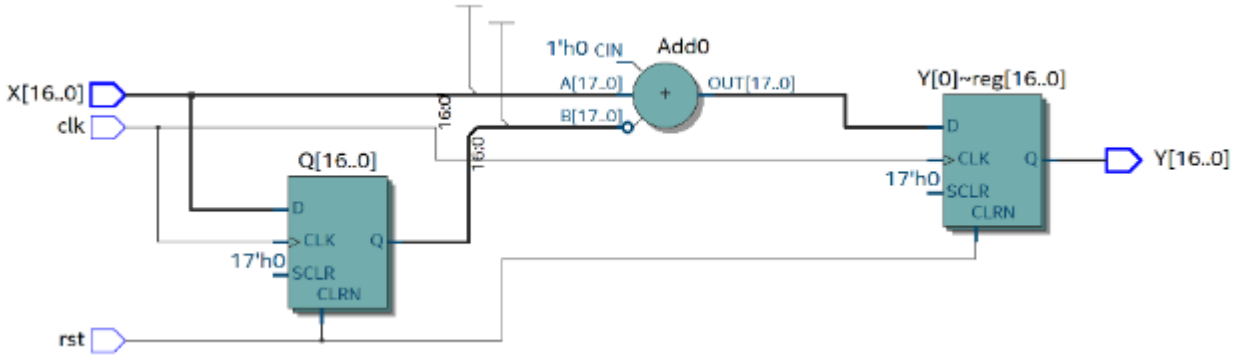

Fig. 3-10. Digital Differentiator filter RTL view.

In Fig. 3-10 the input X is directly connected to an Adder, the other input of the Adder corresponds to a reg output, where its input is connected to X. One important thing to notice is that this register output is inverted right at the Adder input, thus, this operation is performing the subtraction of X with the delayed value of X, which imitates the proposed scheme of Fig. 3-5. The output of this subtraction is connected to another register, and its output is the system output Y.

The second register acts as a down-sampling register as it is required to store data at instances where the clock divider output is $F_s/16$, whereas the output from the differentiator stages is continuous.

The Digital Integrator verified in Modelsim with an 8-bit word length and several values to the input to observe its behavior.

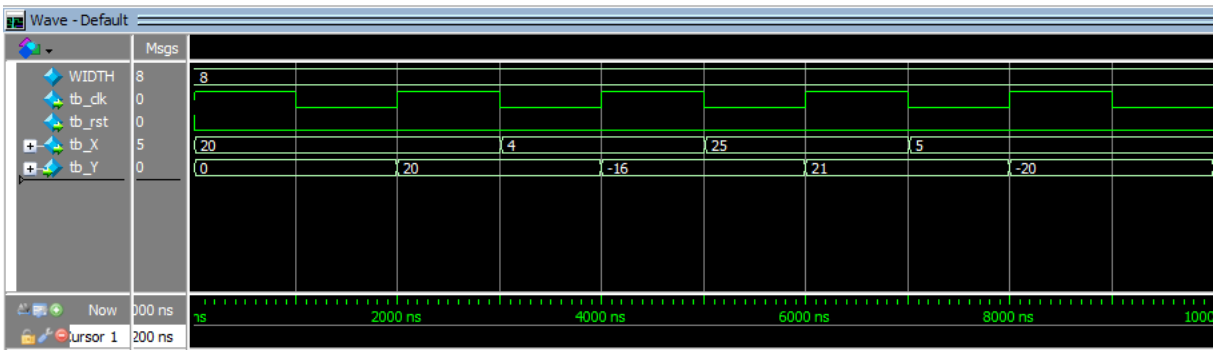

Fig. 3-11. Digital Differentiator output.

In Fig. 3-11, the Digital filter output can be observed under 5 clock edge transitions. In the first transition, the *rst* pin is first kept positive to reset all circuitry to prevent false past logic states.

In the first clock edge, the input X is 20 decimal, and the output Y is 0 as there wasn't a delayed version of X to perform the operation. In the second clock edge, the operation of 20 - 0 is performed, thus Y is equal to 20. Also, at the second half of the clock edge, 4 is forced at X to delay it to the next clock edge.

At third clock edge, as the value of 20 remained in X at the beginning of the previous clock edge, 20 stayed in the delayed version of X, thus Y equals 4 – 20 = -16.

Likewise at the fourth edge, on the third edge the value of 4 remained at the beginning of the edge and ultimately stayed in the register, thus Y equals 25 - 4. At the last clock edge, the same subtraction of X minus the delayed version of X is performed (5 - 25 = - 20).

3.4. Clock divider implementation

The RTL view of the clock divider can be seen in Fig. 3-12.

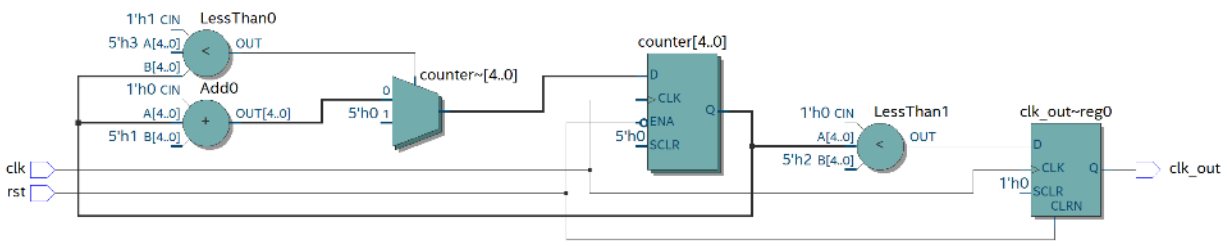

Fig. 3-12. Clock divider RTL view.

In Fig. 3-12 it can be observed that there's a main register that is counting the clock edges, and then there are two comparators that compare the current counter value to the established value, to create an output clock proportional to the dividing ratio.

The clock divider was verified in Modelsim with a 1 MHz input clock frequency and a dividing ratio M = 10 to observe its behavior.

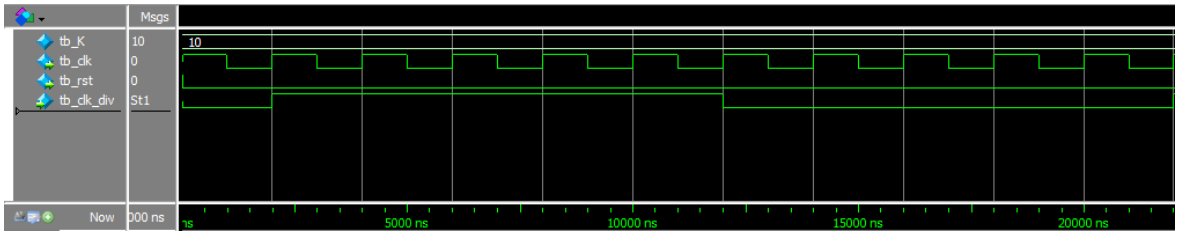

Fig. 3-13. Clock divider output. f_{clk} = 1 MHz, M = 10, $f_{div} = 100\ kHz$.

In Fig. 3-13 it can be observed that the generated output clock clk_div, corresponds to 5 input clock edges for the rising edge and another 5 input clock edges for the falling edge, thus generating a clock M = 10 times slower than the input clock.

3.5. The CIC Filter system integration

After having designed and verified the individual blocks of the integrator, differentiator filter, and the clock divider, the third-order CIC filter was built by looping three integrator filters, three digital filters, and the clock divider for the differentiator filters, as depicted in Fig. 3-14.

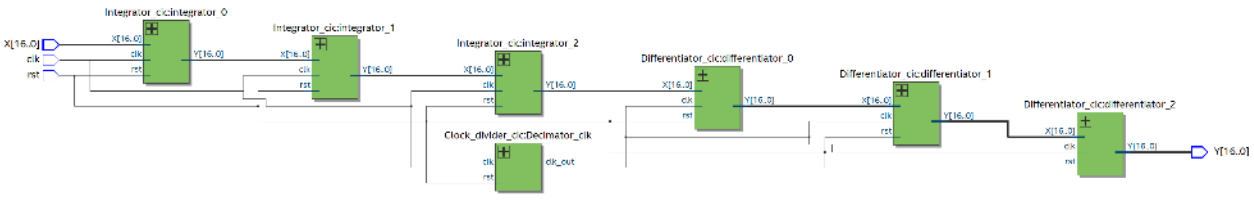

Fig. 3-14. CIC Filter RTL view.

In Fig. 3-14 it can be seen how the filters are connected to perform the third-order CIC filter, where the output of the filter is the input of the next one, and so on. It can also be noted that the clock used for the differentiator comes from the clock divider.

Due to the system complexity, the CIC filter was not verified in Modelsim due to the number of operations between the input X and the output Y, and as it would require precise clock and specific input test vectors from the actual ΣΔ modulator. Instead, it was verified directly on Cadence virtuoso with different input waveforms.

4. Simulation results of the ΣΔ ADC

This chapter presents the simulation results of the ΣΔ ADC, which includes the behavior of the integrated system — comprising the ΣΔ modulator and the CIC filter.

For the transient response, various signal waveforms such as triangular, sinusoidal, and square are injected, and the output is analyzed to obtain static FoMs like DNL, INL, and gain and offset errors. Additionally, key dynamic FoMs are derived through FFT analysis and compared against the targets established at the start of this work.

4.1. Integration of the ΣΔ Modulator with the CIC Filter

Fig. 4-1 depicts the block-level schematic of the ΣΔ ADC, which involves the non-overlapped clocks generator, the ΣΔ Modulator and the Verilog macro model of the CIC filter.

The use of Verilog macro models in the simulation significantly reduces the simulation time for the presented tests in this work, and those models can later be implemented with transistor-level blocks using VLSI techniques.

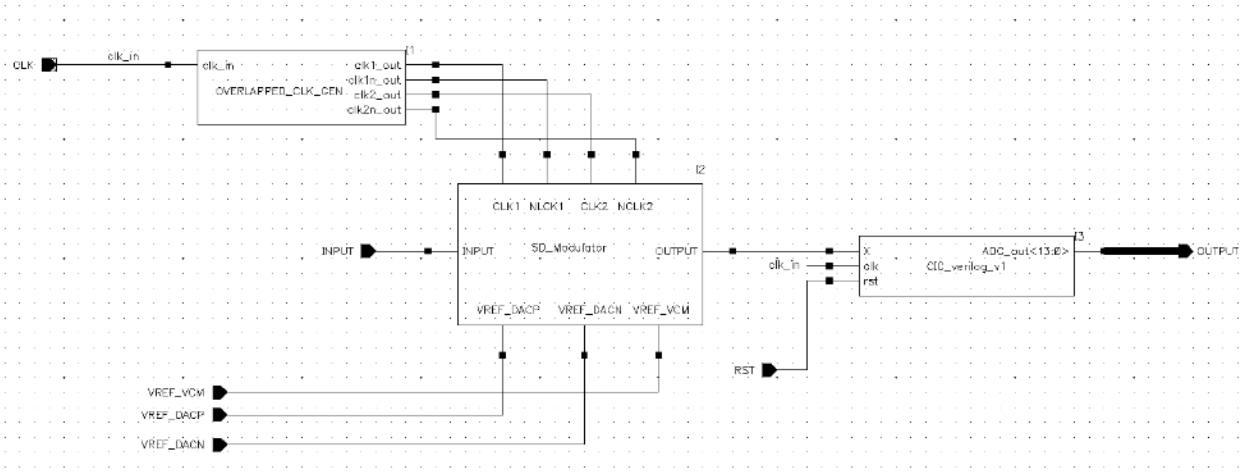

Fig. 4-1. ΣΔ ADC schematic.

The CIC filter requires an extra reset input *rst* to initialize the bit registers of the integrator and differentiator digital filters. The input clock of the CIC filter is the same clock generated by the non-overlapped-clock generator.

The transient response of the ΣΔ ADC was tested with different input waveforms, such as triangular, sine, and square signals with the same f_{in} and V_{pp} at which the ΣΔ was tested.

The test setup diagram is depicted in Fig. 4-2.

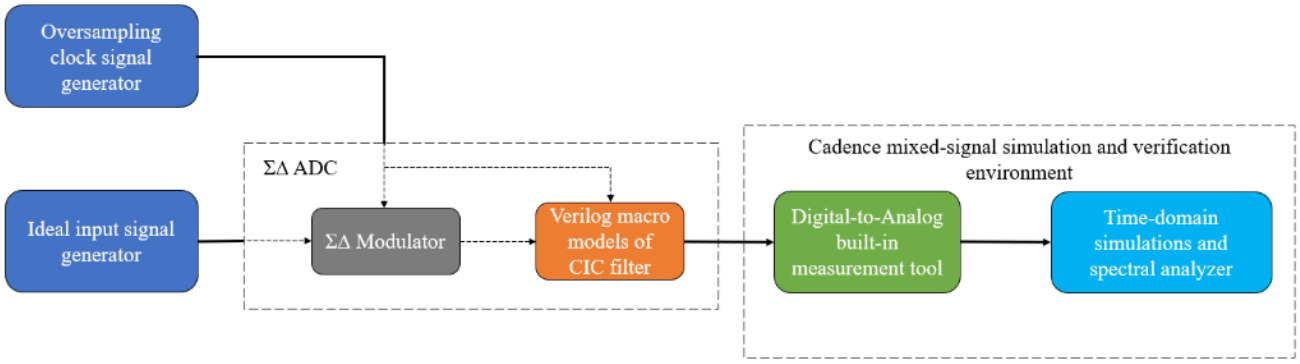

Fig. 4-2. Test setup diagram for the ΣΔ ADC.

In Fig. 4-3 is depicted the transient response of the ΣΔ ADC to a triangular input waveform.

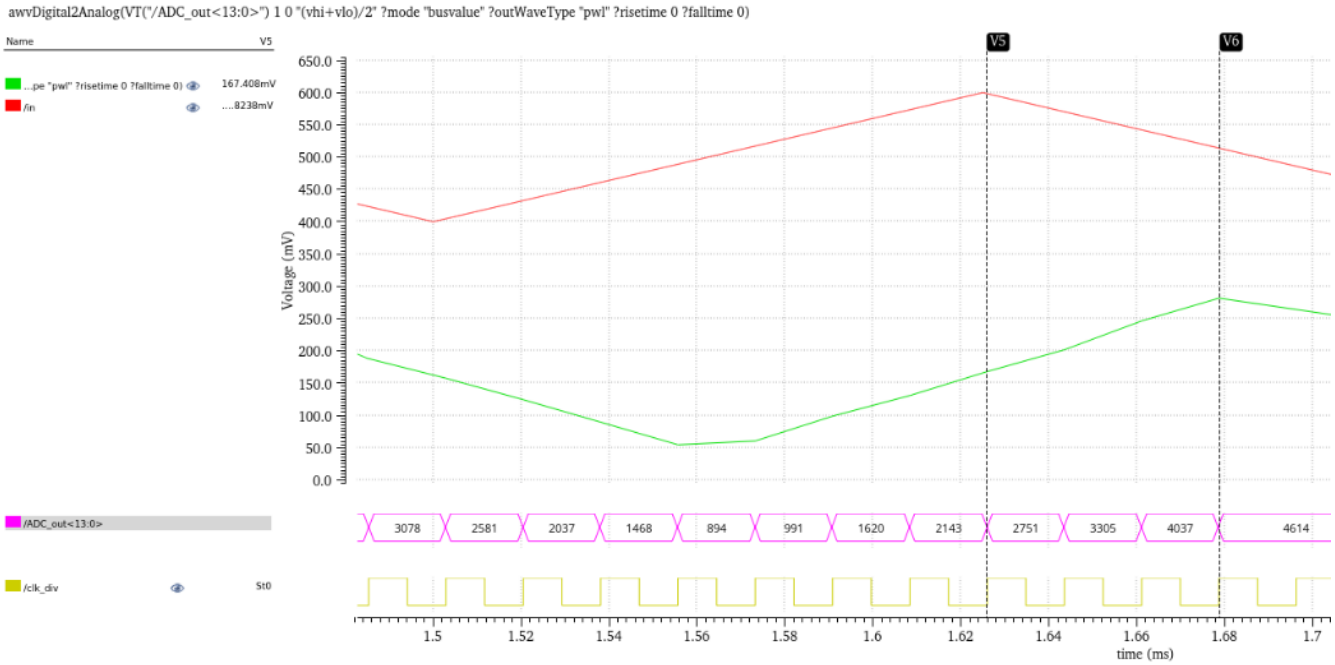

Fig. 4-3. ΣΔ ADC output response to a triangle waveform. $f_{in} = 4\ kHz$, $F_s = 1.024\ MHz$, $K = 128$, $M = 16$.

In Fig. 4-3. the green waveform is the ΣΔ ADC output in an analog format which corresponds to the digital signal (the magenta curve) embedded in the cadence AMS (analog mixed-signal) tool "Digital to Analog".

From Fig. 4-3 it can also be noted a delay between the input and the output. The delay is outlined with the vertical cursors in Fig. 4-3 at the peak of the red and green triangle waveforms. As it can be noted in Fig. 4.3, this delay is equal to three periods of the clock divider signal.

Fig. 4-4 and Fig. 4-5, show the transient response of the ΣΔ ADC, with sine and square signals respectively. It can be noted that with a sine input, the ADC reconstruction represents a sine waveform.

The output signals exhibit a slow slew rate during output transitions, resulting in degraded linearity, which becomes more noticeable in the square waveform with increased rise and fall times. This issue is likely related to the comparator within the ΣΔ Modulator, where its slew rate may be insufficient to respond quickly to signals with frequencies approaching F_s. Measured THD in Table 11 confirms a degradation in the output signal.

Since access to the Cadence environment was lost when these results were analyzed, testing the comparator under frequencies close to F_s is suggested as future work.

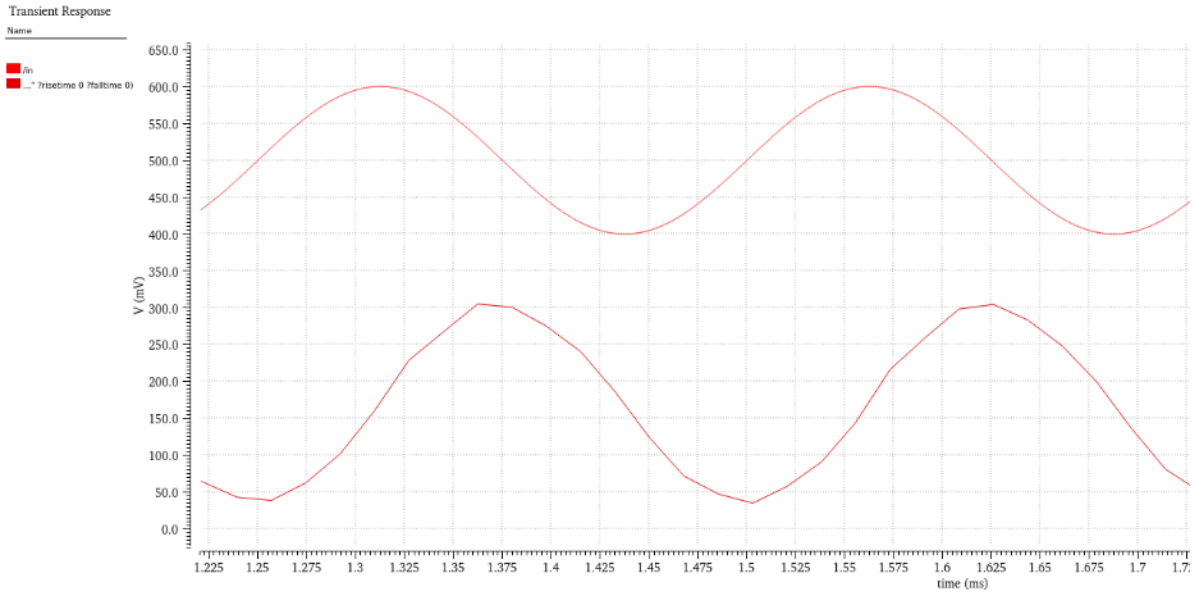

Fig. 4-4. ΣΔ ADC output response to a sine waveform. $f_{in} = 4\,kHz$, $F_s = 1.024\,MHz$, $K = 128$, $M = 16$.

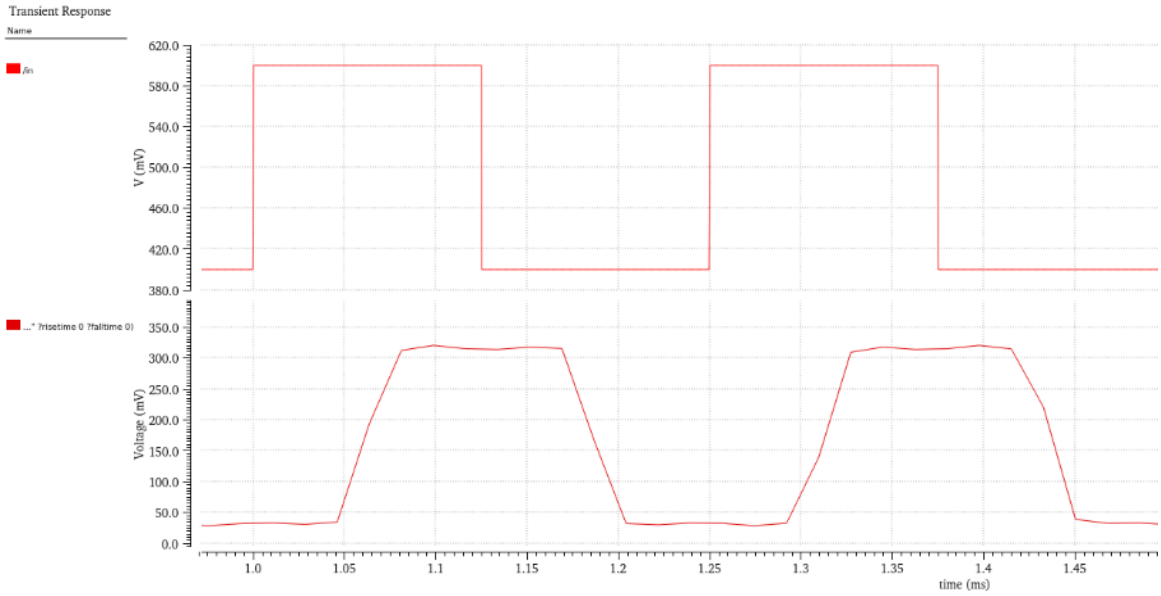

Fig. 4-5. ΣΔ ADC output response to a square waveform. $f_{in} = 4\ kHz$, $F_s = 1.024\ MHz$, $K = 128$, $M = 16$.

There is a systematic delay of 52.82 µs between the input and output of the three tested waveforms.

With the three test-cases, it can be noted that the output of the ΣΔ ADC is the same waveform of the input signal that demonstrates the functionality of the designed ADC. However, in all of the three test-cases, a systematic delay of 52.82 µs is present. Such delay is attributed to the three differentiators stages of the CIC filter, this is because they need at least three clock periods to take the data from the first differentiator up to the last stage in the data path, as their output registers require a clock transition to feed the data to the next block.

Finally, an offset of 65 mV is observed in the output signal. This can be attributed to the offset error introduced by the SC Integrator, as some noise was already present in the output response, as depicted in Fig. 2-15 of chapter 2.

4.2. ΣΔ ADC FoMs

The INL and DNL were measured by changing the ΣΔ ADC input waveform to single ramp (like the positive ramp of Fig 4-3, red waveform), and then visualized its output in a quantized view with the help of the "Digital to Analog" measurement tool, which plots every step of the

digital bus. The raw data obtained is depicted in Fig. 4-6. In the x-axis is displayed the output voltage of the DAC conversion, and in the y-axis the respective DNL.

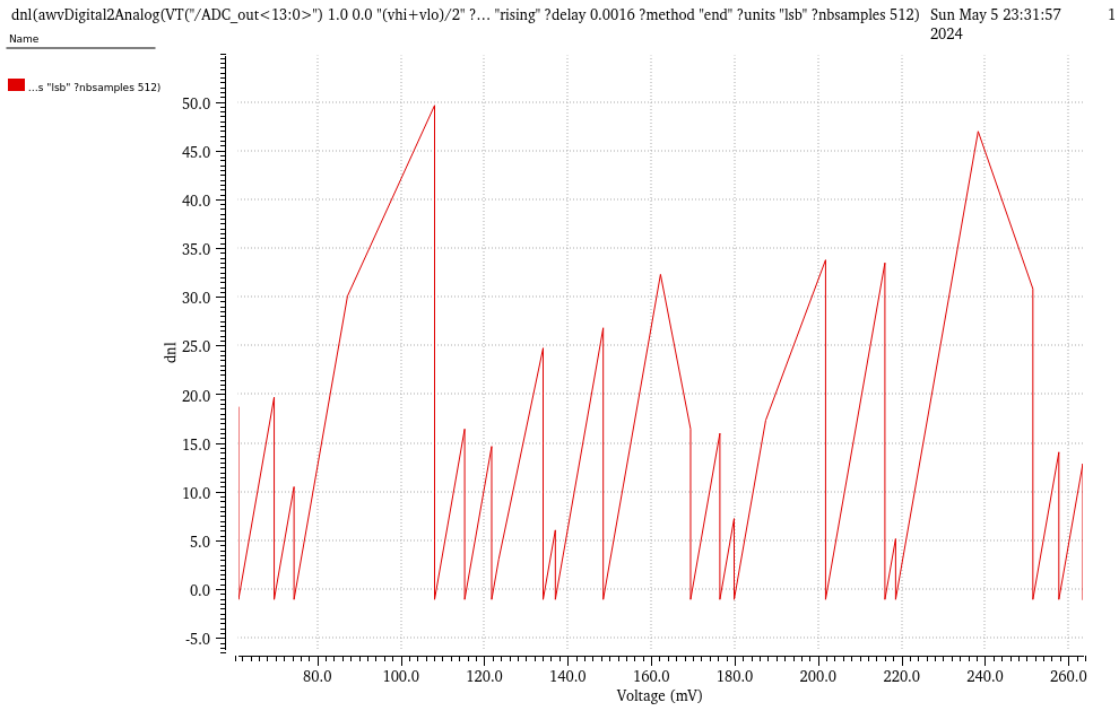

Fig. 4-6. Raw DNL measurement of the ΣΔ ADC.

By manipulating the raw data, the DNL is best displayed when matched with the digital output code of the ΣΔ ADC (see Fig. 4-7). The digital output code is displayed with unsigned decimal format, the same showed in the magenta waveform of Fig. 4-3. It can be noticed a maximum DNL of 50 LSB.

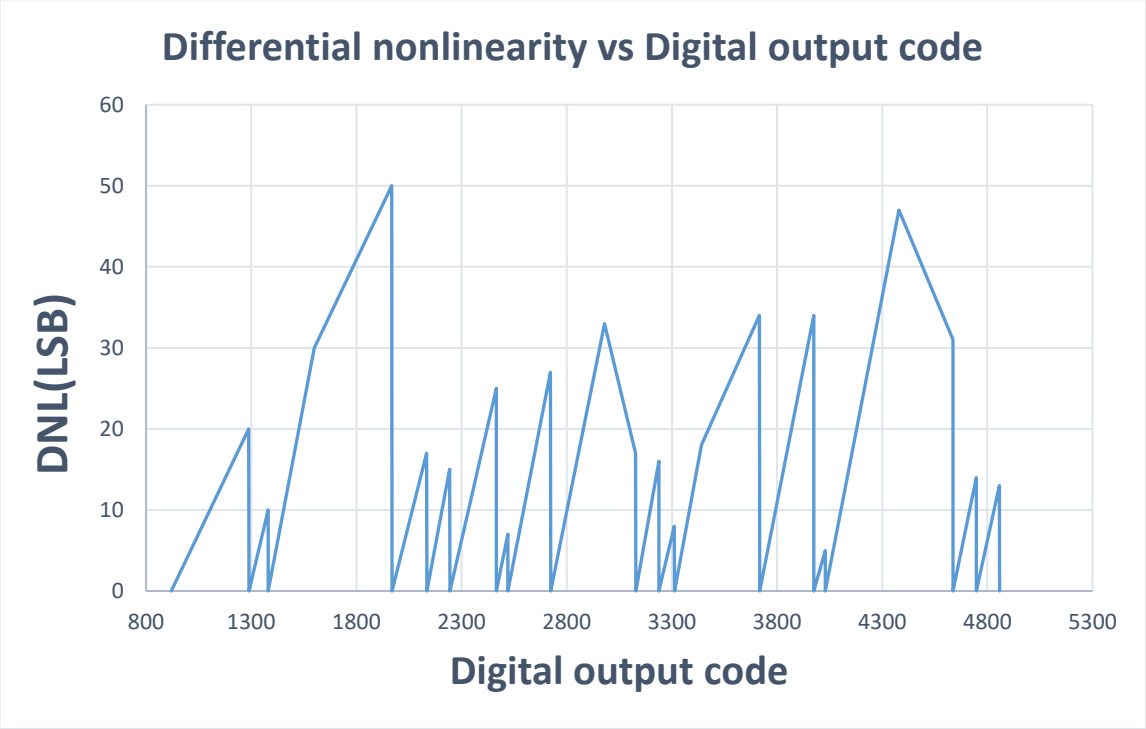

Fig. 4-7. Processed DNL data of the ΣΔ ADC.

The INL measurement is depicted in Fig. 4-8, where the slope corresponds to the interpolation of the steps in the output transfer function. By processing this raw data, a gain error of m = 0.9 is derived. Furthermore, by superimposing an ideal slope with m = 1 (as shown by the black waveform in Fig. 4-9), an offset error of 65 mV is identified (see Fig. 4-9).

The INL is calculated by eliminating the offset error from the ideal slope and identifying the point of maximum deviation between the actual and ideal slopes. An INL of 10 LSB was observed.

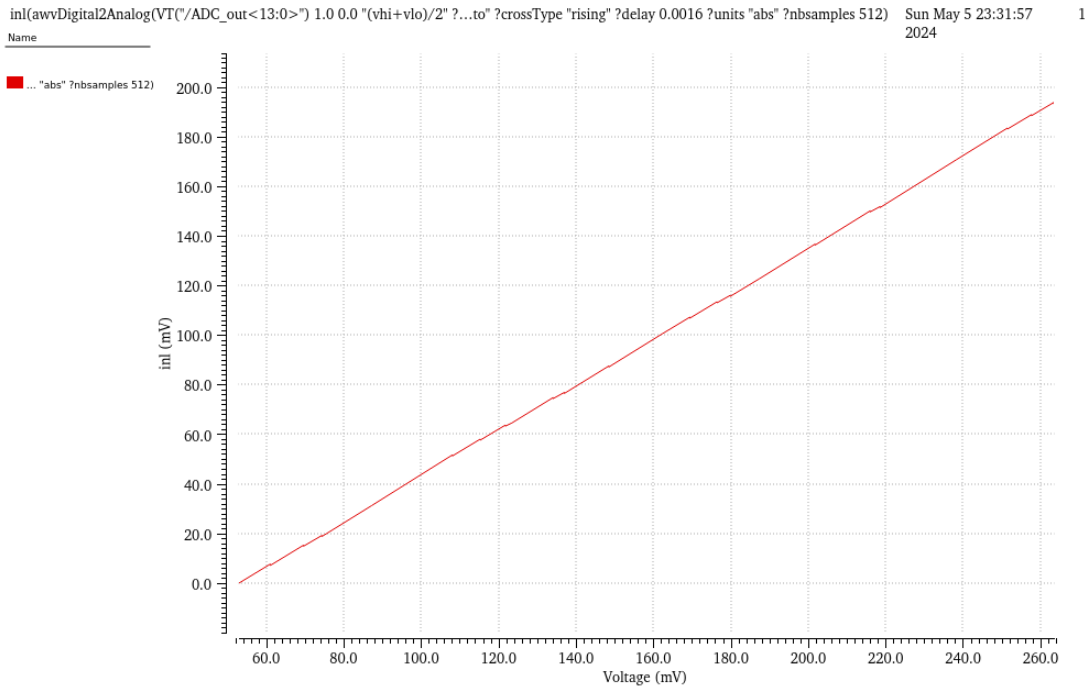

Fig. 4-8. INL measurement of the ΣΔ ADC.

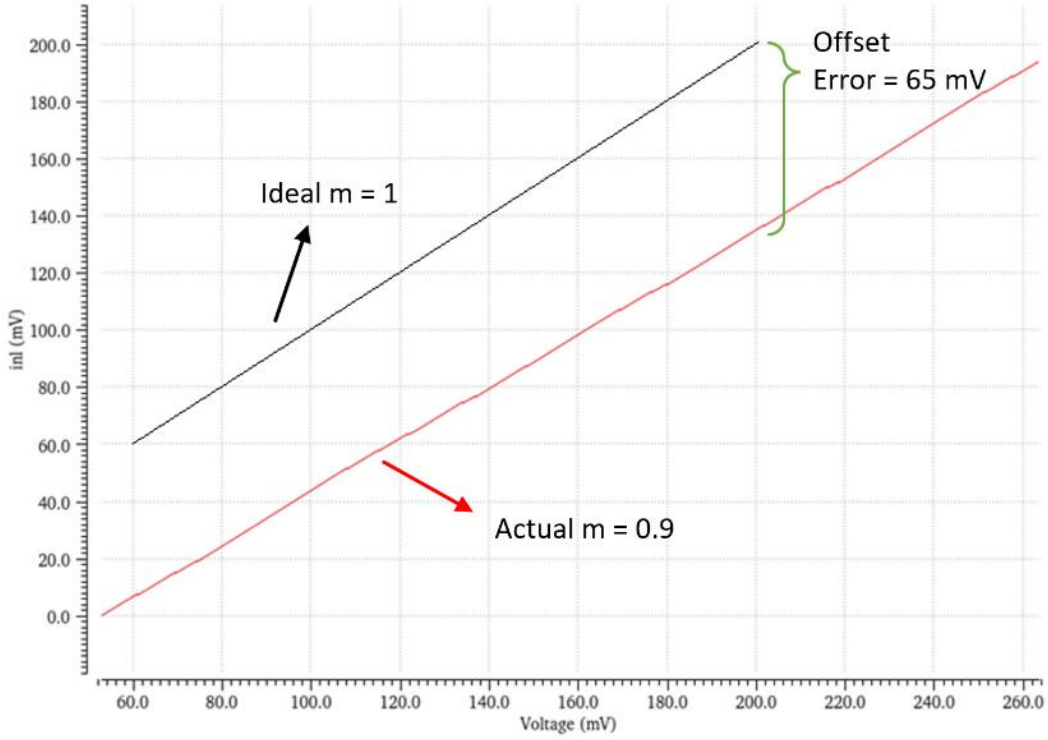

Fig. 4-9 Gain and offset errors measurement of the ΣΔ ADC.

To evaluate additional FoMs, the Cadence "Spectrum" tool was employed. This tool computes the FFT (Fast Fourier Transform, Fig. 4-10) from a time-domain waveform and provides various measurements, including the Signal-to-Noise-and-Distortion Ratio (SINAD), PSD plots (Power Spectral Density, see Fig. 4-11), among others.

For this, the ADC input sine wave frequency and oversampling frequency had to be recalculated with a coherent window sampling to get accurate data and the FFT predominant tone equal to the input frequency.

Coherent sampling refers to the process of sampling a periodic signal in such a way that an exact integer number of cycles fit within a specified sampling window [44]:

$$f_{IN} = \left(\frac{N_{WINDOW}}{N_{RECORD}}\right) * f_{SAMPLE} \tag{4.1}$$

Here, f_{IN} represents the continuous sinusoidal input signal, f_{SAMPLE} is the clock or sampling frequency of the ADC, $N_{\sin}$ denotes the integer number of cycles within the sampling window (which must be an odd integer or a mutually prime number), and N_{RECORD} is the number of data points intended for the sampling window or FFT analysis.

The new test tone of f_{IN} required to calculate N_{WINDOW}, thus f_{IN} $4\ kHz$, $N_{RECORD} = 1024, and\ f_{SAMPLE} = 1\ MHz$ were used as starting values.

$$N_{WINDOW} = int\left(\frac{f_{IN}}{f_{SAMPLE}}\right) * N_{RECORD} = int\left(\frac{4\ kHz}{1\ MHz}\right) * 4096 = int(16.384) = 17$$

$$f_{IN} = \left(\frac{17}{4096}\right) * 1\ MHz = 4.15039\ kHz$$

With $f_{IN} = 4.15039\ kHz$, the oversampling ratio K slightly decreases to 123, hence the temporal response of the ADC and its output it's not dramatically different.

Thus, the FFT of the ADC was obtained with this input tone.

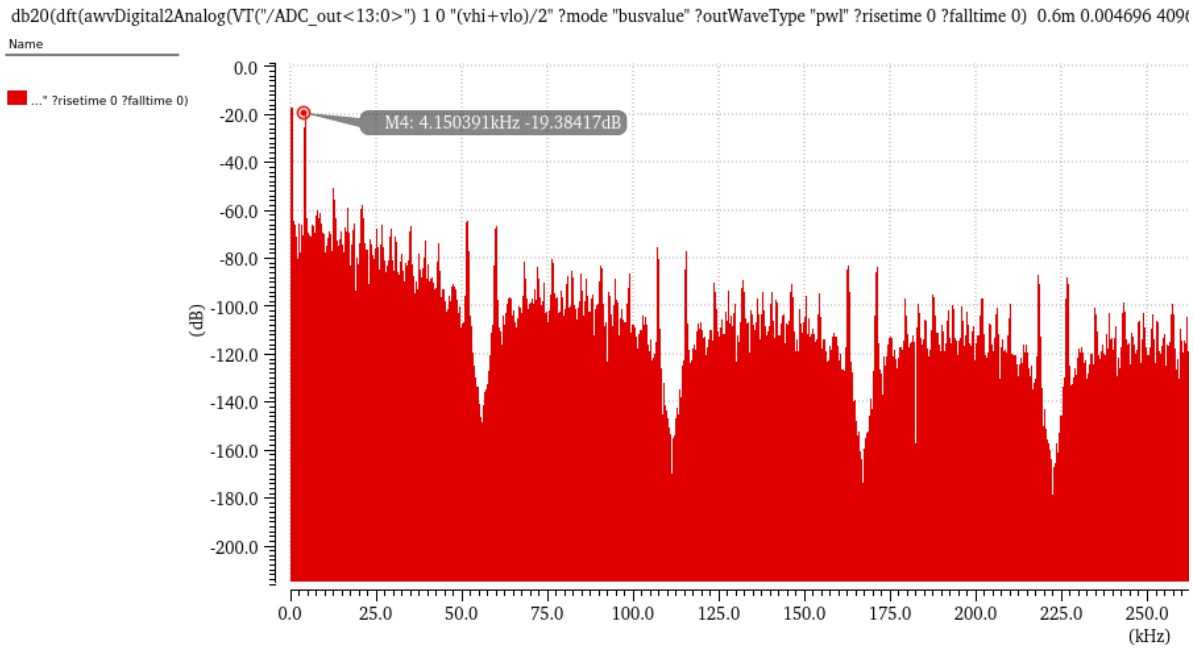

Fig. 4-10. FFT of ΣΔ ADC output. Hanning Window type, 1 Harmonics, one signal bin.

In Fig. 4-10 it can be observed that the test tone is predominant at $f = 4.15039\ kHz$, which is the frequency of the input sine. Some other harmonics are present at higher frequencies with less magnitude. This is due to the non-ideal behavior of the ADC circuit.

It can also be appreciated that both Fig. 4-10 and 4-11 shows a frequency response similar to Fig. 3-5, which combines both Integrator and Differentiator effects. Table 11 summarizes the measured FoM derived from the ADC.

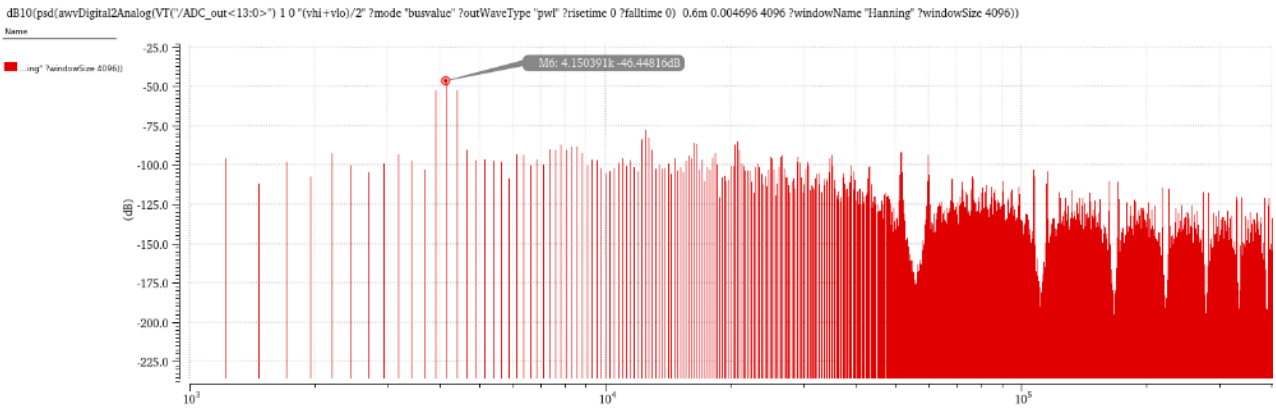

Fig. 4-11. PSD of ΣΔ ADC output.

Table 11. ΣΔ ADC measured FoMs.

FoM	Value
Effective Number of Bits (ENOB)	6 bits
Signal-to-Noise-and-Distortion Ratio (SINAD)	29.86(dB)
Signal-to-Noise Ratio (SNR)	51.42(dB)
Spurious-free dynamic range (SFDR)	37.47(dBc)
Total Harmonic Distortion (THD)	-29.89 (dB)
Signal Power	-13.35 (dB)
DC Power	-10.93(dB)
Noise Floor/Bin	-73.49(dB)
Noise Floor/rtHz	-97.36 (dB)
P_D	38.8 µW

P_D from Table 11 was obtained by measuring the average of I_{AVDD} and then calculated P_{AVDD} from equation (1.13), and it represents the power consumption of the ΣΔ Modulator analog circuits only, as the CIC filter is being macro modeled with Verilog, thus it doesn't represent any power consumption at this level.

By comparing the results in Table 11 with the target FoMs outlined in Table 1 of Chapter 2, it is evident that the resulting SNR falls short by 9 dB, leading to a noisier ADC output, with the digital representation containing more distortion than expected. The SNR directly impacts the ENOB, which is reduced by 2 bits, negatively affecting the converter's output resolution.

The THD is off by -40 dB, where lower THD values indicate less distortion and better signal fidelity, as confirmed by the transient results in Fig. 4-4 and Fig. 4-5.

On the positive side, the resulting power consumption (P_D) is less than half the target, thus improving reliability and allowing the ADC to operate more efficiently over time.

Furthermore, a comparison of state-of-the-art ADCs is displayed in Table 12.

Table 12. Comparison of state-of-the-art ADCs

Parameter	Work [45]	Work [46]	Work [47]	Work [48]	Work [49]	This work
Architecture	SAR	SAR	Flash	Flash-SAR	Flash	ΣΔ
Technology (nm)	130	90	65	45	45	45
Resolution	10-bit	10-bit	6-bit	9-bit	6-bit	12-bit
Supply (V)	1.2	1	1.2	1	0.7	1
F_s (MS/s)	20	30	1000	100	1000	1
Power(μW)	620	980	7700	6100	45.42	38.8*
$ENOB\ (bit)$	9.32	8.68	4.1	8.33	5	6
SNDR (dB)	57.86	54	26.442	51.94	31.9	29.86

Note *: This power consumption doesn't consider the digital blocks of the ADC (CIC Filter) as they are being macro modeled in Verilog.

5. Physical design of ΣΔ ADC

Physical design in CMOS (Complementary Metal-Oxide-Semiconductor) technology, is a critical aspect of integrated circuit engineering, where the analog and digital circuits are transformed into a physical representation that can be fabricated. This process involves arranging and interconnecting transistors within a limited silicon area, ensuring that the circuit operates optimally in terms of performance, power consumption, and occupied area.

In this chapter, the physical design of the ΣΔ ADC is presented.

5.1. Physical design of analog blocks

The layout of an integrated circuit specifies the geometries that will be used in the manufacturing masks. These geometries include n-well, active areas, polysilicon, n+ and p+ implants, interlayer contacts, and metal layers, each tailored to the specific characteristics of the CMOS technology applied in the design.

Compactness is essential for several reasons. First, a more compact design allows for more functionality to be integrated into the same chip area, which is crucial for the miniaturization trend in the semiconductor industry. Additionally, reducing the chip area can lower manufacturing costs since more chips can be produced from a single silicon wafer. A compact design also shortens interconnect lengths, reducing parasitic capacitances and signal losses, thereby improving the circuit's speed and energy efficiency.

To achieve an efficient CMOS physical design, various techniques and tools are employed. Common practices include floorplanning, where the placement of functional blocks on the chip is determined; placement, which assigns specific positions to standard cells; and routing, which electrically connects cells and blocks. Advanced techniques also involve timing optimization, power distribution control, and thermal management, all of which are critical to ensuring that the final design meets performance and reliability requirements.

The layout technique for the ΣΔ Modulator is fully customized, and most compacted as possible. On the following subchapters, every layout block of the ΣΔ Modulator is detailed.

The technique of schematic-driven layout using the pCells of 45 nm CMOS technology is used. Each block was implemented taking care of the design rules of 45 nm CMOS technology, that is the minimum width of interconnect layers, the minimum space between layers, among others; Metal 1 layer was predominantly used on low-level interconnections and Metal 7 was used as a transition layer whenever there wasn't a direct connection on Metal 1, and for long traces to avoid antennas. Pins of each block were placed accordingly to connect other blocks by abutment.

A hierarchical physical design technique was used to assemble all blocks of the ADC core.

5.1.1 Physical design of the clock generator

The layout of the clock's generator depicted in Fig. 5-1 follows accurately its schematic, by having the clock input in the far left-hand side, the delay chain in the middle, and clock buffers at the end of the signal path. The green surrounding area is the capacitors that connect the output of each clock phase and help to dampen the overshoots at transitions.

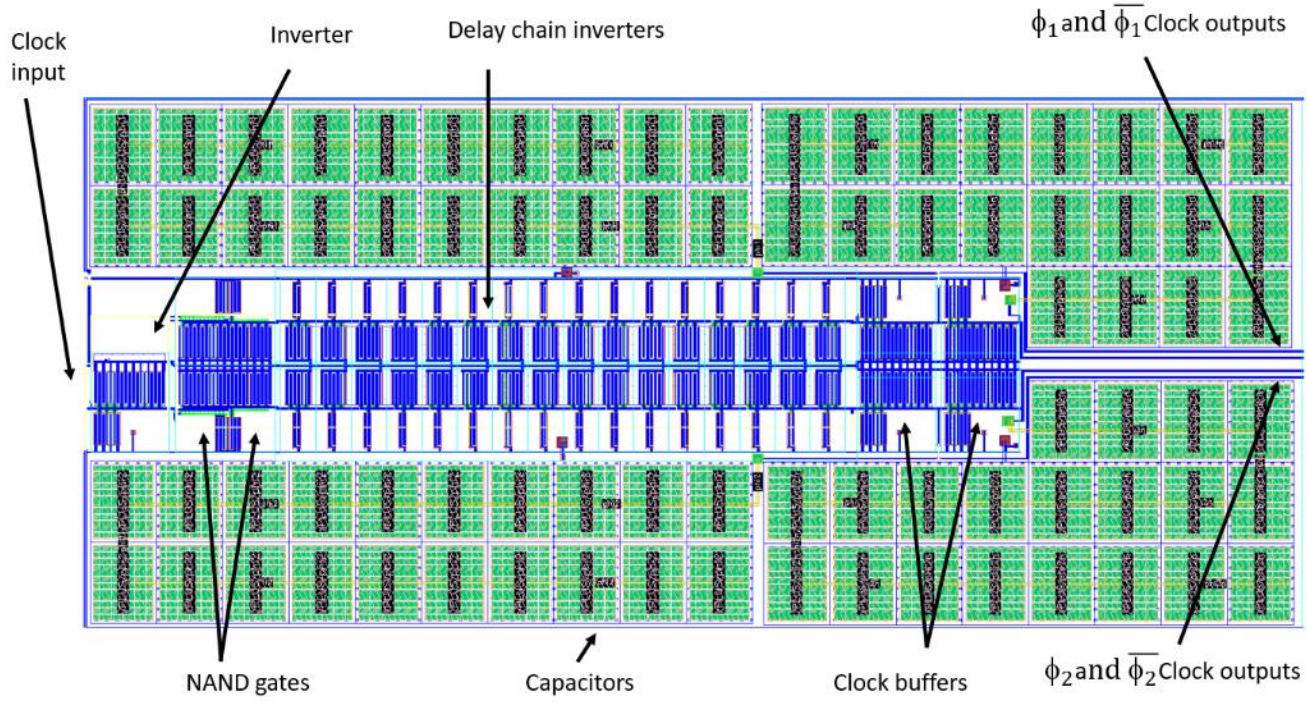

Fig. 5-1. Layout of the non-overlapped clock's generator.

pCells of capacitors has their connection pins on Metal 10 and Metal 11 layers, so we use vias M10-M9, M9-M8, …., M2-M1 to descend to Metal 1 to connect them with transistor pCells.

Smaller capacitors are grouped and connected in an array to get the equivalent capacitance of the required circuit. 25 fF are obtained through a single 5 x 4 µm capacitor.

Fig. 5-2 shows the layout of NAND gate. One common technique for a compact layout is to stack the MOS themselves on the border where they share fingers with the same net. For instance, the two NMOS are stacked on the same Drain finger to save space.

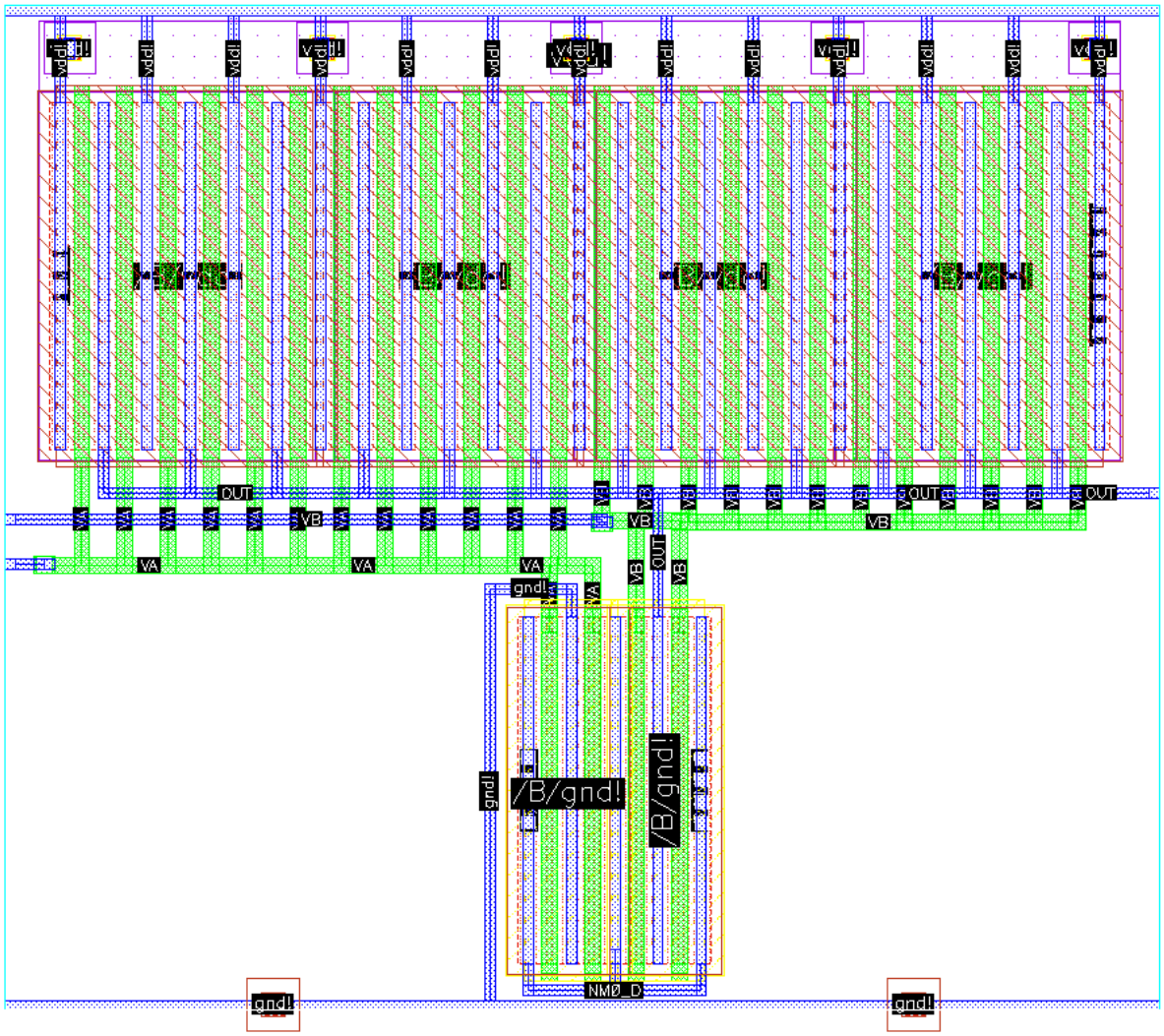

Fig. 5-2. Layout of a NAND logic gate.

Likewise, on the top PMOS's, it can be seen they are stacked on some of the fingers connected to V_{DD}.

One technique to avoid designs with huge finger dimensions is to split the design into several fingers with alternated connections, where their common fingers are stacked with the same net, like previously explored.

The inverter depicted in Fig. 5-3, at the contrary of Fig. 5-2, it has fewer dimensions and overall smaller size, as this inverter is replicated several times in the clock's generator (Fig. 5-1), and its main purpose is to generate the delay between the clock's phases.

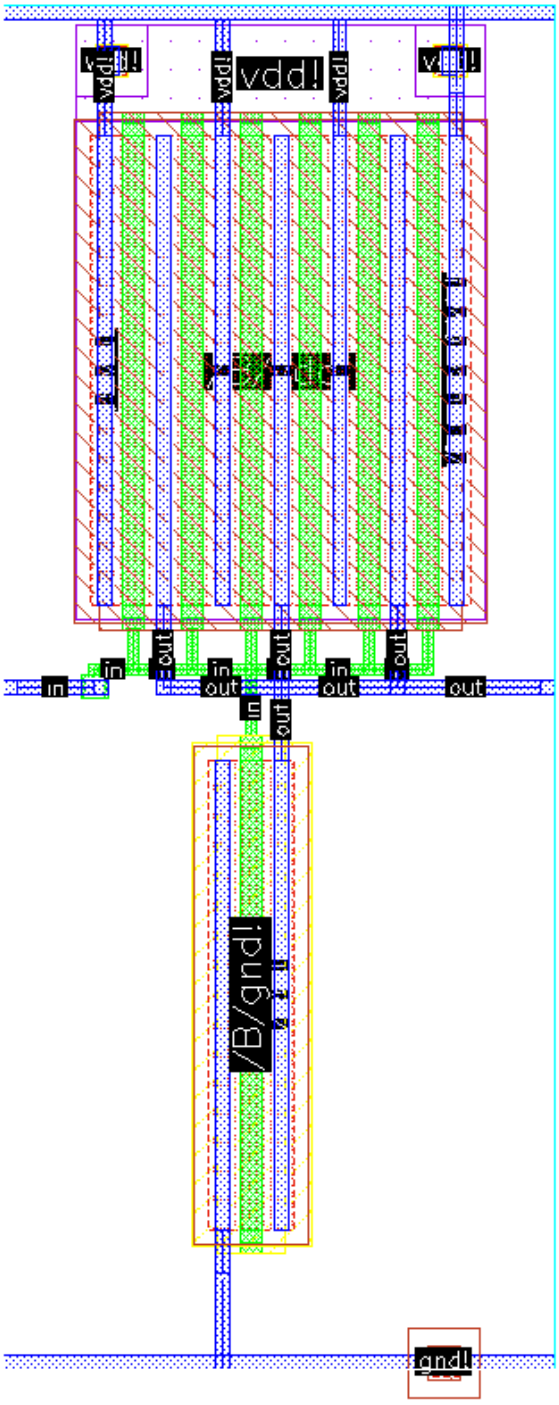

Fig. 5-3. Layout of an inverter, part of the delay chain in the clock generator.

The layout technique of a clock buffer inverter depicted in Fig. 5-4 is like the NAND gate, as the fingers are distributed among several transistors to reduce the finger's size and thus form a compact layout.

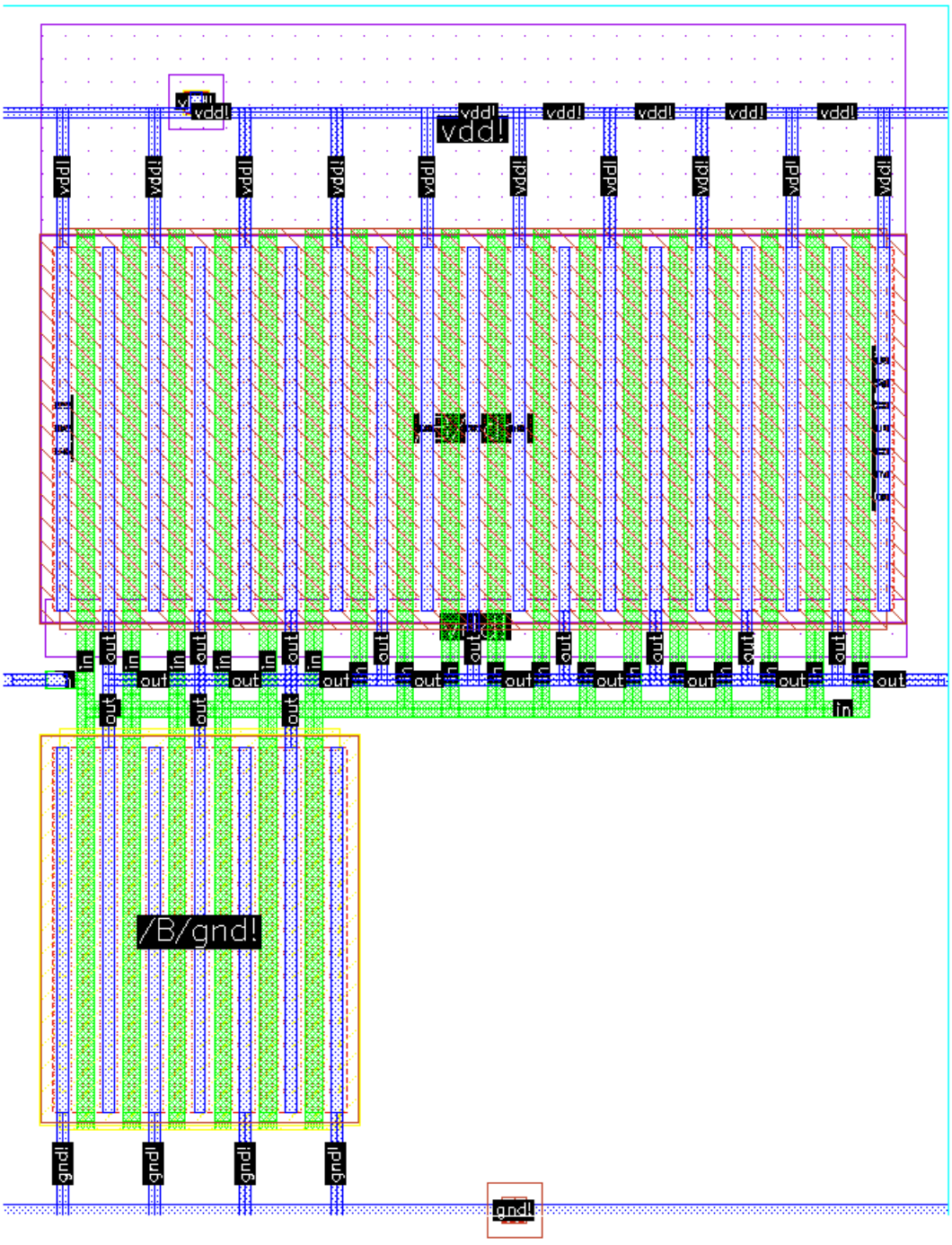

Fig. 5-4. Layout of a clock buffer inverter.

5.1.2 Physical Design of the Switched-Capacitor Integrator

Like the non-overlapped clock's generator layout of Fig. 5-1, the capacitors depicted in Fig. 5-5 contribute to most of the layout of the Switched-Capacitor (SC) Integrator as this technique relies on big capacitors to operate. The capacitors use the same 5 x 4 µm base cell capacitor, requiring up to 200 cells to form the 5 pF capacitor at the input of the self-cascode OTA.

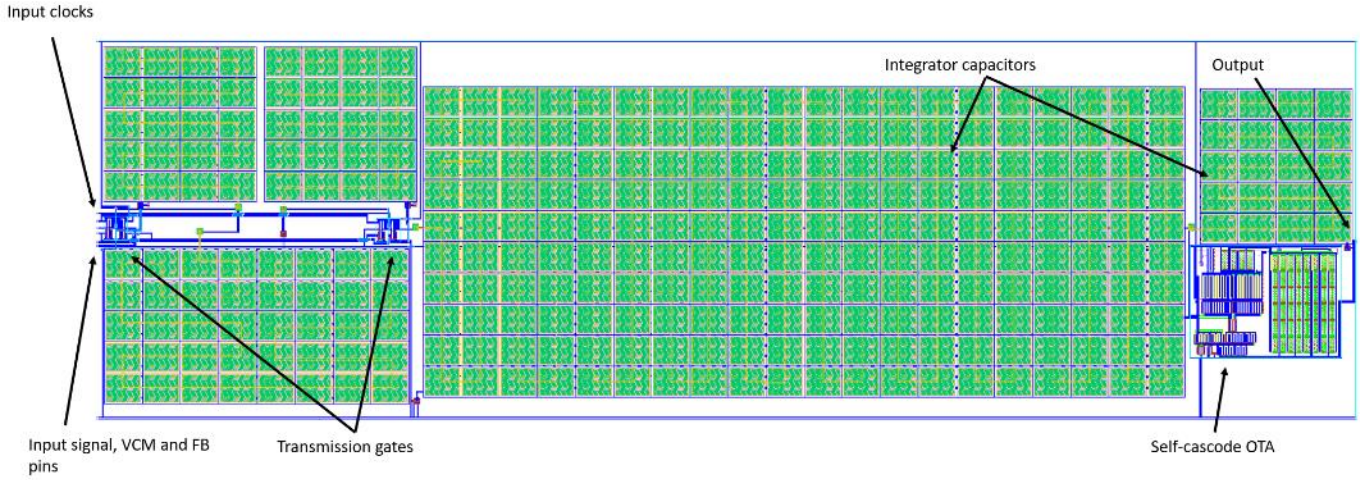

Fig. 5-5. Layout of the SC Integrator.

The transmission gates were placed back-to-back with the pins they had in common and placed near the grounding and main SC capacitor.

In Fig. 5-6 is shown the layout of self-cascode OTA. As the second stage of the OTA required a large area, the cascode transistor was not only split in several fingers, but also in several separated transistors (multiplicity "m" of Table 7) to maintain the layout as compact as possible.

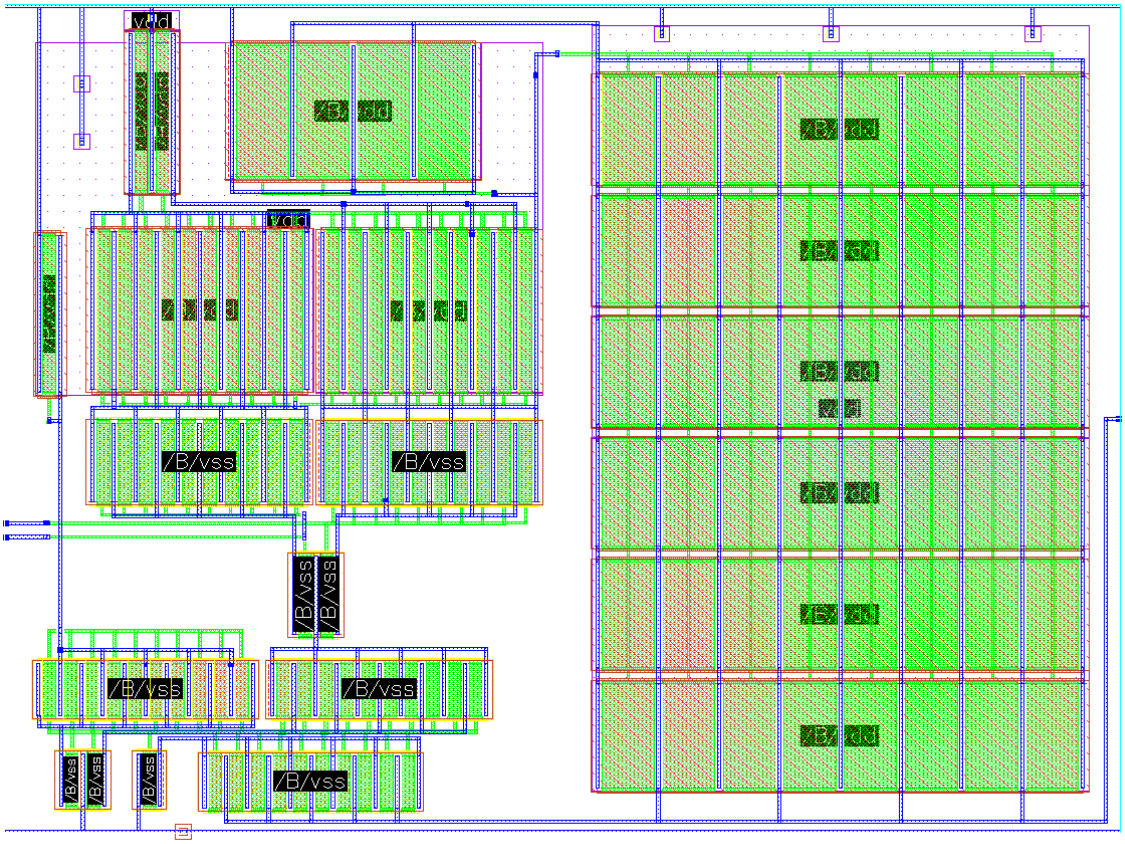

Fig. 5-6. Layout of the self-cascode OTA.

The layout of the TG depicted in Fig. 5-7 is straightforward and very similar to an inverter, with the main difference being the gates of the PMOS and NMOS are not connected to the input as they have a dedicated control pin. This TG is the same implemented on both the 1-bit DAC and SC integrator.

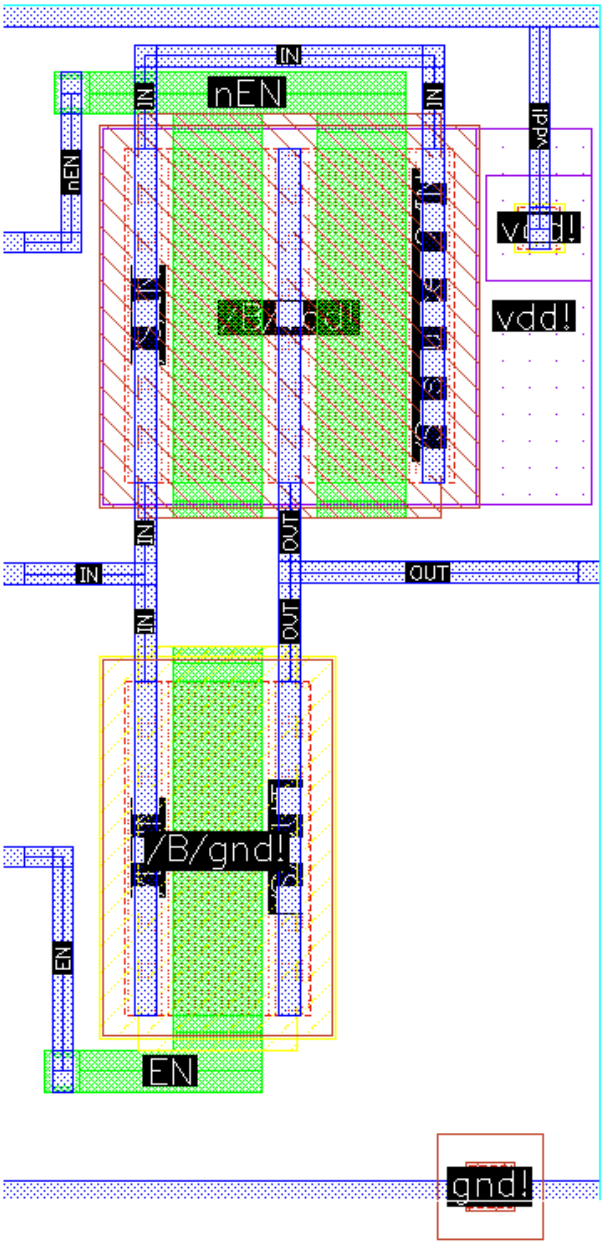

Fig. 5-7. Layout of a Transmission Gate (TG).

5.1.3 Physical design of the Comparator

In the layout of the Comparator depicted in Fig. 5-8 some of the PMOS were stacked on the V_{DD} nets, but on the NMOS it was not possible on all the cells. It can also be noticed some routing on Metal 7 layer as in some nets it wasn't possible to route them in a single trace on Metal 1.

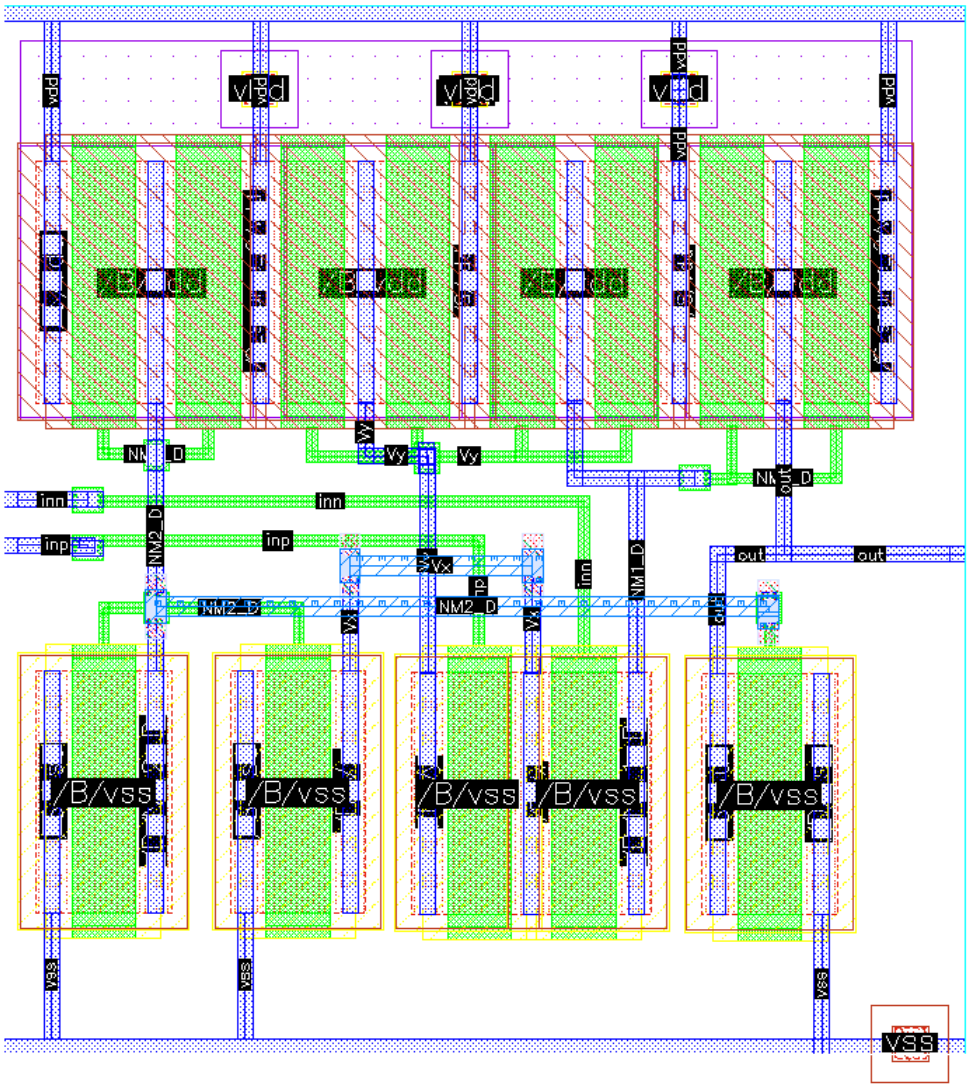

Fig. 5-8. Layout of the Comparator.

5.1.4 Physical design of the 1-bit DAC

The layout of the 1-bit DAC depicted in Fig. 5-9 also required some routing in Metal 7 due to the complexity of routing every net on Metal1, and due to the voltage supply connections of the TG blocks.

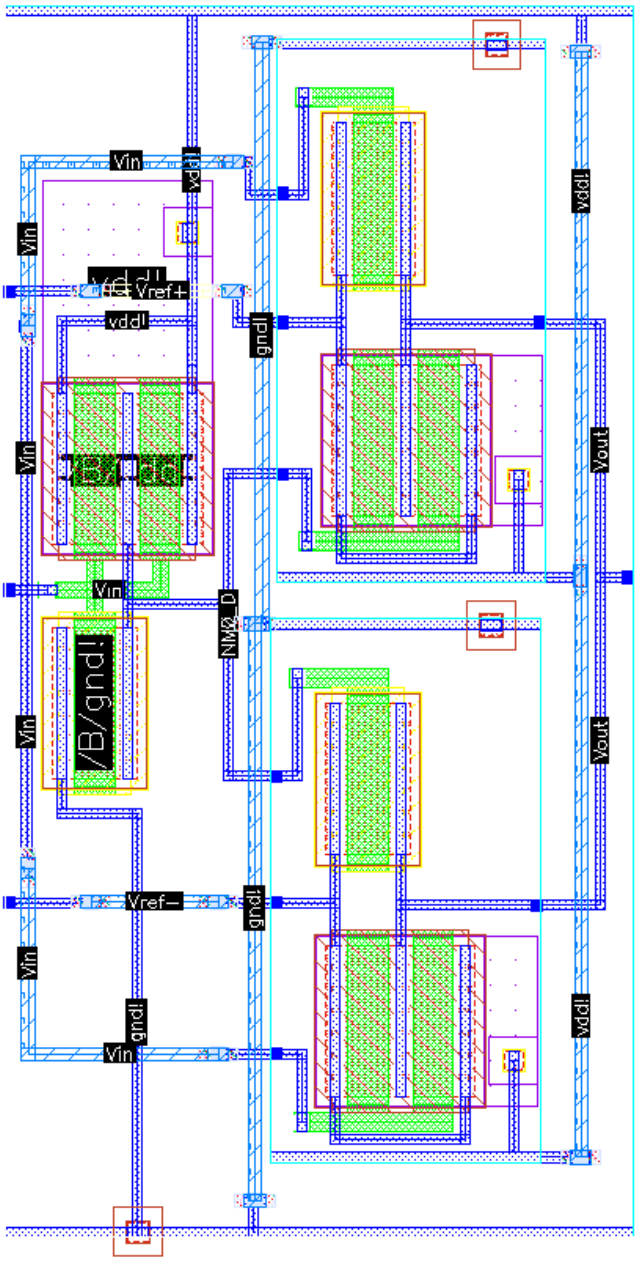

Fig. 5-9. Layout of the 1-bit DAC.

5.1.5 Physical design of the ΣΔ Modulator

In Fig. 5-10 it can be noticed that the SC Integrator takes most of the area of the ΣΔ Modulator due to the big capacitors of the SC technique. The Comparator and 1-bit DAC were place just below the OTA, while the V_{CM} and Feedback (FB) nets were routed back to the SC Integrator in the far left-hand side through Metal 1 and Metal 7 due to the long length it involves, to avoid antennas.

The V_{REF+} and V_{REF-} pins were located near the 1-bit DAC to avoid a long routing near the SC Integrator.

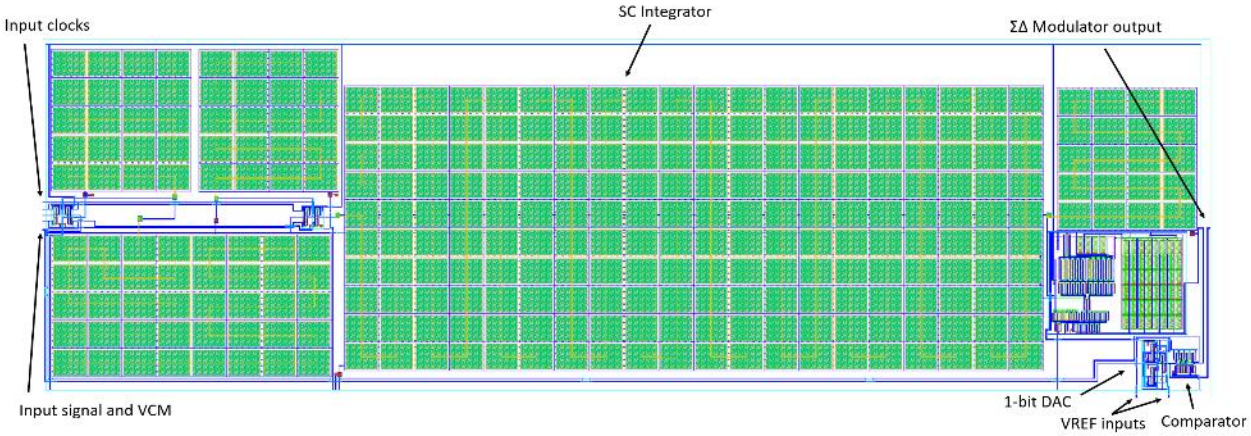

Fig. 5-10. Layout of the ΣΔ Modulator.

Conclusions

This thesis presented the design and implementation of a 12-bit ΣΔ ADC in 45 nm CMOS technology achieving an SNR of 51 dB, an ENOB of 6 bits, and 38.8 µW average power consumption on the ΣΔ Modulator circuitry.

The Switched-Capacitor technique of the integrator, fundamental block on the ΣΔ Modulator, demonstrated a good performance for a variety of oversampling ratios, with a huge trade-off that the capacitors take a huge area in the physical design. The use of TG in the design, increased the clock phases generator complexity as it was needed to create a complimentary clock phase, thus increasing the area of the design. Furthermore, the second stage of the self-cascode OTA helped to achieve the 60 dB gain requirement, although the area was considerably bigger than the transistors of the first stage.

The third-order CIC filter, chosen by its noise shaping and decimation features, helped to achieve a fair ENOB and FOMs, with the main drawback being the delay generated from the cascaded comb filters. The use of Verilog macro models allowed to run simulations and rigorous testing of the ΣΔ ADC outputs, being its RTL views useful for the VLSI implementation in future work.

Overall, even though all the target FoMs of Table 1 weren't completely met, the realization of this mixed-signal oversampling ADC serves as a foundational framework for further research and development, promising enhancements in various domains such as telecommunications, medical instrumentation, and consumer electronics.

Future Work

To improve the SNR and ENOB of the ADC, a differential architecture, and at least a second order ΣΔ Modulator approach should be considered. To address the degraded waveform linearity in the converter's transient response and the extended rise and fall times, the comparator's slew rate should be enhanced.

The individual components of the CIC filter, such as the integrator, differentiator, and clock divider, were modeled using a hardware description language (Verilog). The physical layout is to be implemented using an Automatic Place and Route (APR) tool, which is commonly employed in VLSI (Very Large-Scale Integration) design.

Additionally, the 14-bit output of the CIC filter should be truncated to 12 bits to match the ADC output.

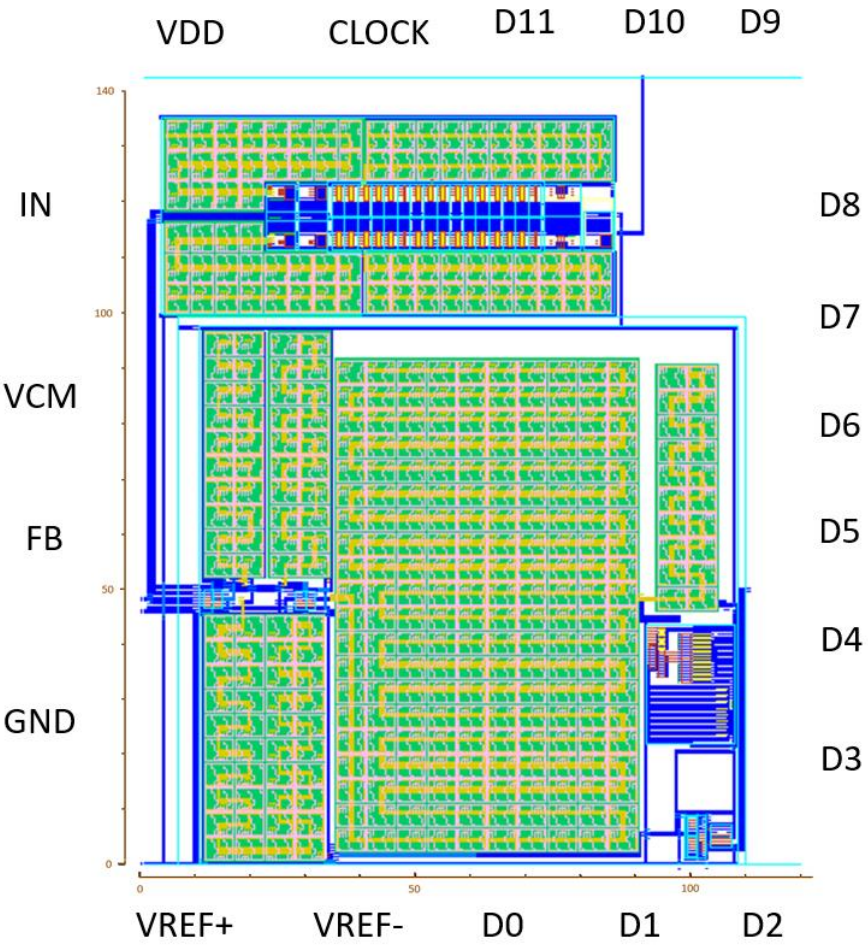

Fig. Floorplan of the ΣΔ ADC.

The Fig. above shows the proposed layout for the ΣΔ ADC. To conserve space, the non-overlapped clocks generator is placed above the ΣΔ ADC modulator, leaving space on the right side for the CIC filter's digital blocks (currently macro models), which are positioned next to the modulator's output.

To accommodate the numerous digital signals, which require a greater number of pins, the reference voltages, feedback signals, and voltage supply pins were situated on the left-hand side, as well as the top-left and bottom-left corners, maximizing available space.

Bibliography

[1] J. Archana and V. Virendra, "Sigma-Delta Modulator Design and Analysis for Audio Application," *International Journal of Engineering Trends and Technology (IJETT),* vol. 28, no. 1, pp. 21-26, 2015.

[2] A. Yeknami, F. Qazi, J. Dabrowski and A. Alvandpour, "Design of OTAs for ultra-low-power sigma-delta ADCs in medical applications," in *International Conference on Signals and Electronic Systems, ICSES'10* , Gliwice, Poland, 2010.

[3] B. Haraoubia, Non-Linear Electronics 2, ISTE Press - Elsevier, 2019.

[4] L. Dután, "Modelación y análisis del relé diferencial para transformadores de potencia con conexión YYd usando ATP-EMTP," 08 2008.

[5] A. Zaalouk, "Waveform Coding Algorithms: An Overview," in *Compression Algorithms*, Aachen, Germany, 2012.

[6] A. A. Eielsen and A. J. Fleming, "Improving Digital-to-Analog Converter Linearity by Large High-Frequency Dithering," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 64, no. 6, pp. 1409-1420, 2017.

[7] T. Eugene and M. sneps-sneppe, "Introduction to signal processing: sampled signals," 05 2019.

[8] R. S. Gamad and D. K. Mishra, "Gain error, offset error and ENOB estimation of an A/D converter using histogram technique," *Measurement,* vol. 42, no. 4, pp. 570-576, 2009.

[9] J. Tourabaly and A. Osseiran, "A Jittered-Sampling Correction Technique for ADCs," *4th IEEE International Symposium on Electronic Design, Test and Applications (delta 2008),* pp. 249-252, 2008.

[10] Y. Tembhre and A. K. Sahu, "Testing of an 8-bit Sigma Delta ADC Based on Code Width Technique Using 45nm Technology," *2016 International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE),* pp. 416-420, 2016.

[11] W. Kester, "Understand SINAD, ENOB, SNR, THD, THD + N, and SFDR so You Don't Get Lost in the Noise Floor," *MT-003,* p. 5, 10 2008.

[12] C. Pappas, "Signal-to-Quantization Noise Ratio of the Parallel Digital Ramp Analog-to-Digital Converter," *Advances in Science, Technology and Engineering Systems Journal,* vol. 4, no. 4, pp. 169-173, 2019.

[13] C. Sosa, "How to use power scaling to maximize power savings in a SAR ADC system," *Analog Design Journal,* p. 2, 2018.

[14] L. Bin, T. Rondeau, J. Reed and C. Bostian, "Analog-to-digital converters," *IEEE Signal Processing Magazine,* vol. 22, no. 6, pp. 69-77, 2005.

[15] S. Badekara Sooryanarayana, "A First Order Discrete Time Sigma Delta Converter," 2018.

[16] M. Sohel, K. Chenna, K. Reddy and S. Abdul Sattar, "Design of Low Power Sigma Delta ADC," *International Journal of VLSI Design & Communication Systems,* vol. 3, 09 2012.

[17] M. Keramat, "Functionality of quantization noise in sigma-delta modulators," *Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems,* vol. 2, no. CH37144, pp. 912-915, 2000.

[18] U. Zakia, "Design and Comparison of 1st Order and 2nd Order Analog Delta Sigma Modulators," *International Journal of Science and Research (IJSR),* vol. 3, p. 1441, 2014.

[19] M. Szermer and A. Napieralski, "Tests of the Sigma-Delta Converter Designed as a Part of Microsystem Dedicated to Water Pollution Monitoring," in *2005 NSTI Nanotechnology Conference and Trade Show - NSTI Nanotech 2005 Technical Proceedings*, Anaheim, 2005.

[20] F. T. Gebreyohannes, M.-M. Louerat and H. Aboushady, "Design of a 4th-Order Feed-Forward-Compensated Operational Amplifier for Multi-GHz Sampling Frequency Continuous-Time Bandpass Sigma-Delta Modulators," *2019 IEEE International Symposium on Circuits and Systems (ISCAS),* pp. 1-5, 2019.

[21] C. Han, T. Kim and N. Maghari, "A continuous-time delta-sigma modulator with self-ELD compensated quantizer," *2018 IEEE Custom Integrated Circuits Conference (CICC),* pp. 1-4, 2018.

[22] S. Manivannan and S. Pavan, "A 1 MHz bandwidth, filtering continuous-time delta-sigma ADC with 36 dBFS out-of-band IIP3 and 76 dB SNDR," *2018 IEEE Custom Integrated Circuits Conference (CICC),* pp. 1-4, 2018.

[23] J. S. Min, H. J. Dong, D. K. Ye, H. Sun, P. K. Jong and T. R. Seung, "A 18.5 nW 12-bit 1-kS/s Reset-Energy Saving {SAR} {ADC} for Bio-Signal Acquisition in 0.18 um," *{IEEE} Trans. Circuits Syst. {I} Regul. Pap.*, Vols. 65-I, no. 11, pp. 3617--3627, 2018.

[24] Z. Huan, C. Weiping, Y. Liang and F. Qiang, "Analysis and design of a fourth-order ΣΔ ADC for MEMS digital gyroscope sensors," *Microelectronics Journal,* vol. 141, 2023.

[25] M. S. Kumar, S. K. Tulasi, R. Arunkanth, M. Nandini and G. Kumar, "A third order sigma delta modulator in 45nm CMOS technology," *Journal of Theoretical and Applied Information Technology,* vol. 95, no. 10, pp. 2139-2146, 2017.

[26] R. Laajimi, "FIRST ORDER SIGMA-DELTA MODULATOR WITH LOW-POWER CONSUMPTION IMPLEMENTED IN AMS 0.35 uM CMOS TECHNOLOGY," *International Journal of Research in Engineering and Technology,* vol. 2, no. 4, pp. 700-705, 2013.

[27] . B. Nowacki, *Design of sigma-delta modulators for analog-to-digital conversion intensively using passive circuits*, Lisboa, 2016.

[28] M. Liu, Demystifying Switched-Capacitor Circuits, China: Newnes, 2006.

[29] M. Smoszna, "Noise Tolerance," *Synchronous Precharge Logic*, pp. 27-45, 2012.

[30] P. Mandal and V. Visvanathan, "A new approach for CMOS op-amp synthesis," in *Proceedings of the IEEE International Conference on VLSI Design*, Bangalore, 1999.

[31] V. Vincence, C. Galup-Montoro and M. Schneider, "A high-swing MOS cascode bias circuit," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 47, pp. 1325 - 1328, 2000.

[32] P. M. Furth, Y.-C. Tsen, V. B. Kulkarni and T. K. Poriyani House Raju, "On the design of low-power CMOS comparators with programmable hysteresis," *2010 53rd IEEE International Midwest Symposium on Circuits and Systems*, pp. 1077-1080, 2010.

[33] Jaydip.H.Chaudhari, "Design and Simulation of 1-bit Sigma Delta ADC in 0.18um," *International Journal of Computer Applications & Information Technology*, vol. II, no. I, p. 52, January 2013.

[34] M. Karimian, "A New SPICE Macro-Model for Simulation of Single Electron Circuits," *Journal of Korean Physical Society*, vol. 56, p. 1202, 2010.

[35] C.-M. Wu, H.-C. Chen, M.-Y. Yen and S.-C. Yang, "Chopper-Stabilized Instrumentation Amplifier with Automatic Frequency Tuning Loop," *Micromachines*, vol. 9, no. 6, p. 289, 2018.

[36] J. B. Burr, L. Weiping and M. P. Allen, Digital Signal Processing Systems: Implementation Techniques, vol. 68, Academic Press, 1995, pp. 1-88.

[37] T. Levi, J. Tomas, N. Lewis and P. Fouillat, "Resizing methodology for CMOS analog circuit.," *Proceedings SPIE VLSI Circuits and Systems III*, vol. 00, May 2007.

[38] L. Bisdounis, S. Nikolaidis and O. Koufopavlou, "Analytical transient response and propagation delay evaluation of the CMOS inverter for short-channel devices," *IEEE Journal of Solid-State Circuits, Solid-State Circuits, IEEE Journal of, IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 302-306, 1 2 1998.

[39] K. Lata and M. Duhan, "Design of a Decimator Filter for Novel Sigma-Delta Modulator," *IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)*, vol. 2, no. 1, pp. 31-37, Mar. – Apr. 2013.

[40] D. Marinov, "VHDL whiz: Part 3: FIR filter types," Jensen Tech, 23 March 2022. [Online]. Available: https://vhdlwhiz.com/part-3-fir-filter-types/. [Accessed 28 January 2024].

[41] R. Teymourzadeh, "VLSI Design Of Advanced Digital Filters," *ArXiv*, 06 2018.

[42] M. Hema Madhuri, "Third order CMOS decimator design for sigma delta modulators," 2009.

[43] C. K. F., G. P.K. and T. T.H., "Low power approach for decimation filter hardware realization," *Proceedings of World Academy of Science, Engineering and*, vol. 32, pp. 2070-3740, August 2008.

[44] Maxim, "Selecting the Optimum Test Tones and Test Equipment for," *Application Note AN-1819*, 18 Dec 2002.

[45] S. P. e. al., "A 10-bit 20-MS/s asynchronous SAR ADC with controllable analog input voltage range and meta-stability detection circuit," in *International SoC Design Conference (ISOCC 2014)*, Korea, November 3–6 2014.

[46] G.-Y. Huang, S.-J. Chang, C.-C. Liu and Y.-Z. Lin, "10-bit 30-MS/s SAR ADC Using a Switchback Switching Method," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 3, pp. 584-588, 2013.

[47] M. Nasrollahpour and S. Hamedi-Hagh, "Extra Bit Generation for High-Speed Time-Based Flash ADCs in 65nm CMOS," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, 2018.

[48] Y.-K. Cho, J.-H. Jung and K. C. Lee, "A 9-bit 100-MS/s flash-SAR ADC without track-and-hold circuits," in *2012 International Symposium on Wireless Communication Systems (ISWCS)*, Paris, France, 2012.

[49] D. Ghai, S. Mohanty and E. Kougianos, "A 45nm Flash Analog to Digital Converter for Low Voltage High Speed System on Chips".

[50] L. A. Carrillo Martinez, *ADC Tipo Folding de 7 Bits en Tecnologia SOI de 45nm*, Tonantzintla, Puebla, 2011.

Appendix A: Verilog Code

```
//Verilog HDL for "Schematic_Mario", "Integrator_cic" "functional"
module Integrator_cic # (parameter WIDTH = 14)

(
input signed [WIDTH -1 : 0]  X,
input clk, rst,
output  reg signed [WIDTH -1 : 0] Y);

always @(posedge rst or posedge clk)
    begin
        if (rst)
            Y <= {WIDTH{1'b0}};
        else
            Y <= Y + X;
    end



//Verilog HDL for "Schematic_Mario", "Differentiator_cic" "functional"
module Differentiator_cic # (parameter WIDTH = 14)

(
input signed [WIDTH -1 : 0]  X,
input clk, rst,
output reg signed [WIDTH -1 : 0] Y);

reg signed [WIDTH -1 : 0] Q;
```

```
always @(posedge rst or posedge clk)
    begin
        if (rst)
            begin
            Y <= {WIDTH{1'b0}};
            Q <= {WIDTH{1'b0}};
            end
        else
            begin
            Q <= X;
            Y <= X-Q;
            end
    end
endmodule
```

```
//Verilog HDL for "Schematic_Mario", "Clock_divider_cic" "functional"
//Output with duty cycle 50%

module Clock_divider_cic # (parameter K = 16, WIDTH = 6)

(
input clk, rst,
output reg clk_out);


reg[WIDTH -1 : 0] counter = {WIDTH{1'b0}};

wire ovf_flag;

assign ovf_flag = (counter == K/2)?1'b1:1'b0;

always @(posedge rst or posedge clk)
    begin
        if (rst)
            begin
            counter <= {WIDTH{1'b0}};
            clk_out <= 1'b0;
            end
        else
            begin

            if(ovf_flag)
            begin
            counter <= {WIDTH{1'b0}};
            clk_out <= ~clk_out;
            end
            else
```

```
            counter <= counter + 1'b1;
            end
    end
endmodule
```

```
//Verilog HDL for "Schematic_Mario", "coder_verilog" "functional"

module coder_verilog #(parameter CN = 14) (
input x,
output reg[CN-1:0] data_out
);

always @ (x)
    begin
    case(x)
    1'b1: data_out = 14'b00000000000000000;
    1'b0: data_out = 14'b11111111111111111;
                default:data_out = 14'b11111111111111111;
    endcase
    end

endmodule

//Verilog HDL for "Schematic_Mario", "CIC_verilog_v1" "functional"


module CIC_verilog_v1 # (parameter WIDTH = 14, K = 16, CLKDIV_WIDTH = 6)

(
input wire X, clk, rst,
output wire signed [WIDTH -1     : 0] ADC_out
);

wire signed [WIDTH -1 : 0] I1, I2, I3, D1, D2, X_coded, Y;
wire clk_div;
```

```
Clock_divider_cic # (.K(K), .WIDTH(CLKDIV_WIDTH)) Decimator_clk (.clk(clk),
.rst(rst),.clk_out(clk_div));
coder_verilog # (.CN(WIDTH)) coder_0(.x(X), .data_out(X_coded));

Integrator_cic # (.WIDTH(WIDTH)) integrator_0 (.X(X_coded), .clk(clk),
.rst(rst), .Y(I1));
Integrator_cic # (.WIDTH(WIDTH)) integrator_1 (.X(I1), .clk(clk), .rst(rst),
.Y(I2));
Integrator_cic # (.WIDTH(WIDTH)) integrator_2(.X(I2), .clk(clk), .rst(rst),
.Y(I3));
Differentiator_cic # (.WIDTH(WIDTH)) differentiator_0 (.X(I3), .clk(clk_div),
.rst(rst), .Y(D1));
Differentiator_cic # (.WIDTH(WIDTH)) differentiator_1 (.X(D1), .clk(clk_div),
.rst(rst), .Y(D2));
Differentiator_cic # (.WIDTH(WIDTH)) differentiator_2 (.X(D2), .clk(clk_div),
.rst(rst), .Y(Y));
assign ADC_out = (Y -10500);

endmodule
```