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Especialidad en Diseño de Sistemas en Chip

Dynamic comparator, SR latch and bootstrap switch for 10 bits SAR ADC for biomedical applications.

TRABAJO RECEPCIONAL que para obtener el **GRADO** de
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Abstract

This document presents the design of a Dynamic Comparator, a SR Latch and a Sample and Hold circuit for a 10 bits SAR ADC. Designs are performed using TSMC 0.18 um CMOS technology with 1.8 V supply voltage.

The Dynamic comparator with Strong Arm topology is chosen to fulfill the requirements of SAR ADC. Its performance is tested at simulation level with a clock frequency of 10 KHz to 310 MHz, using typical parameter of process, nominal supply voltage and room temperature. Although, results are presented only at clock frequency of 100 KHz. This analysis showed that comparator has an input offset of 17.8 mV and power consumption of 36.27 nW. Power consumption is in the power budget of SAR ADC however, the input offset voltage has limited the resolution of SAR ADC.

The SR latch is designed at transistor level using NAND gates. The circuit has additional digital logic and an external reset pin in order to avoid the prohibited condition. After implementing this modification, it shows a correct functionality at a clock frequency of 100 KHz.

The sample and hold circuit is designed with a bootstrap switch for a load capacitance of 300 pF which is the total capacitance of the circuit when it is integrated to the SAR ADC.

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1. ADCs for biosensor applications

1.1. Analog to digital conversion

Analog to digital converters (ADCs) translate analog signals, which are characteristic of most phenomena in the world, into a digital signal, to be processed in digital systems (Floyd, 2014). Since "real world" is analog and processing is digital, data converters are used in electronic circuits as an interface between analog and digital world, and play a fundamental role in most of the applications, such as industrial, telecommunications, automotive, medical, etc.

The basic operation of an ADC in signal processing flow is shown in Figure 1 and can be explained in four steps: sampling, analog to digital conversion, digital signal processing, and digital to analog conversion (Floyd, 2014).

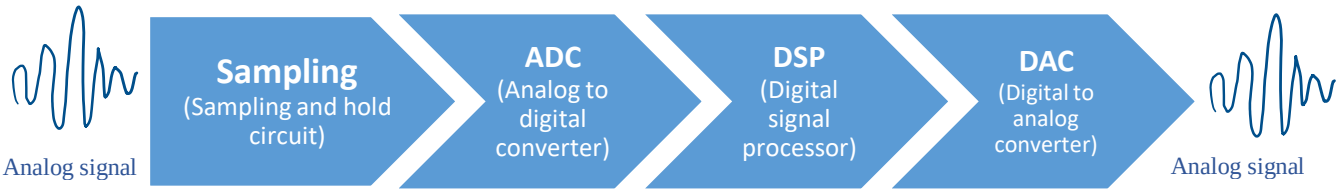


Figure 1: Analog to digital conversion process

Sample and hold.

Sampling is the process to take the value of the input signal sufficient times to have enough information of the input signal. This process converts an analog signal into a series of impulses, each one representing the amplitude of the signal at an instant in time. The more samples are taken, more accurate is the waveform.

The holding operation ensure the sampled value must be held constant for an instant defined, until the next sample is taken. This is necessary for the ADC to have time to process the

sampled value. These sample and hold process results into a stairstep waveform that approximates the analog input signal, this is shown in Figure 2.

Analog to digital conversion

Is the process of converting the output of the sample and hold circuit into a series of binary codes that represent the amplitude of the analog input signal at each sample time. The ADC makes the codification in the time between sample pulses, or the time that sample and hold circuit is holding the sampled value. This process is called quantization.

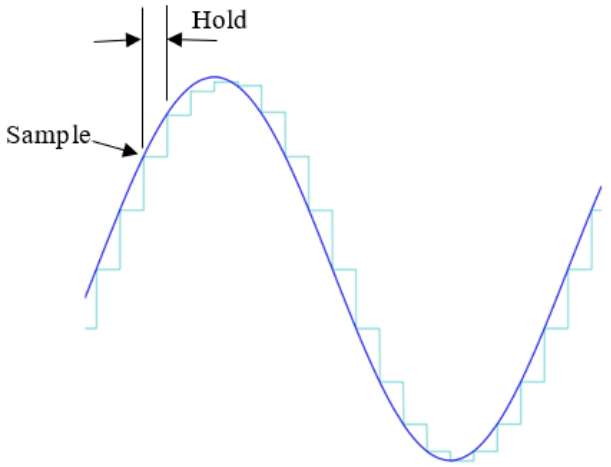


Figure 2: Analog signal and its stairstep approximation.

Digital Signal Processor (DSP)

DSP takes its input of the ADC and produces an output, also digital that goes to a DAC for conversion back into an analog form. It is a specialized microprocessor chip, with its architecture optimized for the operational needs of digital signal processing and its goal is to process data in real time.

Digital to analog conversion

Is the process of transforming data or the result of the digital processing, back to an analog signal to send to back to “real world” most of the DACs perform two basic functions: convert the digital input into an equivalent analog signal and reconstruction of the signal.

1.2. SAR ADC architecture

There are many architectures to convert analog signals to digital. In our proposal, a successive approximation register (SAR) ADC Architecture is chosen. The block diagram of a SAR ADC is shown Figure 3. The operation principle is as follows: the circuit samples an input signal *Vin* and compares it to several voltages that are generated by a digital to analog converter (DAC). The successive approximation register (SAR) controls the voltage of the DAC and saves the results of the comparison.

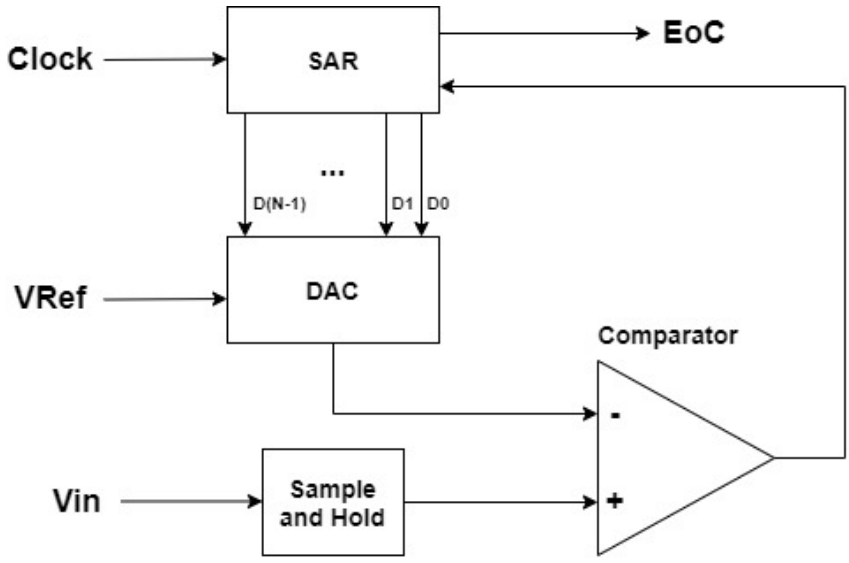


Figure 3: Schematic of a SAR ADC

In Figure 3, the schematic of a basic SAR ADC is show. The main modules of this architecture are: a sample and hold circuit, a comparator, a DAC, and the SAR.

As stated before, the SAR controls the voltage that the DAC outputs. It starts by assigning a 1 to the most significant bit (MSB). This is done because that is the half-way value of the voltage that the DAC works with. The next step is to compare if the sampled voltage is greater than the voltage of the DAC. If it is bigger, the Comparator has an output of 1 (or the equivalent analog voltage) that the SAR saves, and then the SAR assigns a 1 to the next significant bit repeating the

process. But if the sampled voltage is smaller than the original DAC's voltage, then the SAR saves a 0, turn the MSB to 0 and assigns a 1 to the next significant bit, starting the cycle again.

A SAR ADC converts a bit in each cycle, so depending on the resolution of the ADC is the minimum number of cycles that they are needed to do a conversion.

1.3. Capacitive split-array DAC architecture

As explained before, a SAR ADC needs a Digital to Analog Converter (DAC) to generate the voltages that will be compared against the input voltage. Since this project wants to be used in biosensor application, the proposal that we choose must consume the least amount of power and must be as small as possible. For this reason, we choose a capacitive split-array architecture for our DAC.

There are many architectures for implementing a DAC and most of them use either resistors or capacitors to generate voltage as their main component. The difference between using one or the other component is that resistors are elements that are constantly consuming power since they only work in a state, meanwhile capacitors consume power depending on the state the capacitor is in. If the capacitor is working then it consumes power, but if it is not working then it won't. This behavior is what push us to use an architecture based in capacitor.

The most common capacitor architecture that is used is called Charge-Scaling Capacitors which can be seen in Figure 4.

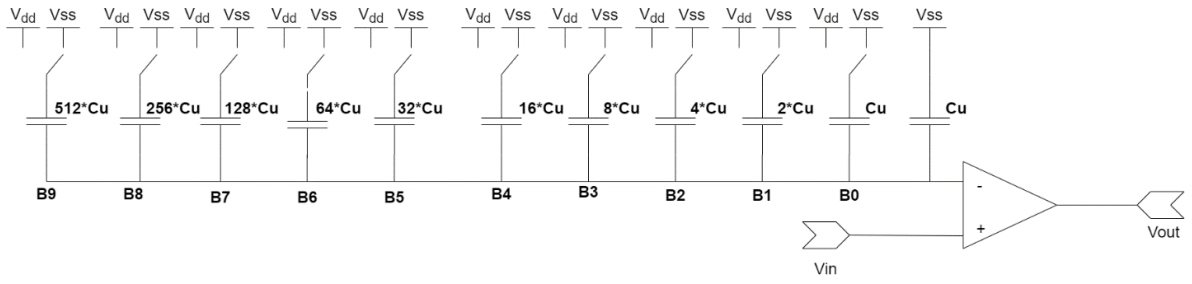


Figure 4: Schematic of Charge-Scaling Capacitors Architecture (Baker, 2010)

The DAC has a capacitor for each of the bits of the resolution of the component. Figure 4 shows the schematic of a 10 bits DAC. Each of the capacitor represents a bit, except the last one that is used to reduce the noise of the node. Each of the capacitor will switch between V_{SS} and V_{DD}, depending on what the SAR will assign to the control signals. This process starts from the MSB to the LSB.

The main problem with this architecture is that capacitor value of the MSB is 2^{n-1}; where *n* is the DAC resolution. In the example of Figure 4, the MSB capacitor is 512 times bigger than the smallest one, i.e., the unity capacitance Cu. Having large capacitors is not desirable because they are area-consuming, and area is an important tradeoff when designing a chip. The larger they are, the more expensive they are, and they consume more power.

In order to reduce the power consumption of DAC, the capacitive split-array topology is utilized. Is shown in Figure 5.

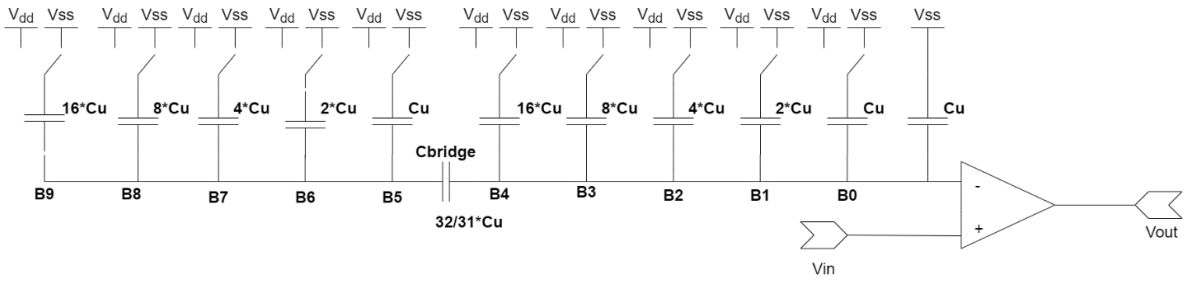


Figure 5: Schematic of capacitive split-array architecture (Baker, 2010)

The architecture called “Capacitive Split-Array” fixes this issue by dividing the capacitors in two arrays, one for the least significant bits (LSB) b0 to b4 and the other one for the most significant bits (MSB) b5 to b9. Both arrays have capacitors from the same magnitude, and this works because of the bridge capacitor between both arrays (Cbridge). The only difference between the array is that the one for the LSBs also has the extra capacitor to provide the correct divisor factor in the inverting node. The value of the bridge capacitor can be calculated using equation 1:

$$C_{bridge} = \frac{Sum\ of\ LSB\ Capacitance}{Sum\ of\ MSB\ Capacitance} * Cu$$

Eq 1: Equation for calculation the bridge capacitor in Capacitive Split-Array architecture

Capacitive split-array have all the benefits of charge-scaling capacitors using smaller capacitors. The only disadvantage is that by adding the Cbridge, the system will stop having a linear behavior which would complicate fixing mistakes if the capacitor arrays are not properly balanced (Zhu, et al., 2014).

1.4. SAR ADC block diagram

Figure 6, shows the block diagram of the low power SAR ADC proposal of this work.

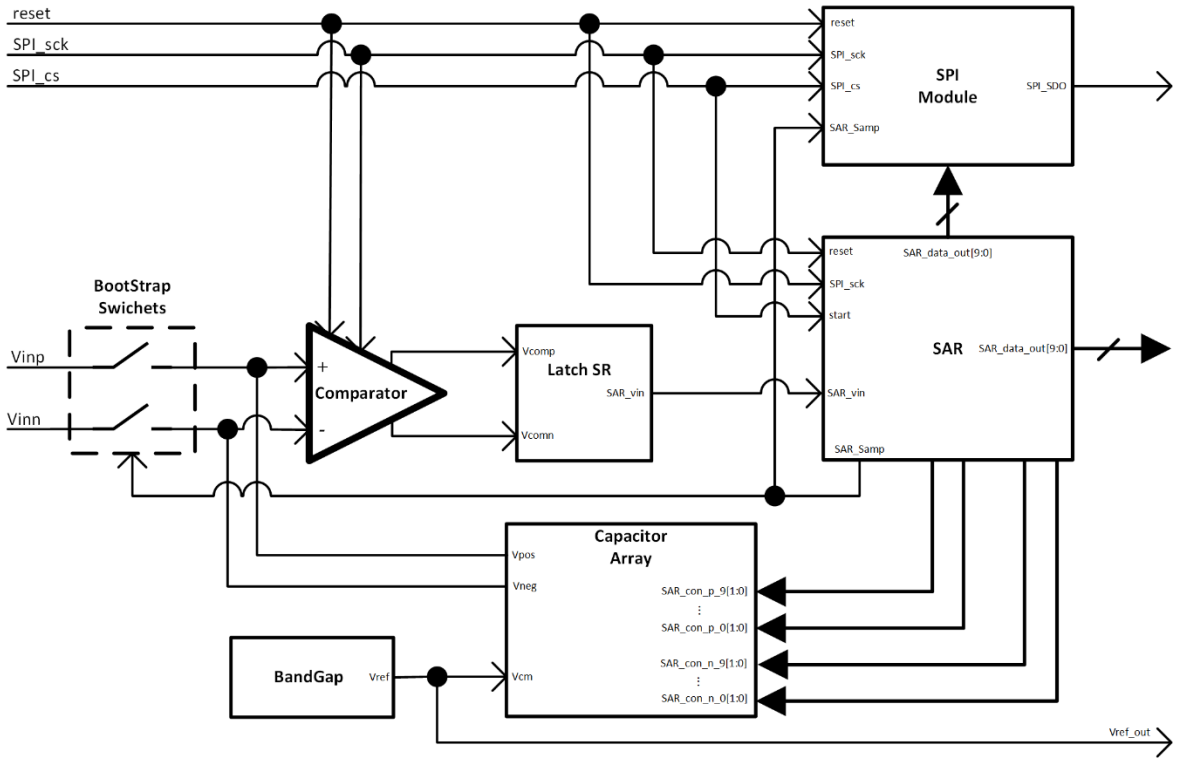


Figure 6: Proposal of low power SAR ADC block diagram.

1.5. Functional description of low power SAR ADC block diagram

The SAR ADC is made by different functional blocks.

Serial Interface: the SPI module is which send the conversion result from the SAR module to an external signal in a serial format.

BandGap: This module supplies a reference voltage to the capacitor array. This module is supplied by 1.8V and provides a stable output of 900 mV ±500 µV.

SAR: It converts the analog signal into a digital signal The digital signal contains 10 bits, named *SAR_data_out [9:0]*, that are sent directly to the SPI module and to the exterior.

Capacitor Array: This module consists of a Digital to Analog block that generates voltages to be compared to two external signals, *Vinp* and *Vinn*.

Comparator: It compares the two external signals, *Vinp* and *Vinn*, after they have been sampled by the BootStrap Switches.

Latch SR: once the comparison between *Vinp* and *Vinn* has been finished, the Latch SR module converts the differential ouput signal, from the comparator to a single ended output.

2. The dynamic comparator

A comparator is a circuit used to compare two analog voltages or currents and generates a logical output according to input difference. If voltage in the positive input (*INP*) is higher than the voltage in the negative input (*INN*), then the output of comparator will be a logic 1. By contrary, if *INP* is smaller than *INN*, then the output of comparator will be a logic 0 (Mishra & Kumar, 2018).

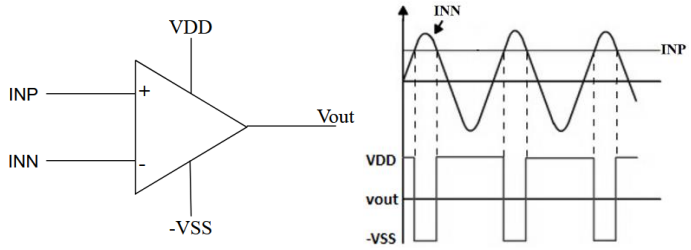


Figure 7: Conceptual diagram of a comparator

In SAR ADC´s, to make the conversion of the analog input voltage into a digital output it is necessary to compare the input voltage captured by Sample and Hold circuit with a digital voltage calculated by SAR module. Thus, the comparator is one of the main modules of a SAR ADC, because it will decide if DAC voltage is higher or lower than the input voltage. Depending on the output of the comparison, the SAR will change its digital output and send it to DAC to convert it into an analog signal and compare it with input voltage again, this process repeats until digital output will be equivalent to the analog input.

There are two types of comparators: static and dynamic comparators, last one also called clocked comparators. Clocked comparators have an extra input to connect a clock signal (Fig. 8), so the output changes according to the clock edges.

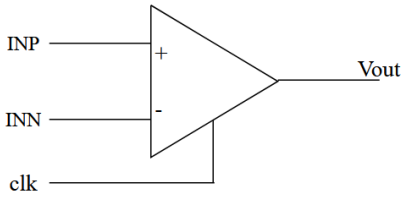


Figure 8: Circuit of a dynamic comparator

The dynamic comparators are mostly preferred to statics because the operating speed of dynamic comparators is faster and power consumption is lower.

Advantages of dynamic comparators are mainly high speed, high slew rate and low power consumption. In contrast, static comparators present high gain, low offset voltage, high input resolution, noise, and input common mode range. A proper selection of a comparator type and topology depends on the application.

In technical literature, one can find different architectures of dynamic comparators: strong ARM, latch Comparator, dynamic latched comparator, resistive divider comparator, conventional dynamic, conventional double tail, lewis Gray Comparator, etc. (Sangeetha, et al., 2019).

2.1. The strong arm comparator

In this project a modified strong arm comparator (Figure 9) presented by (Razavi B. , 2020) will be used. The topology is select because it fulfills requirements for the present project of SAR ADC, that is, low offset, low power, area efficiency and high speed.

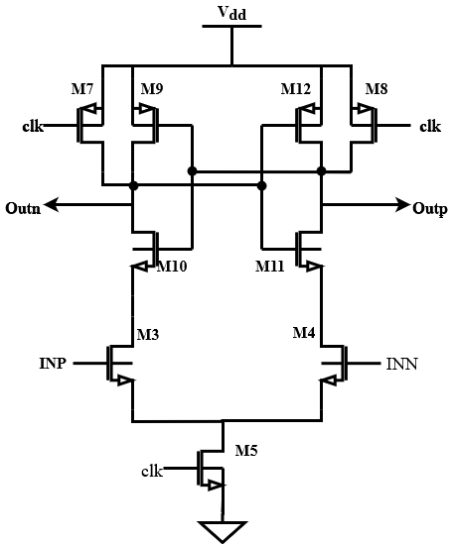


Figure 9: Modified strong arm dynamic latch comparator (Razavi B. , 2020)

Typically, transistors of dynamic comparator are sized in terms of speed, power consumption, and input offset voltage specifications. For the present comparator structure, we have followed the guidelines reported in (Razavi B. , 2020); in this case, the pairs M1 and M2, M3 and M4, and M5 and M6 in Figure 9 appear in the signal path and must be crafted first.

The offset voltage in MOSFET depends inversely on the size ratio W/L according to Eq. 1.1.

$$Vos = \left(\frac{VDsat}{2}\right)\left(\frac{\Delta W/L}{W/L}\right) \quad \text{(1.1)}$$

where ΔW/L is the geometrical variation of W/L in the manufacture process of MOSFET in a differential pair array.

The speed of clocked comparators depends on the propagation delay (Nurul Iffah Mohamad Aziz-2015)

$$Speed = \frac{1}{Propagation\ delay} \quad \text{(1.2)}$$

$$Propagation\ delay = \frac{t_{PHL}+t_{PLH}}{2} \quad \text{(1.3)}$$

Where:

t_{PHL} = delay time when output change from high to low

t_{PLH} = delay time when output change from low to high

$$t_{PHL} = \frac{(C_G+C_P)(C_{OH}/2)}{\mu C_{ox}\,(W/2L)_n\,(V_{OH}-V_{Tn})^2} \quad \text{(1.4)}$$

$$t_{PHL} = \frac{(C_G+C_P)(C_{OH}/2)}{\mu C_{ox}\,(W/2L)_n\,(V_{OH}-V_{Tn})^2} \quad \text{(1.5)}$$

The power of the dynamic comparators has rarely been investigated and usually the formula, (1.6), for dynamic power consumption considering supply current and clock speed is used to estimate the power in clocked comparators (N. Ghaziani, 2020), (S. Babayan-Mashhadi, 2013).

$$Power = (f_{Clk})(V_{DD})(Isupply) \quad \text{.....(1.6)}$$

Since f_{CLk} is defined by the operation frequency of SAR ADC, and the V_{DD} is fixed by the CMOS technology, then the solo variable to define the power consumption is the *Isupply*, this is the reason why we have chosen the simplest structure of dynamic comparator presented in Figure 9.

According to Eq. 1.1, Eq. 1.4, and Eq. 1.5, to achieve a lowest offset voltage and high speed, we should use large size of transistors. In this sense we have defined size of transistors M1 to M6 as they are summarized in Table 1 in Appendix B.

The tail transistor M7 in Figure 7 must draw sufficient current with $V_{GS7}=V_{DD,}$ and $V_{DS7}=Vin_{CM}$ - $V_{GS1,2}$, where Vin_{CM} denotes the input common -mode (CM) level. With Vin_{CM} = 0.5 V and $V_{GS1,2}$. 0.35V, we have V_{DS7}. 0.15 V. The device thus operates in the deep triode region.

2.2 Design of the strong arm comparator

For ADC applications, the comparator design parameters are mainly: input offset, speed, power consumption, metastability, kickback noise, and input-referred electronic noise (Razavi B. , 2020).

The schematic of the modified strong arm dynamic comparator is shown in Figure 10.

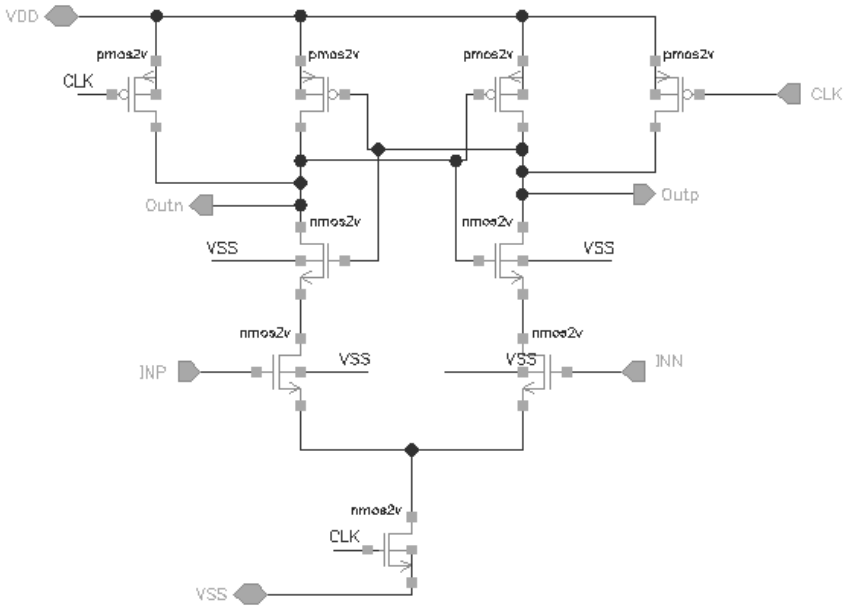


Figure 10: Modified strong arm dynamic latch comparator (Razavi B. , The StrongARM latch [a circuit for all seasons], 2015)

To verify the correct functionality of the comparator, a testbench was created in Virtuoso; it consisted of a sinusoidal signal 1.8 V amplitude with 2 KHz frequency applied at the input terminal *INN*, while a DC voltage is set to 900 mV at the positive terminal *INP*. Clock with frequency of 10 KHz is used to drive the comparator. Figure 11 shows the output voltage of the Comparator, *Outn* in blue color and *Outp* in purple colors respectively.

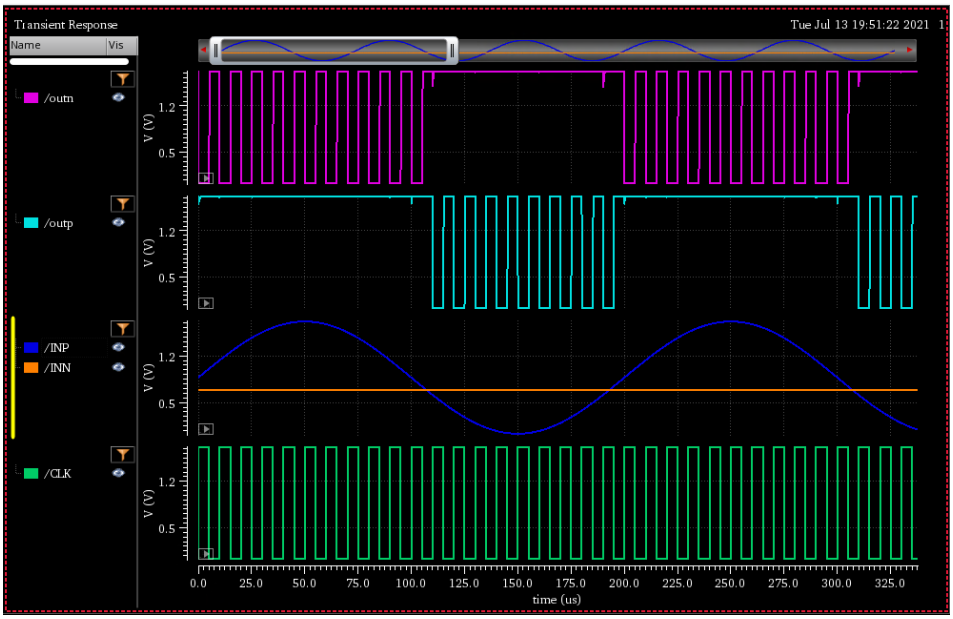


Figure 11: Transient response of the dynamic comparator

It is important to be noted in the comparator response (Figure 11), that the output of the comparator is a pulsed waveform. However, SAR requires a steady output, so according to (Sharuddin & Lee, 2015) a SR latch needs to be added to hold the comparator output during reset to avoid consume unnecessary power. In the next chapter, the design of SR latch is presented.

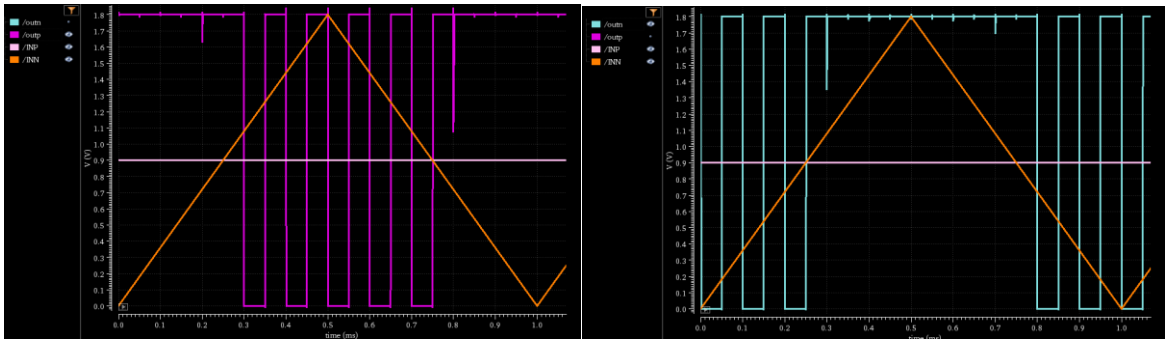
2.3 Strong arm performance

Since comparator is one of the most critical devices in the ADC circuit, is important to characterize its main parameters, so it will be able to respond correctly.

2.3.1 Input offset

Since the input offset voltage affects the comparator resolution, we have considered this as the main important parameter to be measured in the designed comparator. We remember that offset voltage is the differential input voltage necessary to make the comparator toggle.

Figure 12 shows a conventional way to measure input offset, basically it consists in applying a triangle signal in one of the inputs and a DC voltage in the other. From the waveforms obtained it is clear that *outp* does not change immediately when input *INN* (line in orange color) is higher than *INP* (line in rose color) but there is an input offset, and additionally if we compare its behavior with *outn* we can note that offset is not symmetric.



(a) (b)

Figure 12: Conventional offset measurement at *outp* (a) and *outn* (b)

It is difficult to determine properly the input offset voltage of the comparator, as different inputs must be tried to find the actual voltage required to make the comparator toggle. In order to minimize possible error in measuring offset, we will use the technique reported in (T. W. Matthews, 2005) which is shown in Figure 13.

The implementation of the test bench is shown below

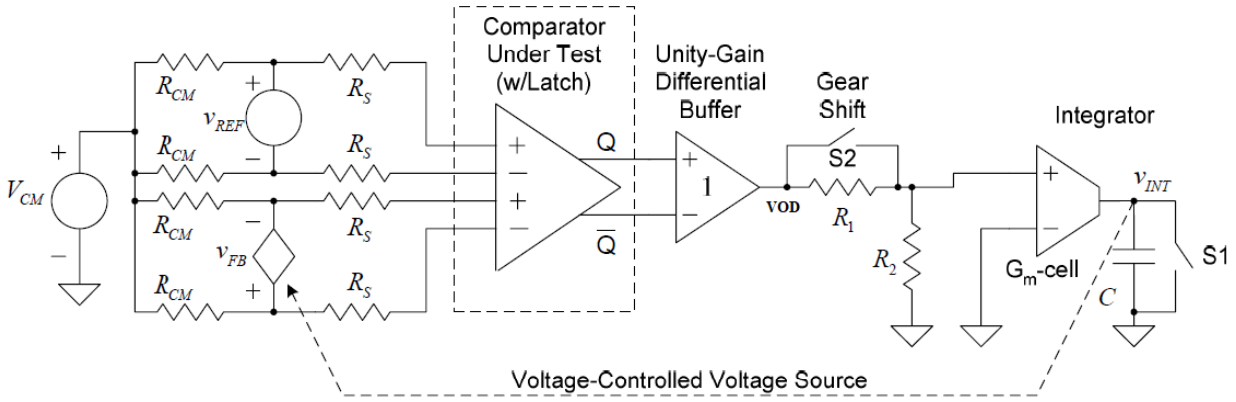


Figure 13: Practical implementation of the dynamic offset test bench implemented by (T. W. Matthews, 2005)

The functionality of this test bench is described in (T. W. Matthews, 2005) "The comparator under test is enclosed in a negative feedback loop containing an integrator. To ensure symmetry at after the comparator the test bench uses an ideal unity gain differential buffer. The loop has infinite DC gain due to the integrator, which implies that in equilibrium the average value of V_{OD} is driven to zero. In this equilibrium condition, the average value of $V_{REF} – V_{FB}$ is equal to the decision threshold of the comparator. After each comparison, the input of the comparator slews across the decision threshold. Since $V_{REF} – V_{FB}$ is a triangle wave, it is straightforward to calculate its average value, which is the input offset voltage."

The implementation of the test bench shows in Figure 14. Ideal dependent sources were used to simulate the unity gain differential buffer and the integrator module, that is, the unity gain differential buffer was replaced by a voltage-controlled voltage source and the integrator by a voltage controlled current source.

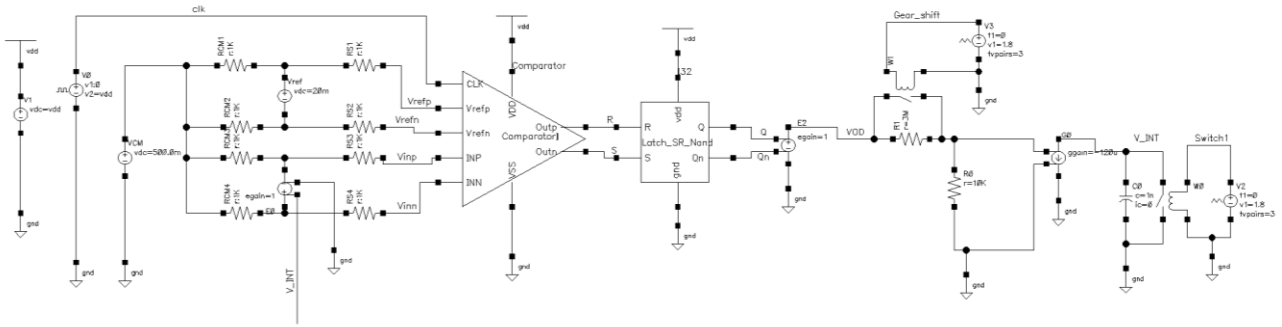


Figure 14: Schematic of the dynamic offset test bench implemented by (T. W. Matthews, 2005).

In the implementation of the test bench, values of the components are RCM=1 KΩ, RS=1 KΩ, VCM=500 mV, V_{REF}=20 mV, V_{FB} is a voltage-controlled voltage source which is controlled by the integrator voltage signal (V_{INT}), R1=3MΩ, R2=10KΩ, gain of the voltage-controlled current source which forms the integrator circuit is –120 us. Switches gear shift and S1 are simulated by piece-wise generators, in the simulation gear shift is closed by 15 ms then remains open. S1 is closed after 250 µs then it remains open. Simulation results are shown in the Figures 15, 16 and 17.

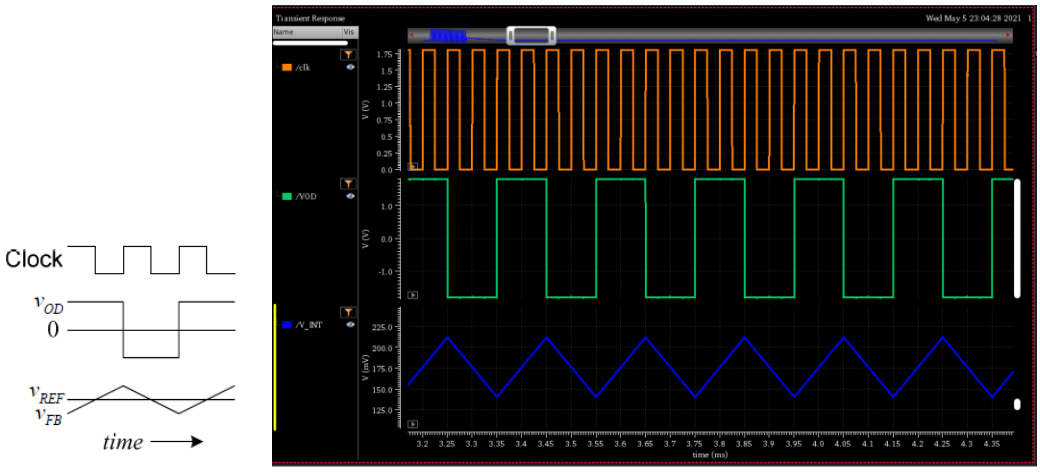


Figure 15: Wave forms of the buffer output V_{OD} (green line) and V_{FB} (blue line) and input signals

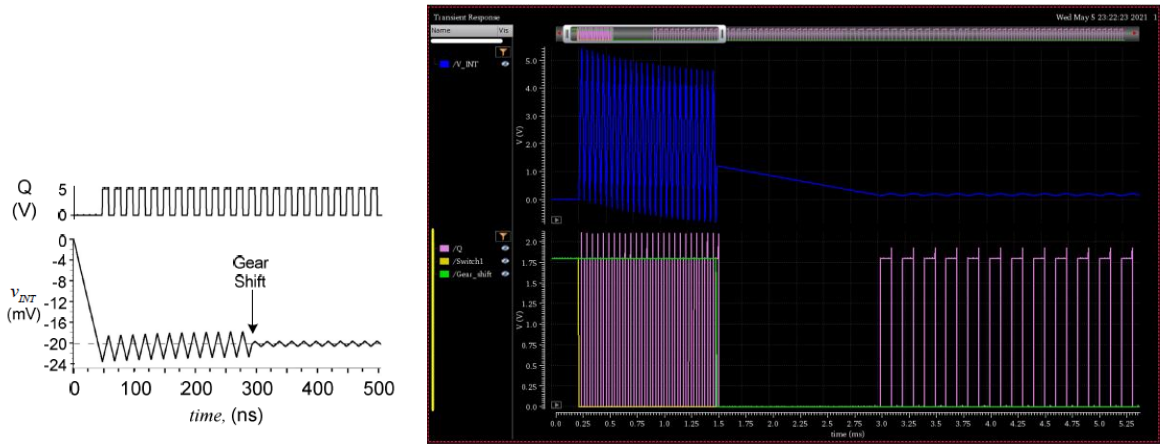


Figure 16: Wave forms of the Latch Q (purple line) and Integrator´s output V_{INT} (blue line)

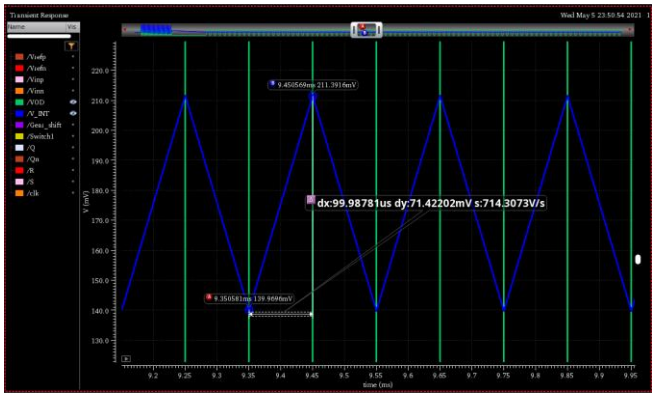


Figure 17: Closed-up of VINT waveform in the time interval of 9-10ms to measure of the dynamic offset

Every simulation result is compared with response of reference (T. W. Matthews, 2005) to show the correct operation of the test bench. In Figure 17, the measurement of the dynamic offset is performed calculating the average of triangular signal which is vp/2. Applying this procedure, we can observe than the input offset voltage of the designed comparator is 17.85 mV

2.3.2 Power consumption

Power consumption was measured using calculator tool of Virtuoso as the product of average value of current in the supply voltage multiplied by V_{DD}. Figure 18 shows current signal (yellow curve) and supply voltage (green curve) in the time interval of 3 ms of simulation. As shown in Figure 19, the power consumption of this comparator is 36.27 nW.

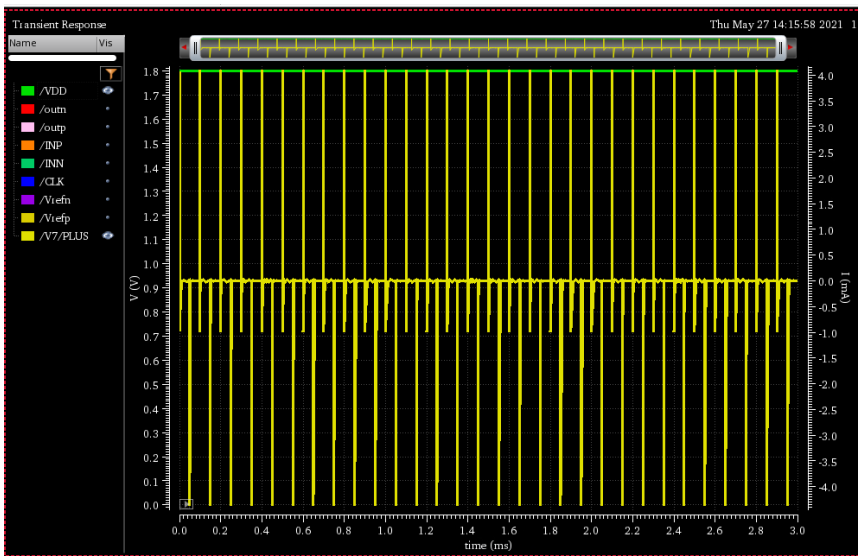


Figure 18: Strong arm current and power supply

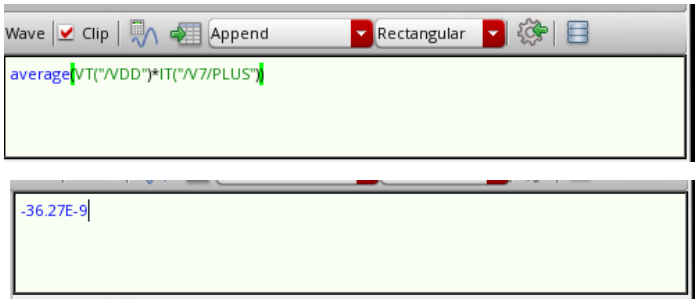


Figure 19: Power consumption of the strong arm comparator

2.3.3 Propagation delay

Because the speed of comparator is compromised by propagation delay, another important parameter to be measured is the propagation delay, which is the time required for the output to reach 50% of its final output level when the input changes to 50% of its final input level. Propagation delay measurement is important because it allows to know the speed of the comparator.

Figure 20 shows the propagation delay measured in the output with respect to the clock. This result shows that propagation delay is 22.8 ns in falling transition and 731 ps in rising transition.

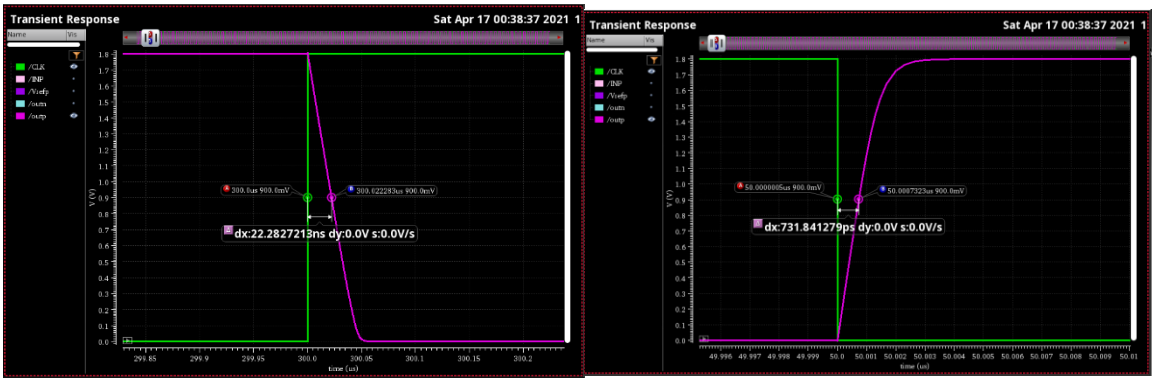


Figure 20: Measure of the propagation delay in the strong arm comparator

The performance of the comparator is summarized in the Table 1:

STRONG ARM COMPARATOR	
Input offset	17.8 mV
Propagation delay	3.22 ns
Speed of operation (1/propagation delay)	310.55 MHz
Power consumption	36.27 nW

Table 1: Characterization of the strong arm comparator

2.4 PVT analysis

In analog design, manufacturing tolerances for devices, temperature range and variations of external signals are verified by corner analysis and process variation simulations.

To test the dynamic comparator, 45 corners: 3 V_{DD}, 3 temperatures, and 5 process corners are analyzed. The corner test results may reveal if dynamic comparator is able to switch properly at different corners of V_{DD} and temperature. Figures 21 to 26 show PVT simulation results only for 3 cases: typical case (1.8 V, typical process, and 27 °C), best case (1.98 V, fast process, and -40 °C), and worst case (1.62 V, slow process, and 85 °C).

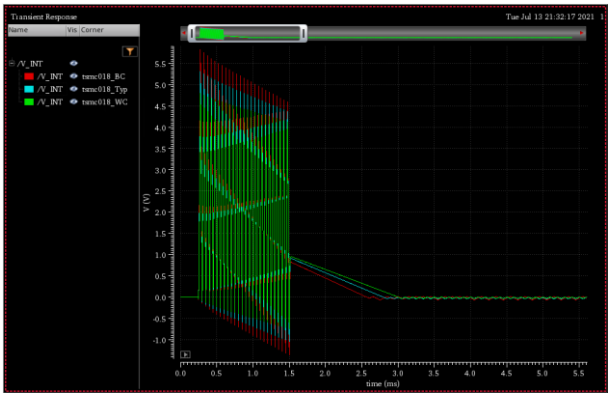


Figure 21: Integrator output for offset measurement

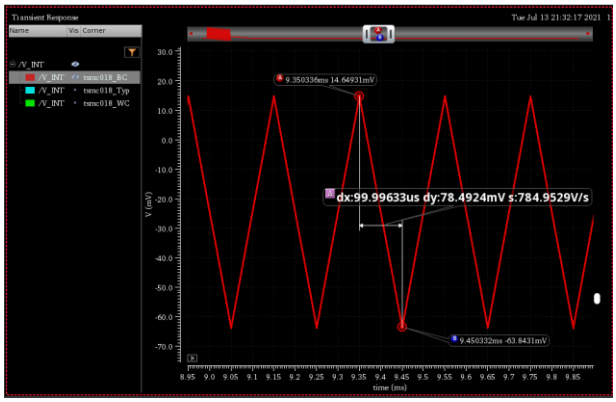


Figure 22: Input offset measurement in best corner

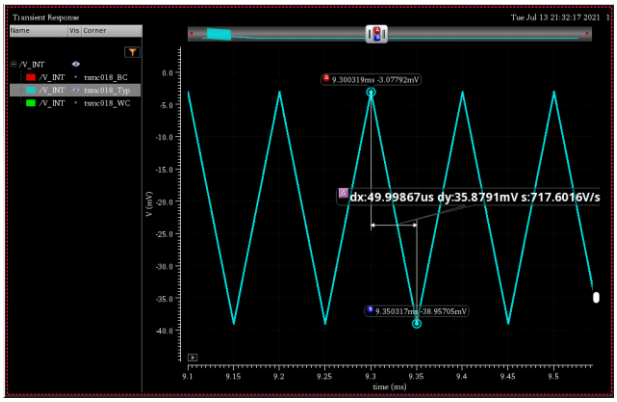


Figure 23: Input offset measurement in typical corner

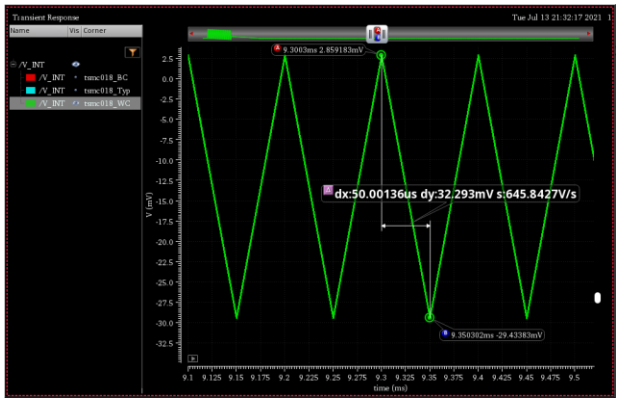


Figure 24: Input offset measurement in worst corner

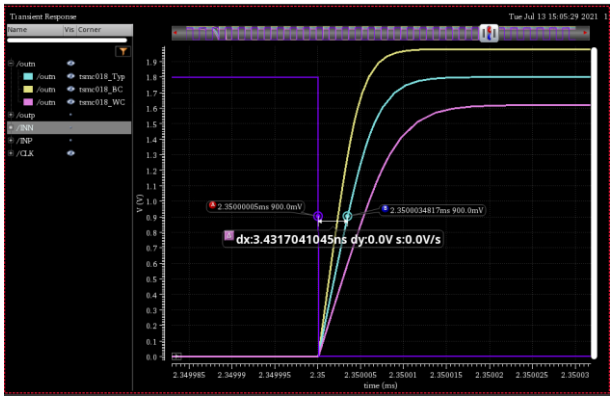


Figure 25: Propagation delay measured at *Outn*

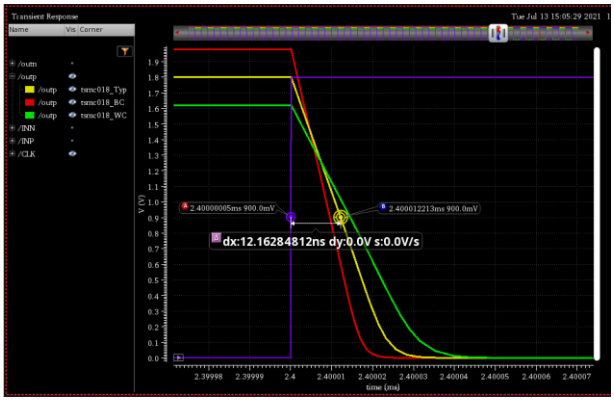


Figure 26: Propagation delay measured at *Outp*

Test	Output	tsmc018_Typ	tsmc018_BC	tsmc018_WC
Karina_simulaciones:Dyn_comp_Strong...	/outn			
Karina_simulaciones:Dyn_comp_Strong...	/outp			
Karina_simulaciones:Dyn_comp_Strong...	/INN			
Karina_simulaciones:Dyn_comp_Strong...	/INP			
Karina_simulaciones:Dyn_comp_Strong...	/CLK			
Karina_simulaciones:Dyn_comp_Strong...	average((VT("/vdd!") * IT("/V7/PLUS")))	-31.62n	-37.54n	-25.89n

Figure 27: Power consumption in the best, worst, and typical corners

Next table shows the summary of the characterization parameters and the results in the three corners previously mentioned.

	Best Case (ff/1.98v/-40°C)	**Typical Case** (tt/1.8v/27°C)	**Worst Case** (ss/1.62v/85°C)
Input offset	39.2462	17.93955	16.1465
Propagation delay - Outp	9.55ns	12.16ns	14.5ns
Propagation delay - Outn	2.296ns	3.431ns	5.273ns
Speed of operation (1/propagation delay)	104.71 Mhz	82.23 MHz	68.96 MHz
Power consumption	37.54nw	31.62nw	25.89nw

Table 2: Strong arm characterization in BC, TYP and WC corners

2.5 Physical design

Physical design is the process of turning a design into manufacturable geometries. It takes several steps, including floorplanning, placement, and routing.

2.5.1 Layout

Placement is the first major step in the layout design. It involves identifying which structures should be placed near others, considering area restrictions, speed, and the various constraints required by components. Placement determines the locations of each component or block on the die, considering timing and interconnect length. Figure 28 shows placement of the components of the strong arm comparator.

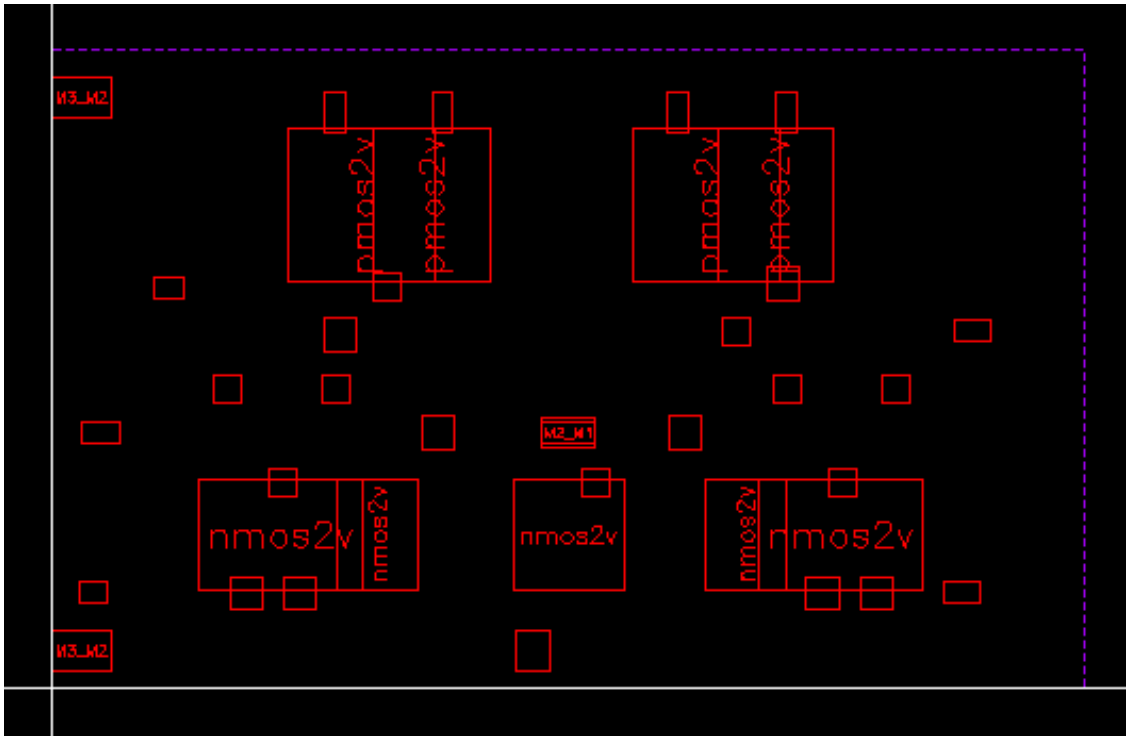


Figure 28: Strong arm comparator placement

Routing determines the paths of interconnects. This stage completes all connections defined in the netlist, in the most efficient way. The layout of the comparator was performed using custom placement and routing procedure. Routing was done using metals 1 and 2 and for all the pins metal 3 is used. Due to floorplaning constraints in the tape-out, the height of custom designed cells must by a multiplier of a standard cell, which is 4.39 µm high. In this sense, the final dimension of the comparator cell is 14 µm long by 8.78 µm high.

In order, to avoid LVS errors, it was necessary to place all input and output pins of the comparator cell next to the PR Boundary and their correspondent label must be also in metal 3.

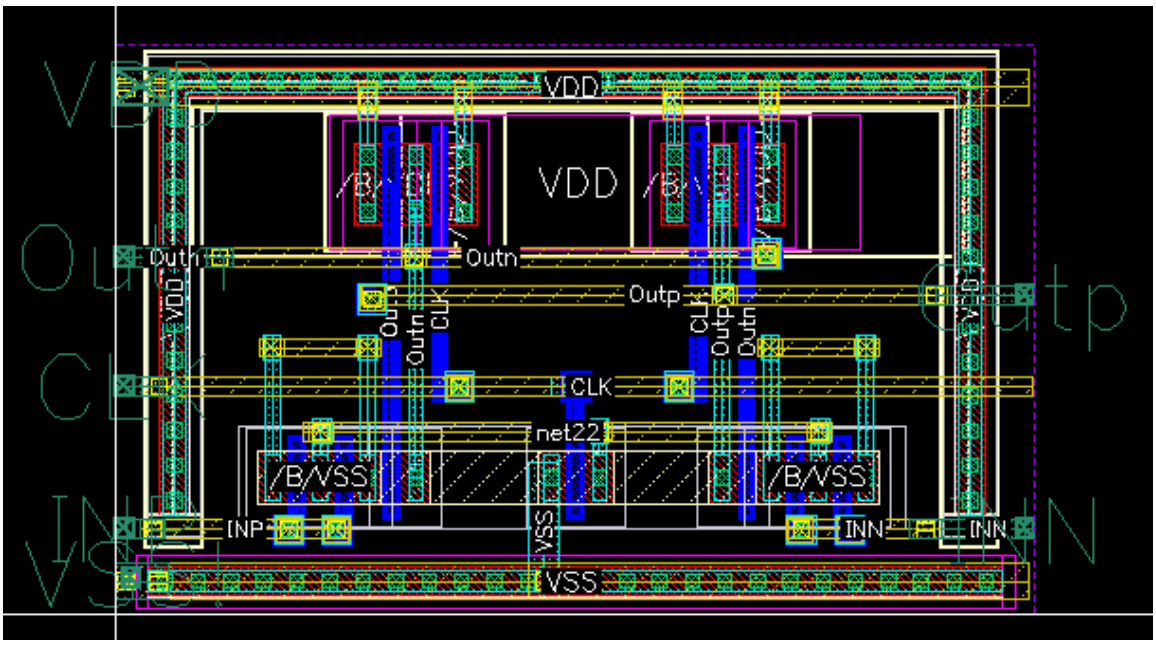


Figure 29: Strong arm comparator layout

2.5.2 Layout verification

Verification of layout is the process to ensure a normal electrical and logical functionality. The comparator verifications include DRC and LVS verifications, and the results are show next.

DRC verification.

Design Rule Checking (DRC) is a physical process in the design of a chip to determine if a layout satisfies the rules defined by the manufacturer. These rules ensure the correct functioning of the chip even with certain variations in the manufacturing process. Some types of design rules include minimum width of interconnections, minimum spacing between metals and minimum enclosure. Figure 30 shows the report of DRC verification of the dynamic comparator. As shown in Figure 30, the comparator has 7 DRC errors, however, these DRC errors are related to density of materials which will be last corrected at the tape-out level.

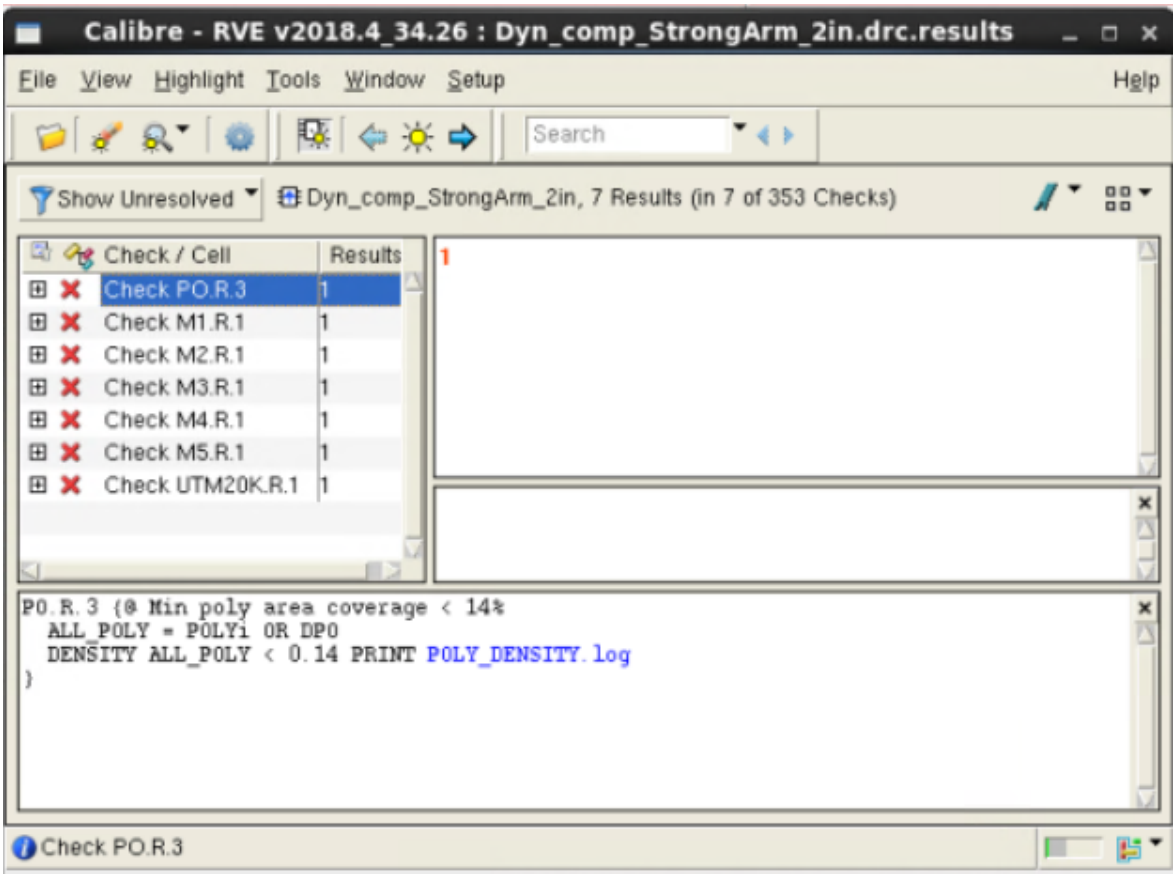


Figure 30: Strong arm comparator DRC verification

LVS verification.

Layout vs Schematic (LVS) is used to ensure that every cell and connection in the schematic is the same in layout view. Some LVS discrepancies that can be found are nets, devices, pins, and parameters. Figure 31 shows the LVS report of the Dynamic comparator. It can be noted from this Figure that comparator cell is free of LVS errors.

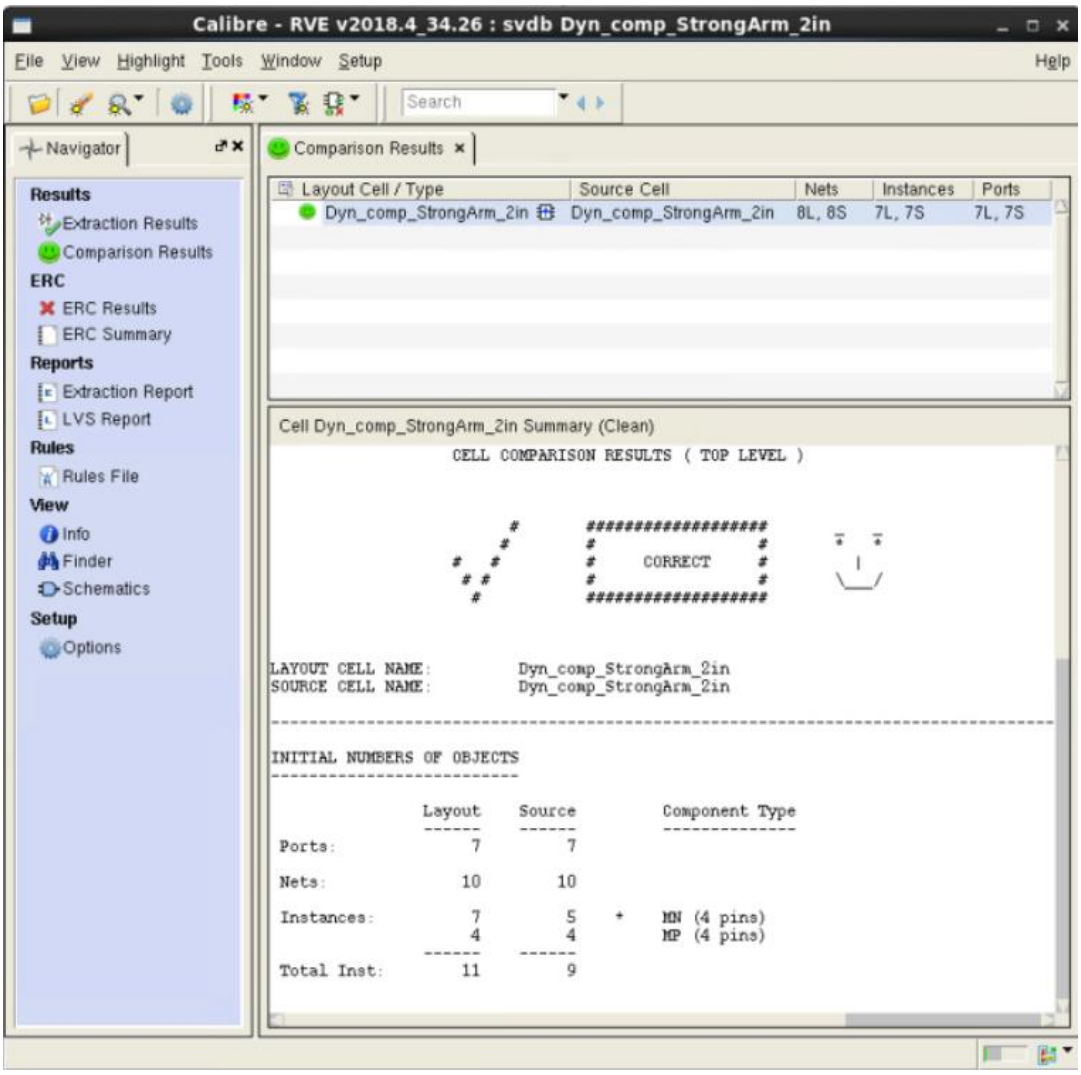


Figure 31: Strong arm comparator LVS verification

3. SR latch

Outputs of the dynamic comparator are the inputs of SR latch, this is because the outputs of the comparator are differential type and depend on the clock frequency. The SAR module needs single ended inputs to know which input voltage is greater.

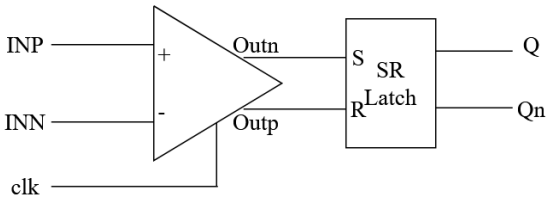
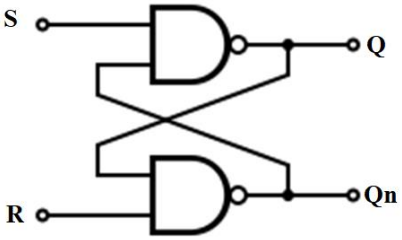


Figure 32: Comparator witch SR Latch

Latches are asynchronous devices which can store one bit of data. Its outputs depend on the inputs changes and there is no need an input clock, this is the difference with flip flops.

There are many topologies of latches, SR latch is the simplest one, it has two inputs called Set and Reset and two outputs: Q and its complement Qn. SR latch can be designed with two NOR gates that have a cross-feedback loop or with two NAND gates, nevertheless, in the last case inputs are active in 0. In this project, a NAND-based SR latch is designed, Figure 33 shows the topology and the truth table.



S	R	Q	Qn
0	0	prohibited	
0	1	1	0
1	0	0	1
1	1	Memory	

Figure 33: (a) SR latch of NAND gates. (b) Truth table SR Latch

3.1. Latch Design

As Figure 33 shows, the input state of S = “0” and R = “0” is a prohibited condition because it causes both outputs Q and Qn to be high together when normally Q is the inverse of Qn. So, latch becomes unstable. Logic is added to avoid this condition as shown in Figure 34. When S’ and R’ = 0 the inputs S and R became 1 forcing memory state. In any other combination of S’ and R’, Q and Qn follow the latch SR truth table.

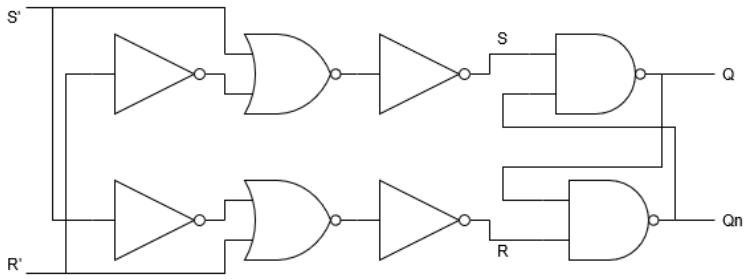


Figure 34: Latch SR avoiding prohibited condition

To be able to integrate the Latch to the ADC, it is neccesary to add an external reset pin, since in the ADC, the reset is active in low, when reset=0 reset condition needs to be forced (S’=1 and R’=0) and when reset=1, S’ and R’ don’t change. In order to add this feature, more logic was added to implement the reset pin to the above SR latch design. This additional logic is shown in the next truth tables.

rst	S''	S
0	0	1
0	1	1
1	0	0
1	1	1

rst	R''	R
0	0	0
0	1	0
1	0	0
1	1	1

Table 3: Truth table for S’ and R’ to force reset state

Next equations model the logic to bring the Latch of Figure 34 to the reset state

$$\bar{S} = rst + \overline{S''} \qquad S = \overline{rst + \overline{S''}}$$

$$R = rst \cdot R''$$

Figure 35 shows the representation of the ecuations

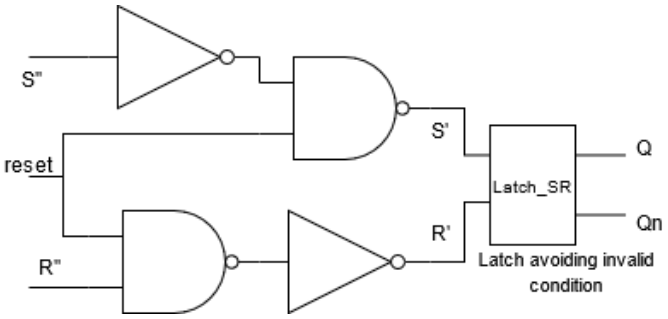


Figure 35: Latch SR with external reset signal

The next step is to design the gates with CMOS transistors. According to the sizing procedure reported in (Guwahati, 2011) to design 2-input NAND and NOR gates for equal rise and fall time it is necessary to first design an inverter with equal rise and fall time. This involves compensating for the difference in electron and hole mobilities. Typically for design process above 90 nm, the electron mobility is about 2.5 to 3 times greater than the hole mobility. To calculate dimensions of the inverter transistors the equation of the medium voltage is used.

$$v_M = \frac{v_{T_N} + v_{DD} + v_{TP}}{2}$$

$$v_M = \frac{v_{DD} \pm \Delta v_T}{2} = \frac{1.8v}{2} = 900mv$$

The W/L ratio of each transistor can be calculated by:

$$\mu_P C_{0x} \left(\frac{W}{L}\right)_P = \mu_n C_{0x} \left(\frac{W}{L}\right)_n$$
$$k_P \left(\frac{W}{L}\right)_P = k_n \left(\frac{W}{L}\right)_n$$

From previous characterization task of TSMC18 process, we know that $k_n = 183\,{}^{\mu A}/_{v^2}$ and $k_p = 68\,{}^{\mu A}/_{v^2}$, so, solving for w_n and w_p, we will have

$$68\,{}^{\mu A}/_{v^2} \left(\frac{w}{200nm}\right)_P = 183\,{}^{\mu A}/_{v^2} \left(\frac{w}{200nm}\right)_n$$
$$0.375 = \frac{\left(\frac{w}{200nm}\right)_n}{\left(\frac{w}{200nm}\right)_p} = \frac{w_n}{w_p}$$

$$w_p = 2.66\, w_n$$

Hence, dimensions of the NMOS and PMOS for the symmetric inverter are:

$$w_p = 2\mu m, \qquad L_p = 200nm.$$
$$w_n = 750nm, \qquad L_n = 200nm.$$

After performing this task, we continue to size the transistors of each NAND and NOR gates under worst-case conditions (of input combination) for charging and discharging resistances Rc and Rd.

For a NAND gate, the worst-case charging corresponds to an input combination where only one of the pMOS is ON and discharging takes place only when both nMOS are turned ON. i.e. in the Worst-case, Rc/Rd=1/2. Thus, in order to equalize both currents (considering also the mobility differences), we must have (W/L)p=(2.666*2)(W/L)n. This can be achieved by choosing Wn=0.75 µm and then Wp=4 µm.

Similarly in case of a NOR gate, (W/L)p must be equal to (2.5*0.5)(W/L)n, which can be achieved by taking Wn=0.75µm and Wp=1µm.

3.2. Simulation results

To ensure the correct functionality of the latch, it is tested with different sequences of inputs in a test bench using piece-wise source generators according to the next truth table:

S	R	Q	Qn	
1	1	x	x	Memory
0	1	1	0	Set
1	1	1	0	Memory
1	0	0	1	Reset
0	0	0	1	Prohibited (Memory)
1	1	1	1	Memory
0	1	1	0	Set

Table 4: Truth table to probe SR Latch

Remember when S=R=0 a regular SR latch shows a prohibited condition; however, this design is modified to go to memory state. Result of the simulation shows in Figure 36.

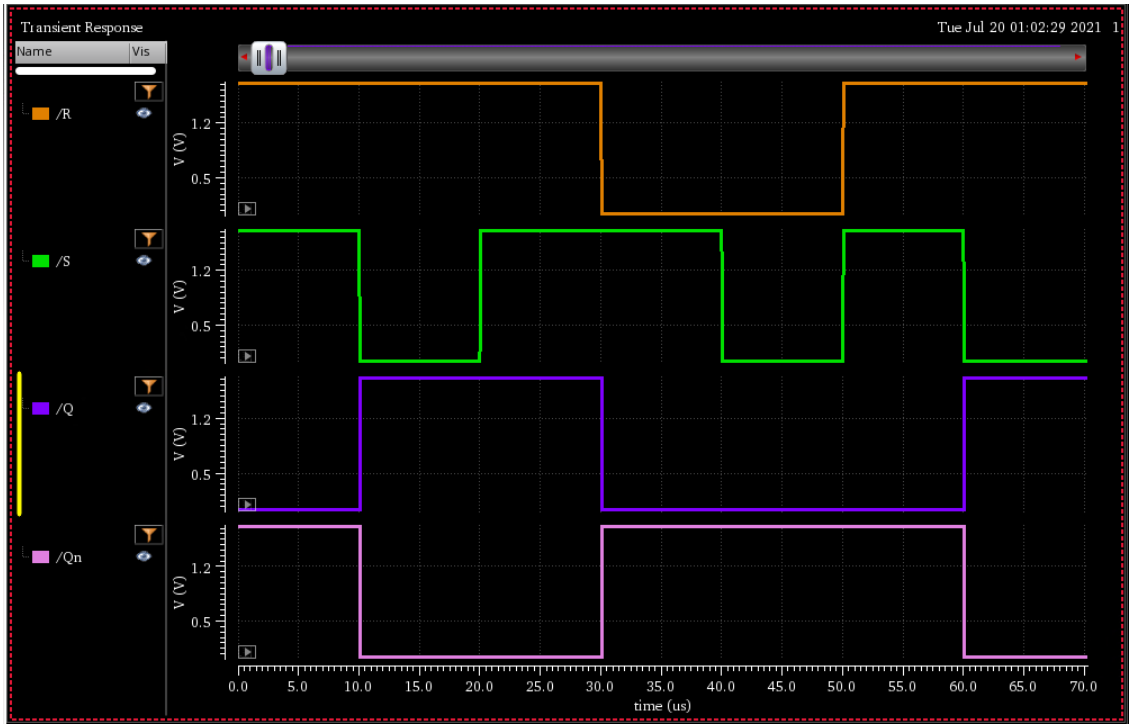


Figure 36: SR Latch simulation results

Figure 37 shows the latch simulation results when reset pin is added. The Figure 37 shows when reset is low (active) output *Q*=0 and *Q*=1, circuit is in the reset state, and when reset is high the outputs *Q* and *Qn* respond to the truth table 4.

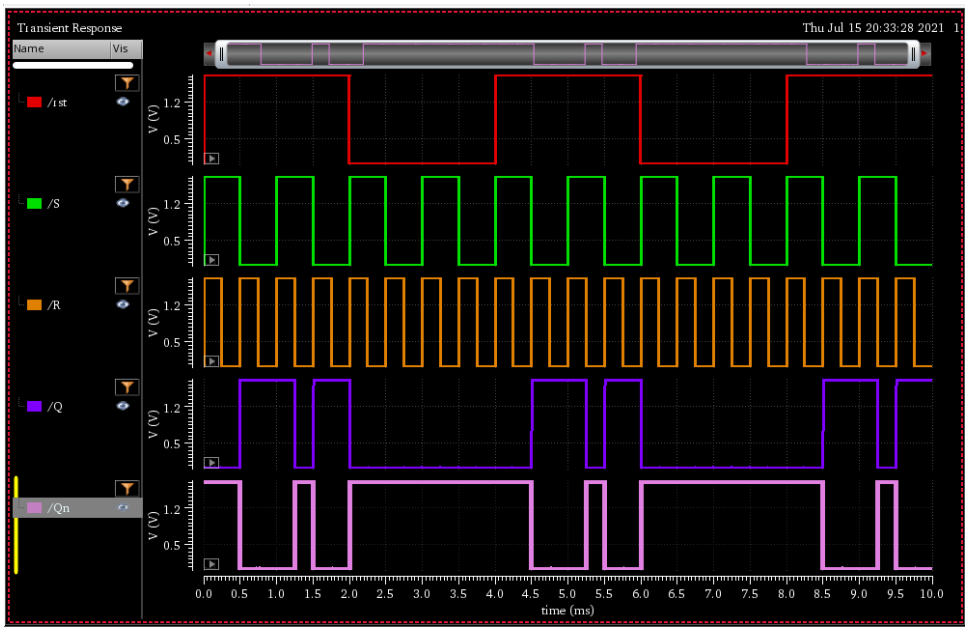


Figure 37: SR Latch simulation results with reset pin

Connection of the latch to the dynamic comparator is shown in Figure 38. Circuit is tested with a sinusoidal signal of 1.8 V amplitude and 100 KHz at the input terminal *INP*, while a DC voltage is set to 900 mV at the terminal *INN* and a Clock frequency of 2 MHz. Since latch is active low, *Outp* must be connected to latch input *R* and *Outn* to Latch input *S*. *Q* is the output which will be connect to the SAR module.

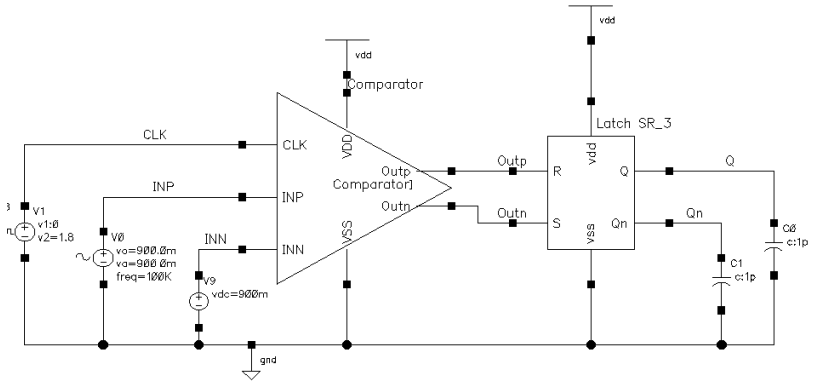


Figure 38: Test bench of the dynamic comparator connected to the SR latch

Figure 39 shows the transient response of the comparator connected to the latch. It can be notice in the time 0 when *INP* is higher than *INN*: *Outp* is high and *Outn* is low, that activates the SET state in latch (Q=1 and Qn=0), then *Outn* changes to high and *Outp* keeps high, so latch is in memory state and still in SET state, so, while *INP* > *INN* then *Q*=1 and *Qn*=0. The opposite occurs when *INP* is lower than *INN*, latch is in RESET and memory states, thus when *INP* < *INN* then *Q*=0 and *Qn*=1 which is the expected behavior.

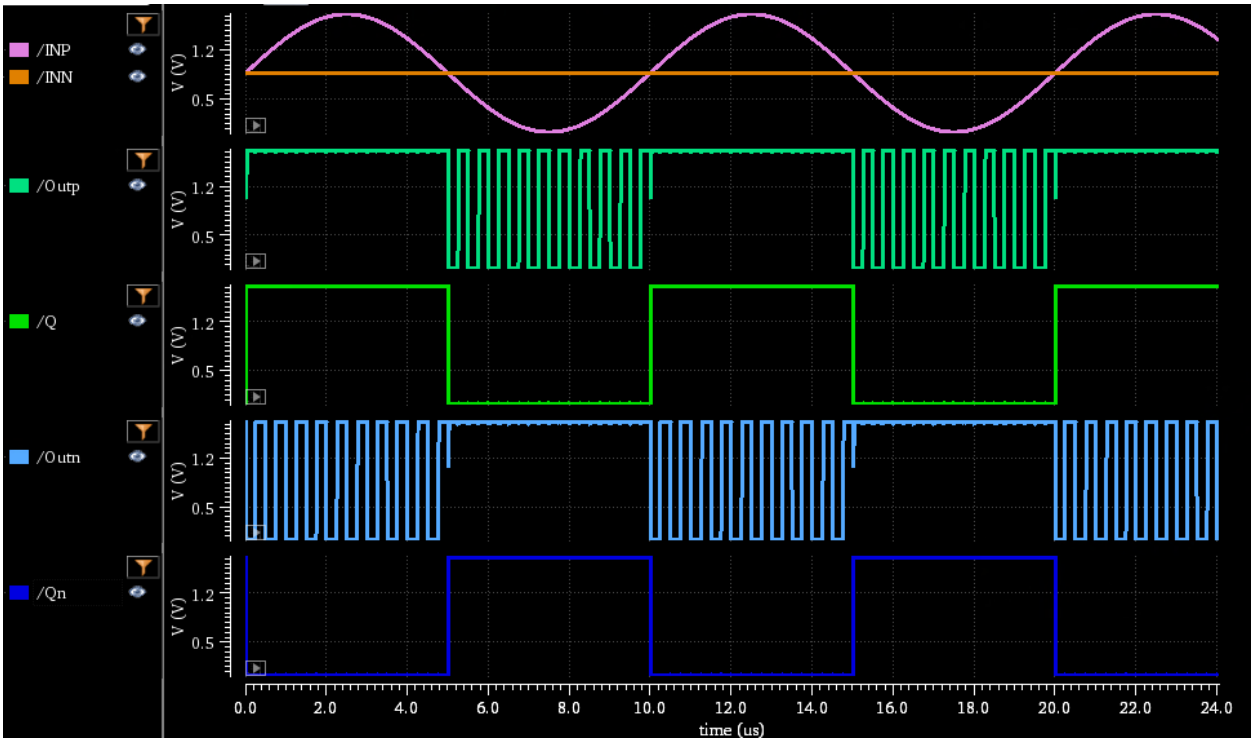


Figure 39: Transient response of the dynamic comparator connected to the SR latch

4. The bootstrap switch

Sample and Hold (S/H) is a circuit that takes a sample of the analog signal for a short interval of time and holds its value over a certain length of time until the ADC can process the information.

These S/H circuits operate in 2 circumstances: hold mode (static), and sample mode (dynamic), and consist of two basic components: holding capacitor and analog switch with a clock signal to controls it. When the switch is closed, output tracks the input signal until the clock signal changes, then the capacitor holds the analog voltage during the analog to digital conversion. In its simplest way, Figure 40 shows the principal components of the S/H.

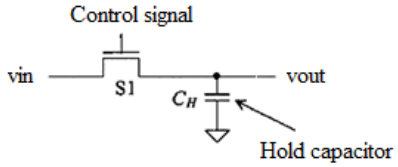


Figure 40: Sample and hold basic circuit

Nanometer MOS switches present high on-resistance (*Ron*), which caused nonlinearity or distortion. That issue can be solved using a technique called bootstrapping. The Bootstrap switch is a circuit that minimizes the switch on-resistance variation in the presence of large input and output voltage swings (Razavi B. , The Bootstrapped Switch, 2015). However, like other switch architectures, the Bootstrap switch can present some errors, that affect the performance of ADC. Below we describe some typical errors that can be present in the Bootstrap switch architectures.

Sample and Hold errors

According to (M. Macedo, 2012), there are some errors that degrade the performance of the Sample and hold circuit: timing errors induced by clock jitter; hold-mode feed-through; settling time; pedestal error; and droop rate.

- **Pedestal error**: this error occurs as a result of charge injection and clock feedthrough in the transistor switch. It is the difference between the ideal output level and the output that results once the S/H has settled down.

- **Droop error**: This error is related to the leakage of current from the capacitor during the hold mode. The level of droop is a function of the amount of leakage and the size of the sampling capacitor

4.1. Design of the bootstrap switch

The ideal switch does not exist, so, when nanometer switches are designed, it is important to consider that output should track input as well as possible, with no delay and no distortion. Imperfections of CMOS switches come from channel charge injection and clock feedthrough that depend on the input voltage. The solution is to keep V_{GS} constant, and the easiest way is to connect it to V_{DD}. In this way the Ron can be minimized avoiding nonlinearity issues in the presence of large input and output voltage swings (Razavi B. , The Bootstrapped Switch, 2015), this concept is shown in the Figure 41.

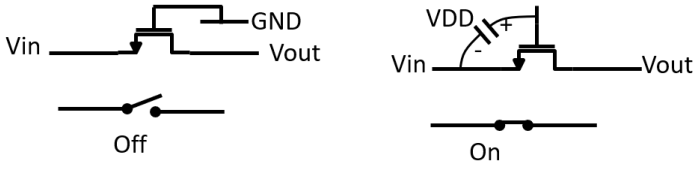


Figure 41: Bootstrap switch concept

To design the bootstrap switch circuit there are necessary one path to charge the hold capacitor to V_{DD} and discharge the switch gate to gnd. And another path to connect V_{GS} to V_{DD}. Figure 42 shows the bootstrap switch topology.

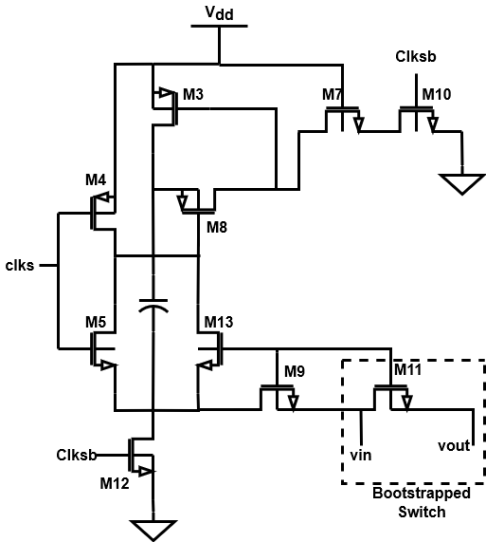
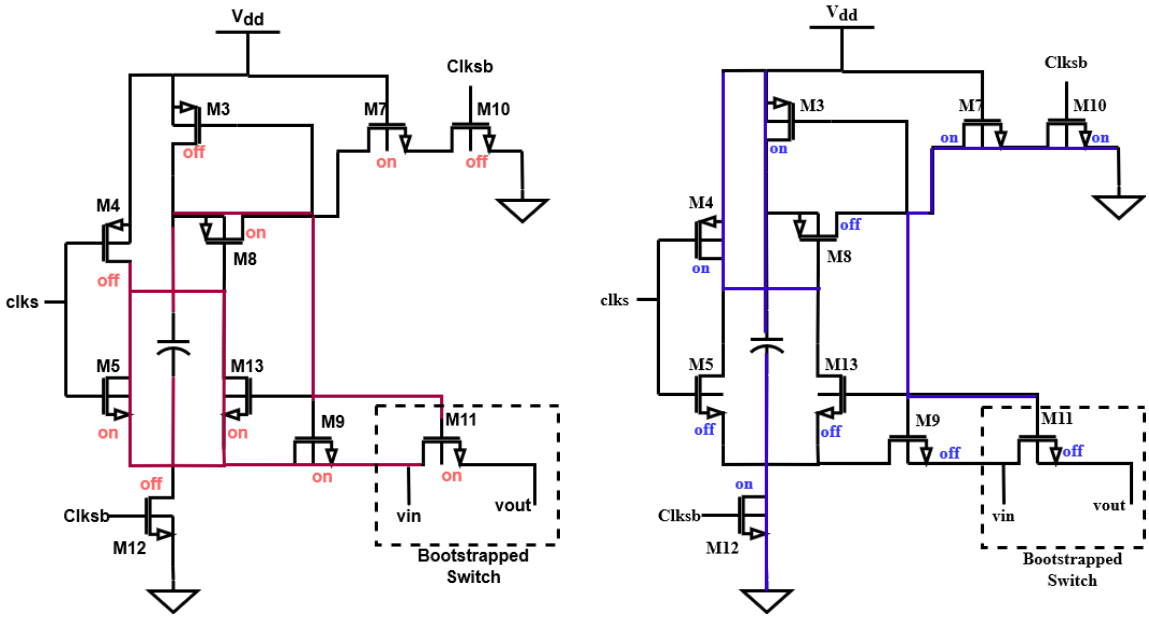


Figure 42: Bootstrap switch topology

NMOS transistor M11 is properly the bootstrapped switch. M10 is used to prevent leakage and since transistors is operating above V_{DD}, substrate of PMOS transistor M8 needs to be connected to source terminal, for protection. Figure 43 shows the bootstrap switch in its two states: state off (left), when *clks*=1, *clksb*=0, hold capacitor is connect to gate and source of the boostrapped switch (M11). And state on, when *clks*=0, *clksb*=1, hold capacitor charges and gate of M11 is connected to gnd.



(a) (b)

Figure 43: (a) Switch on. (b) Switch off.

Since Transistor M11 is properly the bootstrapped switch, it was optimized in size to work for a load capacitance of 300 pF. The other transistor was sized with minimal W/L in order to reduce parasitic capacitances. Appendix C summarize the size of all bootstrap switch.

4.1.1 Simulation results

Once bootstrap switch was designed, a transient simulation was performed to validate the correct functionality of the selected topology. Figure 44 presents the schematic of the bootstrap switch.

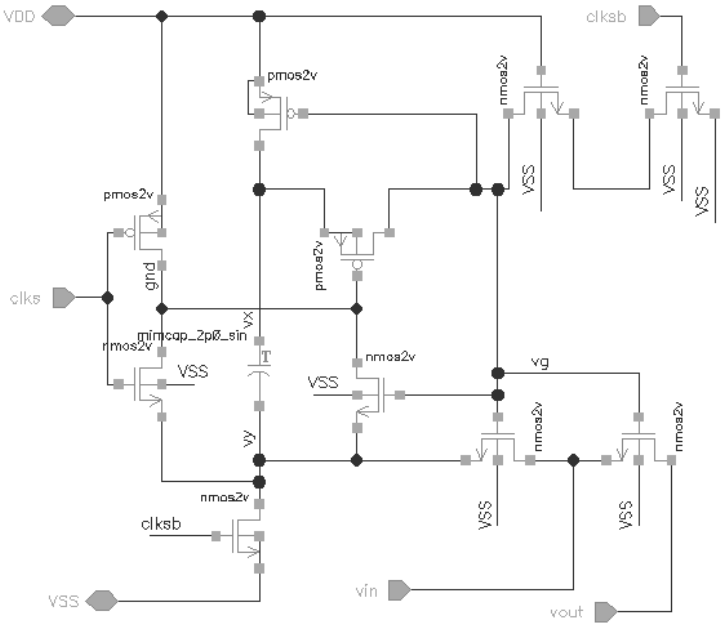


Figure 44: Bootstrap switch schematic

Figure 45 shows the result when we apply a sinusoidal voltage of 1.8 V, 10 KHz, and a clock signal of 200 KHz with a pulse width of 50 ns.

Simulation shows that this switch topology has a suitable linearity and low distortion of the output signal. However, the load that bootstrap must manage can cause some variations in the voltage hold by the capacitor. For this case, bootstrap was tested with a capacitance load of 300 pF since that is the total load of the Capacitive DAC.

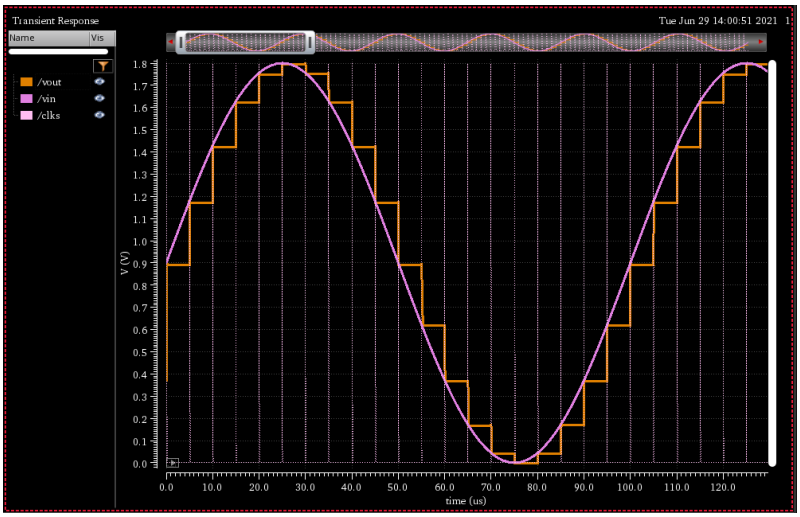


Figure 45: Transient response of bootstrap switch

Pedestal error in this topology is 5.91 mV that means that capacitor do not hold the exact *Vin* voltage but 5.91 mV less. By several tests, it was observed that this error can be minimized to 1.26 mV by connecting the M11 and M4 substrates to source terminal instead of to gnd, however, to make this connection is necessary a triple well CMOS technology which is not the case for the TSMC18 process, then the actual design of the Bootstrap switch remains with 5.91 mV of pedestal error and its optimization remains as a future work.

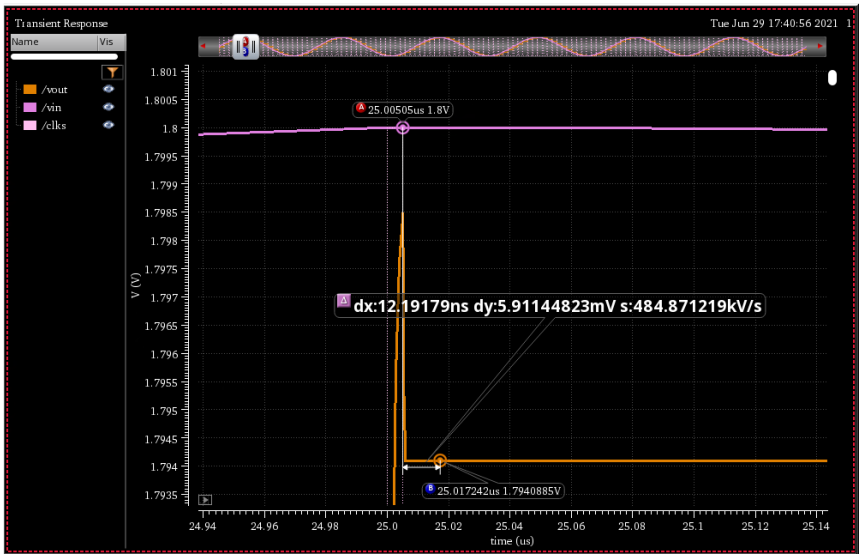


Figure 46: Pedestal error in bootstrap switch for 300pf load

4.2. PTV analysis

To make sure the chip works in all possible conditions, a PTV analysis is made. This is a simulation of the operation of the circuit when 3 variables change: Process, temperature, and supply voltage. Figure 47 shows Transient simulation in typical conditions, conditions that simulates the best-case and the worst-case.

The upper image represents the response under best-case conditions, that is, when voltage is 10% more than nominal voltage (1.98 V), fast process, and lowest temperature (-40 °C). The middle image shows typical case: 1.8 V, 27 °C and typical process parameters. In these two cases, we can observe good linearity of the out signal and no distortion. However, in the last image which corresponds to the worst-case conditions, the output signal shows a little distortion when *Vin* is higher than 1.6 V.

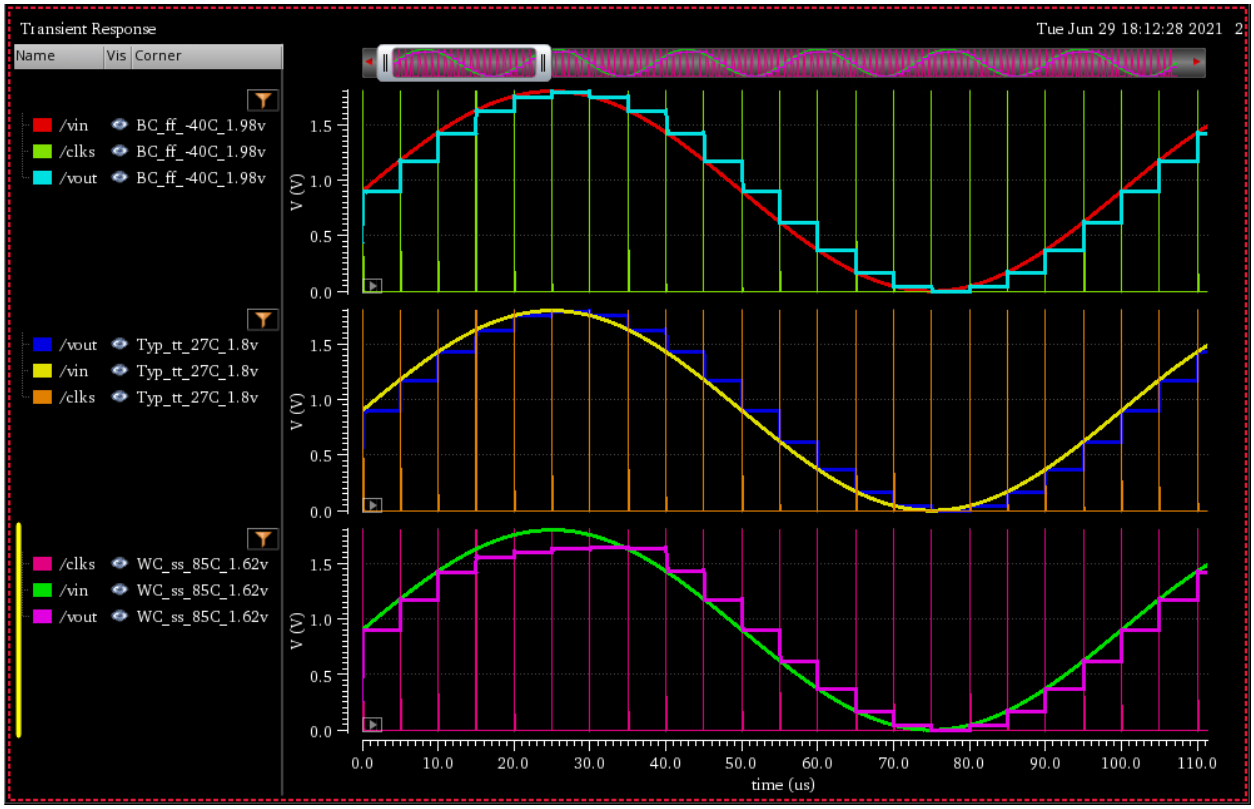


Figure 47: Transient response of the bootstrap switch in best-case (upper image), typical-case (middle image), and worst-case (lower image).

Power consumption in the 3 corners is presented below. In this image we can note that power consumption is 1.448 µW in typical condition, 1.833 µW in the best-case and 1.181 µW in the worst-case. These results are according to the expected results because power depends on the supply voltage.

Test	Output	Spec	Typ_tt_27C_1.8v	BC_ff_-40C_1.98v	WC_ss_85C_1.62v
Karina_simulaci...	/vin				
Karina_simulaci...	/vout				
Karina_simulaci...	/clks				
Karina_simulaci...	average((VT("/net3") * IT("/V2/PLUS")))		-1.448u	-1.833u	-1.181u

Figure 48: Power consumption of the bootstrap switch in best, typical, and worst case.

In Figure 49, pedestal error was measured in the 3 corners. This error indicates the difference between the input voltage that the switch would hold and the real voltage at the output. We can see that in the best and typical case there is an error of about 5 mV but in the worst case this error increase until 173 mV when the input voltage is higher than 1.62 mV.

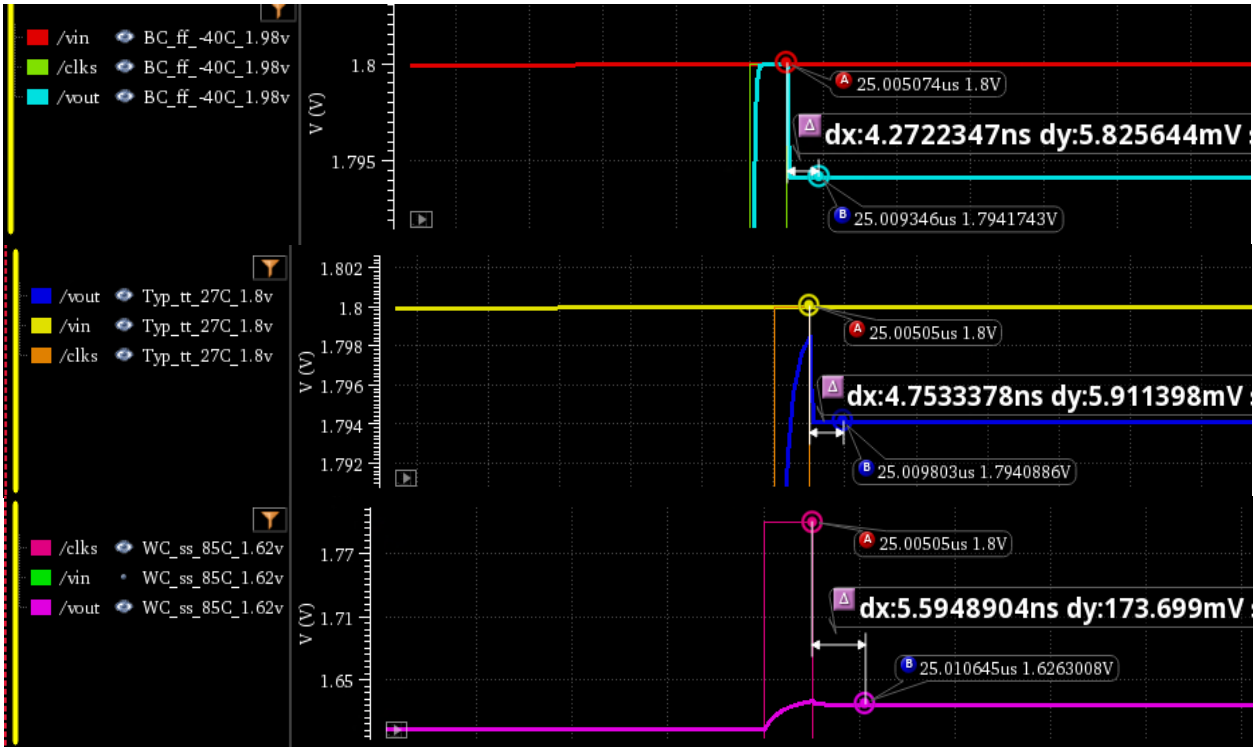


Figure 49: Pedestal error of the bootstrap switch in best, typical, and worst case

4.3. Physical Design

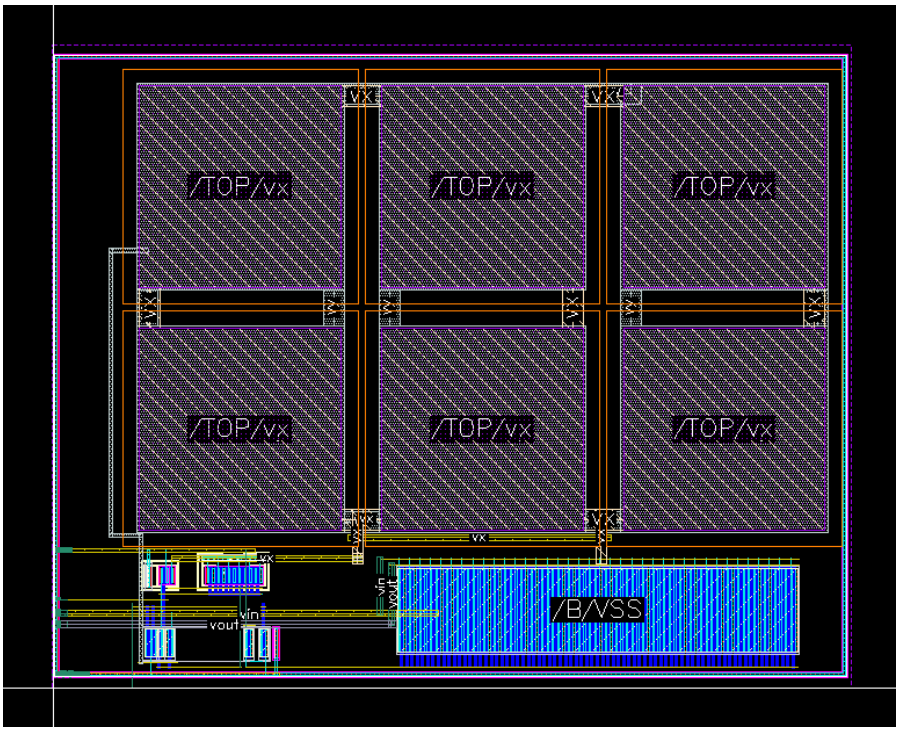
Like the other cells, we performed the layout of the bootstrap switch, and it is present the layout of the cell and DRC and LVS verification results.

4.3.1 Layout

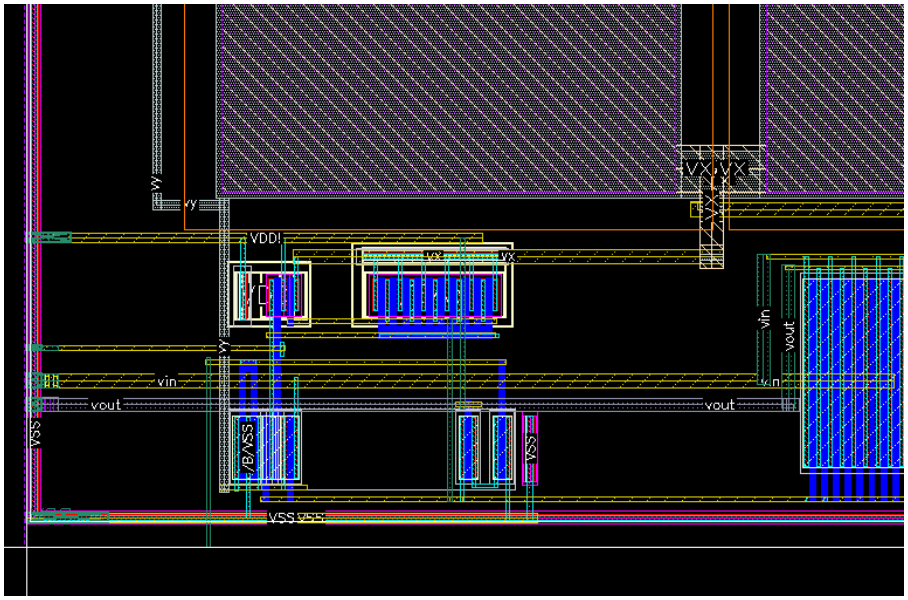
Placement of the bootstrap switch is shown in Figure 50, the major area of the design is the hold capacitor, in this case, a MIM capacitor is used (metal-insulator-metal) which is disposed in 6 smaller capacitors connected in parallel 1.66 pF each to get a total capacitance of 10 pF, since maximum capacitance of MIM Cap is 1.97 pF in this technology. Thus, capacitor dimensions are 103.15 µm long and 68.43 µm high. M11 transistor has the maximum W/L relation to be able to handle the load of the DAC.

Figure 50: Boostrap switch placement

Final layout can be observed in Figures 51 and 52. Dimensions of the designed bootstrap switch is 114.55 µm long and 92.19 µm high, that is, 21 times the height of a standard cell. The routing was done using metal 1 and metal 2, and metals 5 and 6 to connect the MIM Cap. Pins were done in metal 3.



Bootstrap 51: Bootstrap switch layout



Bootstrap 52: Boostrap switch layout

4.3.2 Verification Layout

To ensure a normal functionality of the Bootstrap, DRC and LVS verifications was performed, the results are show next.

DRC Verification.

Design Rule Checking (DRC) is the process to verify all the rules related with manufacturing process. Figure 53 shows there are not violations of minimum spacing between metals, minimum enclosure, or connection width.

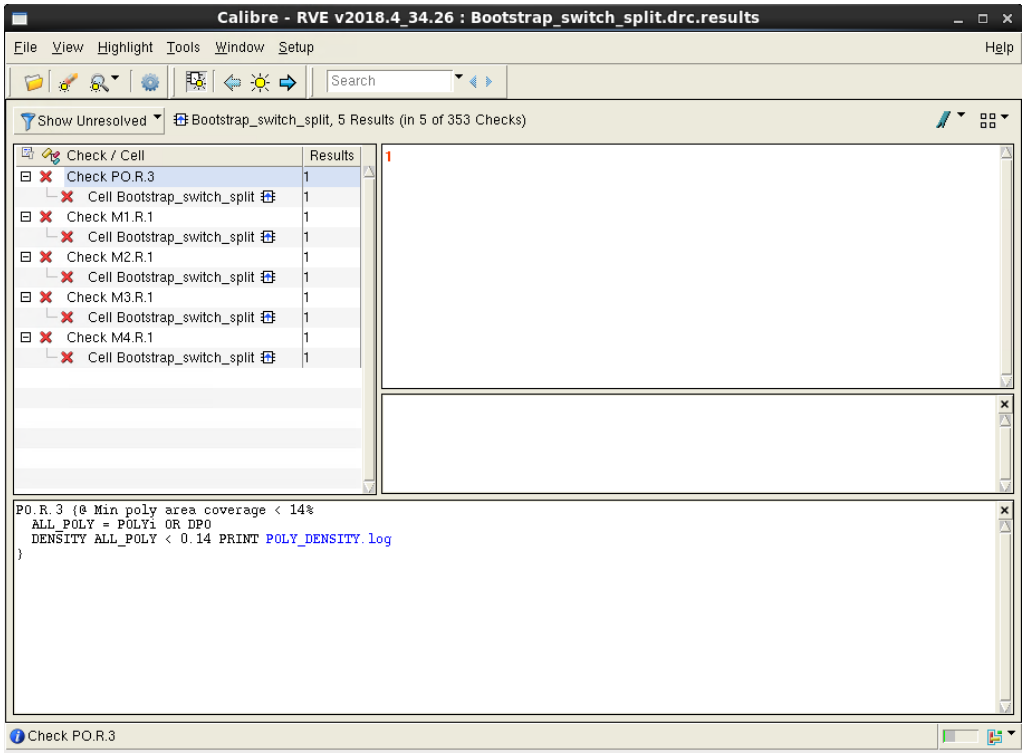
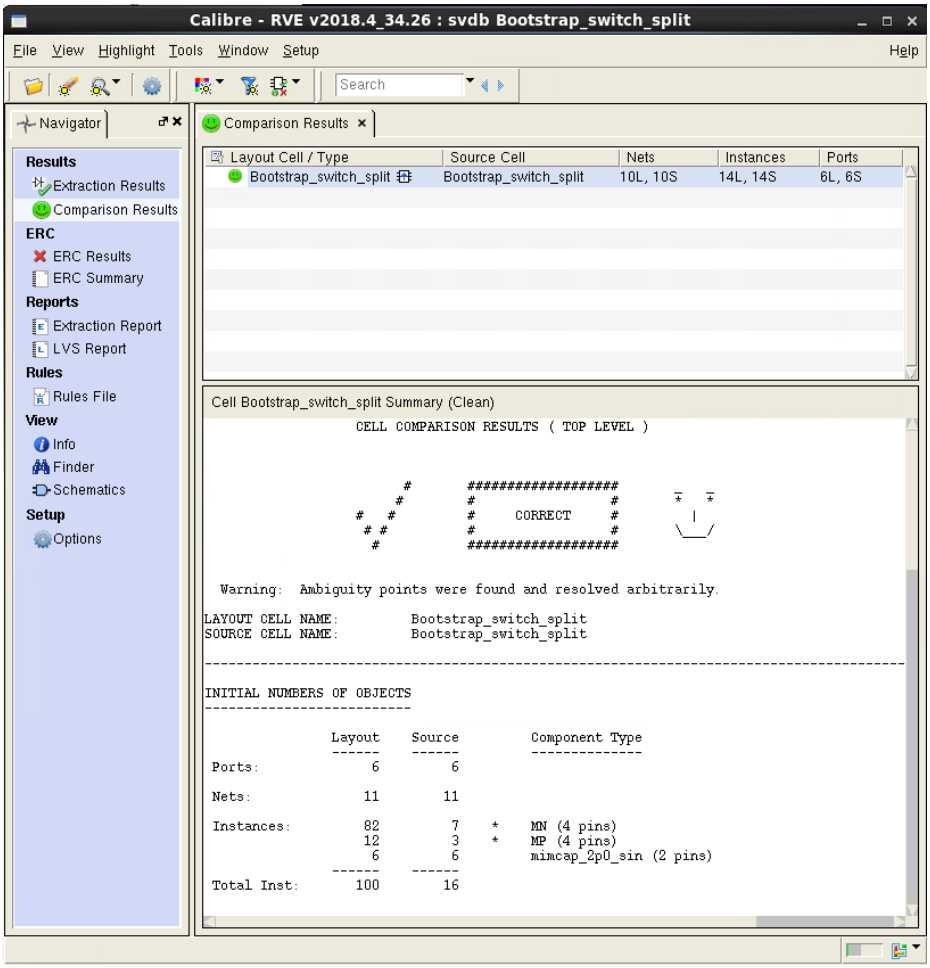


Figure 53: Boostrap switch DRC verification

LVS Verification.

LVS verification is used to find discrepancies between the bootstrap layout and the schematic views. Figure 54 shows all the instances, nets, and ports in the schematic are correspondent in layout.



Bootstrap 54: Boostrap switch LVS Verification

5. Integration of SAR ADC

5.1. Logic synthesis

Logic synthesis transforms behavioral hardware description language (HDL) code into a *netlist* describing the hardware as a model represented by logic blocks and the connections between them. In this project, logic synthesis was done by Encounter RTL Compiler (RC) which needs several files as inputs so it can do the synthesis of the design. The output of RC tool is a netlist and some reports with parameters like total area, fanout, total power consumption, number of used cells, etc.

To synthesize the full custom modules as the band gap, dynamic comparator, bootstrap switch, and DAC capacitive, it is necessary to generate the Library Exchange Format (LEF) files of each cell. LEF files contents information about the area of the cell, metal connection and vias. It is basically the representation of the layout of the cell using coordinates.

The LEF files are generated from the abstract view of the layout once it is DRC and LVS verified. The next figures show the abstracts of the full custom modules of the ADC.

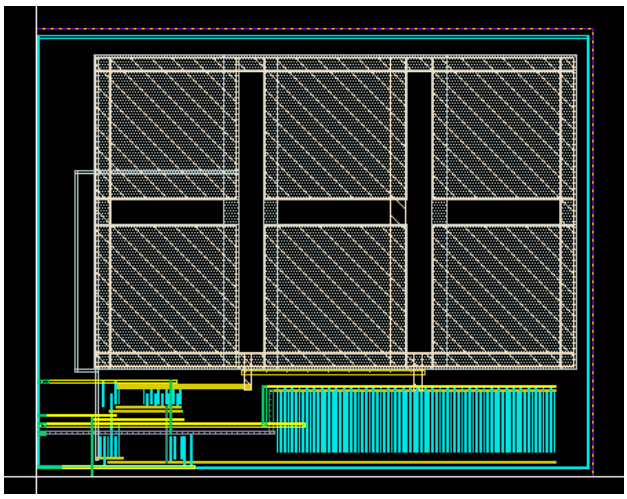


Figure 55: Boostrap switch abstract

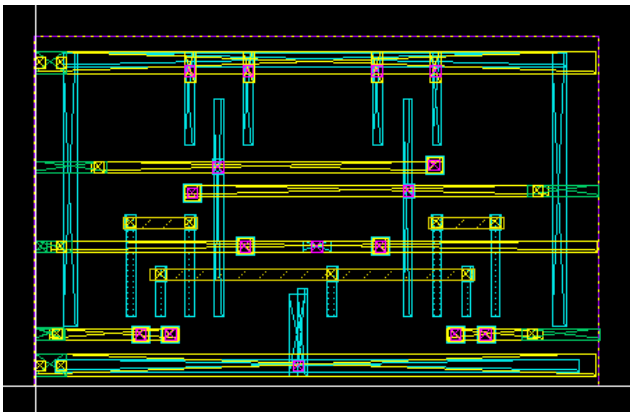


Figure 56: Dynamic comparator abstract

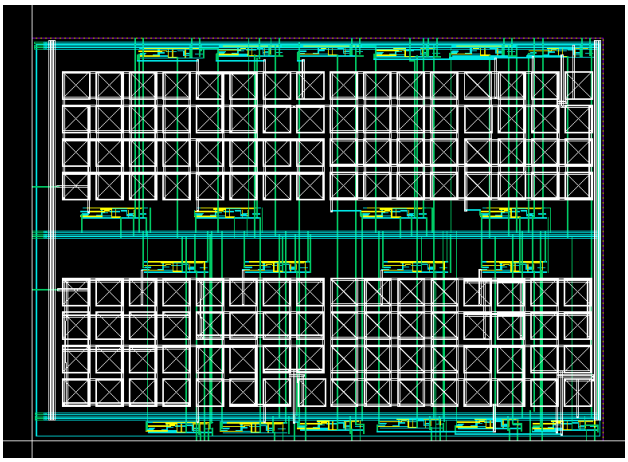


Figure 57: DAC capacitive abstract

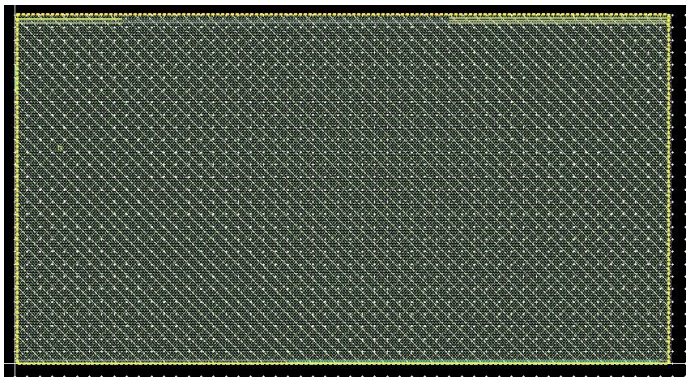


Figure 58: Band gap abstract

The SAR ADC was synthesized using RC tool. For doing a logic synthesis, constraints were defined. This information can be found completely in a sdc file, but some of the most important are the next ones:

- There's only 1 clock (Main_CLK) that works with a period of 4000 picoseconds
- Both the input and the output delay where 10% of the main clock's period
- The external driver that was used was the buffer BUFFD12BWP7T using the pin Z
- The max transition was 65% of the clock's period
- The max capacitance is 6000 femtofarads
- The maximum fanout is 50

Next Figure shows the schematic of the design. There is a top module which connects all the modules that conform the ADC, full custom modules are shown in orange color. The RTL diagram shows all connections are correct.

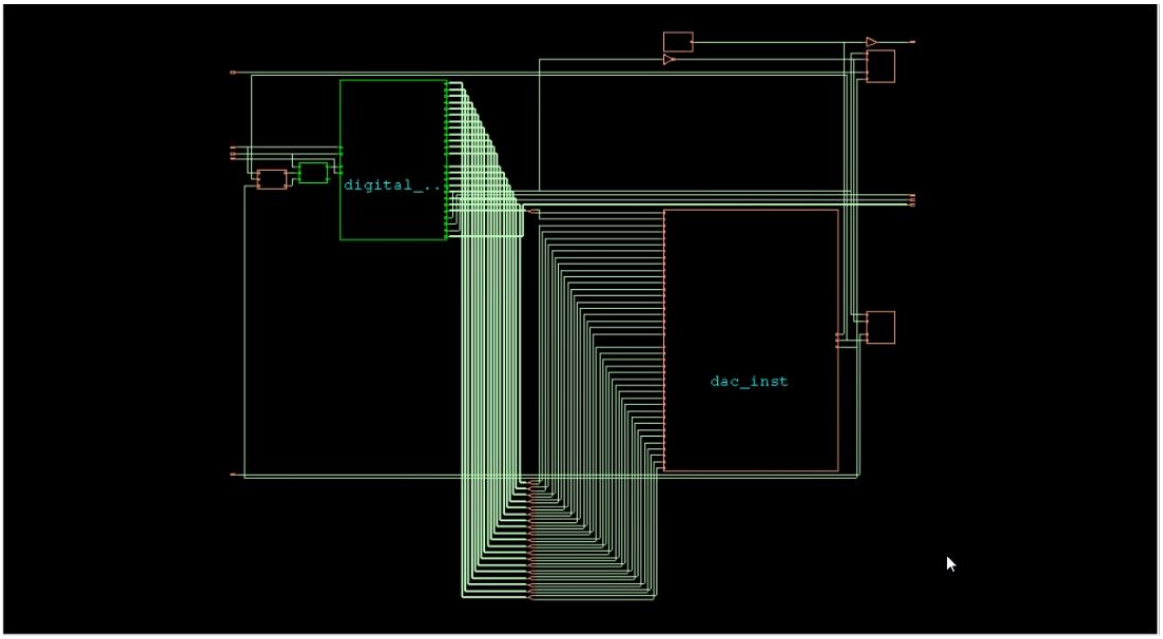


Figure 59: Schematic of synthesized RTL

The following reports were generated by the RC tool for typical and worst case, after the SAR ADC were synthesized.

```
Resultados Typ:
  Module:                 ADC_LP_bb
  Technology libraries:   tcb018gbwp7twc 270
                          tpd018nvwc 280a
                          physical_cells
  Operating conditions:   WCCOM
  Interconnect mode:      global
  Area mode:              physical library
============================================================


Timing
--------


  Clock  Period
---------------
Main_Clk 4000.0



  Cost     Critical       Violating
  Group   Path Slack TNS    Paths
-------------------------------------
C2C            947.2   0          0
C2O           1490.4   0          0
default       3683.9   0          0
I2C           3329.5   0          0
I2O         No paths   0
-------------------------------------
Total                  0          0


Instance Count
--------------
Leaf Instance Count             249
Sequential Instance Count        72
Combinational Instance Count    177
Hierarchical Instance Count      44


Area
----
Cell Area                          227032.622
Physical Cell Area                 0.000
Total Cell Area (Cell+Physical)    227032.622
Net Area                           2232.648
Total Area (Cell+Physical+Net)     229265.270


Power
-----
Leakage Power                      0.139 uW
Dynamic Power                      2148.675 uW
Total Power                        2148.814 uW


Max Fanout                         68 (ADC_SPI_sck)
Min Fanout                         0 (digital_inst/sar_lp_inst/DobleRegs/sw9n/SW_ctrl[0])
Average Fanout                     2.5
Terms to net ratio                 3.3
Terms to instance ratio            3.6
Runtime                            14.996 seconds
Elapsed Runtime                    31 seconds
RC peak memory usage:              175.00
EDI peak memory usage:             no_value
Hostname                           FV00
Final Runtime & Memory.
========================================
The RUNTIME after FINAL is 15 secs
and the MEMORY_USAGE after FINAL is 173.00 MB
========================================
```

```
Results WC:
   Module:                 ADC_LP_bb
  Technology libraries:   tcb018gbwp7twc 270
                          tpd018nvwc 280a
                          physical_cells
  Operating conditions:   WCCOM
  Interconnect mode:      global
  Area mode:              physical library
============================================================


Timing
--------


  Clock  Period
---------------
Main_CLK 4000.0



  Cost     Critical       Violating
  Group   Path Slack TNS    Paths
-------------------------------------
C2C            934.7   0          0
C2O           1348.1   0          0
default       3574.9   0          0
I2C           3250.1   0          0
I2O         No paths   0
-------------------------------------
Total                  0          0

Instance Count
--------------
Leaf Instance Count             249
Sequential Instance Count        72
Combinational Instance Count    177
Hierarchical Instance Count      44

Area
----
Cell Area                          227032.622
Physical Cell Area                 0.000
Total Cell Area (Cell+Physical)    227032.622
Net Area                           2232.648
Total Area (Cell+Physical+Net)     229265.270

Power
-----
Leakage Power                      0.139 uW
Dynamic Power                      2150.416 uW
Total Power                        2150.556 uW

Max Fanout                         68 (ADC_SPI_sck)
Min Fanout                         0 (digital_inst/sar_lp_inst/DobleRegs/sw9n/SW_ctrl[0])
Average Fanout                     2.5
Terms to net ratio                 3.3
Terms to instance ratio            3.6
Runtime                            13.993 seconds
Elapsed Runtime                    26 seconds
RC peak memory usage:              175.00
EDI peak memory usage:             no_value
Hostname                           FV00
Final Runtime & Memory.
```

From this synthesis report, a main clock, *Main_CLK*, were used for both cases with a 4000 ps period, therefore working with a frequency of 250 MHz. Cost group did not show any path violation in typical and worst case.

In this report we can also see the number of instances that are in the design and the area that was used for design. Something that we notice is that the physical cell area is 0. To see the physical cell area, we had to look for another report, that can be found in Figure 60. We can see the area of our modules in the first 5 rows of the report.

Generated by: Encounter(R) RTL Compiler v14.10-s022_1 (Sep 3 2014)
Generated on: Aug 03 2021 22:04:26
Module: ADC_LP_bb
Technology libraries: physical_cells
tcb018gbwp7twc 270
tpd018nvwc 280a
Operating conditions: WCCOM
Interconnect mode: ple

Gate	Instances	Area	
TOTAL	255	227362.23	
Bootstrap_switch_split	2	21166.82	physical_cells
ADC_BGR	1	37113.41	physical_cells
DAC	1	162415.64	physical_cells
Dyn_comp_StrongArm_2in	1	124.68	physical_cells
INVD0BWP7T	59	388.55	tcb018gbwp7twc
MUX2D0BWP7T	51	1007.60	tcb018gbwp7twc
DFCNQD1BWP7T	39	1883.48	tcb018gbwp7twc
DFSND0BWP7T	20	1053.70	tcb018gbwp7twc
AN2D0BWP7T	11	120.74	tcb018gbwp7twc
BUFFD12BWP7T	11	531.24	tcb018gbwp7twc
EDFCNQD2BWP7T	10	658.56	tcb018gbwp7twc
INR2D0BWP7T	9	98.78	tcb018gbwp7twc
HA1D0BWP7T	5	164.64	tcb018gbwp7twc
NR2D0BWP7T	5	43.90	tcb018gbwp7twc

Figure 60: Report of Area utilized in the gates that were used in project

The total power that the ADC will consume is 6587.202 uW. This is high for the functionality that we want to give. And finally, the maximum fanout is 68 and the clock ADC_SPI_sck has it. This is the main clock of the system, so it makes sense that it goes to all those instances since we have not added a clock tree.

5.2. Physical synthesis

The output of the logic synthesis is given to a Place and Route Tool, in this case Encounter Digital Implementation (EDI) is used to perform Physical Synthesis. The objective of the physical synthesis is to optimize the design in terms of area, routing, and timing.

Physical synthesis needs several inputs to be performed: Verilog netlist, LEF libraries, timing libraries and timing constraints. The netlist is the result of the logical synthesis and describes the connections among all the components as logic gates, macros, and pins. Every cell must have a LEF library that contains detail information of area and routing. In this project timing libraries were not generated.

Process of the physical synthesis that is performs in this design consists in six steps: floorplan definition, create power ring, placement, clock tree synthesis, and routing. Figure 61 shows the placement of the modules (DAC, dynamic comparator, bootstrap switches, and band gap) and standard cells when clock tree synthesis is applied.

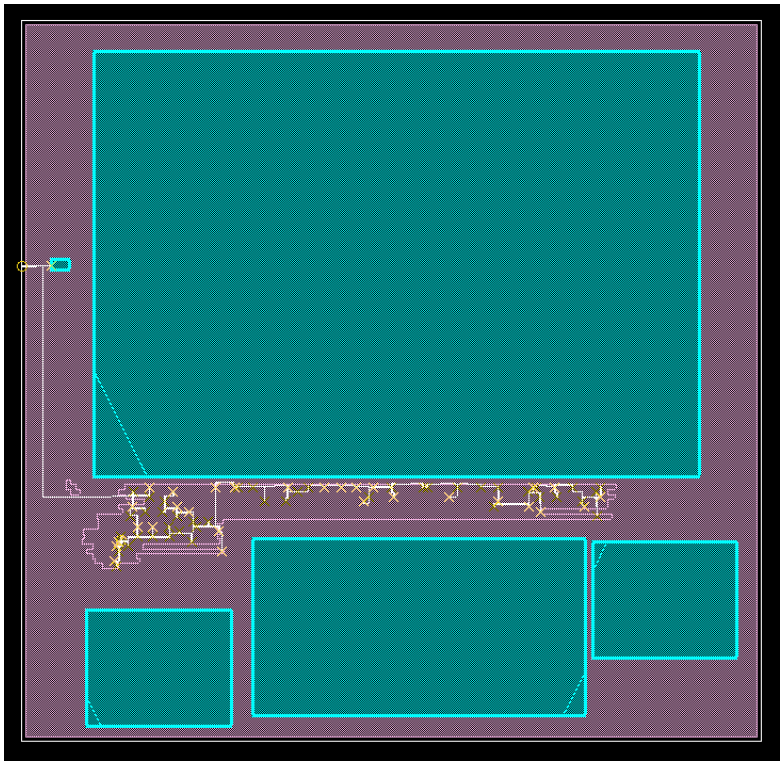


Figure 61: Clock Tree view

After clock tree synthesis was done, nano routing tool is used to generate the connections between modules and standard cells. Figure 62 shows placement of the modules and connections in the layout.

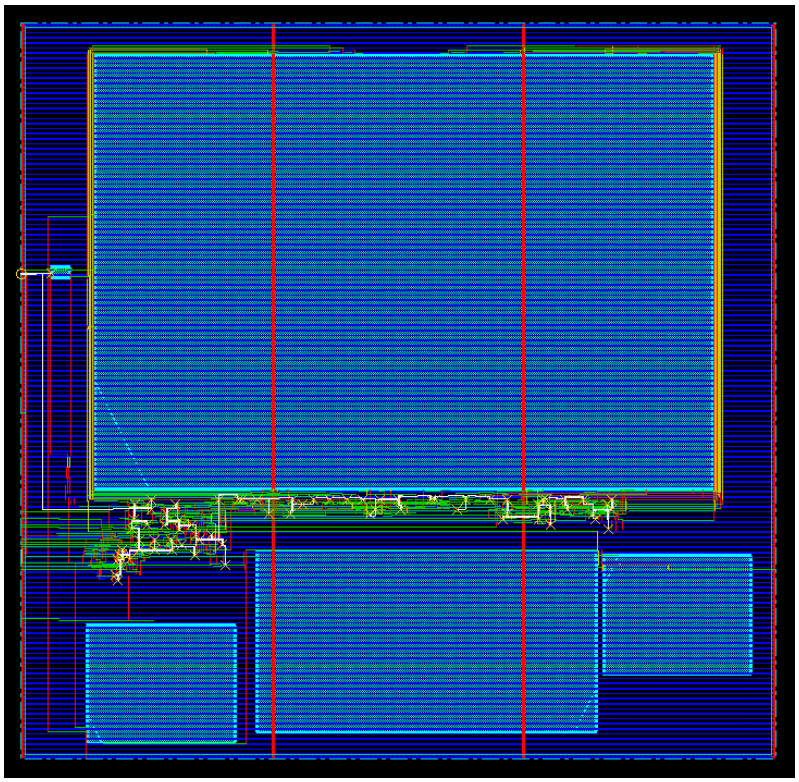


Figure 62: Physical view of the ADC

After routing cells and modules, net step is to verify the design, there are three verifications that can be done in Encounter: connectivity, geometry, and DRC. Next report shows geometry verification, this test check for violations of wiring, shorts between nets, overlap between cells, etc.

```
*** Starting Verify Geometry (MEM: 884.1) ***

  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 8320
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  182 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 182 Viols. 0 Wrngs.
VG: elapsed time: 1.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 2
  Antenna     : 0
  Short       : 180
```

```
  Overlap     : 0
End Summary

  Verification Complete : 182 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
```

Connectivity verification is a test that verify net connections, if there are any missing connection or shortcuts. Results are show below.

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Sun Aug  8 22:12:17 2021

Design Name: ADC_LP_bb
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (587.7050, 572.3200)
Error Limit = 1000; Warning Limit = 50
Check all nets
Net vref_gnd_w: no routing.
Net vref_vdd_w: no routing.

Begin Summary
    2 Problem(s) (ENCVFC-98): Net has no global routing and no special routing.
    2 total info(s) created.
End Summary

End Time: Sun Aug  8 22:12:18 2021
Time Elapsed: 0:00:01.0

******** End: VERIFY CONNECTIVITY ********
```

DRC verification is a test to check for any violations in connections and dimensions between cells. If there are violations in connectivity and geometry there are also show in this report.

```
*** Starting Verify DRC (MEM: 959.9) ***

  VERIFY DRC ..... Starting Verification
  VERIFY DRC ..... Initializing
  VERIFY DRC ..... Deleting Existing Violations
  VERIFY DRC ..... Creating Sub-Areas
  VERIFY DRC ..... Using new threading
  VERIFY DRC ..... Sub-Area : 1 of 1
  VERIFY DRC ..... Sub-Area : 1 complete 182 Viols.

  Verification Complete : 182 Viols.

 *** End Verify DRC (CPU: 0:00:00.1  ELAPSED TIME: 0.00  MEM: 1.5M) ***
```

Conclusions

In order to contribute to the SAR ADC project, three modules are designed: the dynamic comparator, the SR latch and the bootstrap switch. The methodology followed to design such modules consisted of finding the best topology to satisfy the requirements of an ADC for biosensor applications.

To design the dynamic comparator several topologies are examined and tested. Strong-Arm topology is chosen considering its low input offset and power consumption. Also, a technique to measure the dynamic offset is implemented. After simulating the strong-arm comparator exhaustively in 45 corners with all variations of process, temperature and voltage (PTV) it was demonstrated that all results comply with the design specification set. Finally, the physical design of the cell is implemented achieving the required quality for layout verifications, DRC and LVS test are clean. An area for improvement could be in the comparator design, since simulations showed errors in the comparison when both input voltages are between 0 and 270 mV.

The set reset latch module is designed at gate level, a meticulous sizing for most of the transistors is done to achieve symmetric gates and some digital logic is added to avoid prohibited condition in the latch and to add an external reset pin. Simulation is done individually and connected to the comparator making sure the latch eliminates pulses at the output of the comparator and gives a steady output to reduce power consumption. Although the individual latch simulation shows correct results, when the latch is integrated to the complete system, the ADC shows conversion errors, hence, the physical design of the latch is not implemented, and the latch is digital synthesized using a Verilog model and the RTL Compiler synthesis tool.

S/H circuit is designed using the bootstrap switch topology to minimized delay and distortion of the input signal. At this point of the project, the biggest challenge is to allow the switch to operate with the capacitance load of the DAC module, which is 288 pF, this is possible by carefully sizing transistors. Simulation and PTV analysis are completed, and physical design is implemented assuring to be DRC and LVS clean.

After the three modules are implemented and individually tested, showing good results, integration of the SAR ADC is done. The ADC logical synthesis shows a correct interconnection

of the modules and physical synthesis is partially completed since timing libraries are not generated, nevertheless results for the first layouts are shown as well as for the geometry and connectivity verifications. The experience developing this project is very valuable because we are able to know and follow the complete design flow from full custom modules until the integration of a complete system to achieve a functional tape-out. There were several complications and setbacks, but we were able to overcome those complications by applying the theory learned, as a result the knowledge and hands-on experience are very significant.

Appendix

A. CORNERS FOR PVT ANALYSIS

Corner name	Model	Temperature	Voltage
tsmc18_BC	ff	-40°C	1.98v
tsmc18_Typ	tt	27°C	1.8v
tsmc18_WC	ss	85°C	1.62v

B. TRANSISTORS SIZING OF COMPARATOR

Transistor Type	Name	W
PMOS	MP9, MP12	1.25um
PMOS	MP7, MP8	1.25um
NMOS	MN10, MN11	800nm
NMOS	MN1, MN2	800nm
NMOS	Mtail	800nm

C. TRANSISTORS SIZING OF BOOTSTRAP SWITCH

Transistor Type	Name	W	Multiplier
PMOS	MP3, MP4	2um	
PMOS	MP8	8um	
NMOS	MN7, MN10	4um	
NMOS	MN5, MN13	4um	
NMOS	MN9	4um	
NMOS	MN12	4um	
NMOS	MN11	900um	
Capacitor	C0	28.915um	6

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