

Towards Signal-Power Integrity Analysis by Efficient Power Delivery Network Lumped Models Obtained From Parameter Extraction

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Abstract — The combined signal integrity (SI) and power integrity (PI) design process is getting more relevant and complex as a result of the continuous computing system performance growth. This complexity drives longer design cycle times using traditional tools and methods. In this paper, a low computational cost optimization method based on a parameter extraction (PE) technique is proposed to develop accurate and fast power delivery network (PDN) lumped models. Once this model is available, it is used in the simulation process during the SI and PI analysis, making the whole design process much more efficient. Our proposed methodology is applied to a classical dual data rate (DDR) memory sub-system problem, saving 99.8% of the analysis time with only 1.2% of the computational resources typically used in current industrial practices.

Index Terms — amplitude noise, dual data rate, dynamic random access memory, jitter, optimization, parameter extraction, power delivery network, signal integrity, transceiver.

I. INTRODUCTION

System performance is a critical aspect during the design process of modern computer platforms. Performance is affected by many factors; one of them is the noise associated with the digital signal, which produces time (jitter) and amplitude deviations [1]. Amplitude noise and timing jitter can be severely deteriorated if the transceiver voltage supply is not sufficiently stable, which also depends on the power delivery network (PDN). Therefore, a suitable power integrity (PI) performance is critical to ensure adequate signal integrity (SI), making the PDN a key factor in the design process [2].

PDN design can be enhanced by using numerical optimization techniques. For instance, by optimizing decoupling capacitors [3-6], energy dissipation [7], etc. In this paper, we propose using optimization techniques to develop efficient PDN lumped models while preserving the accuracy of more complex and detailed PDN distributed models. We use a low computational cost optimization method based on a parameter extraction (PE) formulation. The resultant PDN lumped model can be used in an efficient SI-PI analysis and co-design. To illustrate our approach, the PDN quality of a dual data rate (DDR) memory sub-system is characterized, assessing its impact on SI to determine if the PDN design allows meeting the system performance targets. A dramatic reduction of the design cycle is achieved, saving 99.8% of the analysis time with respect to typical industrial practices, using only 1.2% of the computational resources.

II. EVALUATING THE INFLUENCE OF PDN ON SIGNAL INTEGRITY

Evaluating the impact of the PDN on SI usually starts by extracting all power interconnections and metallization using electromagnetic field solvers to obtain an accurate but large distributed PDN model. Such distributed models take long simulation time and use large computing resources. On the other hand, a typical single run SI simulation (without the PDN model) can take around an hour. For these reasons, distributed PDN models are not recommended for SI-PI evaluations. Instead, we propose using an optimized PDN lumped model attached to the SI simulation deck in order to size the PI effects on the signal quality.

III. DISTRIBUTED AND LUMPED PDN MODELS DESCRIPTION

A. Distributed Model Description

We model each component of the PDN by extracting its electrical representation. For the sake of accuracy, most of these electrical behavior extractions require electromagnetic full-wave 3D field solvers. After the extraction process, we obtain scattering parameters files to produce SPICE compatible macro-models. Then, we interconnect all modeled units to create a large distributed PDN model, as illustrated in Fig. 1. Simulating this distributed PDN model yields a target response \mathbf{R}^t for our parameter extraction formulation.

B. Lumped Model Description

The proposed lumped model is divided in three independent sections: mother board (MB) section, DIMM and DRAM section, and CPU section. A simplified representation is shown in Fig. 2 (the actual lumped model for this example consists of 55 lumped elements).

Some lumped elements are treated as pre-assigned parameters in our formulation: they remain fixed during PE optimization. Their values are established from datasheets, standards, and engineering expertise. Pre-assigned parameters are in vector $\mathbf{p} \in \mathfrak{R}^m$. Another group of lumped elements, whose parameter values are unknown, are in vector $\mathbf{x} \in \mathfrak{R}^n$ and are treated as design parameters or optimization variables. The response of the lumped model is denoted by $\mathbf{R}(\mathbf{x}, \mathbf{p})$. We aim at finding the optimal design parameters, \mathbf{x}^* , that makes

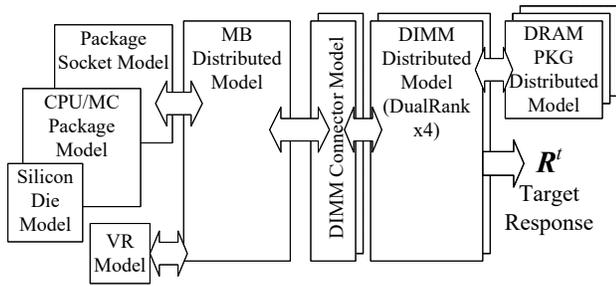


Fig. 1. Block diagram of the distributed PDN of the main power rail of a DDR3 memory sub-system.

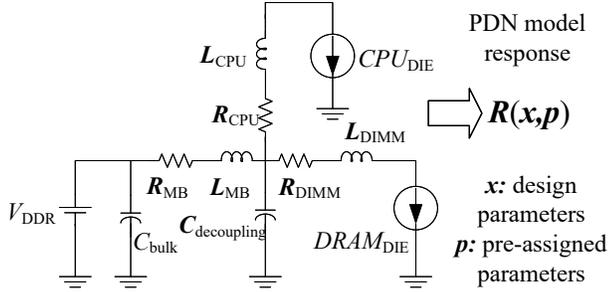


Fig. 2. Simplified lumped PDN model of the main power rail of a DDR3 memory sub-system.

$R(x^*, p)$ as close as possible to the target R^t .

IV. PARAMETER EXTRACTION BY OPTIMIZATION

A. Objective Function

The objective function $u(x)$ that we want to minimize uses three scalar multidimensional error functions: $e_1(x, p)$, $e_2(x)$, $e_3(x)$. It is defined as

$$u(x) = \max\{e_1(x), e_2(x), e_3(x)\} \quad (1)$$

where

$$e_1(x) = \|R(x, p) - R^t\|_2^2 \quad (2)$$

$$e_2(x) = \max(x - x_{\max}) \quad (3)$$

$$e_3(x) = \max(x_{\min} - x) \quad (4)$$

The objective function value in this PE problem is given by the maximum value among the three error function values. Error function e_1 represents the absolute difference between the AC responses of the PDN lumped model response $R(x, p)$ and the target AC response R^t from the distributed model. Error functions e_2 and e_3 are penalty functions; they are used to constrain the optimization variables in a feasible region defined by upper and lower bounds x_{\max} and x_{\min} .

B. Problem Formulation and Optimization Method

The aim of PE in this work consists of finding within a feasible region the optimal x that minimizes the error between $R(x, p)$ and the target response R^t , by solving

$$x^* = \arg \min_x u(x) \quad (5)$$

Error function (2) uses a least squares l_2 norm for matching both responses, and it is complemented with box constraints defined by (3) and (4) as penalty terms. To solve (5), we use

the direct search method Nelder-Mead available in Matlab¹.

C. Seed Values

The seed values or starting point $x^{(0)}$ for optimization are selected by estimating the resistance and inductance values by transforming the corresponding S-parameter matrix from the distributed parameter model.

D. Optimization Results

The system response using seed values $R(x^{(0)}, p)$ is evaluated and compared with target response R^t . As a result, it is found that the empirical methodology using S-parameter matrices for estimating lumped values is not accurate enough for predicting the PDN behavior. Fig. 3 shows the impedance profile response of the PDN for the lumped model using seed values and the distributed model or target response. The impedance errors across all frequencies are notably high.

System response after optimization $R(x^*, p)$ and the target response R^t are now much better matched, as show in Fig. 4. In this comparison, the impedance error at very low frequencies (below 1 KHz) is negligible, the impedance error at the first resonance frequency is just 1%, the impedance error at second resonance frequency is about 5% with no frequency shift, and the error at the third resonance frequency is about 32%. This third peak is governed by the DRAM package parasitics. However, these lumped elements are not included as optimization variables, thus, we believe this is the reason why matching that resonance peak does not improve.

We simulate both circuits: distributed and lumped models in transient regimen using HSPICE² simulation engine. We found a dramatic computational cost reduction using the lumped model. Lumped model uses only 1.2% of the total memory and 0.2% of the CPU time used by the distributed model. Although the PDN lumped model generation and optimization process could take around 8 hours; in many applications this extra time is worthwhile, as confirmed in the Section V.B.

V. OPTIMIZED PDN LUMPED MODEL APPLIED TO DDR SIGNAL INTEGRITY ANALYSIS

We attach the optimized lumped model into a SI model simulation deck in order to assess the benefits of the proposed PE optimization methodology during the design process of a DDR sub-memory system.

A. SI Analysis Assumptions

The memory configuration in evaluation consists of populating one memory channel with two DIMMs per channel (2 DPC), the DIMMs type are dual rank (2R) running at 1600 MT's. The PDN stimuli and the IO bit pattern assumes a 1 to 0 interleaving pattern (10101010 ...).

¹ MATLAB, Version 9.1.0, the MathWorks, Inc., 3 Apple Hill Drive, Natick MA 01760-2098, 2016.

² HSPICE®, ver. B-2008.09-SP1, Synopsys Inc., Mountain View, CA, 2008.

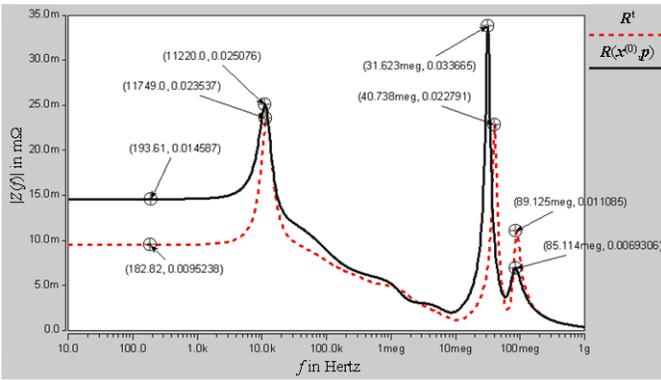


Fig. 3. Lumped model impedance profile response at the starting point $R(x^{(0)}, p)$ vs. target response R^t from the distributed model.

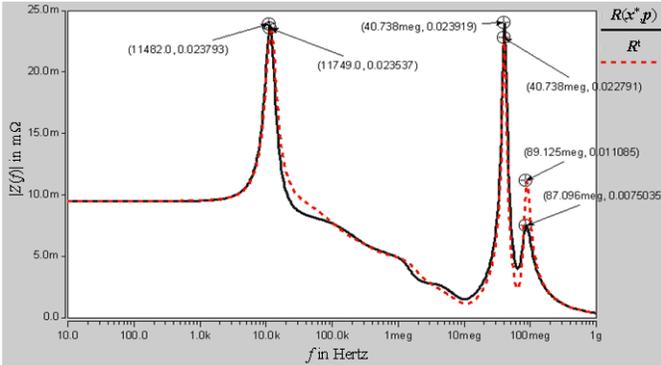


Fig. 4. Optimized lumped model impedance profile response $R(x^*, p)$ vs. target response R^t from the distributed model.

B. SI-PI Tests Description and Results

The evaluation consists of running the simulation by driving a 64 train of bits in 10 DQ lanes with 101010... bit pattern transitions with PDN noise stimuli. SI simulation time for a single run without PDN takes around 30-40 minutes, and once the optimized lumped PDN is incorporated the simulation time for a single run takes 11-12 hours. This time increment is caused by the complex transient stimulus applied to the PDN at multiple nodes. SI simulation time, using distributed PDN, is not tested due to the much longer simulation time implied. A very large simulation time reduction with a reasonable accuracy is the main benefit of using the lumped model instead of the distributed PDN model.

SI-PI evaluation results shows that the Rx and Tx signal amplitude of the 64 bit train of pulses is modulated by a noise signal coming from the DDR power rail (see Fig. 5); this noise is the resulting voltage variation due to the PDN noise. In consequence, the PDN causes a 90 mV degradation in the high-level input voltage (V_{IH}) at the receiver side Rx and 120 mV degradation at transmitter Tx, as showed in Fig. 5. This signal degradation due to PDN can severely affect the eye height (EH) margins in a units per million (UPM) analysis [8] which will significantly degrade the SI performance of the DDR channel. Potential solutions consist of adjusting the decoupling capacitors (caps) or improving the copper connection path to these caps by either placing them closer to

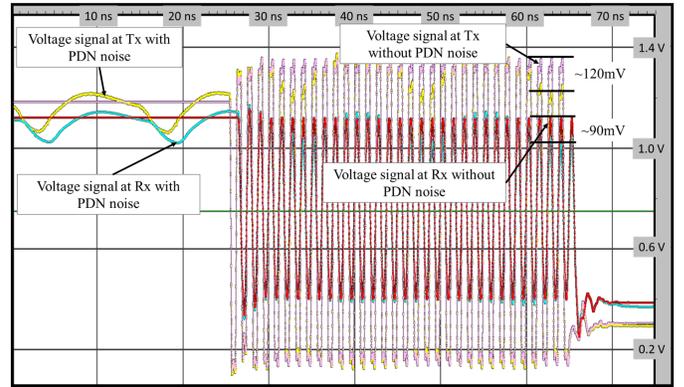


Fig. 5. Transmitter (Tx) and receiver (Rx) signals with and without PDN noise. 64 bits in 10 DQ lines with 101010 pattern is used.

the DRAM or strengthen the power plane, among others.

VI. CONCLUSION

A new PDN modeling methodology was introduced to allow efficient coupled SI-PI analysis and assessment. Our methodology exploits a simplified PDN lumped model obtained from a PE technique based on optimization methods. This methodology was tested into a SI-PI co-design of a DDR sub-memory system. In this testing deck, it was found that PDN noise impacted the signal integrity by injecting excessive noise into the Rx and Tx signals. It was demonstrated that the proposed method can significantly increase the design efficiency by reducing the simulation time of the PDN by approximately 99.8% of the simulation time using a standard industry methodology based on distributed models obtained from 3D full-wave EM field solvers. It was also demonstrated that the optimized PDN lumped model keeps a sufficient correlation with respect to the PDN distributed models.

REFERENCES

- [1] M. P. Li, *Jitter, Noise, and Signal Integrity at High-Speed*. Boston, MA: Prentice Hall, 2007.
- [2] V. S. Pandit, W. H. Ryu, and M. J. Choi, *Power Integrity for I/O Interfaces: with Signal Integrity/Power Integrity Co-Design*. Upper Saddle River NJ: Prentice Hall, 2011.
- [3] J. Chen and L. He, "Efficient in-package decoupling capacitor optimization for I/O power integrity," *IEEE Tran. Computer-Aided Design of Integrated Cir. Syst.*, vol. 26, no. 4, Apr. 2007, pp. 734-738.
- [4] S. Pan and B. Achkir, "Optimization of power delivery network design for multiple supply voltages," in *2013 IEEE Int. Symp. Electromagnetic Compatibility*, Denver, CO, Nov. 2013, pp. 333-337.
- [5] Intel Altera. (2005). *Using the Altera PDN Tool to Optimize your Power Delivery Network Design* (rev Jul. 2015) [Online]. Available: <https://www.intel.com/content/www/us/en/programmable/documentation/jba1434040249865.html>
- [6] T. Xu, *Circuit and System Level Design Optimization for Power Delivery and Management*, Ph.D. thesis, Dep. Graduate and Professional Studies, Texas A&M University, Texas, 2014.
- [7] H. Jung and M. Pedram, "Optimizing the power delivery network in dynamically voltage scaled systems with uncertain power mode transition times," in *2010 Design, Automation & Test in Europe Conf.*, Dresden, Germany, March 2010, pp. 351-356.
- [8] H. Zhang, S. Krooswyk, and J. Ou, *High Speed Digital Design: Design of High Speed Interconnects and Signaling*. Waltham, MA: Morgan Kaufmann, 2015.