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Departamento de Electrónica, Sistemas e Informática

**Maestría en Diseño Electrónico**

# REPORTE DE FORMACIÓN COMPLEMENTARIA EN ÁREA DE CONCENTRACIÓN EN DISEÑO ELECTRÓNICO DE ALTA FRECUENCIA

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**TRABAJO RECEPCIONAL** que para obtener el **GRADO** de **MAESTRO EN DISEÑO ELECTRÓNICO**


Presenta: **ADRIANA ELIZABETH GALINDO VERGARA**

Asesor **OMAR HUMBERTO LONGORIA GANDARA**


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# Introducción

En este documento se presentarán los proyectos realizados en la Maestría de Diseño Electrónico con tres asignaturas especializadas en el tema de Alta frecuencia. Las materias cursadas son las siguientes:

- Diseño Electrónico en Alta Frecuencia.
- Método de Simulación de Circuitos Electrónicos.
- Modelado y Diseño de Circuitos basado en Optimización.

El objetivo del documento es presentar evidencia del conocimiento adquirido, así como el impacto de los proyectos realizados durante cada una de las materias.

Los proyectos diseñados fueron pensados para resolver problemas existentes en la industria y que de esta manera se tuviera un impacto del cual se pudiera tomar ventaja y optimizar procesos en el trabajo diario que nos permita entregar tarjetas de circuito impreso (siglas en inglés PCB) con señales de alta velocidad mejorando la integridad de la señal, así como el entendimiento de los parámetros que podrían afectar las señales y los planos ruteados en una tarjeta.

Es importante resaltar que cada materia fue importante ya que se iban sentando las bases de conceptos teóricos y prácticos que ayudarían a generar un conocimiento que más adelante permitiría desarrollar proyectos que tuvieran impacto en la industria.

# 1. Resumen de los proyectos realizados

## 1.1. Cálculo de antipad para señales de alta velocidad en PCBs

### 1.1.1 Introducción

En el diseño de PCBs de alta velocidad es necesario realizar simulaciones en las cuales se utilizan herramientas como HFSS. En este proyecto se diseñó una tarjeta de validación eléctrica de un chip de Intel la cual requería optimizaciones de ruteo. Este diseño incluye un conector tipo *"Bulls eye"* de Samtec.
La topología que se simula va del conector hacia el chip por medio de un trazo con una impedancia controlada de 50 ohms. Esta topología se describe en la Fig. 1-1.

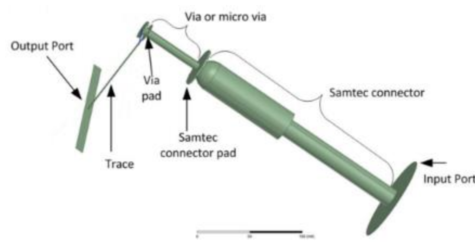


*Fig. 1-1 Topología simulada en HFSS: Samtec – Via – Trazo.*

Se debe mantener una impedancia de 50 ohms en la topología con el fin de evitar reflexiones. La impedancia se afecta por la capacitancia parásita de la vía por lo tanto se realizan simulaciones para encontrar el valor óptimo del diámetro del *antipad* para los planos de tierra y mantener bajo el valor de la capacitancia parásita. El *antipad* es descrito en la Fig. 1-2.

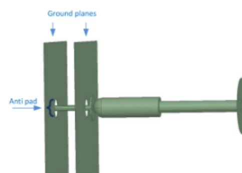


*Fig. 1-2 Antipad en los planos de tierra.*

### 1.1.2 Antecedentes

En el diseño PCBs de alta velocidad, es importante tener en cuenta los elementos parásitos.

La ecuación para el cálculo de la impedancia en el caso de un trazo en un PCB es la siguiente:

$$Z = R + jX_L + \frac{1}{jX_C} = R + jwL + \frac{1}{jwC} \qquad \textbf{(1-1)}$$

Donde $X_L$ = 2πfL es la componente que se relaciona con los trazos en el PCB.

$$X_C = \frac{1}{2\pi f C} \qquad \textbf{(1-2)}$$

$$w = 2\pi f_C \qquad \textbf{(1-3)}$$

Como se puede observar en la ecuación (1-1), la capacitancia es un factor clave en el cálculo de la impedancia. Por lo tanto, la capacitancia de la vía se debe tener en cuenta para el cálculo de la impedancia de la topología, como se describe en Fig. 1-1.

Se puede predecir la capacitancia parásita para una vía.

$$C = \frac{1.41\varepsilon r\, TD_1}{D_2 - D_1} \qquad \textbf{(1-4)}$$

Donde:

$D_1$ = Diámetro del antipad para planos de tierra.

$D_2$ = Diámetro del pad.

T = Grosor del PCB.

$\mathcal{E}_r$ = Permeabilidad eléctrica del dieléctrico.

C = Capitancita parásita de la vía (pF).

### 1.1.3 Solución desarrollada

El stack-up (capas de cobre y dieléctrico de una tarjeta de circuito impreso) mostrado en Fig. 1-3 fue utilizado como referencia para crear el modelo HFSS.

| | | | Customer Stack-up | OPCM Stack-up Information | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Layer | | Cu Weight | Thickness (mils) | Proposed Thickness (mils) | Structure | Via | Assume copper density | Ref | Diffential 100ohm +/- 10% | | Diffential 100ohm +/- 10% | |
| | | | | | | | | | Target LW/SP | Finished LW/SP | Target LW/SP | Finished LW/SP |
| | Soldermask | | 0.50 | 0.50 | | | | | | | | |
| L1 | Top | 1/3oz+Plating | 1.80 | 1.80 | | | 75% | | | | | |
| | Prepreg | | 3.60 | 3.60 | 1078RC72 | | | L1 & L3 | | 3.4/4.6 | | 3.8/8.2 |
| L2 | Signal | Hoz | 0.60 | 0.60 | | | 25% | | | | | |
| | Core | | 4 | 4 | 4mil core | | | | | | | |
| L3 | GND | Hoz | 0.60 | 0.60 | | | 75% | | | | | |
| | Prepreg | | 8.90 | 10.00 | 2116RC56 * 2 | | | | | | | |
| | Core | | 26 | 26 | 26mil dummy core | | | | | | | |
| | Prepreg | | 8.90 | 10.00 | 2116RC56 * 2 | | | | | | | |
| L4 | GND | Hoz | 0.60 | 0.60 | | | 75% | | | | | |
| | Core | | 4 | 4 | 4mil core | | | | | | | |
| L5 | Signal | Hoz | 0.60 | 0.60 | | | 25% | L4 & L6 | | 3.4/4.6 | | 3.8/8.2 |
| | Prepreg | | 3.60 | 3.60 | 1078RC72 | | | | | | | |
| L6 | Bottom | 1/3oz+Plating | 1.80 | 1.80 | | | 75% | | | | | |
| | Soldermask | | 0.50 | 0.50 | | | | | | | | |
| | | | | | | | | | | | | |
| Finished Thickness (mils) | | | | 68.20 | | | | | | | | |

*Fig. 1-3 Stack-up definido por el Fabricante.*

Se usó el modelo del conector proporcionado por la compañía SAMTEC. Se puede observar el PCB y el conector SAMTEC en la Fig. 1-4. La impedancia de la topología debe ser 50 ohms con

una tolerancia de ±5%. Se realizaron dos modelos de simulación uno con vías *through hole* y otro con microvías.

### 1.1.4 Análisis de resultados

Una vez que los modelos fueron creados se realizaron varias simulaciones para encontrar el valor óptimo del *antipad*. Se realizó la configuración para la simulación y se obtuvo un reporte de impedancias en el cual se muestra la impedancia y el tamaño de *antipad*. Para el caso de la vía *through hole* la impedancia obtenida con *antipads* de 60 mils y 28 mils fue de 53.56 ohms (este valor estaba fuera de especificación) y para la microvía se obtuvo una impedancia de 51.26 ohms, el cual cumplía con los requerimientos, en este caso el *antipad* era 45 mils y 50 mils.

### 1.1.5 Conclusión

Este proyecto permitió resolver un problema real de la industria, así como el entendimiento de los simuladores y su funcionamiento. Se hicieron varias simulaciones para la vía *through hole*, pero nunca se cumplió con la especificación lo importante de esto es saber jugar con los parámetros que se tienen ya sea *antipad*, material del dieléctrico, grosor del PCB etc.

## 1.2. Filtro pasa bandas

### 1.2.1 Introducción

El propósito de este documento es presentar las técnicas de diseño, análisis y simulaciones para un filtro pasa bandas con una frecuencia de corte de 1.45GHz y un ancho de banda de 145MHz.

### 1.2.2 Antecedentes

Un filtro pasa bandas solo permite señales dentro de un determinado bloque de frecuencia deseado y atenúa otras señales cuyas frecuencias están debajo o por encima de la misma. El rango de frecuencias que un filtro pasa bandas permite lo que se denomina banda de paso. Un filtro pasa bandas es usado en comunicaciones, radares e instrumentación. El diseño de filtros en líneas de transmisión *microstrip* es común para la implementación de filtros pasa bandas.

### 1.2.3 Solución desarrollada

Diseño de un filtro pasa bandas con las siguientes especificaciones.

*Center frequency* = $f_c$ = 1.45GHz.

*Bandwidth* = BW = 145MHz.

Orden = 3.

| $g_0$ | $g_1$ | $g_2$ | $g_3$ | $g_4$ |
|---|---|---|---|---|
| 0 | 1.5963 | 1.0967 | 1.5963 | 1.0000 |

Frecuencia de respuesta = 0.5dB Chebyshev.

Impedancia = 50Ω.

Material: Rogers (R04003C).

| Constante dieléctrica | Grosor de dieléctrico | Onzas de cobre | Loss tangent |
|---|---|---|---|
| 3.55 | 0.032” (0.813mm) | ½ oz | 0.0021 |

Se realizaron los cálculos con Scilab usando las fórmulas de la Fig. 2-1.

- The final element values for a band-pass prototype are obtained from ($R_0$ is the actual source resistance):

$$R_L = R_0 / g_{N+1}$$

If $g_k$ corresponds to an inductor in the low-pass prototype:

$$L_k = \frac{R_0 g_k}{\omega_0 \Delta} \quad \text{in series with} \quad C_k = \frac{\Delta}{R_0 \omega_0 g_k}$$

If $g_k$ corresponds to a capacitor in the low-pass prototype:

$$C_k = \frac{g_k}{R_0 \omega_0 \Delta} \quad \text{in parallel with} \quad L_k = \frac{R_0 \Delta}{\omega_0 g_k}$$

*Fig. 1-1 Componentes paralelos y seriales.*

El modelo circuital de filtro pasa bandas con los valores obtenidos se muestra en la Fig. 2-2.

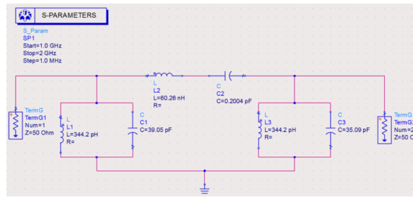

*Fig. 2-2 Modelo circuital de la primera topología.*

Los cálculos del diseño se realizaron sin sintonización para los cuales fue necesario calcular la impedancia en modo par e impar. Usando la calculadora de ADS y teniendo en cuenta los parámetros del material se obtuvieron los siguientes valores que se muestran en la Tabla 1.1.

| N | $Z_{oo}(\Omega)$ | $Z_{oe}(\Omega)$ | $Z_o(\Omega)$ | Ancho (mm) | Largo (mm) | Gap (mm) |
|---|---|---|---|---|---|---|
| 1 | 39.235544 | 70.604689 | 52.632817 | 1.1414600 | 31.888300 | 0.215276 |
| 2 | 39.509156 | 69.463428 | 52.387471 | 1.441860 | 31.838800 | 0.233158 |
| 3 | 39.509156 | 69.463428 | 52.387417 | 1.441860 | 31.838800 | 0.233158 |
| 4 | 39.235544 | 70.604689 | 52.632817 | 1.1414600 | 31.888300 | 0.215876 |

*Tabla 1.1*

### 1.2.4 Análisis de resultados

Se requiere sintonización para lograr el ancho de banda requerido. Esto se logra con ayuda de la opción de Tune en ADS. En la Fig. 2-3 se muestra el diseño del layout con la sintonización requerida.

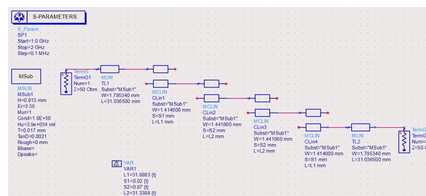

*Fig. 2-3 Esquemático con sintonización.*

### 1.2.5 Conclusiones

El filtro pasa bandas fue diseñado satisfactoriamente con ayuda del programa ADS. El diseño fue simulado como circuito, esquemático y layout, pero se debe tener en cuenta que para lograr los requerimientos es necesario realizar algunas optimizaciones.

## 1.3. Cálculo de antipad para señales de alta velocidad en PCBs usando métodos de optimización

### 1.3.1 Introducción

En este proyecto se diseñó una tarjeta de validación eléctrica para un chip de Intel la cual requería optimizaciones de ruteo. La topología que se deseaba simular va del conector *"Bulls eye"* de Samtec hacia el chip por medio de un trazo con una impedancia controlada de 50 ohms. Esta topología se describe en la Fig. 1-1.

Este proyecto fue la continuación de la materia de Métodos de Simulación de Circuitos Electrónicos, pero en esta asignatura se implementó una optimización por medio de un *driver*, el cual utiliza el modelo del conector y el modelo del PCB, para el cual era importante mantener la impedancia de 50 ohms para evitar reflexiones.

La impedancia se ve afectada por la capacitancia parásita de la vía por lo tanto se utilizó el método *fminsearch* y de esta manera se obtuvieron varias optimizaciones las cuales eran mostradas por medio de gráficas y así se obtuvo el mejor valor para los distintos *antipads* en los planos de tierra y por lo tanto mantener un valor bajo para la capacitancia parásita.

### 1.3.2 Antecedentes

En el diseño PCBs de alta velocidad, es importante tener en cuenta los elementos parásitos.

La ecuación para el cálculo de la impedancia en el caso de un trazo en un PCB es la siguiente:

$$Z = R + jX_L + \frac{1}{jX_C} = R + jwL + \frac{1}{jwC} \quad \textbf{(1-1)}$$

Donde $X_L$ = 2πfL es la componente que se relación con los trazos en el PCB.

$$X_C = \frac{1}{2\pi f C} \quad \textbf{(1-2)}$$

$$w = 2\pi f_C \quad \textbf{(1-3)}$$

Como se puede observar en la ecuación (1-1), la capacitancia es un factor clave en el cálculo de la impedancia. Por lo tanto, la capacitancia de la vía se debe tener en cuenta para el cálculo de la impedancia de la topología, como se describe en Fig. 1-1

Se puede predecir la capacitancia parásita para una vía.

$$C = \frac{1.41\varepsilon r\, TD_1}{D_2 - D_1} \quad \textbf{(1-4)}$$

Donde:

$D_1$ = Diámetro del antipad para planos de tierra.

$D_2$ = Diámetro del pad.

T = Grosor del PCB.

$\mathcal{E}_r$ = Permeabilidad eléctrica del dieléctrico.

C = Capitancita parásita de la vía (pF).

La tecnología de optimización de diseño automatizada está siendo adoptada en las principales industrias. Sin embargo, una de las desventajas que ofrece esto es que es complicado elegir un algoritmo de búsqueda de optimización apropiado para un determinado problema.

No existe un método o algoritmo único que funcione para una amplia solución de problemas. Para elegir un método se debe comprender el espacio de diseño, es decir, tipos de respuestas y variables. La computadora se usa para evaluar el modelo y buscar un mejor diseño.

### 1.3.3 Solución Desarrollada

El stack-up mostrado en Fig. 1-3 fue utilizado como referencia para crear el modelo HFSS.

Se uso el modelo del conector proporcionado por la compañía SAMTEC. Se puede observar el PCB y el conector SAMTEC en la Fig. 1-4. La impedancia de la topología debe ser 50 ohms con una tolerancia de ±5%. Se realizaron dos modelos de simulación uno con vías *through hole* y otro con microvías.

### 1.3.4 Análisis de resultados

Se realizó una simulación en HFSS en la cual los tamaños del *antipad* fueron cambiados manualmente. Las variables de optimización para este diseño son *antipad* 1 para la capa de Top y *antipad* 2 para capas internar y bottom, con un valor para la semilla de 46 mils y 56 mils respectivamente.

Para realizar la optimización fue necesario crear un *driver* en cual requería tener el modelo dibujado en HFSS, se generaba un archivo que contenía la información de como abrir un proyecto en HFSS, stack-up, modelo del conector, modelo del PCB y las variables que requerían ser optimizadas. Con el *driver* se obtenía un archivo de Excel que contenía impedancia y tiempo.

El código utilizado contenía las restricciones para la optimización. La impedancia de la señal de alta velocidad debería tener un valor de 50 ohms, pero el modelo tiene una tolerancia de 15%. La impedancia mínima y máxima es dada por el archivo de Excel.

Por último, se tiene otro código el cual usa el método *fminsearch* usado para la optimización y obtención de graficas.

Una vez que se corrió el programa de optimización varias simulaciones fueron realizadas. El mejor valor obtenido para el *antipad* 1 fue de 59.51 mils con una impedancia de 55.51 ohms y para el *antipad* 2 fue de 32.5 mils con una impedancia de 42.65 ohms, ambos con una tolerancia de 15%.

### 1.3.5 Conclusiones

Fue interesante trabajar con una herramienta para implementar nuestro diseño de PCB e integrar el modelo proporcionado por Samtec. De esta manera se realizaron simulaciones sobre tarjetas que se estarían diseñando.

Varias simulaciones fueron realizadas para el modelo *through hole*, pero la especificación no se estaba cumpliendo al 100%, pero se tenía una buena aproximación al valor deseado.

# 2. Conclusiones

Como Ingeniera de Diseño de Circuito Impreso el estudio de las diversas asignaturas cursadas en el área de concentración de Alta Frecuencia fueron clave para mi desarrollo Profesional ya que pude entender conceptos teóricos los cuales me ayudaron a profundizar en temas de mi interés que me ayudarán a realizar mi trabajo de una manera eficiente y con excelente calidad.

El conocimiento adquirido en el área de concentración elegida me permitió tomar ventaja de las herramientas, programas y método disponibles para de esta manera poder resolver problemas que enfrento en mi trabajo diario.

El desarrollo profesional que logré mientras cursaba estas materias me permitió tener un panorama más amplio y de esta manera me fue posible analizar e interpretar los datos de las simulaciones realizadas y con esto lograr optimizaciones que hoy en día en el diseño de alta velocidad son cruciales para su buen funcionamiento.

Actualmente el conocimiento adquirido durante la Maestría de Diseño Electrónico sigue teniendo gran impacto en mi trabajo diario.

# Apéndices

# A. ANTI PAD CALCULATION FOR A HIGH-SPEED PCB

INSTITUTO TECNOLÓGICO Y DE ESTUDIOS SUPERIORES DE OCCIDENTE

ITESO
Universidad Jesuita
de Guadalajara

# MAESTRÍA EN DISEÑO ELECTRÓNICO

## MÉTODO DE SIMULACIÓN DE CIRCUITOS ELECTRÓNICOS

PROFESOR: DR. ERNESTO RAYAS

**FINAL PROJECT: Anti pad calculation for a High-Speed PCB**


Adriana Galindo md690881
Jaime De La Torre Aguirre md692104

Mayo, 2016

December 2015
October 2015

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# 1 Introduction

In the design of PCBs that contains high speed signals, is very common to perform signal integrity simulations in certain areas of the design (the most critical ones), using tools like HFSS (High Frequency Structural Simulation) from ANSYS. In the case of this project, there was a need to design a board to perform electrical validation of one of the chips designed by Intel. The board include in its design a Samtec connector bulls eye type, like the one depicted in the figure 1.1

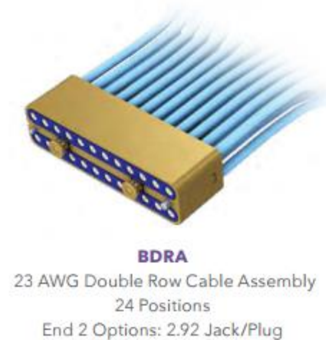



Figure 2.1 Samtec connector (bulls eye type).

The Samtec connector goes to the CPU via single ended lines with a controlled impedance of 50 ohms, and this was the part of the design that was simulated, which corresponds to the path: Samtec connector – connector pad - via – via pad - trace, which is described in the figure 1.2.

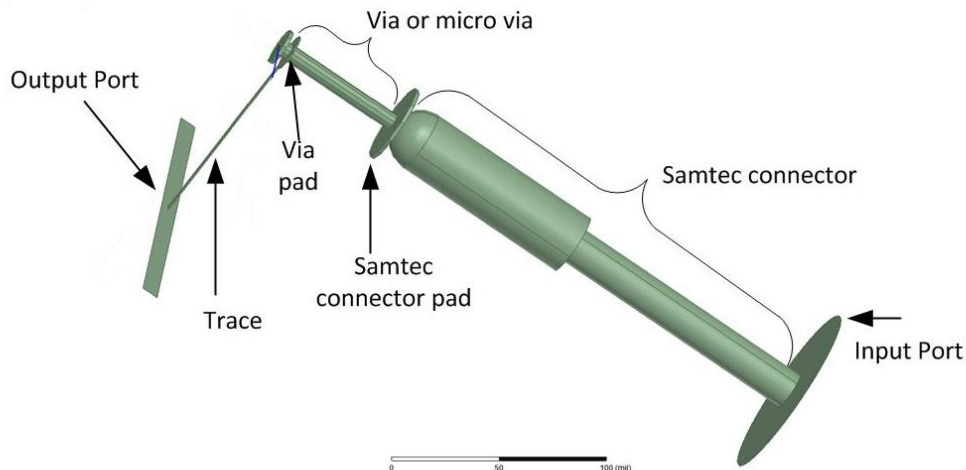



Figure 3.2 Path simulated: Samtec – Via - Trace

It is very important for the design, to maintain as much as possible the 50 ohms impedance in the path. One key element that is affecting the impedance is the parasitic capacitance of via, hence the importance to perform the simulations, to find the right value of the anti-pad diameter in the ground planes, to maintain that parasitic capacitance very low. The anti-pad is described in the figure 1.3.

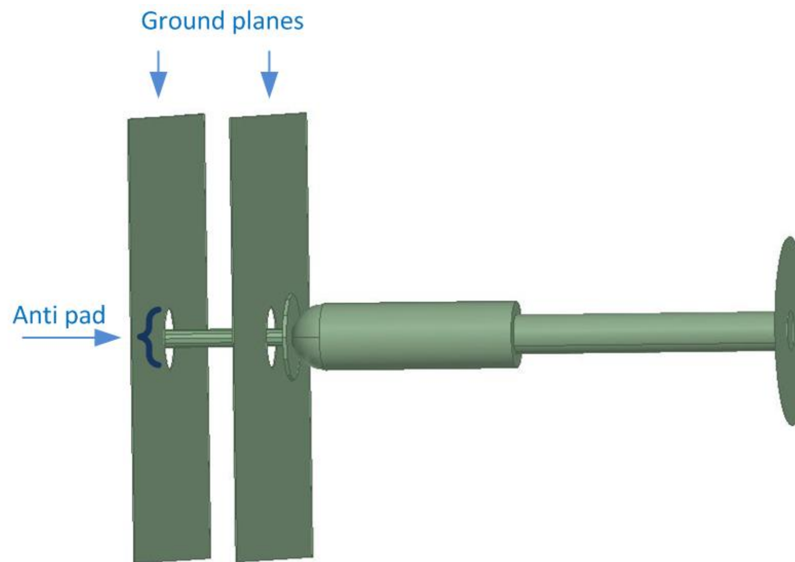



Figure 4.3 Anti pads in the ground planes

The present report contains the following elements:

- Theory to describe why is important to reduce the parasitic capacitance of the via
- Specifications of the PCB:
  - Board stack up
  - SAMTEC connector model
- Results of the models created in HFSS
  - Through hole via
  - Micro via
- Simulation results for through hole via and micro via
- And finally, the conclusions.

# 2 Theory

In the design of PCB boards that include higher speed frequencies, it is very important to take into account the parasitic elements that are intrinsic in the physical design. In this project, the parasitic capacitance of via is affecting the impedance of the complete signal path.

For the impedance equation, various forms exist depending on whether we are examining plane wave impedance, circuit impedance, and the like. For wire, or a PCB trace, the following equation is used:

$$Z = R + jX_L + \frac{1}{jX_C} = R + jwL + \frac{1}{jwC} \qquad (2.1)$$

where $X_L = 2\pi fL$ (the component in the equation that relates only to wires or PCB traces) [1]

$$X_C = \frac{1}{2\pi f C} \qquad (2.2)$$

$$w = 2\pi f_C \qquad (2.3)$$

As we can see in the equation 2.1, the capacitance is a key factor in the calculation of the impedance, that in the case of this project, the capacitance of the via was key for the calculation of the impedance for the complete path, which is formed by the SAMTEC connector, the via and the PCB trace, as described in the figure 2.1.

Every via has parasitic capacitance to ground. Vias being physically small structures, they behave very much like lumped circuit elements. We can predict, within an order of magnitude, the amount of parasitic capacitance for a via: [2]

$$C = \frac{1.41\varepsilon r\, TD_1}{D_2 - D_1} \qquad (2.4)$$

Where D2 = diameter of clearance hole in ground plane(s), in.
D1 = diameter of pad surrounding via, in.
T = thickness of printed circuit board, in.
εr = relative electric permeability of circuit board material
C = parasitic via capacitance, pF

When the pad size approaches the clearance hole diameter, pads pick up a lot more capacitance. If your ground clearance holes must remain small to maintain ground continuity, shrink or eliminate the pads on ground layers. For trace routing vias, it doesn't matter if you get some breakout on the plane layers. [2]

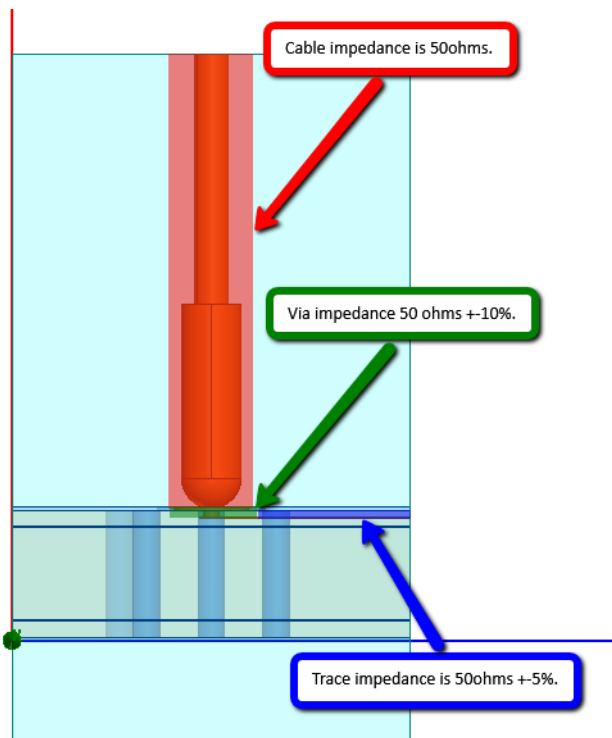



Figure 5.1 Impedance of the cable, via and trace.

The primary effect of via capacitance is that it slows down, or degrades, the rising edge of digital signals.

If we must make many pad capacitance predictions, it is recommended to use electromagnetic field modeling software, since these packages can (with enough computer resources) accurately model the inductance and capacitance of three-dimensional structures. [2]

In the development of this project, the PCB simulation that was used was HFSS.

As we can see in the equation 2.1, also the inductance is a key element that influence the calculation of the impedance, however, in this project was considered to be in control, because of the use of 7 ground vias that surrounds the via signal, following the recommendation of the Samtec connector designer. In this way, the influence of the inductance is kept in control. Those ground vias can be observed in the figure 2.2.

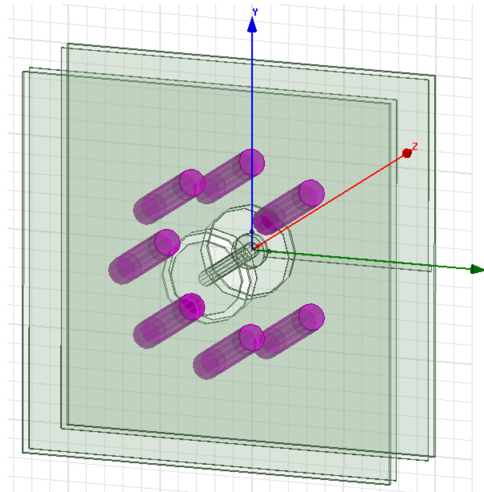



Figure 6.2 Ground vias surrounding the via signal

# 3 Project Development

## 3.1 Design Specifications

The PCB board with the following stack up has to be used, it was part of the requirement, to be able to design a board to transmit the high-speed signals. This stack up was provided by the PCB manufacturer vendor. The PCB material is low loss (Megtron6).

| | | | Customer Stack-up | OPCM Stack-up Information | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Layer | | Cu Weight | Thickness (mils) | Proposed Thickness (mils) | Structure | Via | Assume copper density | Ref | Diffential 100ohm +/- 10% Target LW/SP | Diffential 100ohm +/- 10% Finished LW/SP | Diffential 100ohm +/- 10% Target LW/SP | Diffential 100ohm +/- 10% Finished LW/SP |
| | Soldermask | | 0.50 | 0.50 | | | | | | | | |
| L1 | Top | 1/3oz+Plating | 1.80 | 1.80 | | | 75% | | | | | |
| | Prepreg | | 3.60 | 3.60 | 1078RC72 | | | L1 & L3 | | 3.4/4.6 | | 3.8/8.2 |
| L2 | Signal | Hoz | 0.60 | 0.60 | | | 25% | | | | | |
| | Core | | 4 | 4 | 4mil core | | | | | | | |
| L3 | GND | Hoz | 0.60 | 0.60 | | | 75% | | | | | |
| | Prepreg | | 8.90 | 10.00 | 2116RC56 * 2 | | | | | | | |
| | Core | | 26 | 26 | 26mil dummy core | | | | | | | |
| | Prepreg | | 8.90 | 10.00 | 2116RC56 * 2 | | | | | | | |
| L4 | GND | Hoz | 0.60 | 0.60 | | | 75% | | | | | |
| | Core | | 4 | 4 | 4mil core | | | | | | | |
| L5 | Signal | Hoz | 0.60 | 0.60 | | | 25% | L4 & L6 | | 3.4/4.6 | | 3.8/8.2 |
| | Prepreg | | 3.60 | 3.60 | 1078RC72 | | | | | | | |
| L6 | Bottom | 1/3oz+Plating | 1.80 | 1.80 | | | 75% | | | | | |
| | Soldermask | | 0.50 | 0.50 | | | | | | | | |
| | | | | | | | | | | | | |
| Finished Thickness (mils) | | | | 68.20 | | | | | | | | |

Figure 3.1 Stack up defined by the PCB Manufacturer

Using the stack up described in the figure 3.1 as a reference, the PCB model was created at the HFSS tool.

Another requirement was to use the SAMTEC connector model provided by the SAMTEC Company. The connector model contains all the characteristics needed to properly simulate the connector. The PCB model created was connected to the SAMTEC connector model, forming the complete model used in the HFSS simulations. The PCB and the Samtec connector can be seen in the Figure 3.2 and 3.3 respectively.

The requirement of the impedance path is that it must be 50 ohms ± 5%.

Figure 3.2 PCB and Samtec connector

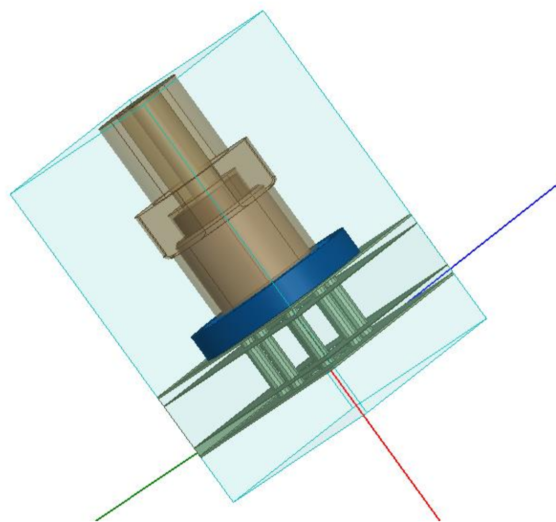


Figure 3.3 PCB and Samtec connector assembled

## 3.2 HFSS models

As we can see in the stack up described in the figure 3.1, there are two types of vias: A through hole via going from layer 1 thru 6, and micro vias going from layers 1 thru 2, and 5 thru 6. Therefore, two models were created. In one model we simulated the through hole via, and in the second model we simulated the micro vias.

### 3.2.1 HFSS model with the through hole via

The following pictures represents how the through hole via model was created. At the left-hand picture, the pads, connector, via and trace are highlighted. Then, at the right-hand picture, can be observed the PCB with the 7 via grounds, with the 4 ground layers.

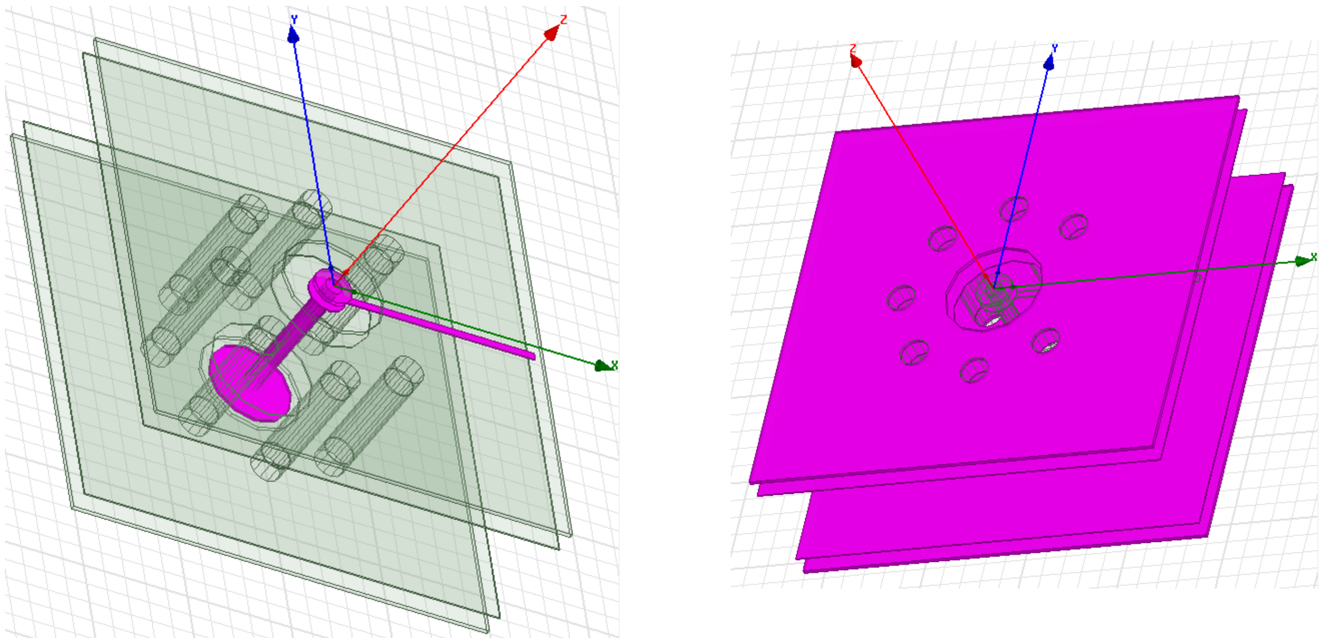



Figure 3.4 HFSS model for the through hole via

### 3.2.2 HFSS model with the micro via

The following pictures represents how the micro via model was created. At the left-hand picture, the pads, connector, via and trace are highlighted. Then, at the right-hand picture, can be observed the PCB with the 7 via grounds, with the 4 ground layers.

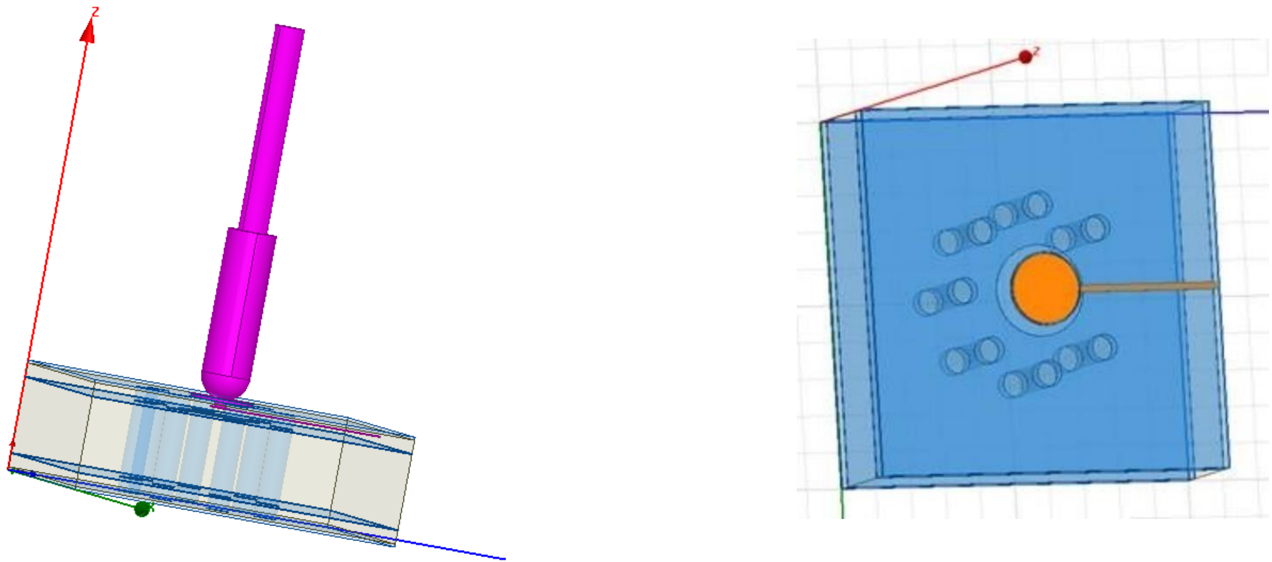


Figure 3.5 HFSS model for the micro via

## 3.3 Simulation results

Once the models were created, several simulations were performed to find the right values of the anti- pads. The tool was setup and the report was defined to obtain a Terminal TDR impedance. Those are the reports that will be presented in the graphs. The setup for the simulation is described below.

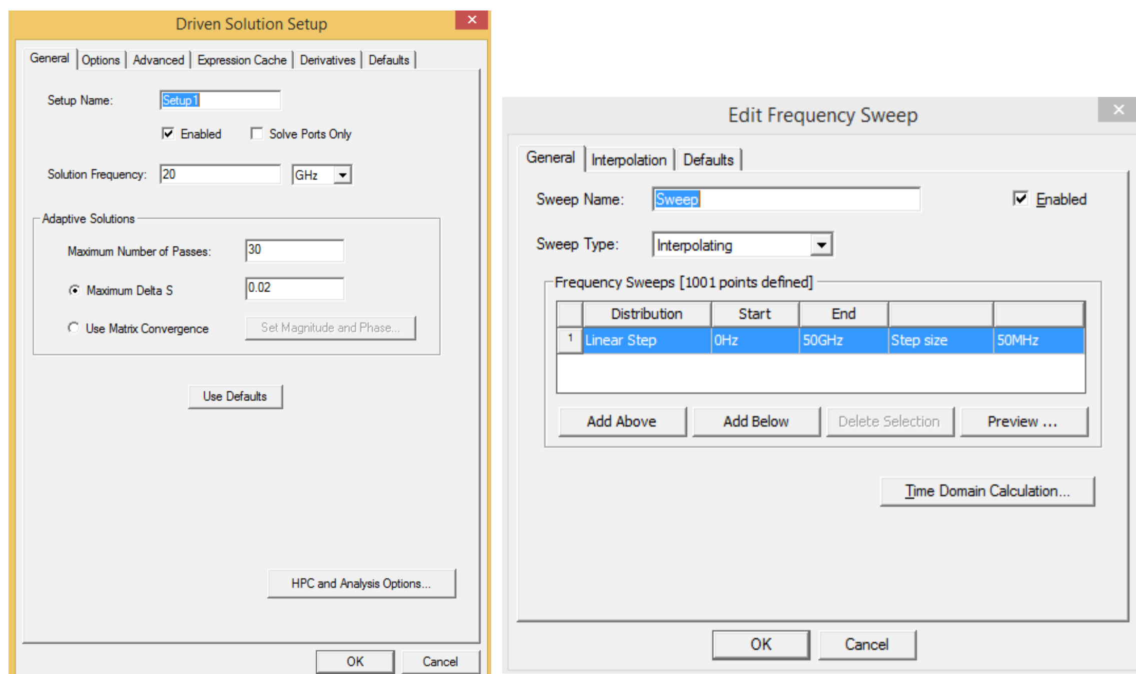



Figure 3.6 Simulation setup

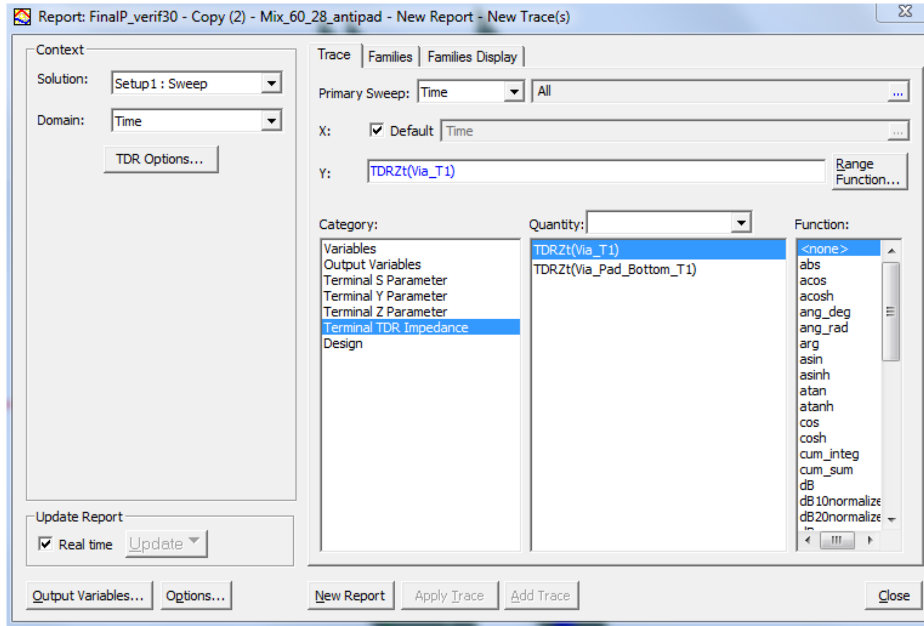



Figure 3.7 HFSS report setup

Now, since the size of the pad of the connector is different than the size of the pad of via, there are two anti-pad values that need to be modified. The figure 3.7 describe the 2 different anti-pads that were used. There is an anti-pad 1 that is used in ground layer 1 and an anti-pad2 that is used in ground layers 3,4 and 6.

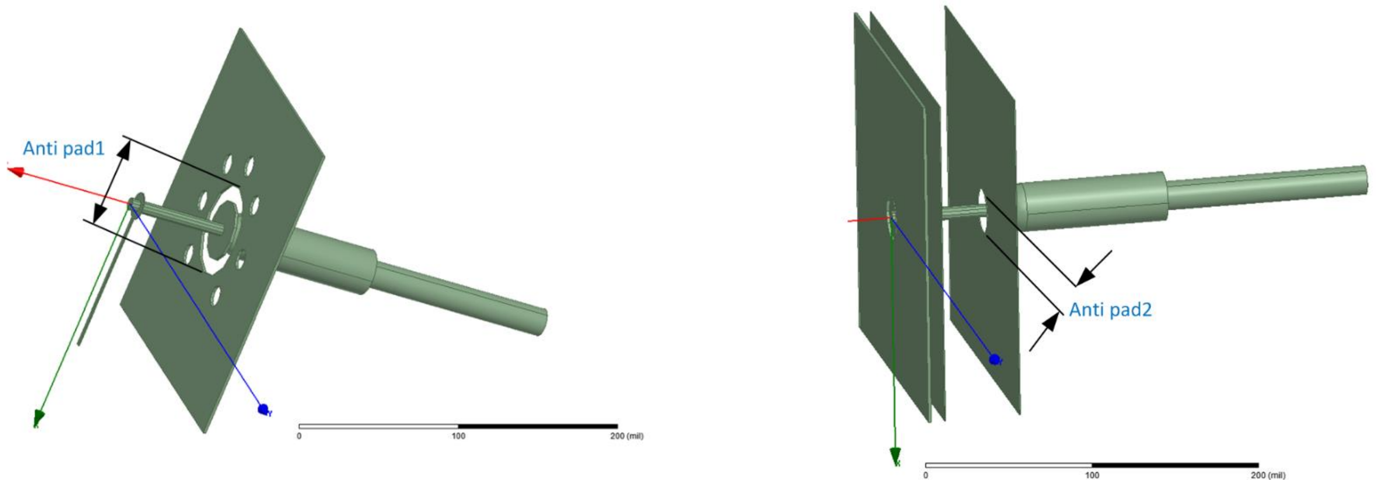



Figure 3.8 Anti-pad1 and Anti-pad2 definition

### 3.3.1 Through hole via results

The simulation results were divided in two parts. In the first part, the simulations were performed using the value of the anti-pad1 = antipad2, trying to find a common solution for both anti-pads to facilitate the PCB design work. The values of the anti-pad that were used, started at 40 mils and finished at 56 mils. However, the values of the impedance did not comply with the requirement of 50 ohms ± 5%. Those results can be observed in the Figure 3.8 below. The best value was obtained with an anti-pad diameter of 46.5 mils, but in some cases, the impedance was above 60 ohms. These results can be observed in the figure 3.8.

In the second part of the experiment, several values of anti-pad1 and anti-pad2 were tested, and the best value was obtained with anti-pad1 diameter = 60 mils and anti-pad2 diameter = 28 mils. In this case, the maximum impedance obtained was 53.56 ohms and the minimum was 44.06 ohms. Even though, is still out of specification, its values are really close to the expected values, and therefore it is acceptable. The results can be observed in the figure 3.9.

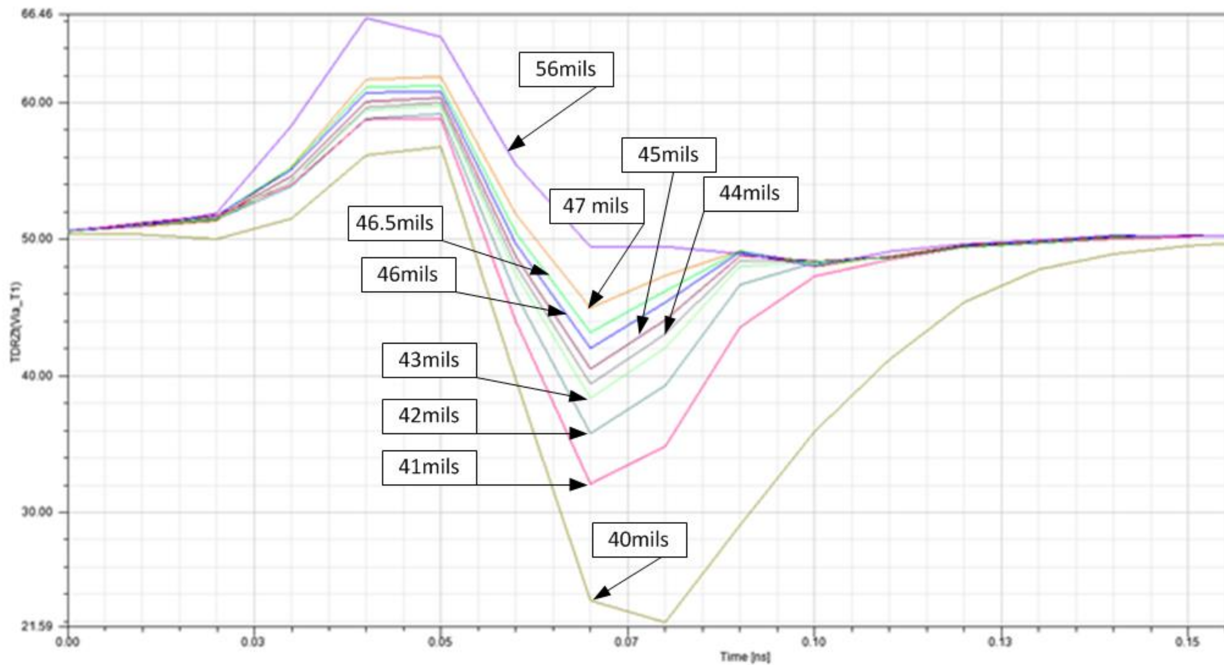



Figure 3.9. Through hole via results with Anti-pad1 diameter = Anti-pad2 diameter

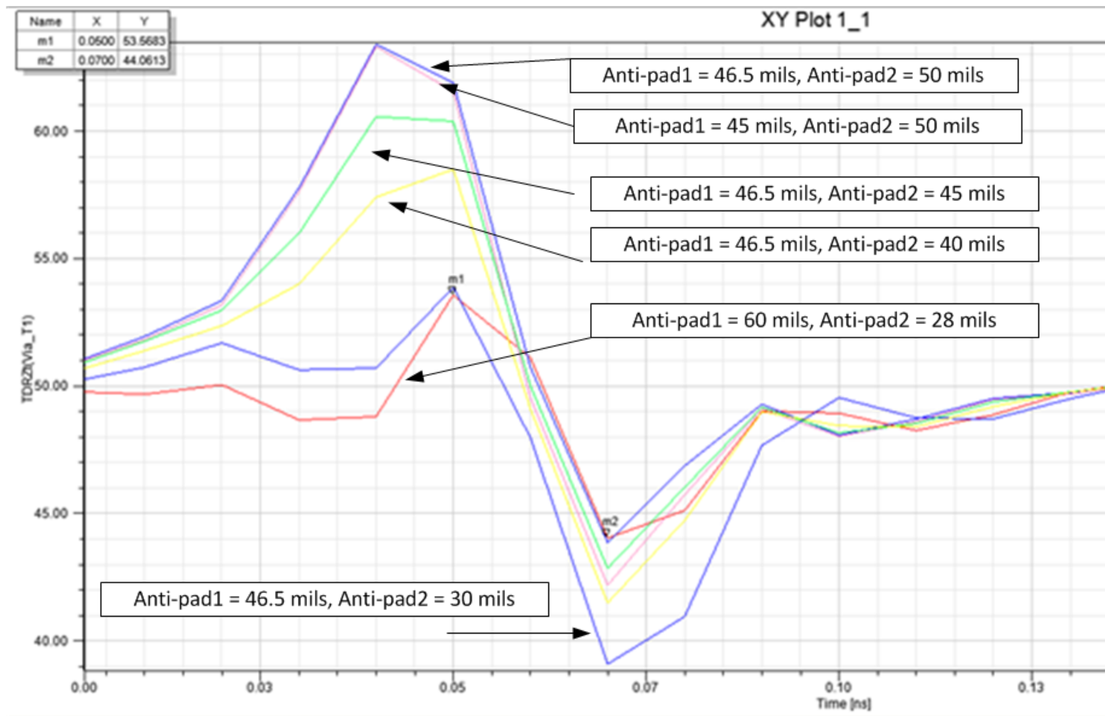



Figure 3.10. Through hole via results with Anti-pad1diameter different than Anti-pad2 diameter

### 3.3.2 Micro via results

In the case of the micro-via, better results were obtained. The best result was obtained with anti-pad1 diameter = 45 mils and anti-pad2 diameter = 50 mils. The results can be observed in the figure 3.10.

The maximum impedance value obtained was 51.26 ohms and the minimum impedance value obtained was 46.98 ohms. Both values comply with the specification of 50 ohms ± 5%. Those can be observed in the figure 3.11.

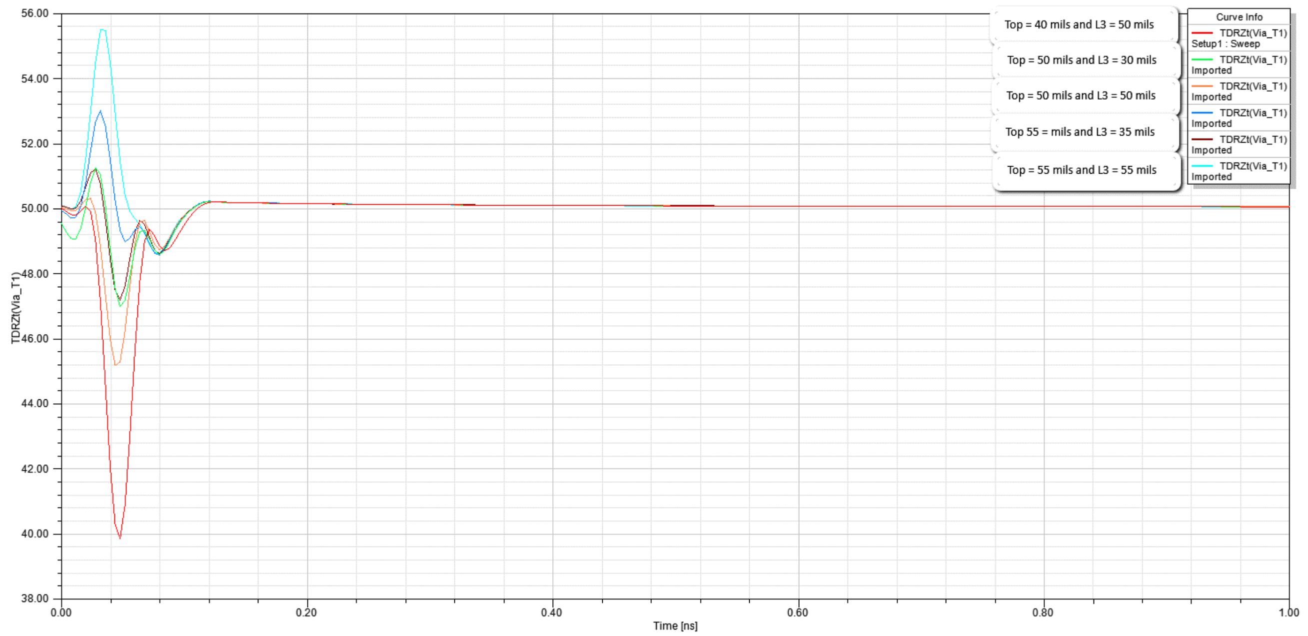



Figure 3.11 micro via results

TDR
Top_45_L3_50
Curve Info
TDRZt(Via_T1)
Setup1 : Sweep
0.03
51.26
4.28
46.98
TDRZt(Via_T1)
Time [ns]

Figure 3.12 Micro via best result value.

# 4 Conclusions

It was very interesting to work in a tool where we were able to implement our own PCB model and then integrate it with a model provided by a connector manufacturer. In this way, the simulations performed for our designs, will be closer to the reality, and we take advantage of the work performed by the connector manufacturer.

Several simulations were performed for the through hole via model, but we were not able to comply 100% with the specification, although it was very close. However, looks like this is not unusual. At the end, the idea is to be as close as possible to the ideal state, even though sometimes cannot be implemented in this way. However, it is a very good approximation.

Even though this tool was not reviewed in class, the basics and the elements for the Sonnet tool, helped a lot to understand easily this tool. The main ideas were clear, the rest is was just a matter of playing with the tool.

It was very nice to work in a project that Signal Integrity Engineers normally does. In this way, we got a better understanding of the work that they develop.

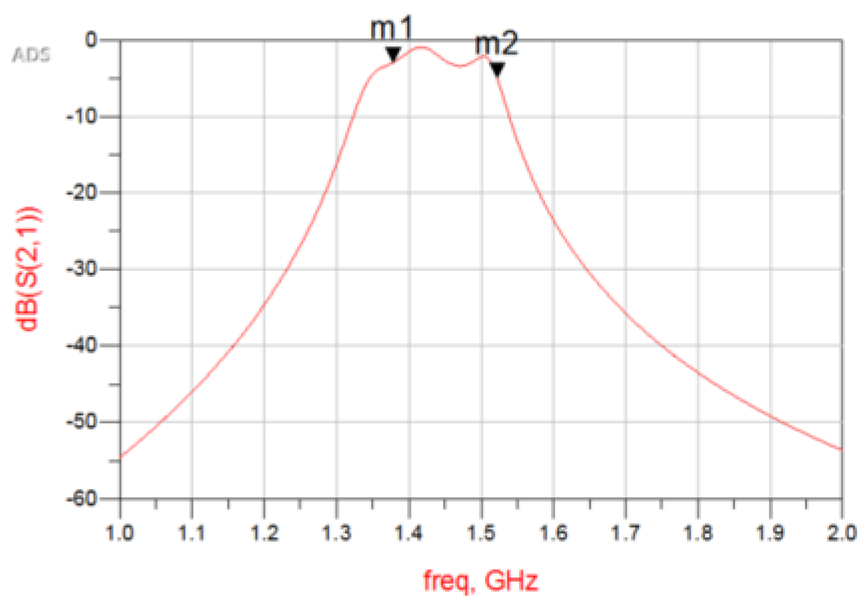
# 5 Bibliography


[1] Mark I. Montrose, “EMC and Printer Circuit Board”, Wiley, 1999, pp 34.

[2] Howard Johnson, Martin Graham, “High-Speed Digital Design”, Prentice Hall, 1993, pp 257.

## B. BANDPASS FILTER

# Bandpass filter





**Adriana Elizabeth Galindo Vergara**

**Número de Expediente: md690881**

**10-Octubre-2016**


ITESO
Universidad Jesuita
de Guadalajara

## Introduction of a Band-Pass filter

### Introduction

This document contains the design of a parallel-coupled microstrip bandpass filter. The aim of this document is to present the design technique, parameters analysis and simulations for a band pass filter with a cut frequency of 1.45GHz and a bandwidth 145MHz.

A bandpass filter only passes the frequencies within a certain desired band and attenuates other signals whose frequencies are either below a lower cutoff frequency or above an upper cutoff frequency. The range of frequencies that a passband filter allows to pass through is referred as passband. A typical bandpass filter can be obtained by combining a low –pass filter or applying conventional low pass to bandpass transformation.

### Bandpass filter

Bandpass filters serve a variety of functions in communications, radar and instrumentation subsystems. Of the available techniques based upon low pass elements of a prototype filter have yield successful results in a wide range of applications. The low pass prototype elements are the normalized values of the circuit components of a filter that have been synthesized for a unique passband respond, and in some cases, a unique out-of-band response. The low pass prototype elements are available to the designer in a number of tabulated sources and generally given in a normalized format, that is, mathematically related to a parameter of the filter prototype.

Low pass prototype filters are lumped elements networks that have been synthesized to provide a desired filter transfer function. The element values have been normalized with respect to one or more filter design parameters (cutoff frequency, for example) to offer the greatest flexibility, ease of use and tabulation. The elements of the low pass prototype filter are capacitors and inductors of the ladder networks of the synthesized filter network as shown in Figure 1.

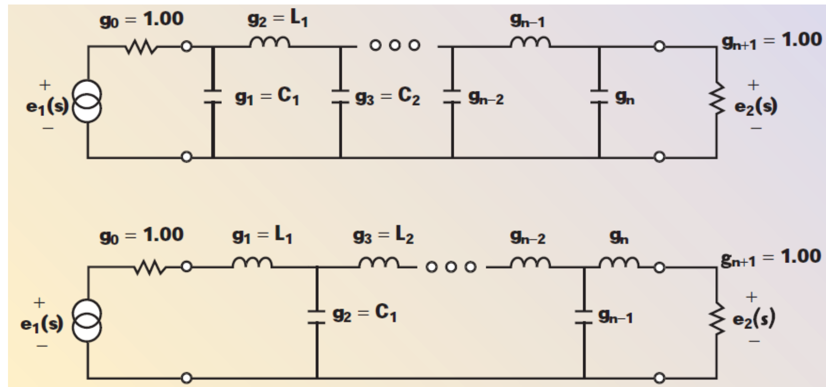



*Figure 7. Circuit topologies of low pass prototype filters.*

The transfer function T(s), is a polynomial of order n, where n is the number of elements of the low pass filter prototype.

A low pass filter may be converted to a band pass filter by employing a suitable mapping function. A mapping function is simply a mathematical change of variables such that a transfer function may be shifted in frequency. The mapping function may be intuitively or mathematically derived. A known low pass to bandpass mapping function may be illustrated mathematically as:

$$f' = \frac{f_0}{\Delta f}\left(\frac{f}{f_0} - \frac{f_0}{f}\right)$$

where

$$f_0 = \sqrt{f_1 f_2}$$
$$\Delta f = f_2 - f_1$$

and $f_0$, $f_1$ and $f_2$ represents the center, lower cutoff and higher cutoff frequencies of the corresponding band-pass filter, respectively. If the substitution of variables is made within the Chebyshev power transfer function. The power transfers function of the corresponding bandpass filter may be determined as shown in Figure 2.

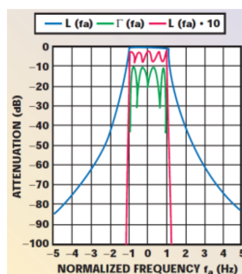



*Figure 8. Chebyshev bandpass filter schematic.*

The schematic diagram of the bandpass filter, which was derived from the low pass prototype filter via the introduction of complementary elements and producing shunt and series resonators, is shown in Figure 3. This is a basic low pass to bandpass transformation, and unfortunately sometimes leads to component values, which are not readily available of have excessive loss. As described later, the mapping function need to be considered as part of the bandpass filter design procedure. It is presented here as a supplement to the filter theory.

It bears repeating that the low pass prototype filter elements, that is, the g-values, are the result of network synthesis techniques to produce a desired characteristic of the prototype filter transfer function. The desired characteristics might include a flat amplitude response, maximum out-of-band rejection, linear phase response, Gaussian or other amplitude response minimum time sidelobes and match signals filters.

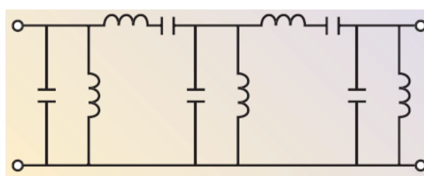


*Figure 9/ Chebyshev bandpass filter transfer function.*

**Microstrip**

A microstrip line filter includes stub impedances, step impedance and coupled line filter. Parallel coupled transmission-line filter in microstrip and stripline technology are very common for implementation of bandpass. Due to their relatively weak coupling, this type of filter has narrow fractional but instead has desired advantages such a low-cost fabrication, easy integration and simple designing procedure. Designing equations for the coupled line parameters such as space-gap between lines, line widths and lengths, can be found in classical microwave books. This way, following a well-defined systematic procedure, the required microstrip filter parameters can be easily derived for Butterworth and Chebyshev prototypes. The same can be done by using ADS software too.

## Theoretical Analysis

**Specifications for design:**

- Filter type: Band-Pass.

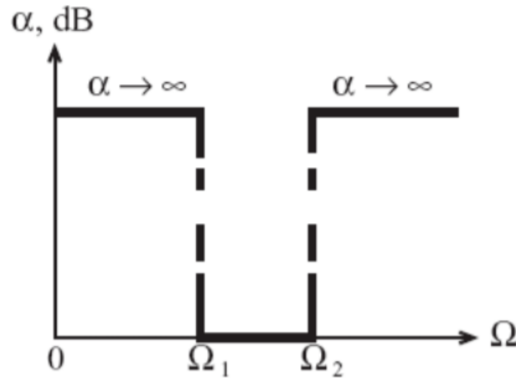



*Figure 10. Band Pass Filter.*

- $f_{center}$ = 1.45 GHz
- BW = 145 MHz
- Filter order = 3
  - $g_0$ = 0
  - $g_1$ = 1.5963
  - $g_2$ = 1.0967
  - $g_3$ = 1.5963
  - $g_4$ = 1.0000

(Assuming $g_0 = 1$ and $\omega_c = 1$)

0.5 dB Ripple

| $N$ | $g_1$ | $g_2$ | $g_3$ | $g_4$ | $g_5$ | $g_6$ | $g_7$ | $g_8$ | $g_9$ | $g_{10}$ | $g_{11}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0.6986 | 1.0000 | | | | | | | | | |
| 2 | 1.4029 | 0.7071 | 1.9841 | | | | | | | | |
| 3 | 1.5963 | 1.0967 | 1.5963 | 1.0000 | | | | | | | |
| 4 | 1.6703 | 1.1926 | 2.3661 | 0.8419 | 1.9841 | | | | | | |
| 5 | 1.7058 | 1.2296 | 2.5408 | 1.2296 | 1.7058 | 1.0000 | | | | | |
| 6 | 1.7254 | 1.2479 | 2.6064 | 1.3137 | 2.4758 | 0.8696 | 1.9841 | | | | |
| 7 | 1.7372 | 1.2583 | 2.6381 | 1.3444 | 2.6381 | 1.2583 | 1.7372 | 1.000 | | | |
| 8 | 1.7451 | 1.2647 | 2.6564 | 1.3590 | 2.6964 | 1.3389 | 2.5093 | 0.8796 | 1.9841 | | |
| 9 | 1.7504 | 1.2690 | 2.6678 | 1.3673 | 2.7239 | 1.3673 | 2.6678 | 1.2690 | 1.7504 | 1.0000 | |
| 10 | 1.7543 | 1.2721 | 2.6754 | 1.3725 | 2.7392 | 1.3806 | 2.7231 | 1.3485 | 2.5239 | 0.8842 | 1.9841 |

(In this case, $\omega_c$ is at −0.5dB)

*Figure 11. Element Values L-P Prototypes (Chevyshev).*

- Type of frequency response = 0.5 dB Ripple Chebyshev.

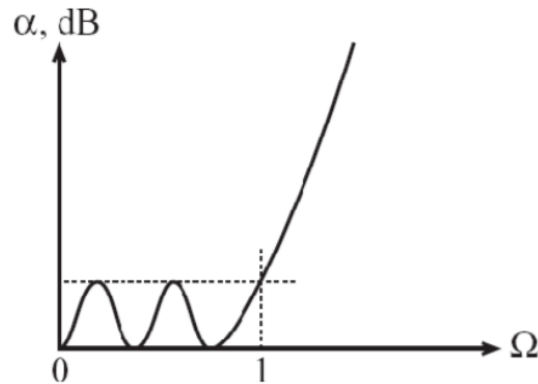



*Figure 12. Chevyshev*

- Reference impedance = 50Ω.
- Rogers (http://www.rogerscorp.com/acs/producttypes/9/RO4000-Laminates.aspx)
  - H = 0.813mm (Dielectric thickness).
  - Cladding of 0.5oz = Trace thickness = 17µm = $17X10^{6}$ meters.
  - Er = 3.55 (Relative permitiavility).

Material: R04003C

| **Dielectric constant (Er – Relative permitiavility)** | 3.55 |
|---|---|
| **Standard thickness (Dielectric thickness)** | 0.032” (0.813mm) |
| **Standard copper cladding** | ½ oz (17µm) electrodeposited copper foil (0.5ED/0.5ED) |
| **Dissipation factor tan (Loss tangent at 2.5GHz/23C)** | 0.0021 |

**Formulas to solve the problem:**

Low pass to band transformation:

We apply the following transformation:

$$\omega \leftarrow \frac{\omega_0}{\omega_2 - \omega_1}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) \qquad \omega_0 = \sqrt{\omega_1 \omega_2}$$

Low-pass Scaled      Band-pass

$P_{LR}$   $-1$   $1$   $\omega$      $P_{LR}$   $-\omega_0$   $\omega_0$   $-\omega_2$   $-\omega_1$   $\omega_1$   $\omega_2$   $\omega$

*Figure 13. Low pass to band transformation.*

De-Normalized Element Values B-P Prototypes

- The final element values for a band-pass prototype are obtained from ($R_0$ is the actual source resistance):

$$R_L = R_0 / g_{N+1}$$

If $g_k$ corresponds to an inductor in the low-pass prototype:

$$L_k = \frac{R_0 g_k}{\omega_0 \Delta} \quad \text{in series with} \quad C_k = \frac{\Delta}{R_0 \omega_0 g_k}$$

If $g_k$ corresponds to a capacitor in the low-pass prototype:

$$C_k = \frac{g_k}{R_0 \omega_0 \Delta} \quad \text{in parallel with} \quad L_k = \frac{R_0 \Delta}{\omega_0 g_k}$$

*Figure 14. De-Normalized Element Values B-P Prototypes.*

## **Circuital Model: Circuit for design for first topology:**

### 1) Calculations in Scilab:

```
// Requirements:

fc = 1.45e9;    // Central Frequency
Zo = 50;       // Characteristic Impedance
N  = 3;       // Filter Grade

// Calculations:

BW = 145e6; // Bandwidth
A = BW/2; // To obtain Low frequency and high frequency
f1 = 1.45e9 - A; // Low Frequency
f2 = 1.45e9 + A; // High Frequency
D   = (f2-f1)/fc //Fractional bandwidth
iat = (f2/fc)-1;
Wo  = sqrt((2*%pi*f1)*(2*%pi*f2));
Vp  = 3e8/sqrt(Er);

// The G parameters for a 3rd order Chebyshev Filter are:

g0 = 1;
g1 = 1.5963;
g2 = 1.0967;
g3 = 1.5963;

// Transforming the low pass filter to band pass filter  //

//Paralel Components

L1=(Zo*D)/(Wo*g1);
C1=g1/(Zo*Wo*D);

L3=(Zo*D)/(Wo*g3);
C3=g3/(Zo*Wo*D);

//  Serial Components

L2=(Zo*g2)/(Wo*D);
C2=D/(Zo*Wo*g2);
```

```
// Concentrate Components Topology:

 disp("WLAN BAND-PASS FILTER");

 disp("Concentrate Components Topology:");
 disp("-- Z0 ---------L2--C2--------------");
 disp("       |  |       |  |       ");
 disp("      L1  C1      L3  C3      ");
 disp("       |  |       |  |       ");
 disp("-----------------------------------");

 disp("L1 = "+string(L1));
 disp("C1 = "+string(C1));

 disp("L2 = "+string(L2));
 disp("C2 = "+string(C2));

 disp("L3 = "+string(L3));
 disp("C3 = "+string(C3));
```

2) Topology:

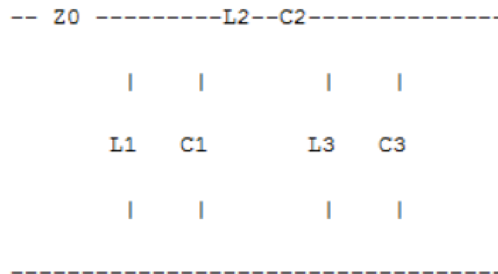



*Figure 15. Topology for Bandpass Filter.*

3) Values:

Parallel:

$L_1$ = 3.442X$10^{-10}$ = 344.2pH.
$C_1$ = 3.509X$10^{-11}$ = 35.09pF
$L_3$= 3.442X$10^{-10}$ = 344.2pH.
$C_3$= 3.509X$10^{-11}$ = 35.09pF.

Serie:
$L_2$ = 6.026X$10^{-8}$ = 60.26nH.
$C_2$ = 2.004X$10^{-13}$ = 0.2004pH.

4) Circuit for design for first topology:

   a) Define the geometry

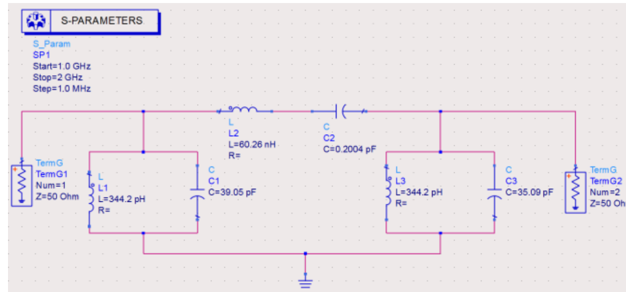



*Figure 16. Circuital model.*

5) Simulations:

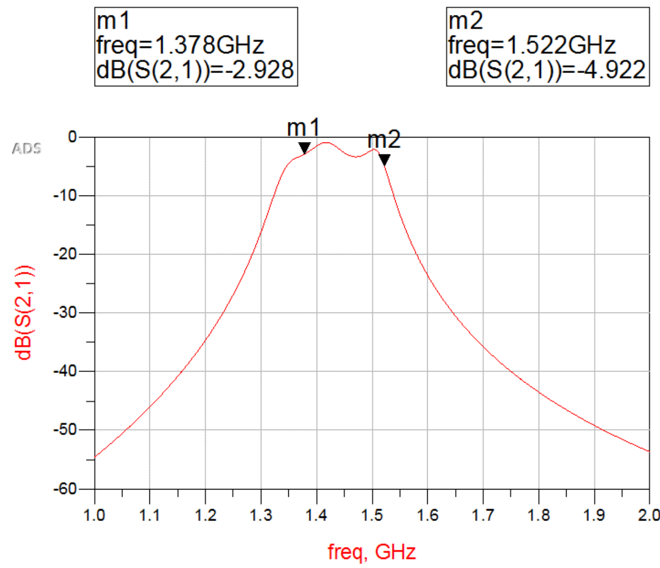



*Figure 17. F1 = 1.378GHz and F2 = 1.522GHz*

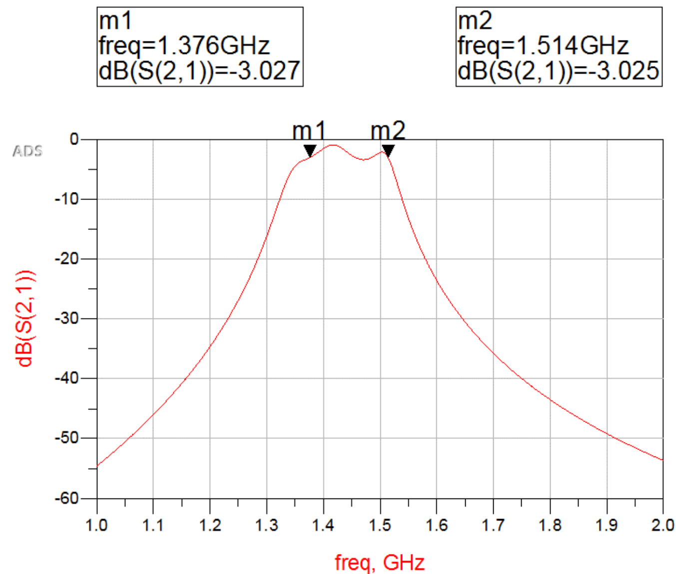



*Figure 18. F1 = 1.376GHz and F2 = 1.514GHz.*

## Schematic Model: Design with no tuning.

### 1) Calculations in Scilab:

```
// Requirements:

fc = 1.45e9;    // Central Frequency
Zo = 50;       // Characteristic Impedance
N = 3;       // Filter Grade

// PCB parameters:

Er = 3.55;     // Relative permitiavility or dielectric constant
lt = 0.0021     // Loss Tangent
H  = 0.000813;   // Dielectric thickness specified in meters
T = 17e6; // Trace thickness specified in meters

// Calculations:

BW = 145e6; // Bandwidth
A = BW/2; // To obtain Low frequency and high frequency
f1 = 1.45e9 - A; // Low Frequency
f2 = 1.45e9 + A; // High Frequency
D   = (f2-f1)/fc //Fractional bandwidth
iat = (f2/fc)-1;
Wo  = sqrt((2*%pi*f1)*(2*%pi*f2));
Vp  = 3e8/sqrt(Er);

// Defining column vectors to store values/results

J_N  = zeros(5,1);
ZO_N = zeros(5,1);
ZE_N = zeros(5,1);
```

```
// The G parameters for a 3rd order Chebyshev Filter are:

g0 = 1;
g1 = 1.5963;
g2 = 1.0967;
g3 = 1.5963;
g4 = 1;

// Transforming the low pass filter to band pass filter //

//Paralel Components

L1=(Zo*D)/(Wo*g1);
C1=g1/(Zo*Wo*D);

L3=(Zo*D)/(Wo*g3);
C3=g3/(Zo*Wo*D);

//  Serial Components

L2=(Zo*g2)/(Wo*D);
C2=D/(Zo*Wo*g2);

//  Odd and Even Z characteristics calculations:

J_N(1,:) = (1/Zo)*sqrt((%pi*D)/(2*g0*g1));
J_N(2,:) = (1/Zo)*sqrt((%pi*D)/(2*g1*g2));
J_N(3,:) = (1/Zo)*sqrt((%pi*D)/(2*g2*g3));

ZO_N(1,:) = Zo*(1-(Zo*J_N(1))+((Zo*J_N(1))^2));
ZO_N(2,:) = Zo*(1-(Zo*J_N(2))+((Zo*J_N(2))^2));
ZO_N(3,:) = Zo*(1-(Zo*J_N(3))+((Zo*J_N(3))^2));

ZE_N(1,:) = Zo*(1+(Zo*J_N(1))+((Zo*J_N(1))^2));
ZE_N(2,:) = Zo*(1+(Zo*J_N(2))+((Zo*J_N(2))^2));
ZE_N(3,:) = Zo*(1+(Zo*J_N(3))+((Zo*J_N(3))^2));

// Concentrate Components Topology:

    disp("WLAN BAND-PASS FILTER");

    disp("Concentrate Components Topology:");
    disp("-- Z0 ---------L2--C2--------------");
    disp("       |   |        |   |       ");
    disp("      L1   C1       L3   C3       ");
    disp("       |   |        |   |       ");
    disp("-----------------------------------");

    disp("L1 = "+string(L1));
    disp("C1 = "+string(C1));

    disp("L2 = "+string(L2));
    disp("C2 = "+string(C2));

    disp("L3 = "+string(L3));
    disp("C3 = "+string(C3));
```

2) Values:

```
Zodd = 39.235544

Zodd = 39.509156

Zodd = 39.509156

Zodd = 39.235544

Zodd = 0

Zeven = 70.604689

Zeven = 69.463428

Zeven = 69.463428

Zeven = 70.604689

Zeven = 0
```

*Figure 19.Scilab results for odd and even impedances.*

We use the following design equations to get the inverter constant for a coupled line filter with N+1 sections:

$$Z_0 J_1 = \frac{\sqrt{\Pi\Delta}}{\sqrt{2g_1}}$$

$$Z_0 J_n = \frac{\Pi\Delta}{2\sqrt{g_{n-1} g_n}} \qquad ; n = 2,3,4 \ldots . N$$

$$Z_0 J_{n+1} = \sqrt{\frac{\Delta\Pi}{2 g_n g_{n+1}}}$$

Using these equations, we get:

| $Z_0J_1$ | 0.0062738 |
|---|---|
| $Z_0J_2$ | 0.0059909 |
| $Z_0J_3$ | 0.0059909 |

The even and odd mode impedances can be calculated as follows:

$$Z_{oe} = Z_0[1 + JZ_0 + (JZ_0)^2]$$

*Figure 20. Even mode impedance.*

$$Z_{oo} = Z_0[1 + JZ_0 + (JZ_0)^2]$$

*Figure 21. Odd mode impedance.*

The results these calculations are tabulated below:

| N | $Z_{oe}$ (Ω) | $Z_{oo}$(Ω) |
|---|---|---|
| 1 | 39.235544 | 70.604689 |
| 2 | 39.509156 | 69.463428 |
| 3 | 39.509156 | 69.463428 |

The subtracted used is RO4003C (MSUB) with $E_r$ = 3.55, H = 0.00081 mm, T = 17µm and Tand = 0.0021. Using a start line calculator in Advanced Design System (ADS), Agile Technologies version 2011 version software the dimensions of width, spacing and length of each stage are calculated by using even and odd characteristic impedance. The characteristic impedance $Z_0$ typically assumed as 50 ohms. Each stage length chose to be guided wavelength ($\lambda_g$) whereas it corresponds to an electrical length (Eeff) as 90. The calculated dimensions of width, gap and length of each stage are show in the table below.

| N | $Z_{oo}$ (Ω) | $Z_{oe}$(Ω) | $Z_0$(Ω) | Width (mm) | Length (mm) | Gap (mm) |
|---|---|---|---|---|---|---|
| 1 | 39.235544 | 70.604689 | 52.632817 | 1.414600 | 31.888300 | 0.215276 |
| 2 | 39.509156 | 69.463428 | 52.387417 | 1.441860 | 31.838800 | 0.233158 |
| 3 | 39.509156 | 69.463428 | 52.387417 | 1.441860 | 31.838800 | 0.233158 |
| 4 | 39.235544 | 70.604689 | 52.632817 | 1.414600 | 31.888300 | 0.215276 |

Mlin Start line calc:

- 50 ohms:

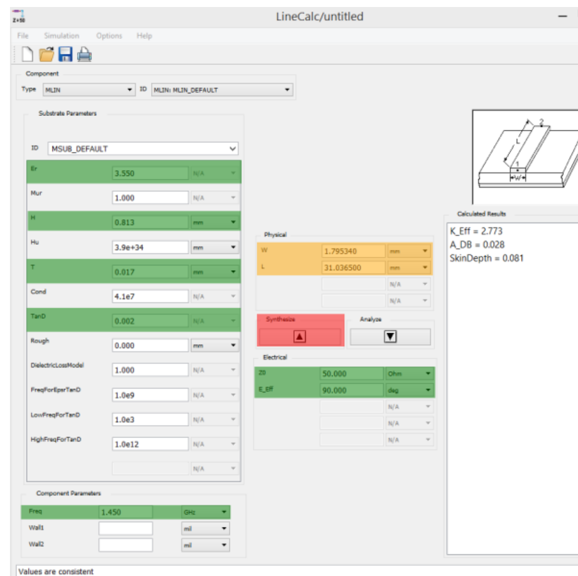



*Figure 22. Mlin 50 ohms in mm.*

Mclin Start line calc:

- N = 1:

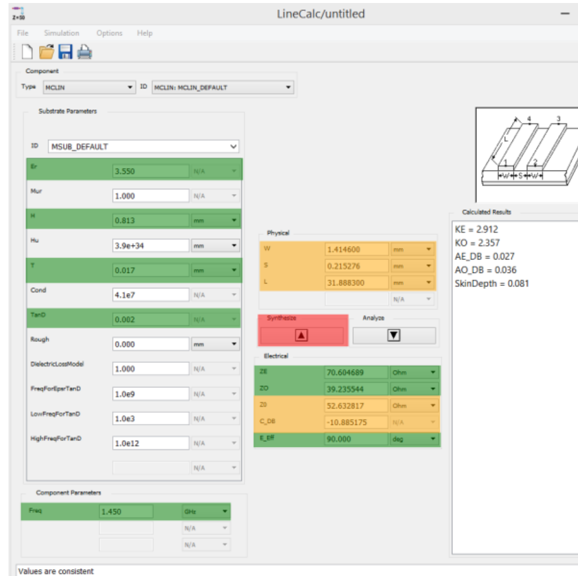



*Figure 23. Mclin N = 1 in mm.*

- N = 2:

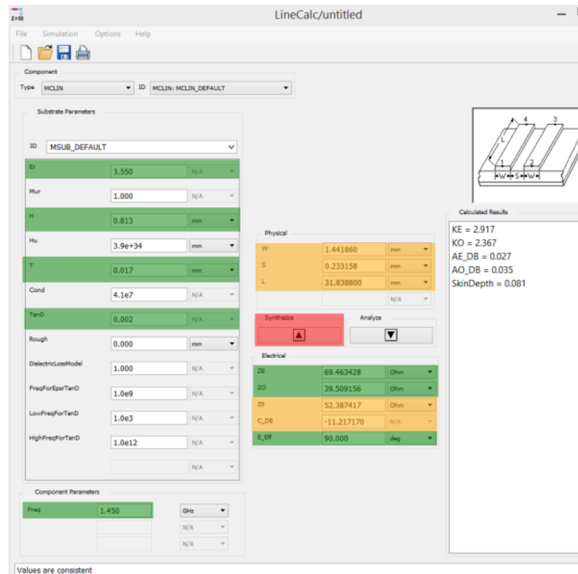



*Figure 24. Mclin N = 2 in mm.*

- N = 3:

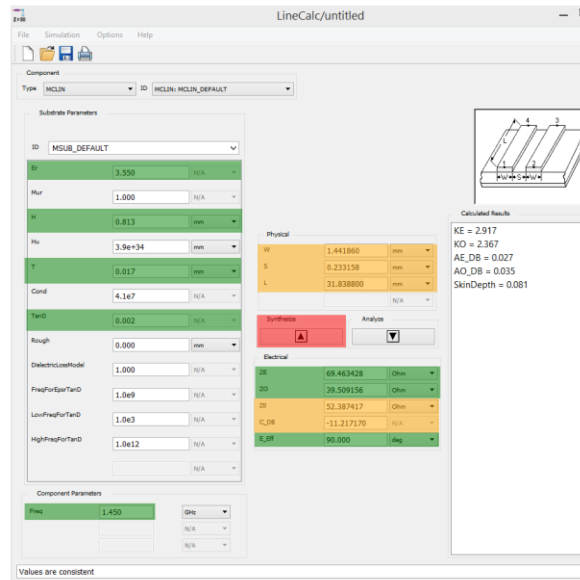



*Figure 25. Mclin N = 3 in mm.*

- N = 4:

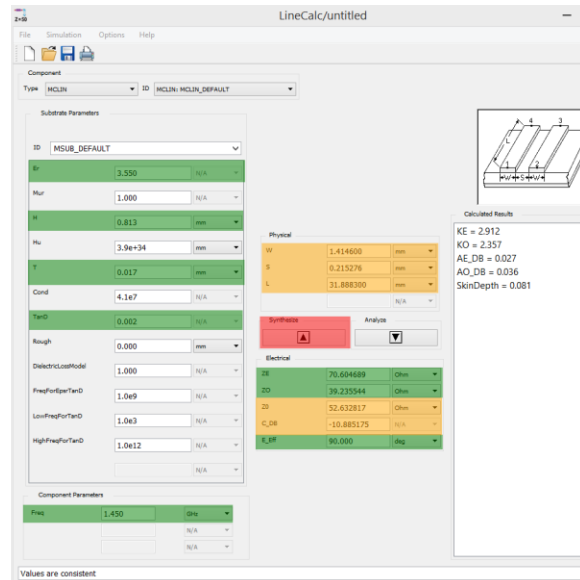



*Figure 26. Mclin N = 4 in mm.*

3) Schematic design with microstrip lines:

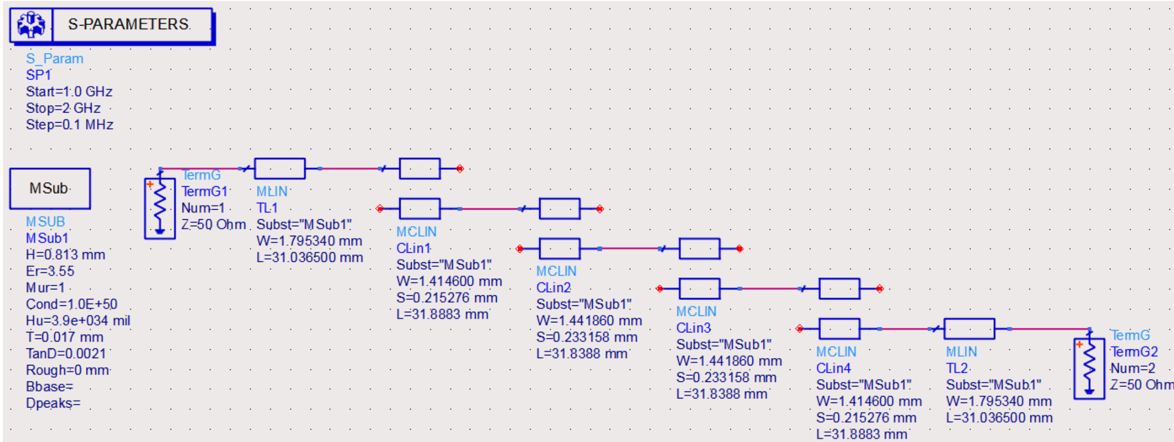



*Figure 27. Schematic design with tuning.*

4) Simulations:

dB (S21): F1 = 1.378GHz and F2 = 1.522GHz. We need to do the tuning in order to have the required bandwidth.

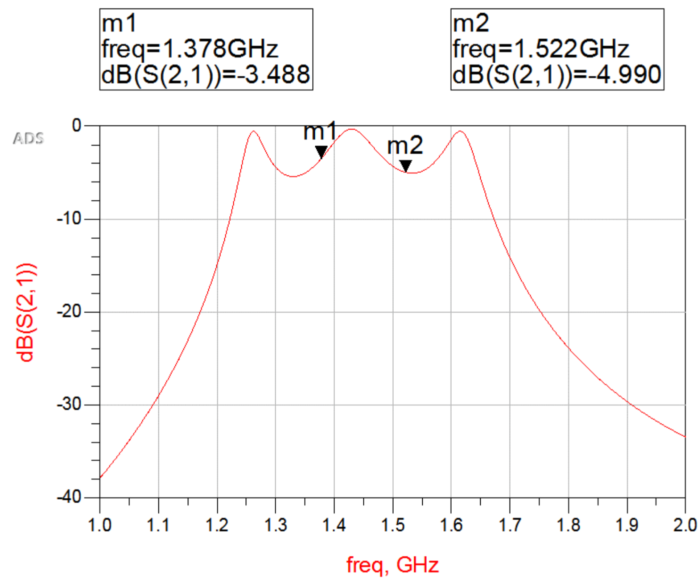



*Figure 28. F1 = 1.378GHz and F2 = 1.522GHz.*

dB (S21): F1 = 1.246GHz and F2 = 1.637GHz. We need to do the tuning in order to have the required bandwidth.

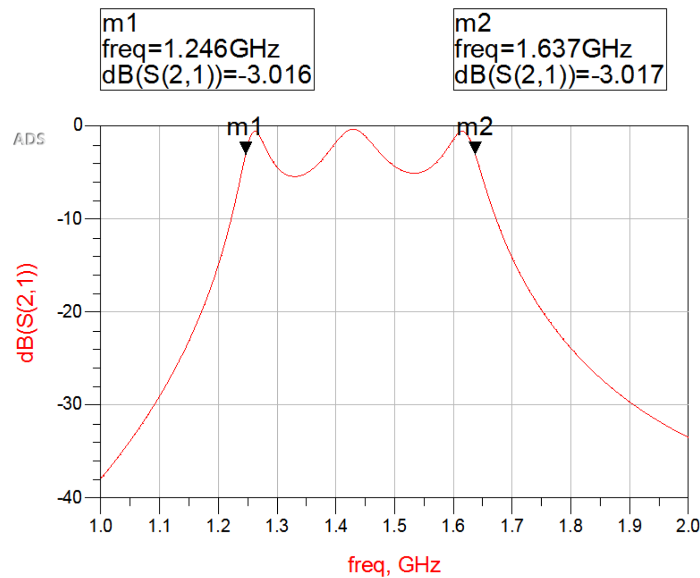



*Figure 29. F1 = 1.246GHz and F2 = 1.637GHz.*

## Circuit for design for first topology with tuning:

1) To implement the tuning, we need to follow the next steps:

*Add variables 0110 VAR / Double click over the "Var Eqn" icon/ Appear "Edit instance Parameters.

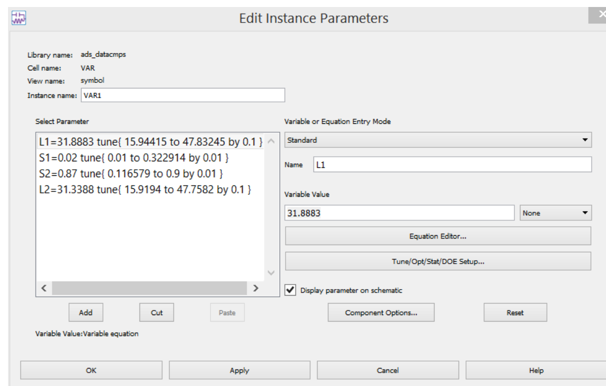



*Figure 30. Variables editor.*

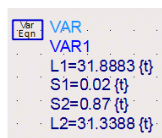



*Figure 31. Variables in ADS.*

*Open tuning tool / Appear “Tune Parameters” window

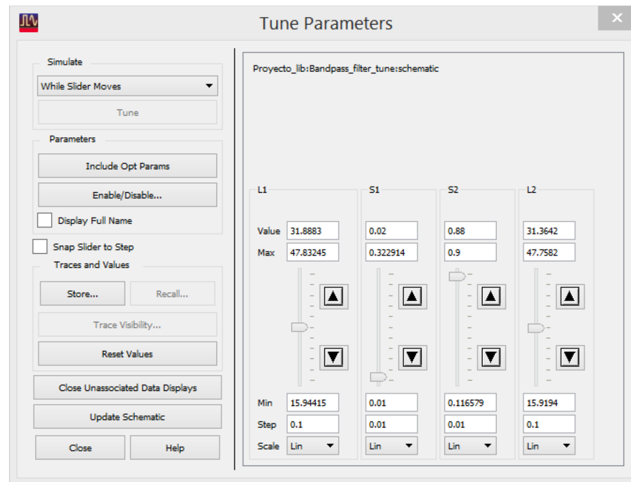



*Figure 32. Tune Parameters window.*

2) Schematic design with microstrip lines:

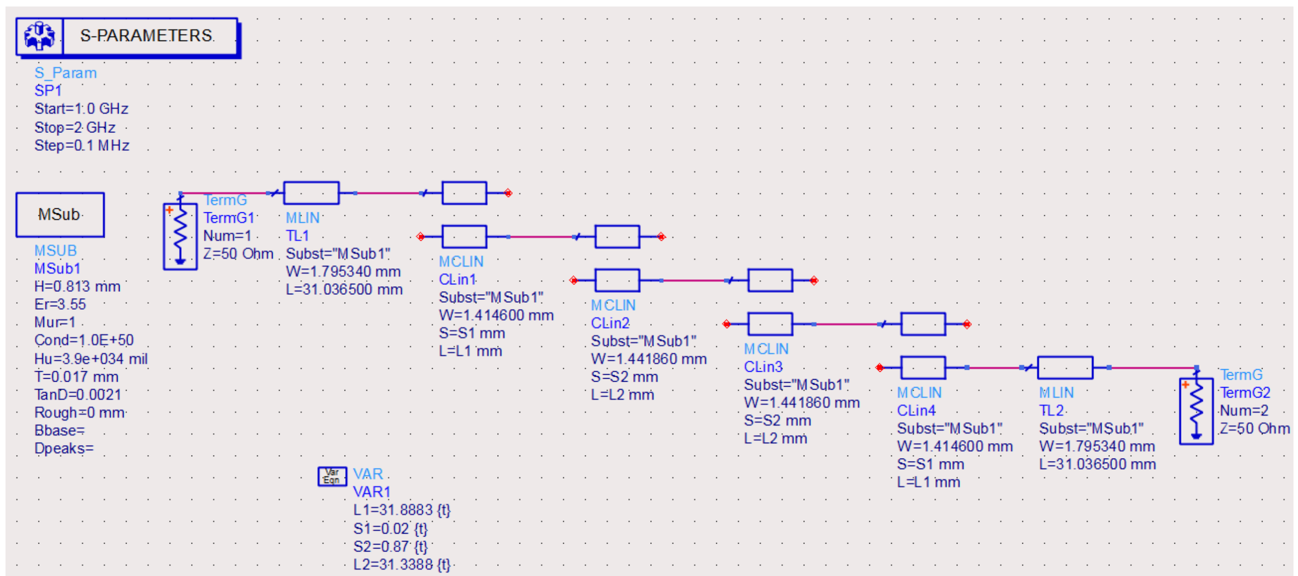



*Figure 33. Schematic design with tuning.*

3) Simulations:

dB (S21): F1 = 1.378GHz and F2 = 1.522GHz.

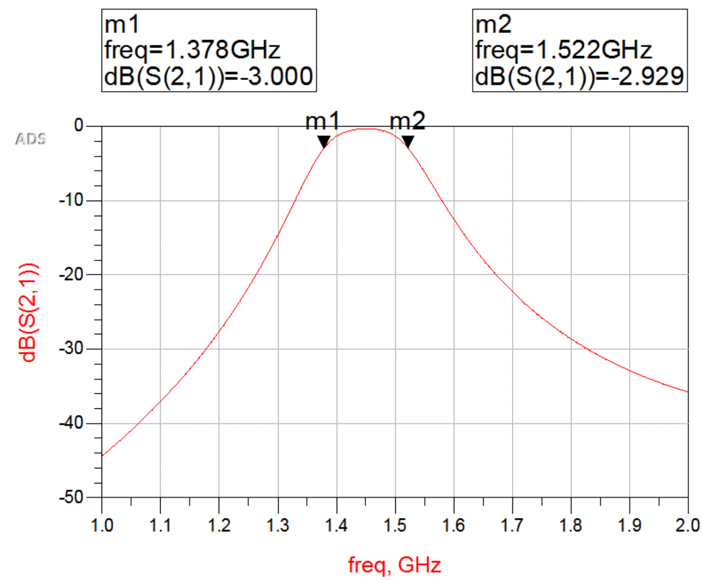



*Figure 34. F1 = 1.378GHz and F2 = 1.522GHz.*

dB (S21): F1 = 1.378GHz and F2 = 1.523GHz.

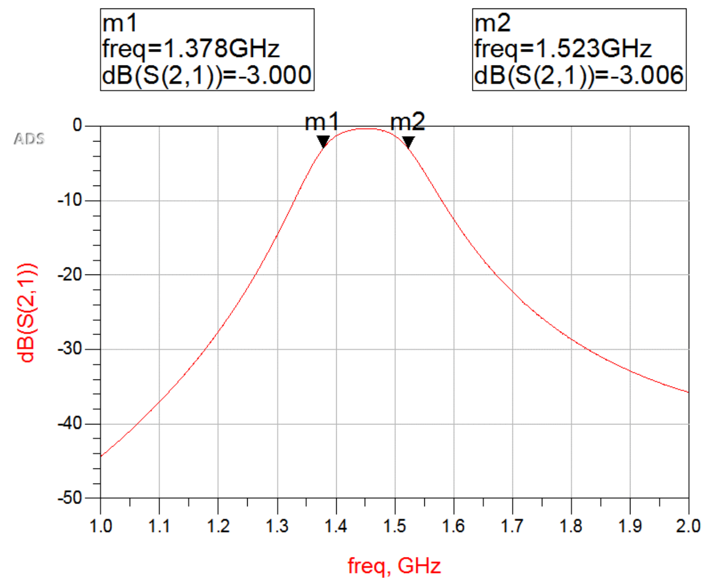



*Figure 35. Figure 24. F1 = 1.378GHz and F2 = 1.523GHz.*

**Layout design for first topology with tuning:**

1) Create the layout with the tuning values for $L_1$, $S_1$, $L_2$ and $S_2$ with no variables.

2) Select “New Layout Window”.

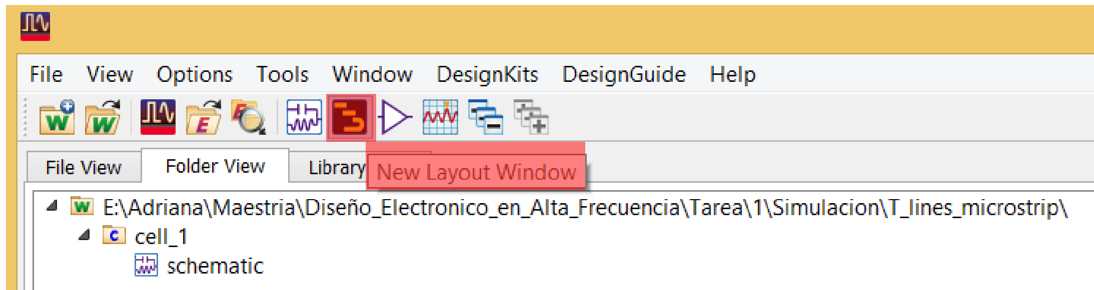



*Figure 36. New Layout window.*

3) Then appear “New Layout”/Cell: Write the cell name/ Ok.

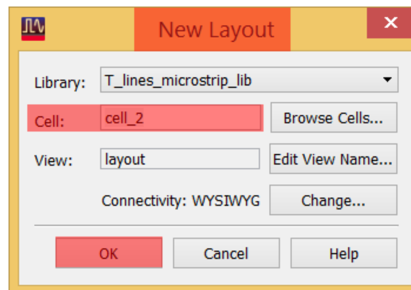



*Figure 37. Cell name.*

4) Appear the “Bandpass_filter_tuning_layout…….” Window

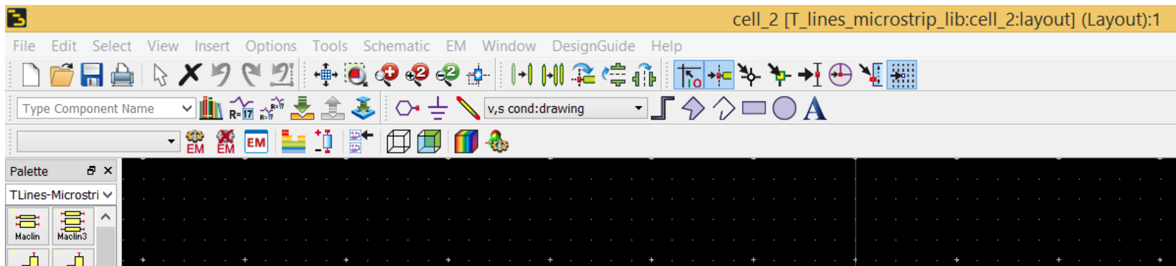
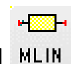



*Figure 38. Layout window.*

5) Select the “T-lines-Microstrip” to create the Bandpass filter. For this design we use MLIN 

and MCLIF

.

6) To edit the parameters in the TLines-Microstrip double click over the TLines.

*MLIN.

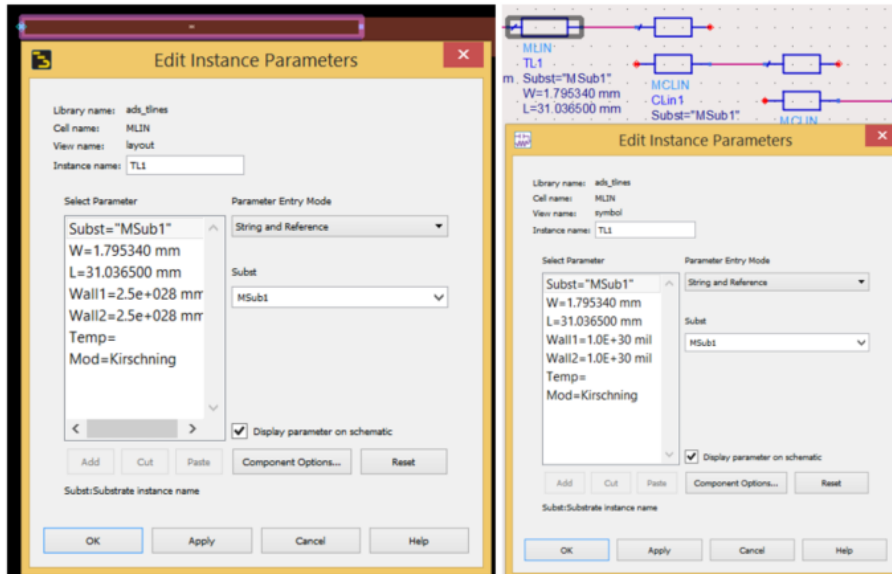



Figure 39. Layout vs schematic for MLIN 50 ohms.

*MCFIL for N = 1 and N = 4:

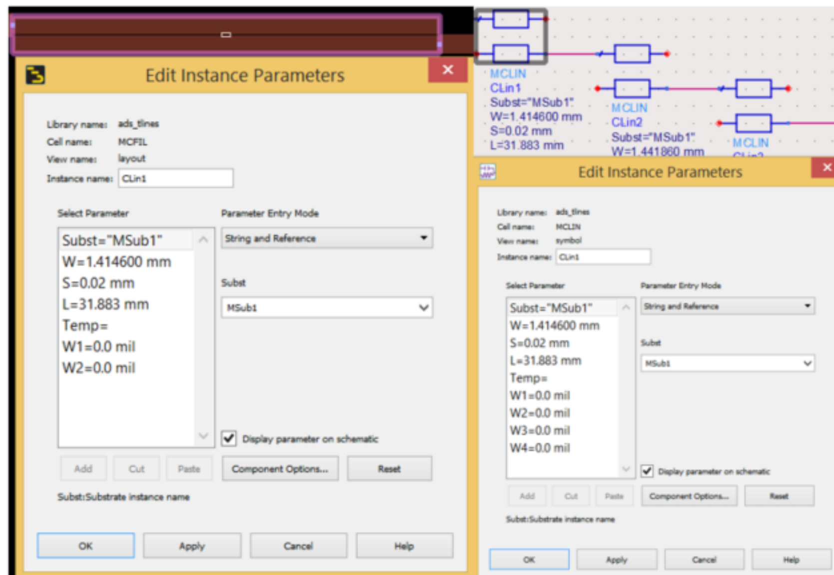



Figure 40.Layout vs schematic for MCFIL N = 1 and N = 4 in mm.

*MCFIL for N = 2 and N = 3:

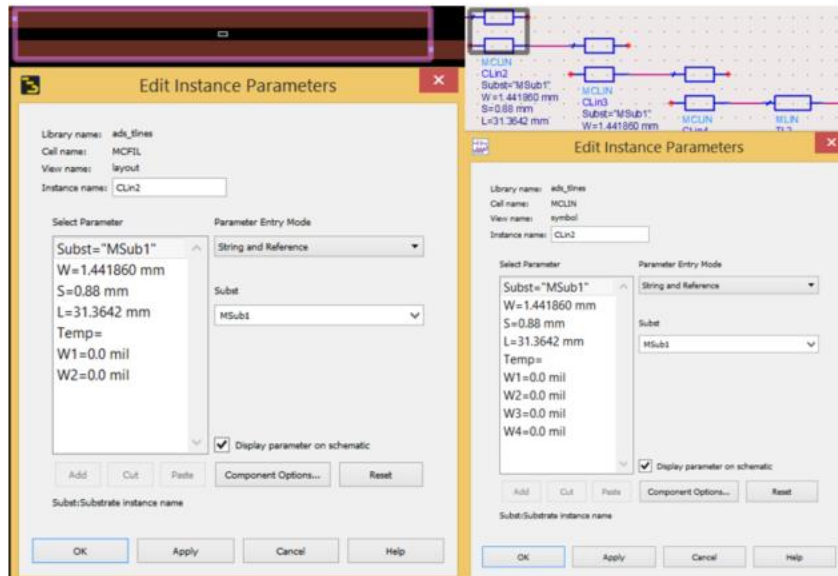



*Figure 41. Layout vs schematic for MCFIL N = 2 and N = 3 in mm.*

7) Insert the Ports/ Insert Pin.

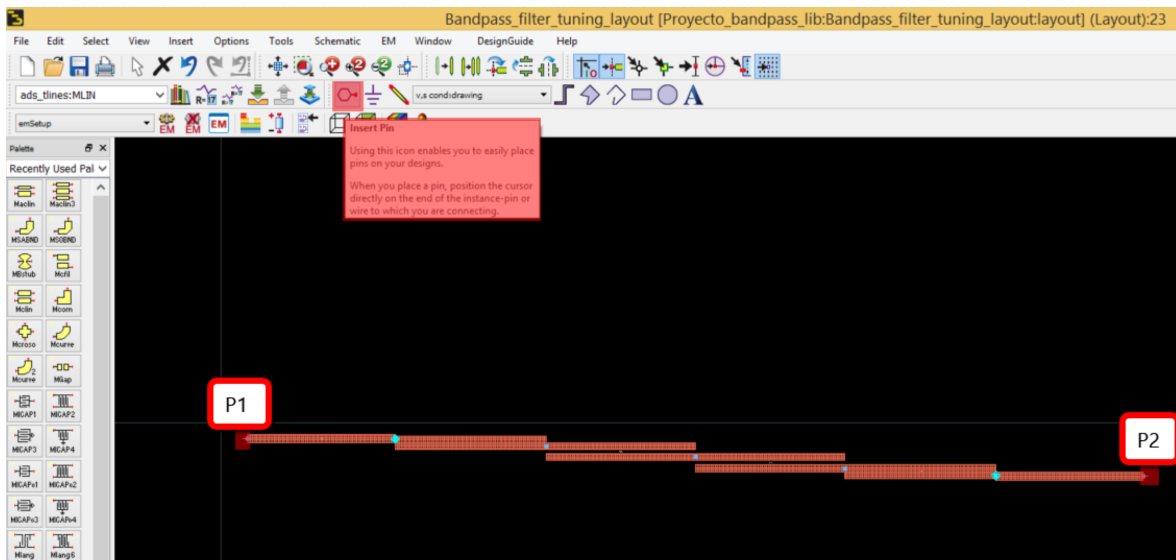



*Figure 42. Ports for the layout.*

8) Add substrate/ Click over “Substrate editor”.

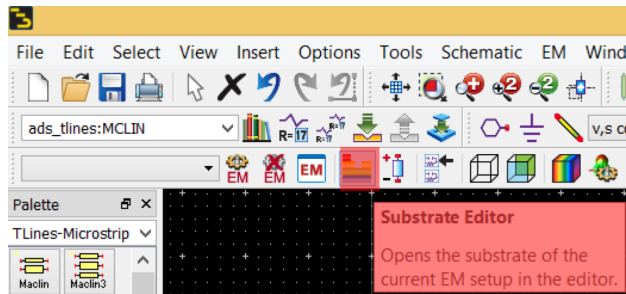



*Figure 43. Substrate Editor icon.*

9) Add substrate name:

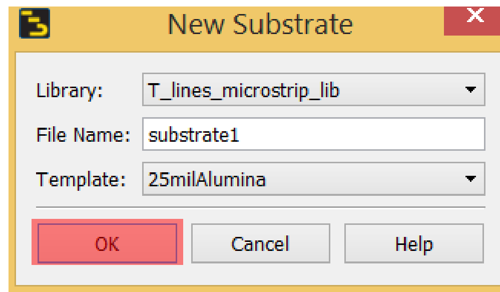



*Figure 44. Substrate name.*

10) Appear the “substrate [T_lines_microstrip_lib] (Sustrate):24”.

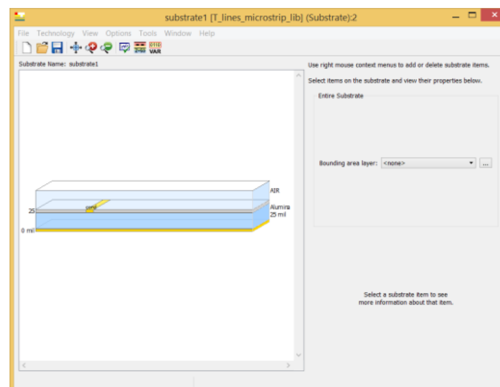


*Figure 45. Substrate window setup.*

11) Select dielectric material:

*Add the thickness:

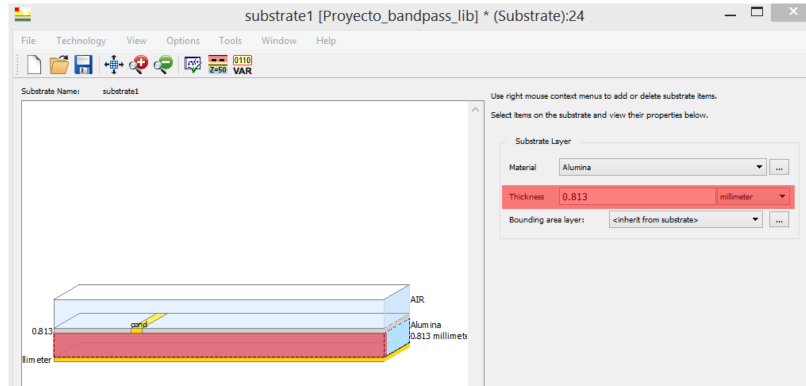



Figure 46. Thickness of the board.

*Add material: Click over …

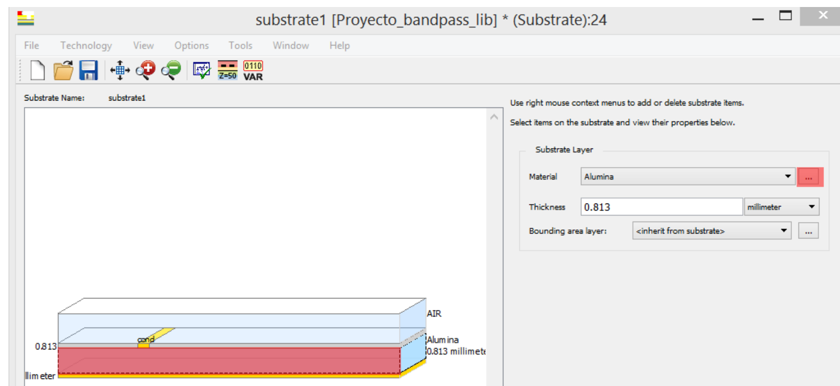



Figure 47. Material selection.

*Appear “Material definitions” window/ Add from Database.

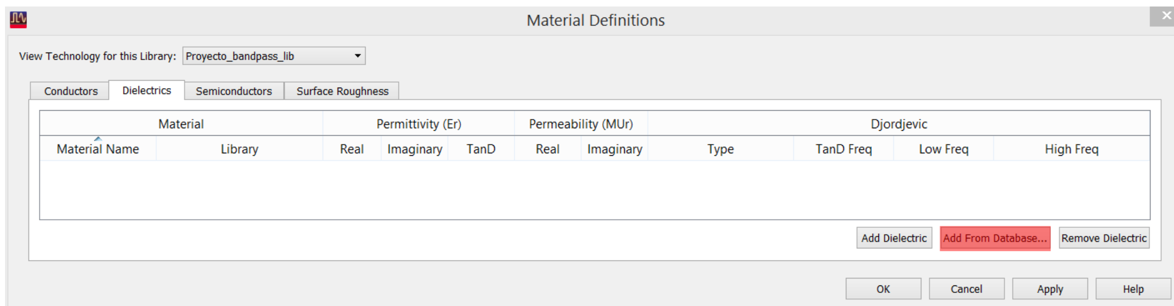



Figure 48. Select the material.

*Appear Add Materials from Database/ Choose the RO4003 material.

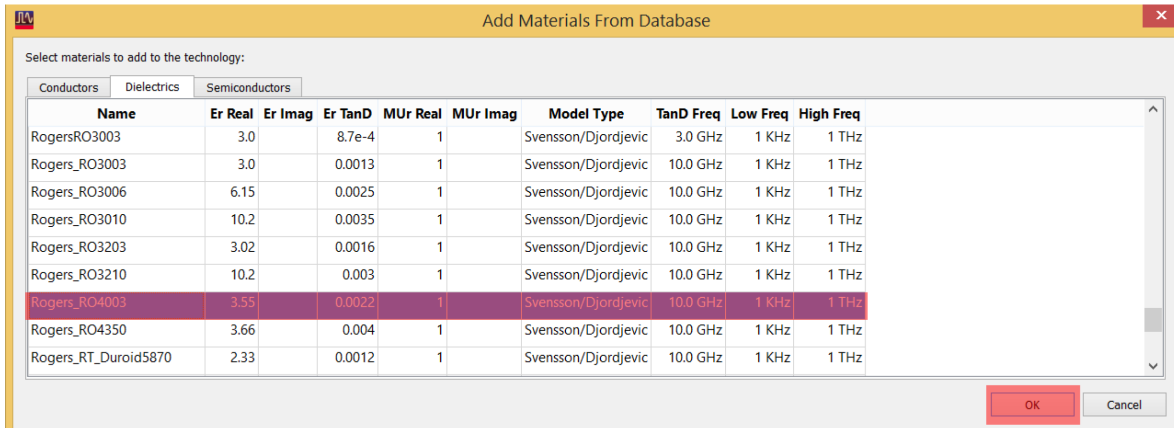



*Figure 49. Material RO4003.*

*Click Apply/ Ok.

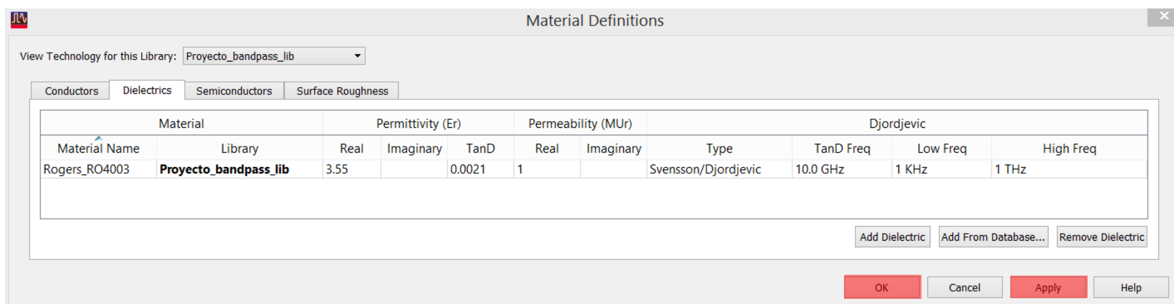



*Figure 50. Material definition.*

*Substrate definition:

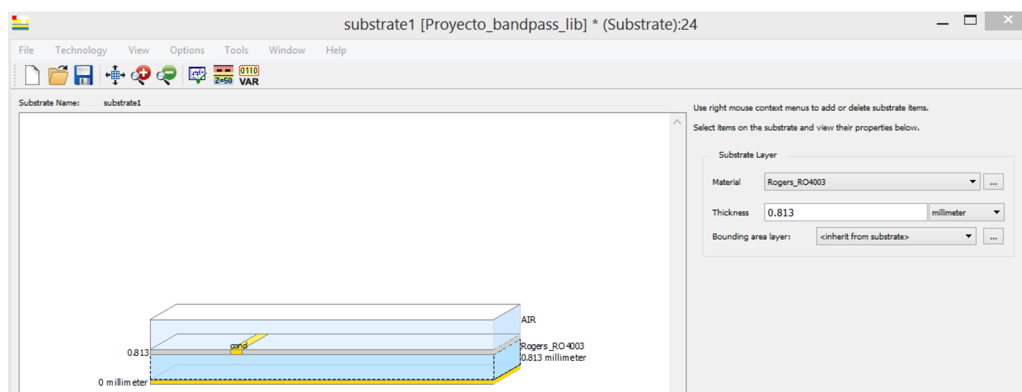



*Figure 51. Substrate RO4003.*

12) Setup for cupper:

*Select the cupper in the window:

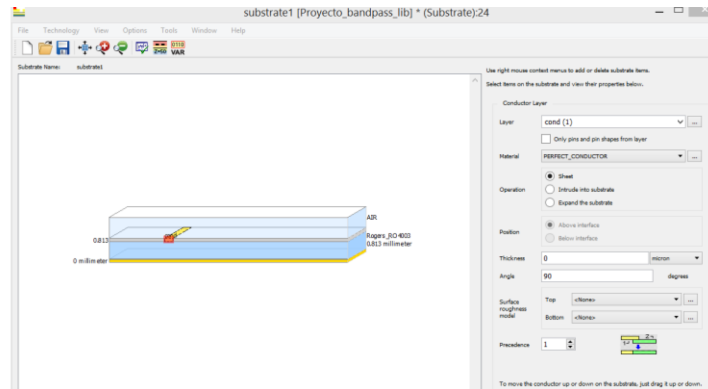


*Figure 52. Cupper.*

*Click over …

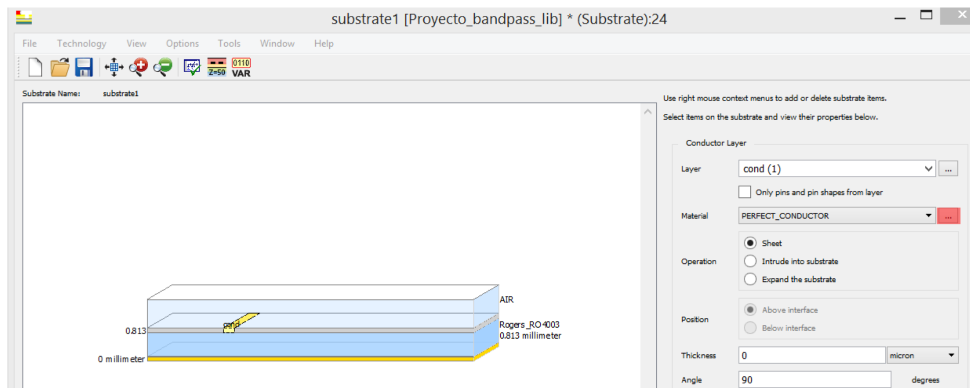



*Figure 53. Perfect conductor.*

*Appear “Materials Definitions”/ Click on “Add from Database”.

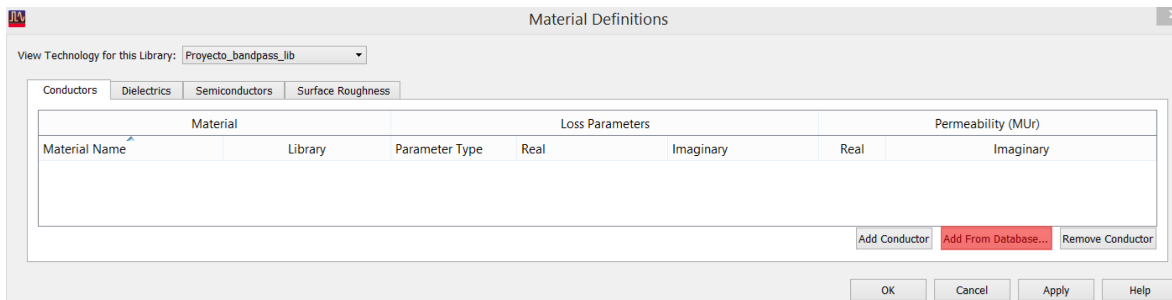



*Figure 54. Materials Definitions window.*

*Appear “Add materials from database”/ Select “Copper”/ Ok.

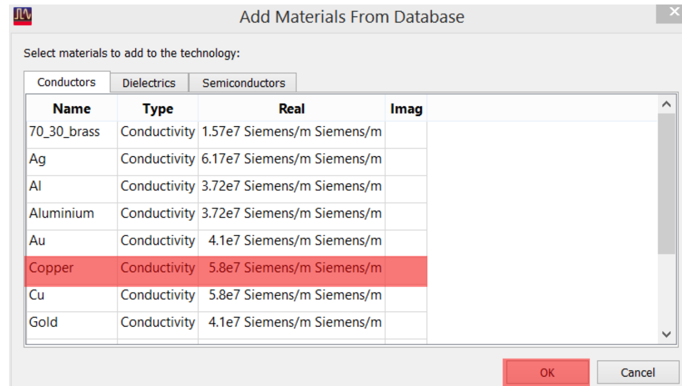



*Figure 55. Copper.*

*In “Material Definitions” window/ Apply/ Ok.

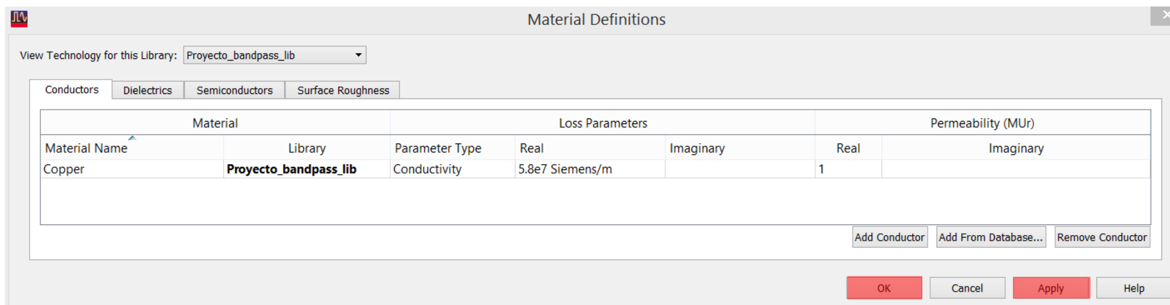



*Figure 56. Material setup.*

*Select the options in color red and add the copper thickness indicated in the stack-up.

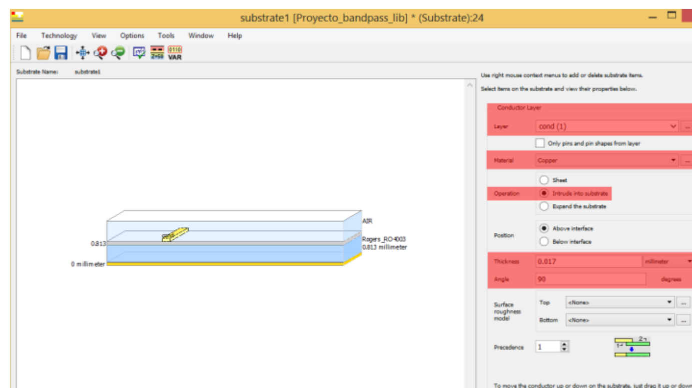



*Figure 57. Copper parameters.*

*Save changes.

13) Simulation setup:

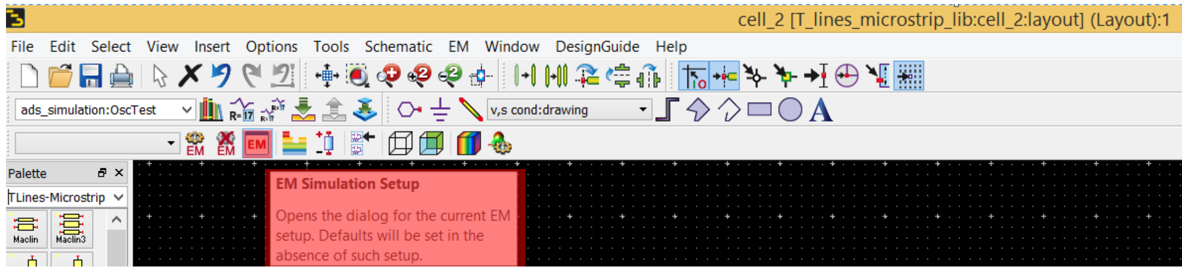



*Figure 58. EM simulation setup.*

*Appear “Proyecto_bandpass_lib:Bandpass_filter_tuning_layout:emSetup*(EM Setup for simulation)”.

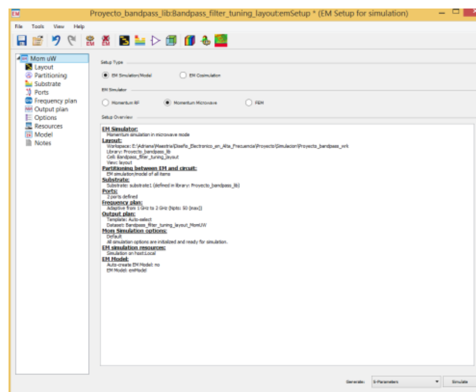


*Figure 59. EM window.*

*Frequency plan:

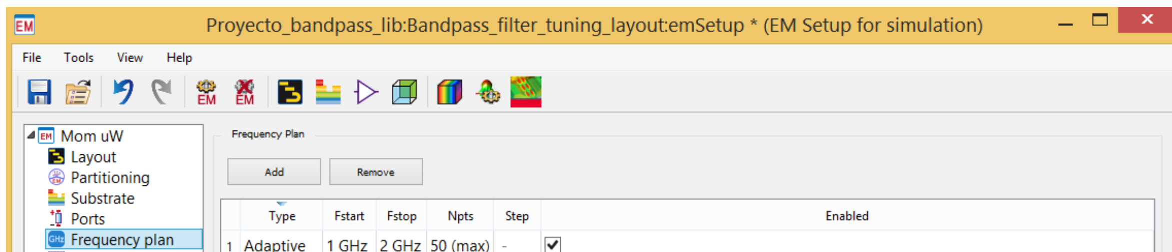



*Figure 60. Frequency plan.*

*Options/ Mesh.

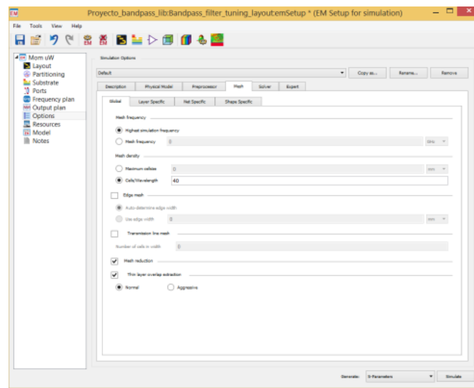



*Figure 61. Options.*

*S-parameters/ Simulate.

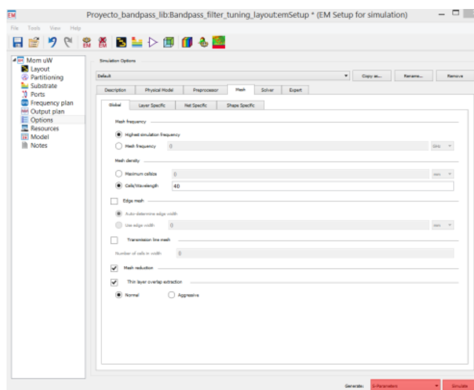



*Figure 62. Simulation.*

13) Simulations and Layout:

*Mesh 20:

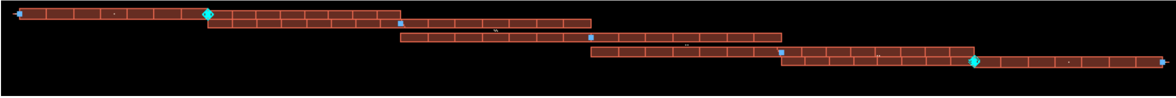


*Figure 63. Layout with mesh of 20.*

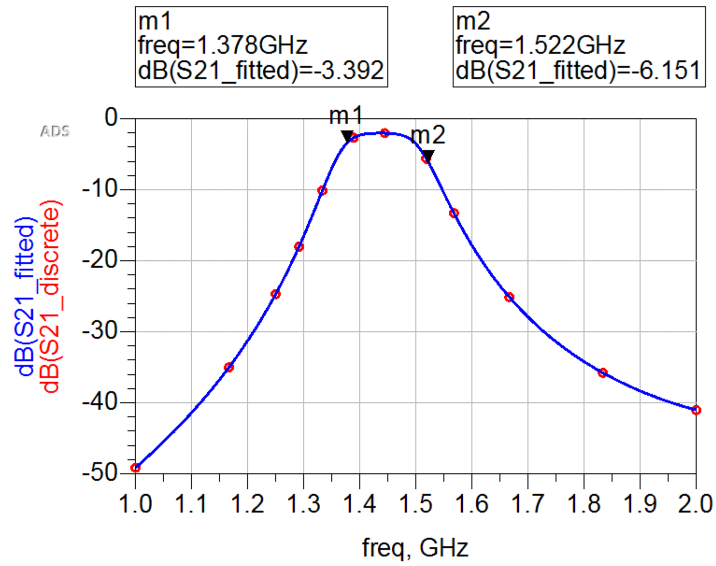



*Figure 64. F1 = 1.378GHz and F2 = 1.522GHz.*

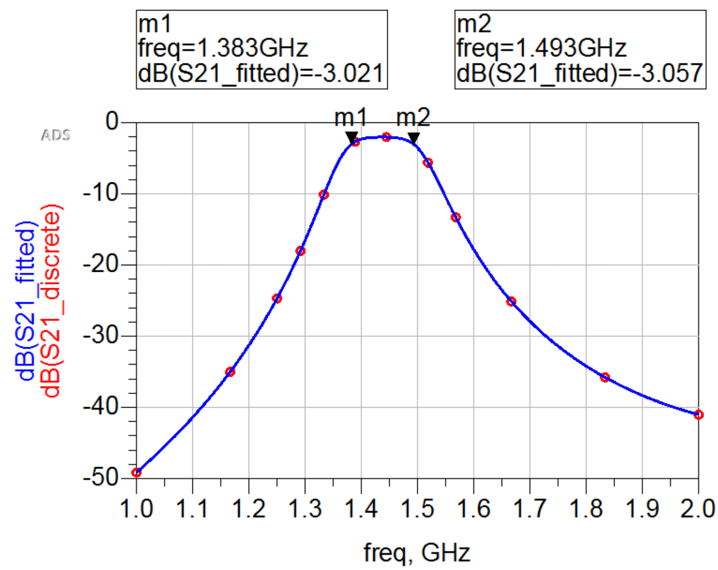



*Figure 65. F1 = 1.383GHz and F2 = 1.493GHz.*

*Mesh 40:

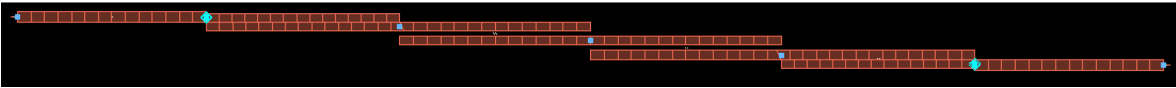


Figure 66. Layout with mesh of 40.

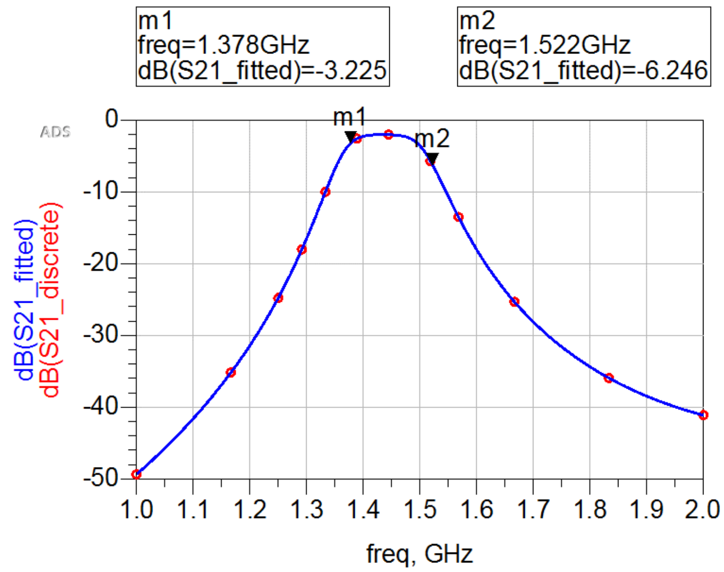



Figure 67. F1 = 1.378GHz and F2 = 1.522GHz.

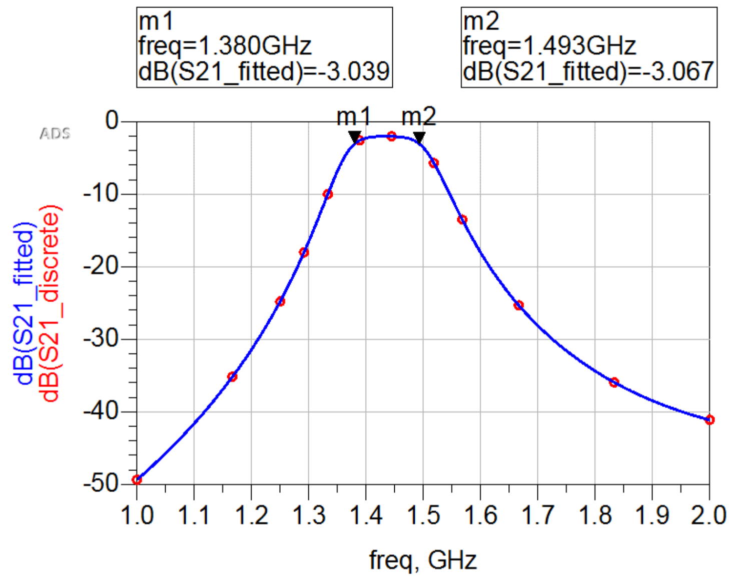



Figure 68. F1 = 1.380GHz and F2 = 1.493GHz.

*Mesh 80:

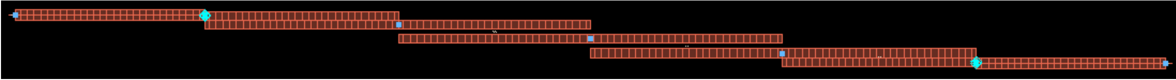


*Figure 69. Layout with mesh of 80.*

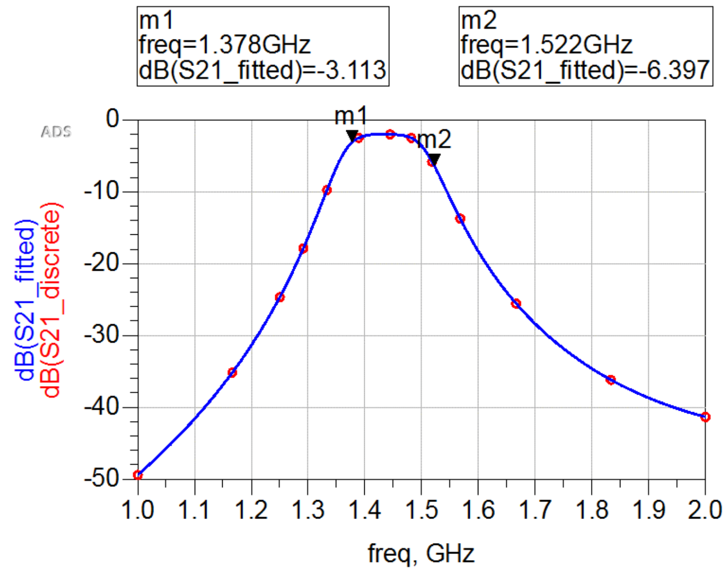



*Figure 70. F1 = 1.378GHz and F2 = 1.522GHz.*

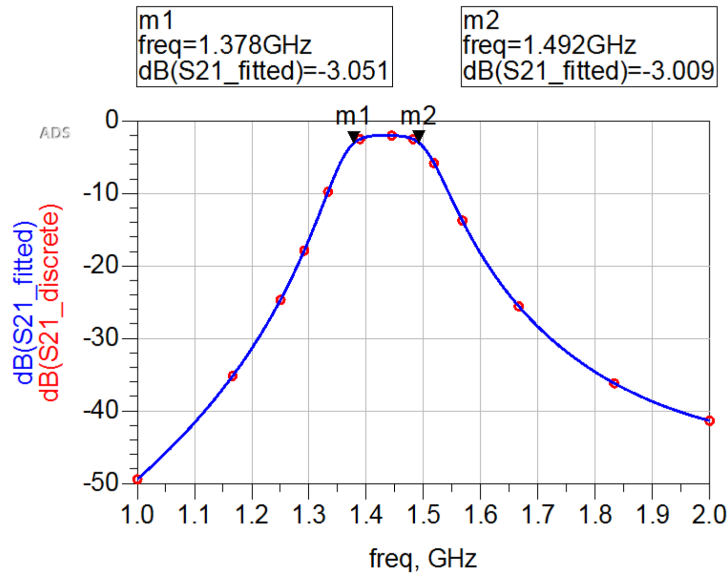



*Figure 71. F1 = 1.378GHz and F2 = 1.492GHz.*

*Mesh 100:

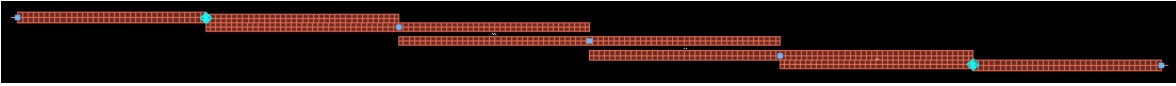


*Figure 72. Layout with mesh of 100.*

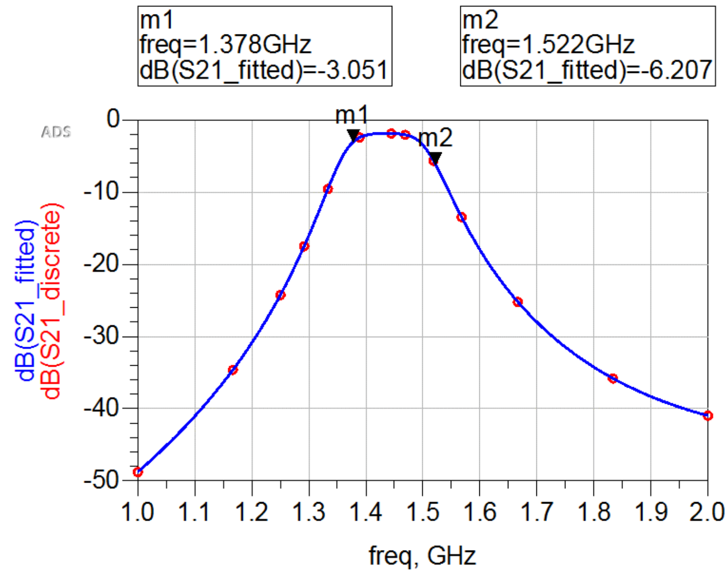



*Figure 73. F1 = 1.378GHz and F2 = 1.522GHz.*

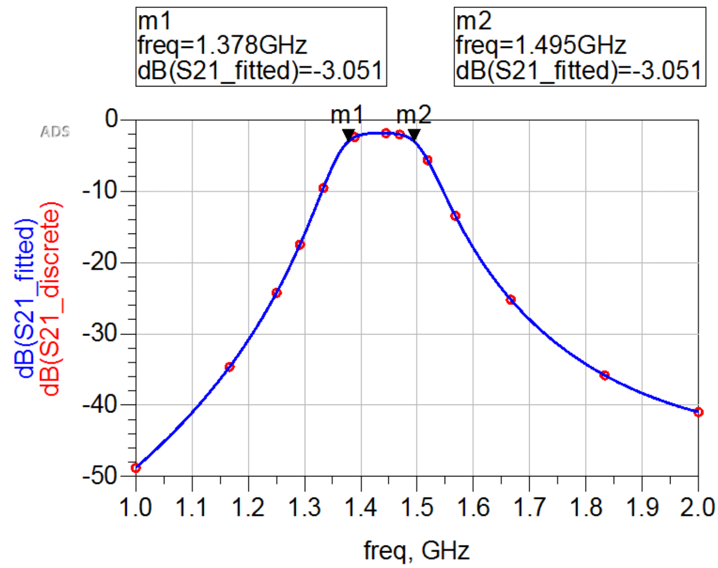



*Figure 74. F1 = 1.378GHz and F2 = 1.495GHz.*

*Mesh 200:

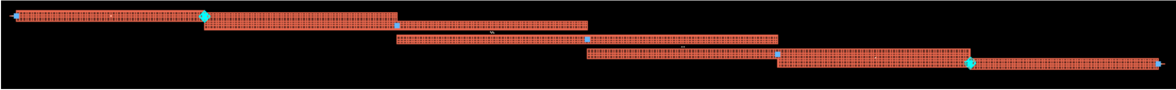


*Figure 75. Layout with mesh of 200.*

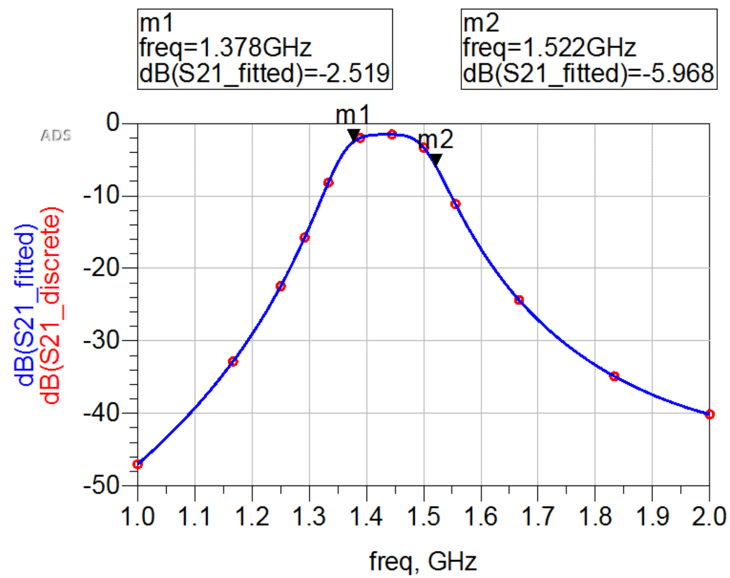



*Figure 76. F1 = 1.378GHz and F2 = 1.522GHz.*

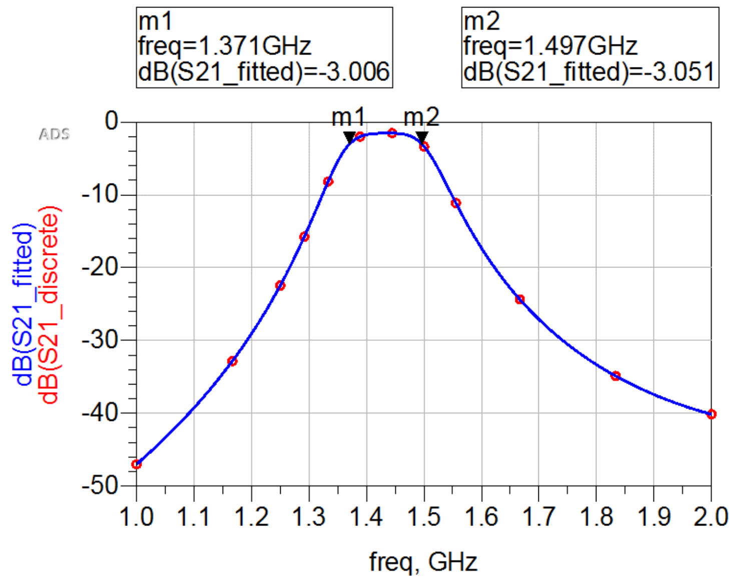



*Figure 77. F1 = 1.371GHz and F2 = 1.497GHz.*

**Conclusions**

In conclusions, and FR4 microstrip parallel coupled line bandpass filter is well designed and simulating by using the ADS software tool form Agilent Technologies. The filter is simulating circuital, schematic and in layout. The simulations is showing the S1 parameter, but as we can see in the schematic design we need to perform a tuning in order to achieve the bandwidth for the bandpass filter and for the layout we need to do a tuning in order to have the expected bandwidth.

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Shreyasi Srivastava. Dept. of Telecommunication, R.V.C.E, Bangalore, India.

R.K. Manjunath. Depy. of Instrumentation Sri. Krishna Devaraya University, Anantpur, India.

Shanti P. Dept. of telecommunication. R.V.C.E, Bangalore, India.

*Design of 4$^{th}$ order parallel coupled microstrip bandpass filter at dual frequencies of 1.8GHz and 2.4GHz for wireless application.

S. Srinath.

UG Student, Dept. of ECE, Vellore Institute of Technology, Vellore, Tamilandu, India.

## C. ANTIPAD CALCULATION FOR A HIGH-SPEED PCB USING MATLAB.

INSTITUTO TECNOLÓGICO Y DE ESTUDIOS SUPERIORES DE OCCIDENTE

ITESO
Universidad Jesuita de Guadalajara

# MAESTRÍA EN DISEÑO ELECTRÓNICO

MÉTODO DE SIMULACIÓN DE CIRCUITOS ELECTRÓNICOS
PROFESOR: DR. ERNESTO RAYAS

**FINAL PROJECT: Anti pad calculation for a High-Speed PCB using Matlab**

Adriana Galindo md690881
Jaime De La Torre Aguirre md692104
March 2016

December 2015
October 2015

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# 1 Introduction

In the design of PCBs that contains high speed signals, is very common to perform signal integrity simulations in certain areas of the design (the most critical ones), using tools like HFSS (High Frequency Structural Simulation) from ANSYS. In the case of this project, there was a need to design a board to perform electrical validation of one of the chips designed by Intel. The board include in its design a Samtec connector bulls eye type, like the one depicted in the figure 1.1

Figure 78.1 Samtec connector (bulls eye type).

The Samtec connector goes to the CPU via single ended lines with a controlled impedance of 50 ohms, and this was the part of the design that was simulated, which corresponds to the path: Samtec connector – connector pad - via – via pad - trace, which is described in the figure 1.2.

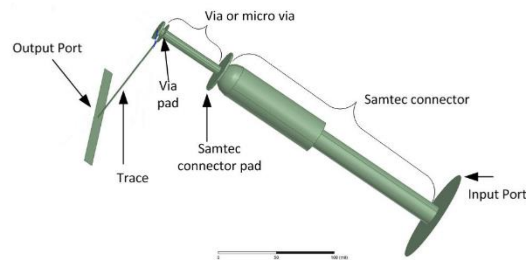



Figure 79.2 Path simulated: Samtec – Via - Trace

It is very important for the design, to maintain as much as possible the 50 ohms impedance in the path. One key element that is affecting the impedance is the parasitic capacitance of via, hence the importance to perform the simulations, to find the right value of the anti-pad diameter in the ground planes, to maintain that parasitic capacitance very low. The anti-pad is described in the figure 1.3.

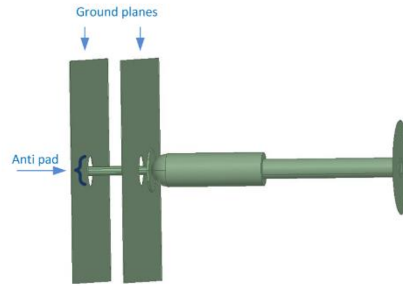


Figure 80.3 Anti pads in the ground planes

This simulation was already performed without using any optimization script, the simulation was done by changing manually the antipads of the via in the HFSS tool. The objective to using the same HFSS model is to make an optimization of the anti-pad via using a driver for HFSS using Matlab, an objective function and a method to optimize the anti-pad size. The idea is to compare manually simulations using only HFSS with the simulations using an optimization method.

The present report contains the following elements:

- Theory to describe why is important to reduce the parasitic capacitance of the via
- Fixed parameters: Board stack up, SAMTEC connector model, frequency, via size etc.
- Optimization: HFSS driver, optimization variables and starting point.
- Results of the models created in HFSS using Matlab: Through hole via
- And finally, the conclusions.

# 2 Theory

## 2.1 Parasitic elements in a PCB

In the design of PCB boards that include higher speed frequencies, it is very important to take into account the parasitic elements that are intrinsic in the physical design. In this project, the parasitic capacitance of via is affecting the impedance of the complete signal path.

For the impedance equation, various forms exist depending on whether we are examining plane wave impedance, circuit impedance, and the like. For wire, or a PCB trace, the following equation is used:

$$Z = R + jX_L + \frac{1}{jX_C} = R + jwL + \frac{1}{jwC} \qquad (2.1)$$

where $X_L = 2\pi fL$ (the component in the equation that relates only to wires or PCB traces) [1]

$$X_C = \frac{1}{2\pi f C} \qquad (2.2)$$

$$w = 2\pi f_C \qquad (2.3)$$

As we can see in the equation 2.1, the capacitance is a key factor in the calculation of the impedance, that in the case of this project, the capacitance of the via was key for the calculation of the impedance for the complete path, which is formed by the SAMTEC connector, the via and the PCB trace, as described in the figure 2.1.

Every via has parasitic capacitance to ground. Vias being physically small structures, they behave very much like lumped circuit elements. We can predict, within an order of magnitude, the amount of parasitic capacitance for a via: [2]

$$C = \frac{1.41\varepsilon r\, T D_1}{D_2 - D_1} \qquad (2.4)$$

Where D2 = diameter of clearance hole in ground plane(s), in.
D1 = diameter of pad surrounding via, in.
T = thickness of printed circuit board, in.
εr = relative electric permeability of circuit board material
C = parasitic via capacitance, pF

When the pad size approaches the clearance hole diameter, pads pick up a lot more capacitance. If your ground clearance holes must remain small to maintain ground continuity, shrink or eliminate the pads on ground layers. For trace routing vias, it doesn't matter if you get some breakout on the plane layers. [2]

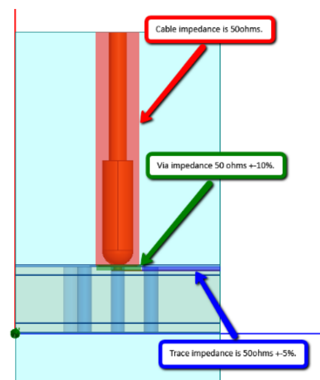



Figure 81.1 Impedance of the cable, via and trace.

The primary effect of via capacitance is that it slows down, or degrades, the rising edge of digital signals.

If we must make many pad capacitance predictions, it is recommended to use electromagnetic field modeling software, since these packages can (with enough computer resources) accurately model the inductance and capacitance of three-dimensional structures. [2]

In the development of this project, the PCB simulation that was used was HFSS.

As we can see in the equation 2.1, also the inductance is a key element that influence the calculation of the impedance, however, in this project was considered to be in control, because of the use of 7 ground vias that surrounds the via signal, following the recommendation of the Samtec connector designer. In this way, the influence of the inductance is kept in control. Those ground vias can be observed in the figure 2.2.

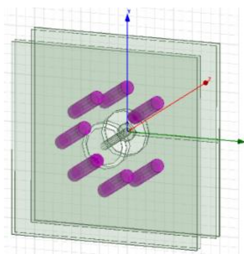


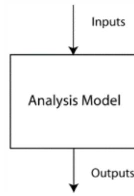
Figure 82.2 Ground vias surrounding the via signal

## 2.1 Optimization methods

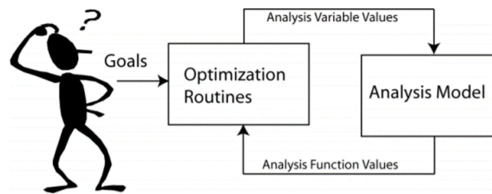
Automated design optimization technology is rapidly being adopted by engineers in nearly all major industries. The potential for delivering better designs in less time compared to manual optimization approaches makes automated design optimization very attractive from both a technical and a business point of view. However, one of the main barriers to widespread usage of design optimization in industry is the difficulty of choosing an appropriate optimization search algorithm for a given problem.

It is well known that all search methods have at least some limitations. For example, some methods work effectively only when it is possible to accurately compute gradients of the solution with respect to the variables. Some methods work only for continuous or discrete variables (but not both), or for a relatively small number of variables. And some methods require a relatively large number of design evaluations to be performed in order to find an optimal solution. There is no single method or algorithm that works best on all or even a broad class of problems. In order to choose the best method for a given problem, one must first understand the type of design space that is being searched. The design space for a given problem is defined by the types of responses and by the number, types and ranges of the design variables.

A model requires some inputs in order to make calculations. Analysis models require inputs—analysis variables— and compute outputs—analysis functions.




The designer specifies a set of inputs, evaluates the model, and examines the outputs. Suppose in some respect, the outputs are not satisfactory. Using intuition and experience, the designer proposes a new set of inputs which he or she feels will result in a better set of outputs. The model is evaluated again. This process may be repeated many times. The computer is now used to both evaluate the model and search for a better design.




# 3 Project Development

## 3.1 Design Specifications for optimization model

### 3.1.1 Fixed parameters

The design has some parameters that are not be part of optimization variables. Those parameters are
stack-up, frequency design (the high-speed simulating in this project works at 20GHz, shielding vias (ground) around the singled ended trace, via size, trace width, impedance trace of 50 ohms and the SAMTEC connector model provided by SAMTEC company

The PCB board with the following stack up has to be used, it was part of the requirement, to be able to design a board to transmit the high-speed signals. This stack up was provided by the PCB manufacturer vendor. The PCB material is low loss (Megtron6).

| | | | Customer Stack-up | OPCM Stack-up Information | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Layer | | Cu Weight | Thickness (mils) | Proposed Thickness (mils) | Structure | Via | Assume copper density | Ref | Diffential 100ohm +/- 10% Target LW/SP | Diffential 100ohm +/- 10% Finished LW/SP | Diffential 100ohm +/- 10% Target LW/SP | Diffential 100ohm +/- 10% Finished LW/SP |
| | Soldermask | | 0.50 | 0.50 | | | | | | | | |
| L1 | Top | 1/3oz+Plating | 1.80 | 1.80 | | | 75% | | | | | |
| | Prepreg | | 3.60 | 3.60 | 1078RC72 | | | L1 & L3 | | 3.4/4.6 | | 3.8/8.2 |
| L2 | Signal | Hoz | 0.60 | 0.60 | | | 25% | | | | | |
| | Core | | 4 | 4 | 4mil core | | | | | | | |
| L3 | GND | Hoz | 0.60 | 0.60 | | | 75% | | | | | |
| | Prepreg | | 8.90 | 10.00 | 2116RC56 * 2 | | | | | | | |
| | Core | | 26 | 26 | 26mil dummy core | | | | | | | |
| | Prepreg | | 8.90 | 10.00 | 2116RC56 * 2 | | | | | | | |
| L4 | GND | Hoz | 0.60 | 0.60 | | | 75% | | | | | |
| | Core | | 4 | 4 | 4mil core | | | | | | | |
| L5 | Signal | Hoz | 0.60 | 0.60 | | | 25% | L4 & L6 | | 3.4/4.6 | | 3.8/8.2 |
| | Prepreg | | 3.60 | 3.60 | 1078RC72 | | | | | | | |
| L6 | Bottom | 1/3oz+Plating | 1.80 | 1.80 | | | 75% | | | | | |
| | Soldermask | | 0.50 | 0.50 | | | | | | | | |
| | | | | | | | | | | | | |
| Finished Thickness (mils) | | | | 68.20 | | | | | | | | |

Figure 3.1 Stack up defined by the PCB Manufacturer

Using the stack up described in the figure 3.1 as a reference, the PCB model was created at the HFSS tool. Another requirement was to use the SAMTEC connector model provided by the SAMTEC Company. The connector model contains all the characteristics needed to properly simulate the connector. The PCB model created was connected to the SAMTEC connector model, forming the complete model used in the HFSS simulations. The PCB and the Samtec connector can be seen in the Figure 3.2.

The requirement of the impedance path is that it must be 50 ohms ± 15%.

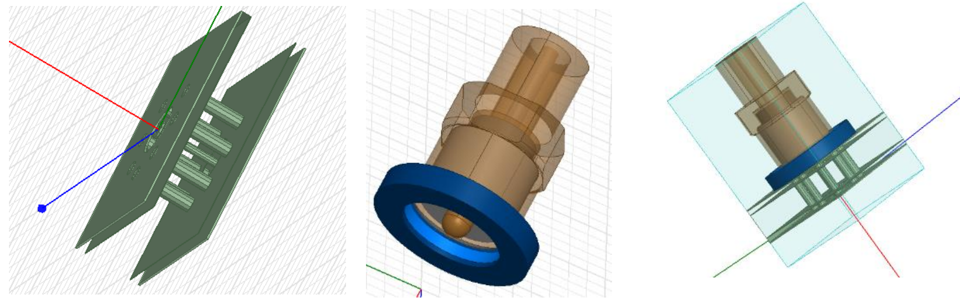


Figure 3.2 PCB, Samtec connector and PCB assembled with Samtec connector

### 3.1.2 Design Specifications: Starting point and optimization variables

This simulation was already performed in HFSS but without any optimization method, the anti-pad sizes were changed manually by the user. The optimization variables for this design are anti-pad 1 this is for the top side of the board and the anti-pad 2 this for the internal and bottom layers. Also, for the optimization algorithm the starting point was the obtained result in the manually HFSS simulation and the seed is:

| Seed | | |
|---|---|---|
| Size (mils) | Anti-pad 1 | Anti-pad 2 |
| | 46 | 52 |

### 3.1.3 Formulation of the optimization model

The optimization has three Matlab scripts:

- antipad_HFSS_driver.m: To develop this driver it was necessary to have the model drawn in the HFSS tool, then with help of HFSS script it was obtained a .vbs file. The .vbs file contain the information of how to open a project in HFSS, the PCB and Samtec connector model and the fixed parameters and the variables that will be optimized. This driver provide a .cvs file which contain the time and impedance.

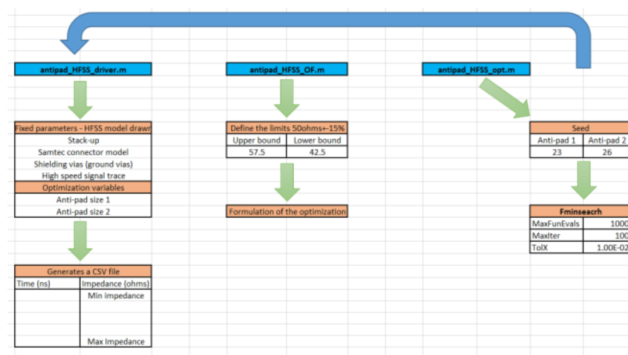
- antipad_HFSS_OF.m:
    - This script contains the restriction for the optimization.
    - Minimax formulation: The impedance of the high-speed signal supposed to be close to 50 ohms, but the model has a tolerance of 15%. The minimum and maximum impedance value is provided by the csv file.

$$x^* = \arg\min_{x \in X} U(x) = \arg\min_{x} \max\{\ldots e_k(x) \ldots\}$$

    - Where a negative valor in the k-th error function $e_k$(x), implies that the corresponding design specification is satisfied, otherwise it is violated.

- antipad_HFSS_opt.m: This script has the fminsearch method used for the optimization and the plots.

The optimization developed works as the following diagram:




## 3.2 HFSS models with through hole via

The following pictures represents how the through hole via model was created. At the left-hand picture, the pads, connector, via and trace are highlighted. Then, at the right-hand picture, can be observed the PCB with the 7 via grounds, with the 4 ground layers.

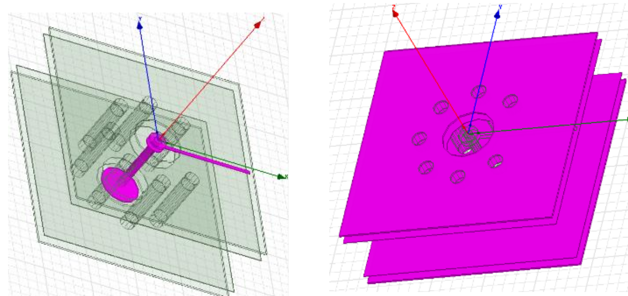


Figure 3.4 HFSS model for the through hole via.

## 3.3 Simulation results using Matlab

Once the optimization was run, several simulations were performed to find the right values of the anti- pads. The results are the following:

| Tolerance: 15% (57.5 ohms - 42.5 ohms) | | | | | |
|---|---|---|---|---|---|
| antipad 1 (mils) | antipad 2 (mils) | Zmax (ohms) | Zmin (ohms) | Maxerror | Duration (min) |
| 46 | 52 | 64.36 | 43.64 | 0.1193 | 21.46 |
| 48.3 | 52 | 64.12 | 45.51 | 0.1151 | 17.57 |
| 46 | 54.6 | 67.75 | 43.85 | 0.1435 | 17.33 |
| 48.3 | 49.4 | 63.11 | 45.24 | 0.0976 | 20.71 |
| 49.45 | 46.8 | 61.47 | 45.13 | 0.069 | 18.22 |
| 51.75 | 46.8 | 61.42 | 46.14 | 0.0683 | 18.32 |
| 54.62 | 44.2 | 60.5 | 46.011 | 0.05 | 17.94 |
| 55.77 | 39 | 58.54 | 44.42 | 0.0181 | 19.45 |
| 59.51 | 32.5 | 55.51 | 42.65 | 0 | |

Now, since the size of the pad of the connector is different than the size of the pad of via, there are two anti-pad values that need to be modified. The figure 3.7 describe the 2 different anti-pads that were used. There is an anti-pad 1 that is used in ground layer 1 and an anti-pad2 that is used in ground layers 3, 4 and 6.

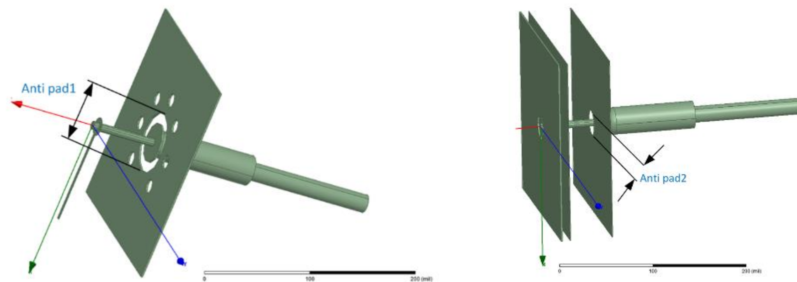
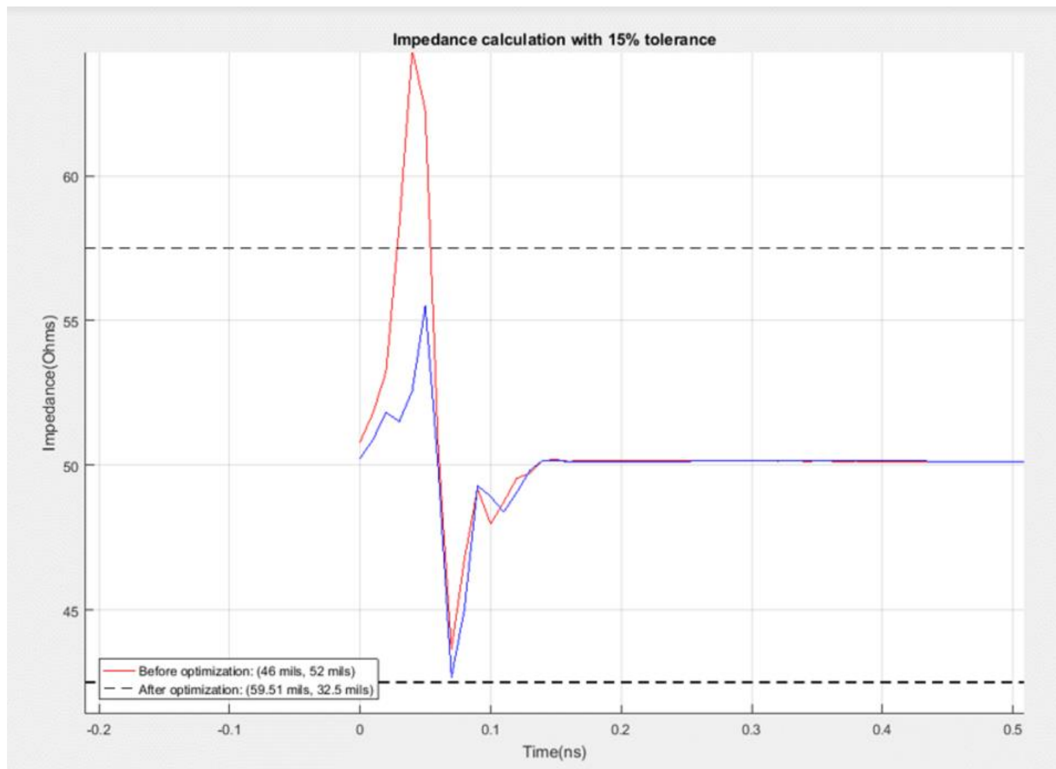



Figure 3.8 Anti-pad1 and Anti-pad2 definition

### 3.3.1 Through hole via results

The best value was obtained with an anti-pad 1 diameter of 59.51 mils with a impedance is 55.51 with a tolerance of 15% and the anti-pad 2 diameter is 32.5 mils with a impedance of 42.65 with the same tolerance.




# 4 Conclusions

It was very interesting to work in a tool where we were able to implement our own PCB model and then integrate it with a model provided by a connector manufacturer. In this way, the simulations performed for our designs, will be closer to the reality, and we take advantage of the work performed by the connector manufacturer.

Several simulations were performed for the through hole via model, but we were not able to comply 100% with the specification, although it was very close. However, looks like this is not unusual. At the end, the idea is to be as close as possible to the ideal state, even though sometimes cannot be implemented in this way. However, it is a very good approximation.

Even though this tool was not reviewed in class, the basics and the elements for the Sonnet tool, helped a lot to understand easily this tool. The main ideas were clear, the rest is was just a matter of playing with the tool.

It was very nice to work in a project that Signal Integrity Engineers normally does. In this way, we got a better understanding of the work that they develop.

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pp 3, 6 and 7.

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# 6 Appendix