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High-Speed Links Receiver Optimization in Post-Silicon Validation Exploiting Broyden-based Input Space Mapping

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***Abstract* — One of the major challenges in high-speed input/output (HSIO) links electrical validation is the physical layer (PHY) tuning process. Equalization techniques are employed to cancel any undesired effect. Typical industrial practices require massive lab measurements, making the equalization process very time consuming. In this paper, we exploit the Broyden-based input space mapping (SM) algorithm to efficiently optimize the PHY tuning receiver (Rx) equalizer settings for a SATA Gen 3 channel topology. We use a good-enough surrogate model as the coarse model, and an industrial post-silicon validation physical platform as the fine model. A map between the coarse and the fine model Rx equalizer settings is implicitly built, yielding an accelerated SM-based optimization of the PHY tuning process.**

***Index Terms* — aggressive space mapping, Broyden, DoE, eye diagram, equalization, HSIO, metamodels, SATA, SM, surrogate-based optimization.**

I. Introduction

Adaptive tuning circuits have been broadly adopted to confront the silicon process variation, and to cancel undesired effects such as jitter, attenuation, crosstalk, and inter-symbol interference. These tunable elements provide a way to reconfigure high-speed input/output (HSIO) links in post-silicon computer servers [1], as illustrated in Fig. 1. Typical industrial practices for physical (PHY) layer tuning involve exhaustive testing of these tunable parameters, requiring massive lab measurements, making it one of the most time-consuming processes in post-silicon validation [1]-[3].

Several methods have been proposed to address this challenge. A statistical framework, referred to as Bayesian model fusion (BMF), is proposed in [4]-[6]. This methodology is based on the assumption that pre-silicon models are already available. However, that BMF approach is not feasible in a post-silicon environment where not enough pre-silicon data is available. In order to overcome this limitation, other methods [1], [7], [8] have been proposed by using surrogate models developed from a set of learning base points generated from design of experiments (DoE) [9]. These metamodels treat the system as a black box, aiming to approximate the input-output relationship for the system under study [10]. Once a very-accurate surrogate model is developed, direct optimization can be applied to find the optimal PHY tuning parameters.

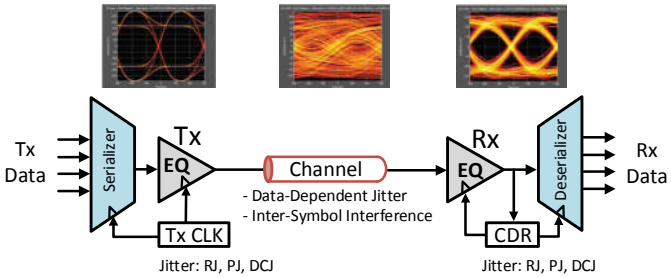

Fig. 1. HSIO link reconfiguration in post-silicon server validation to cancel out the effects of system channels' variability. From [12].

While an accurate surrogate model is desirable for direct surrogate-based optimization (SBO), it can be computationally expensive to develop. By combining an adequate modeling technique with a suitable DoE approach, a coarse surrogate model can be efficiently developed with a very reduced set of data, as in [11], [12]. Once this coarse model is available, space mapping (SM) techniques can be exploited.

In the present work, the Broyden-based input space mapping algorithm, better known as aggressive SM (ASM) [13], [14], is used for the first time in HSIO PHY tuning optimization. Our SM approach takes advantage of a coarse surrogate model developed following [11]. In our case, the fine model is a measurement-based post-silicon validation industrial platform. Our approach is illustrated by optimizing the PHY tuning receiver (Rx) equalizer settings for a SATA Gen 3 channel topology, accelerating tuning from several days to a few hours.

II. Broyden-based Input Space Mapping

SM optimization methods belong to the general class of surrogate-based optimization algorithms [15]. They are specialized on the efficient optimization of computationally expensive models. The most widely used SM approach to efficient design optimization is the ASM or Broyden-based input space mapping algorithm [14]. ASM efficiently finds an

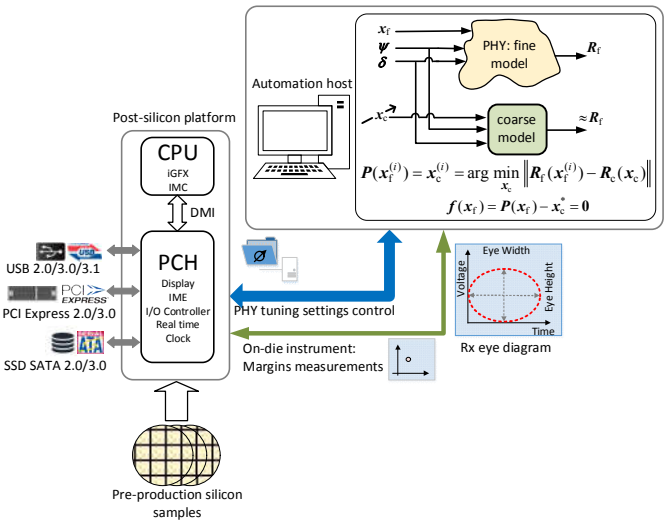

Fig. 2. Test setup: an Intel server post-silicon validation platform.

approximation of the optimal design of a computationally expensive model (fine model) by exploiting a fast but inaccurate surrogate representation (coarse model) [14]. ASM aims at finding a solution that makes the fine-model response close enough to the desired response.

A. Fine Model

Our fine model is an Intel server post-silicon validation platform in an industrial environment, as shown in Fig. 2. The platform is comprised mainly of a CPU and a platform controller hub (PCH) [1]. The PCH is a family of Intel microchips that controls data paths and support functions used in conjunction with the Intel CPU through direct media interface (DMI) [1]. Within the PCH, our methodology is applied to a HSIO link SATA Gen3 [16]. The SATA channel topology is comprised of the Tx driver, the Tx base board transmission lines, several via transitions, an I/O card connector, and 1 m SATA cable used to connect the base board to the device I/O card, as illustrated in Fig. 3. The measurement system is based on an Intel process called system margin validation (SMV) [1], [17], which is a methodology to assess how much margin is in the design relative to silicon characteristics and processes that vary over time, including voltage, and temperature. The fundamental process behind the SMV consists of systematically adjusting the corner conditions under which the validation platform operates, then measure the Rx functional eye opening by using on-die design for test (DFT) features until the eye opening has been shrunk to a point where the Rx detects errors or the system fails [8].

Let $\boldsymbol{R}_\mathrm{f} \in \Re^m$ represent the actual (measured) electrical margining system response, denoted as a fine model response, which consists of the eye width $e_\mathrm{w} \in \Re$ and eye height $e_\mathrm{h} \in \Re$ of the measured eye diagram,

$$\boldsymbol{R}_\mathrm{f}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = \left[e_\mathrm{w}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \quad e_\mathrm{h}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \right]^\mathrm{T} \tag{1}$$

This electrical margining system response depends on the PHY tuning settings $\boldsymbol{x}$ (EQ coefficients), the operating conditions $\boldsymbol{\psi}$ (voltage and temperature), and the devices $\boldsymbol{\delta}$ (silicon skew and external devices). We use five input variables that represent the SATA Rx PHY tuning coefficients, which are settings used in three main Rx circuitry blocks (CTLE, VGA, and CDR). $e_\mathrm{w} \in \Re$ and $e_\mathrm{h} \in \Re$ are obtained from measured parameters,

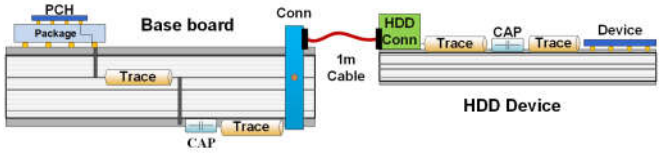

Fig. 3. SATA3 Rx channel topology. From [8].

$$e_\mathrm{w}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = e_\mathrm{wr}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) + e_\mathrm{wl}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \tag{2}$$

$$e_\mathrm{h}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) = e_\mathrm{hh}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) + e_\mathrm{hl}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta}) \tag{3}$$

where $e_\mathrm{wr} \in \Re$ and $e_\mathrm{wl} \in \Re$ are the eye width-right and eye width-left measured parameters, respectively, and $e_\mathrm{hh} \in \Re$ and $e_\mathrm{hl} \in \Re$ are the eye height-high and eye height-low parameters, respectively.

B. Coarse Model

Surrogate models can be constructed using data from high-reliability models or from measurements, and provide fast approximations of the original system or component at new design points [18]. In [11], we analyze several surrogate models trained with different DOE techniques to find a good coarse model able to approximate a USB3.1 Gen1 HSIO link with a very reduced amount of measurements, selecting the best combination of surrogate modeling technique and DOE in terms of accuracy and development time. Here, we follow [11] to develop a coarse surrogate model for a HSIO link SATA Gen3. By using the PHY tuning setting coefficients as inputs $\boldsymbol{x}$ and the corresponding eye height and width as outputs $\boldsymbol{R}_\mathrm{c}$, we select a Kriging surrogate modeling technique [7] with a Sobol [11] DoE approach with only 50 samples.

C. Objective Function

We want to find the optimal set of PHY tuning settings $\boldsymbol{x}$ that maximize the functional eye diagram area. Therefore, our objective function is given by

$$u(\boldsymbol{x}) = -\left[e_\mathrm{w}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right]\left[e_\mathrm{h}(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})\right] \tag{4}$$

During optimization, both $\boldsymbol{\psi}$ and $\boldsymbol{\delta}$ are kept fixed.

III. ASM Optimization Results

After applying the Broyden-based input space mapping algorithm [14], we arrive to a space-mapped solution, $\boldsymbol{x}^\mathrm{SM}$, in just 6 iterations (or fine model evaluations), as shown in Fig. 4. The set of Rx EQ coefficients contained in $\boldsymbol{x}^\mathrm{SM}$ makes the measured SATA Rx inner eye height and width of the PCH as open as that one predicted by the optimized coarse surrogate model. The SM solution ($\boldsymbol{x}^\mathrm{SM}$) found makes an improvement of 85% on the fine model eye diagram area as compared to that one with the initial settings ($\boldsymbol{x}_\mathrm{c}^{(0)}$), and a 33% improvement as compared to that one with the optimal coarse model solution ($\boldsymbol{x}_\mathrm{c}^*$), as shown in Fig. 5.

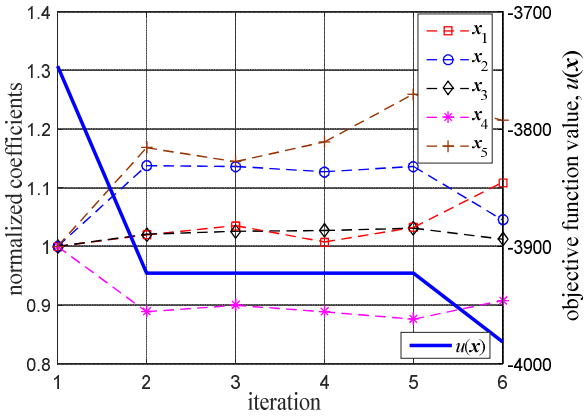

Fig. 4. Normalized coefficients and objective function values across SM optimization iterations.

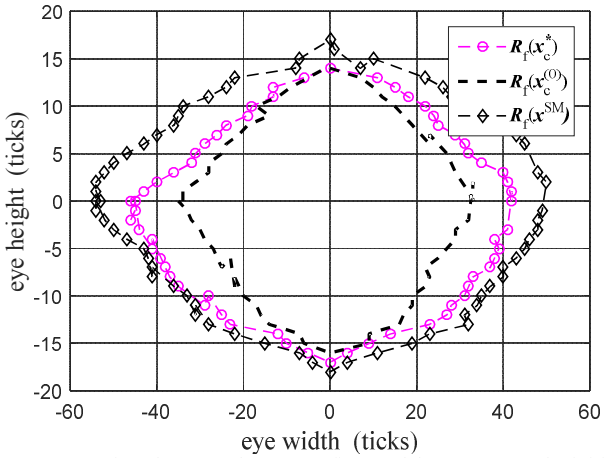

Fig. 5. Comparison between the system fine model responses at the initial Rx EQ coefficients, $\boldsymbol{x}_c^{(0)}$, at the optimal coarse model solution, $\boldsymbol{x}_c^*$, and at the space-mapped solution found, $\boldsymbol{x}^{SM}$.

The efficiency of this approach is also demonstrated by a very significant time reduction in post-Si validation and PHY tuning Rx equalization. While the traditional industrial process requires days for a complete empirical optimization, the method proposed here can be completed in a few hours. The technique can easily be applied to other interfaces like USB and PCI express.

IV. Conclusion

In this paper, we demonstrated how the Broyden-based input SM algorithm, better known as aggressive space mapping, can efficiently optimize the PHY tuning Rx equalizer settings by using a low-cost low-precision surrogate model, and a measurement-based post-silicon validation platform as the fine model. Our experimental results, based on a real industrial validation platform, demonstrated the efficiency of our method to deliver an optimal eye diagram, showing a substantial performance improvement and accelerating the typical required time for PHY tuning.

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