Industry-Oriented Research Projects on Computer-Aided Design of High-Frequency Circuits and Systems at ITESO Mexico

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***Abstract* — The Mexican Federal Government, through its National Council of Science and Technology (CONACYT, for its initials in Spanish), recently started a new initiative for encouraging the creation of high-quality industry-oriented graduate programs. In line to this initiative, ITESO – the Jesuit University of Guadalajara, Mexico, opened in 2013 an industry-oriented doctoral program in engineering sciences. In this paper, we briefly describe the main research production of this doctoral program in the area of computer-aided design techniques for RF and microwave modeling, design, and optimization of circuits and systems in industrial settings. We summarize the main recent contributions involving surrogate-based modeling and optimization as applied to post-silicon validation of high-speed computer interfaces, signal-integrity testing, power integrity enhancement, and low-cost high-speed interconnect multi-physical characterization. Research contributions validated on realistic industrial platforms in collaboration with high-tech companies are emphasized.**

***Keywords* — ANN, DoE, equalization, eye diagram, high-speed interconnects, HSIO, Kriging, neural network, optimization, polynomial, post-silicon validation, power integrity, SATA, signal integrity, support vector machines, surrogate models, temperature effects, USB.**

I. Introduction

Starting in 2012, CONACYT (the Mexican National Council of Science and Technology), established a formal new modality of graduate studies with the main purpose of increasing industrial competitiveness through high-level education of professionals enabled for industrial research and innovation. ITESO – the Jesuit University of Guadalajara, Mexico, opened in 2013 one of such graduate programs: an industry-oriented doctoral program in engineering sciences. Among the different research lines supported by this Ph.D. program, that one on computer-aided design (CAD) of high frequency circuits and systems is experiencing significant growth and highly relevant impact in terms of scientific and intellectual property generation in collaboration with local industries. In this paper, we briefly describe the main research production of this doctoral program in the area of CAD techniques for RF and microwave modeling, design, and optimization of circuits and systems in industrial settings. In particular, we summarize the main recent contributions involving surrogate-based modeling and optimization – including metamodeling approaches based on artificial neural networks, polynomial surrogates, Kriging, support vector machines, design of experiments sampling, efficient direct optimization algorithms and space mapping techniques – as applied to post-silicon validation of high-speed computer server platforms, signal-integrity testing, power integrity driven design, and low-cost high-speed interconnect multi-physical characterization for automotive applications. We emphasize research contributions applied on realistic industrial scenarios in collaboration with high-tech companies.

II. High-Speed Links Optimization in Industrial Post-Silicon Validation

The computer server industry generally imposes non-flexible high-speed physical channel designs. In consequence, physical layer (PHY) tuning based on equalization (EQ) techniques is used to mitigate undesired effects [1]. Typical industrial practices for PHY tuning rely on exhaustive enumeration methods, turning them into the most time-consuming processes in post-silicon validation [2].

A. Receiver Equalization Surrogate Optimization

In the current industrial practice for receiver (Rx) PHY tuning, the eye diagram margins are measured and empirically optimized. After that, a trade-off analysis is done with the jitter tolerance (JTOL) tests to get a set of EQ coefficients values that comply with the link specifications. We present in [1]-[2] a holistic approach to concurrently optimize Rx system margins and JTOL, by defining an objective function that combines both types of measurements. Our approach was tested on three different HSIO links (USB3.0, SATA, and PCIe3) in a post-silicon industrial environment, as that one shown in Fig. 1. Our results show an improvement of 175% on eye diagram area as compared with the initial coefficients, and a 34% improvement as compared with the trade-off

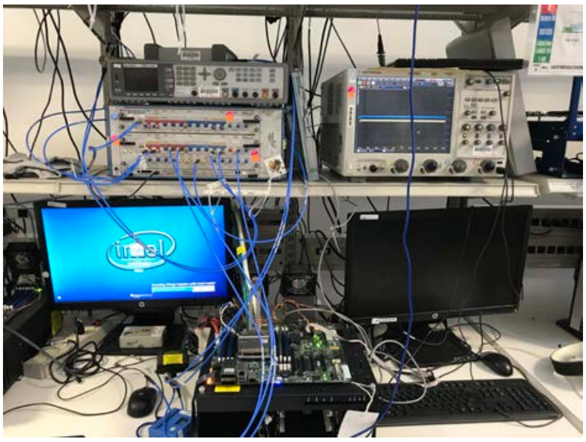

Fig. 1. The holistic methodology test setup for simultaneous system margining and JTOL optimization.

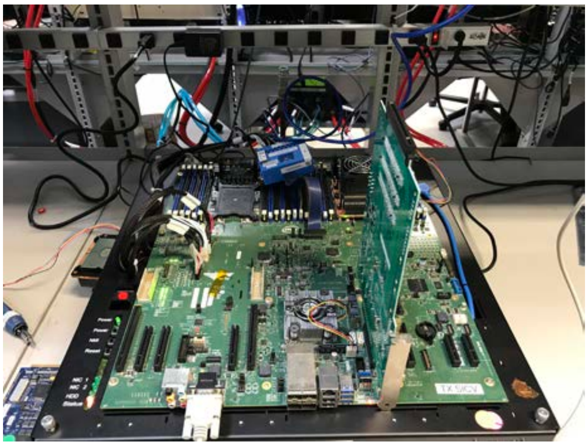

Fig. 2. An Intel post-silicon validation platform.

approach. Similarly, the JTOL results show a substantial improvement [1],[2].

B. PCIe Transmitter/Receiver Equalization Direct Opt.

PCI Express (PCIe) specification defines an adaptive mechanism for EQ to determine the optimum value of the transmitter (Tx) and Rx EQ coefficients. The current industrial practice consists of finding a subset of coefficient combinations during post-silicon validation, and then program it into the system BIOS. The method consists of using maps of EQ coefficients, which are obtained by measuring the Rx system margins. In [3], we propose an efficient optimization methodology to find the optimal subset of Tx and Rx coefficients to maximize the eye diagram in an Intel validation platform (see Fig. 2). The optimized coefficients yield an eye diagram improvement by 35% as compared to that one with the initial coefficients; our approach also reduces the eye diagram asymmetries (yielding more centered eye diagrams), and significantly reduce the post-silicon validation time [3].

C. SFP Tx Equalization Direct Optimization

Ethernet enhanced small form factor pluggables (SFP+) are regulated by a Tx eye diagram mask in terms of voltage and time. SFP+ Tx FIR filter is not self-adaptive, and then tuning is required during post-silicon validation. The current post-silicon industrial practices for SFP+ tuning are too time consuming. We proposed in [4] an efficient direct optimization technique in a post-silicon validation platform, showing again a substantial improvement on eye diagram and a significant reduction of validation time.

D. Coarse Modeling for Space Mapping (SM)

While an accurate surrogate model is desirable for direct surrogate-based optimization, its development can still be computationally expensive. In [5]-[6], we apply several surrogate modeling methods and design of experiments (DoE) techniques to find a model that approximates the system with a very reduced set of data. In a future work, we will use this coarse surrogate for SM optimization [7].

III. Numerical Techniques to Accelerate Industrial Tests of HSIO Links

A. Design of Experiments

Modern HSIO links use EQ circuitry to overcome noise impairments and other high-frequency undesired effects (reflections, crosstalk, EMI, etc.). With a large number of EQ parameters, it is unfeasible to carry out complete enumeration or “one factor at a time” experimental strategies. We have exploited DoE techniques to establish a reduced set of experiments to find the optimal EQ parameters. In [8], response surface models (RSM) are combined with DoE methods. Fractional factorial design is used to generate a first order RSM, where the confounding technique allows to reduce the number of required experiments. This first order RSM is used to find the improvement trajectory using steepest ascent method. Once in the optimal region, a central composite design (CCD) is generated to model second order effects. The optimal EQ parameters are finally found by maximizing the second order RSM in closed form. The objective function used throughout this procedure is based simply on the multiplication of the eye width and eye height measurements of the Rx eye diagram.

B. Golden Section Technique

Jitter tolerance (JTOL) tests take several hours to execute when running at the specification bit error rate (BER), which is typically 10^{-12} for HSIO links. A JTOL test consists of measuring the BER while varying the injected periodic jitter (J_P) in both amplitude and frequency. For any given frequency point, the problem of finding the largest J_P amplitude that yields a BER above the target value becomes a unidimensional optimization problem. The golden section search algorithm is among the most efficient methods for such problems. In [9], we propose a new algorithm that exploits the golden section search method to accelerate the JTOL test. Results show that the proposed method is 13.7 times faster than the traditional industrial approach, while maintaining the same accuracy in results.

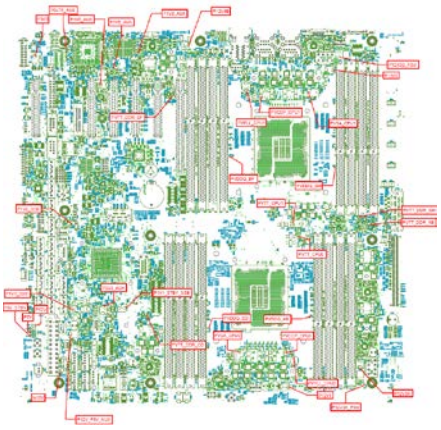

Fig. 3. Intel's 2010 Romley platform overview. Each red rectangle indicates a dedicated voltage regulator for individual power domains.

C. Polynomial Surrogate Modeling

We have exploited polynomial functions and the multinomial theorem for modeling and design optimization of high frequency (HF) circuits, including HSIO computer platforms. Compared to other similar approaches [10], [11], our formulation in [12] avoids redundant terms, assigns a different order of the polynomial at each frequency point, and calculates the weighting factors in two different closed forms according to the system matrix conditioning.

Initially, we developed polynomial surrogate models (PSM) of three HF structures [4]: a) an SIW interconnect with transitions to microstrip lines, b) a dual-band planar inverted-F handset antenna with slotted ground, and c) a package interconnect. The resultant PSM was compared against four well-known surrogate techniques: RSM, artificial neural networks (ANN), Kriging, and support vector machines (SVM). Our results demonstrate that PSM exhibits the best performance, in terms of the maximum absolute generalization error, when the region of interest for modeling is small and a very limited number of learning base points is used.

In [13], the PSM technique was used to model the multiphysical behavior of a microstrip line. The multiphysics model considers the dependency to temperature of conductivity in metals, as well as the mechanical and elasticity properties of dielectric and metallic materials. Then, varying the circuit temperature causes a mechanical deformation, affecting the corresponding EM response. Our results show a largest maximum absolute testing error in $|S_{11}|$ of 0.017 for all the frequency points and operating temperatures [13].

Ongoing efforts [14] consider polynomial functions for surrogate-based optimization using SM to reduce the computational cost of optimizing high-fidelity HF structures.

IV. Power Integrity Design Challenges

In the last two decades, power integrity has become increasingly relevant [15]. Particularly, in the computer server industry, many tradeoff decisions must be taken to come up with a suitable low-cost power solution (see Fig. 3).

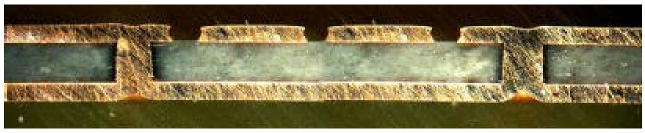

Fig. 4. Cross-section of a proposed coplanar-differential TL [19].

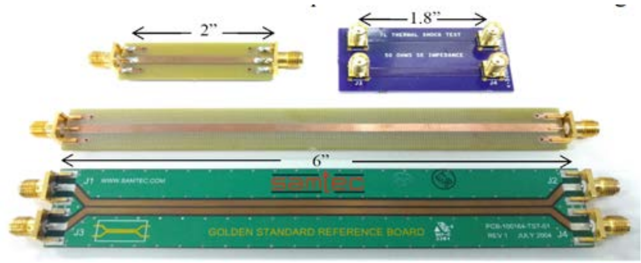

Fig. 5. FR-4 TL structures tested up to 15 GHz over a temperature span from −40 to 105 °C in a frequency range [20].

One of the biggest challenges is the capability to accurately predict adequate decoupling at the output of each voltage regulator (VR). To address this problem, we adopted DoE techniques in [16] to reduce platform cost while keeping adequate performance. This is possible by finding better compensation schemes that require less decoupling capacitance at the VR output.

Since the introduction of embedded HF switching VRs, the design of power package inductors started to become an important bottleneck. It implies finding an adequate inductor size to fit into the power domain without compromising signal routing. For that reason, we explore in [17] SM techniques to calculate inductor sizes that comply with power domain requirements and enable to accommodate signal routing.

Another challenge associated to the use of HF switching VR consists of finding optimal switching phases to minimize power losses. To achieve such goal, we have applied optimization techniques such as sequential quadratic programming and genetic algorithms [18].

V. Cost-Effective High-Speed Interconnects for the Connected Car

As the so-called "connected car" evolves, keeping the automotive industry cost-effective is essential for seamless customers' adoption. Fully digitized automobile vehicles with 5G connectivity and advanced driver information systems, require powerful computing entities with state of the art interconnects that should be able to withstand automotive temperature ranges alongside single-digit parts per million (PPM) in quality. This particular research work involves three different approaches towards robust and cost-effective high-speed interconnects for the connected car.

A. Impedance Matching Analysis and EMC Validation of a Low-Cost PCB Differential Interconnect

An impedance-matched planar printed circuit structure for high-speed interconnects employing low-cost substrates is proposed in [19]. To achieve enough speed to fulfill current transmission technologies and EMC requirements, 3D EM models along with optimization methods are exerted. A 2-

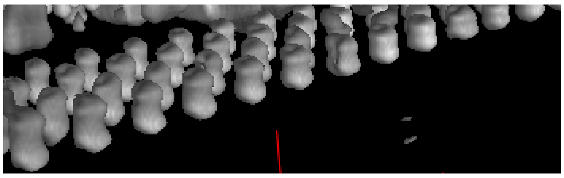

Fig. 6. Flexible metallic interconnects in an elongated state [21].

layer, FR4-based planar differential pair transmission line (TL) geometry with coplanar reference is proposed, as shown in Fig. 4. This interconnect was measured and full-wave EM simulated for EMC validation [19].

B. Temperature Effects in Automotive Grade High Speed Interconnects

The frequency response (up to 15 GHz) of several FR4-based automotive grade microstrip transmission line structures (see Fig. 5) over a temperature span from –40 to 105 °C is discerned in [20]. S-parameter responses are acquired in an industrially controlled environment. Results show that temperature has a major impact on these high-speed interconnects in frequencies above a few GHz, setting the need of employing accurate multi-physical models [20].

C. Flexible Metallic Interconnect for High Frequency Signal Transfer between Two Printed Circuit Boards

In an officially registered patent application [21], a cost-effective interconnect geometry (see Fig. 6) between two printed circuit boards is proposed. This interconnect allows high-frequency data transfer by the coalescence or fusion of a vastly malleable metal alloy, whose flexibility guarantees the interconnect integrity without fractures against multiple thermal shocks in a temperature range from –40 °C to 105 °C.

VI. Conclusion

We have summarized in this paper the main industry-oriented research contributions on CAD of high frequency circuits and systems of the Ph.D. program in engineering sciences at ITESO, Mexico.

References

[1] F. Rangel-Patino, A. Viveros-Wacher, J. E. Rayas-Sánchez, E. A. Vega-Ochoa, I. Duron-Rosales, and N. Hakim, "A holistic methodology for system margining and jitter tolerance optimization in post-silicon validation," in *IEEE MTT-S Latin America Microw. Conf. (LAMC-2016)*, Puerto Vallarta, Mexico, Dec. 2016, pp. 1-4.

[2] F. E. Rangel-Patiño, A. Viveros-Wacher, J. E. Rayas-Sánchez, I. Durón-Rosales, E. A. Vega-Ochoa, N. Hakim and E. López-Miralrio, "A holistic formulation for system margining and jitter tolerance optimization in industrial post-silicon validation," *IEEE Trans. Emerging Topics Computing*, vol. 6, 2018. (published online: 29 Sep. 2017)

[3] F. E. Rangel-Patiño, J. E. Rayas-Sánchez, E. A. Vega-Ochoa, and N. Hakim, "Direct optimization of a PCI Express link equalization in industrial post-silicon validation," in *EEE Latin American Test Symp. (LATS 2018)*, Sao Paulo, Brazil, Mar. 2018, pp. 1-6.

[4] I. Duron-Rosales, F. Rangel-Patino, J. E. Rayas-Sánchez, J. L. Chávez-Hurtado, and N. Hakim, "Reconfigurable FIR filter coefficient optimization in post-silicon validation to improve eye diagram for optical interconnects," in *Int. Caribbean Conf. Devices, Circuits, and Systems (ICCDCS-2017)*, Cozumel, Mexico, Jun. 2017, pp. 85-88.

[5] F. E. Rangel-Patiño, J. L. Chávez-Hurtado, A. Viveros-Wacher, J. E. Rayas-Sánchez, and N. Hakim, "System margining surrogate-based optimization in post-silicon validation," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 9, pp. 3109-3115, Sep. 2017.

[6] F. Rangel-Patino, J. L. Chávez-Hurtado, A. Viveros-Wacher, J. E. Rayas-Sánchez, and N. Hakim, "Eye diagram system margining surrogate-based optimization in a server silicon validation platform," in *European Microw. Conf. (EuMC-2017)*, Nuremberg, Germany, Oct. 2017, pp. 540-543.

[7] J. E. Rayas-Sánchez, "Power in simplicity with ASM: tracing the aggressive space mapping algorithm over two decades of development and engineering applications," *IEEE Microw. Magazine*, vol. 17, no. 4, pp. 64-76, Apr. 2016.

[8] A. Viveros-Wacher and J. E. Rayas-Sánchez, "Eye diagram optimization based on design of experiments (DoE) to accelerate industrial testing of high speed links," in *IEEE MTT-S Latin America Microw. Conf. (LAMC-2016)*, Puerto Vallarta, Mexico, Dec. 2016, pp. 1-3.

[9] A. Viveros-Wacher, R. Baca-Baylón, F. E. Rangel-Patiño, M. A. Dávalos-Santana, E. A. Vega-Ochoa, and J. E. Rayas-Sánchez, "Jitter tolerance acceleration using the golden section optimization technique," in *EEE Latin American Symp. Circuits and Systems Dig. (LASCAS 2018)*, Puerto Vallarta, Mexico, Feb. 2018, pp. 1-4.

[10] J. E. Rayas-Sánchez, J. L. Chávez-Hurtado, and Z. Brito-Brito, "Design optimization of full-wave EM models by low-order low-dimension polynomial surrogate functionals," *Int. J. Numerical Modelling: Electron. Networks, Dev. Fields.*, vol. 30, no. 3-4, e2094, May-Aug. 2017.

[11] J. E. Rayas-Sánchez, J. L. Chávez-Hurtado, and Z. Brito-Brito, "Enhanced formulation for polynomial-based surrogate modeling of microwave structures in frequency domain," in *IEEE MTT-S Int. Conf. Num. EM Mutiphysics Modeling Opt. RF, Microw., Terahertz App. (NEMO-2015)*, Ottawa, Canada, Aug. 2015, pp. 1-3.

[12] J. L. Chávez-Hurtado and J. E. Rayas-Sánchez, "Polynomial-based surrogate modeling of RF and microwave circuits in frequency domain exploiting the multinomial theorem," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4371-4381, Dec. 2016.

[13] J. L. Chávez-Hurtado, J. E. Rayas-Sánchez, and Z. Brito-Brito, "Multiphysics polynomial-based surrogate modeling of microwave structures in frequency domain," in *IEEE MTT-S Latin America Microw. Conf. (LAMC-2016)*, Puerto Vallarta, Mexico, Dec. 2016, pp. 1-3.

[14] J. L. Chávez-Hurtado, *Multiphysics Design of High Frequency Circuits by Polynomial Surrogate Modeling exploiting the Multinomial Theorem*, PhD Thesis, Dept. of Electronics, Systems, and Informatics, ITESO, Tlaquepaque, Mexico, 2017.

[15] T. Wu, H. Chuang, and T. Wang, "Overview of power integrity solutions on package and PCB: decoupling and EBG isolation," *IEEE Trans. on Electromagnetic Compat.*, vol. 52, no.2, pp. 346-356, May 2010.

[16] F. Leal-Romo, J. E. Rayas-Sánchez, and J. He, "Design of experiments implementation towards optimization of power distribution networks," in *IEEE Latin American Symp. Circuits and Systems Dig. (LASCAS 2017)*, Bariloche, Argentina, Feb. 2017, pp. 1-4.

[17] F. Leal-Romo, M. Cabrera-Gómez, J. E. Rayas-Sánchez, and D. M. García-Mora, "Design optimization of a planar spiral inductor using space mapping," in *Int. Conf. Electrical Performance of Electronic Packaging and Systems (EPEPS 2017)*, San Jose, CA, Oct. 2017, pp. 1-3.

[18] F. Leal-Romo, J. L. Silva-Perales, C. López-Limón, and J. E. Rayas-Sánchez, "Optimizing phase settings of high-frequency voltage regulators for power delivery applications," in *IEEE Workshop on Signal and Power Integrity (SPI 2018),* Brest, France, May 2018, pp. 1-4.

[19] J. R. del-Rey, Z. Brito-Brito, and J. E. Rayas-Sánchez, "Impedance matching analysis and EMC validation of a low-cost PCB differential interconnect," in *IEEE Latin American Test Symp. (LATS-2015)*, Puerto Vallarta, Mexico, Mar. 2015, pp. 1-5.

[20] J. R. del-Rey, Z. Brito-Brito, J. E. Rayas-Sánchez, and N. Izquierdo, "Temperature effects in automotive-grade high speed interconnects," in *IEEE MTT-S Latin America Microw. Conf. (LAMC-2016)*, Puerto Vallarta, Mexico, Dec. 2016, pp. 1-4.

[21] J. R. del-Rey and Z. Brito-Brito, "*Interconexión metálica flexible para transferencia de señales eléctricas de alta frecuencia entre dos circuitos impresos,*" Mexican Patent Application MX/A/2018/003154 (IMPI), March 14, 2018.