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Departamento de Electrónica, Sistemas e Informática

Maestría en Diseño Electrónico

High-Speed USB4 Interface: Validation Across Gen 2 and Gen 3 Variants

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TRABAJO RECEPCIONAL que para obtener el **GRADO** de
MAESTRO EN DISEÑO ELECTRÓNICO

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Summary

Almost 30 years ago, in 1996, a serial bus interface was designed with the main idea of standardizing the connection of peripheral device computers, replacing the parallel bus, and becoming common for many types of external devices connected to computers, such as peripherals like printers, keyboards, and mass storage.

The first idea was to use a defined form factor, with a specific architecture, connection-oriented, electrical physical interface, and trying to create an environment with a central focus on the computer system and devices connected by the Universal Serial protocol, sending common voltage to energize the devices and an electrical common ground between them. It is good to say that, since then, there have been several generations of USB specifications, changing the speed, connectors, protocol, etc.

For the electronics companies, this Serial bus opened a huge universe of possibilities, from the computers world, laptops, devices and external products with the idea to standardize the functionality of their products using the USB protocol in a scheme of host-device, but beyond the computers world, any industry can design any device connected by USB product, medicine industry, automotive industry, Banks, Super-Markets, etc, can use this USB protocol to connect any device to provide data to computers.

The constant evolution of the Universal serial Bus has come with changes in how the devices are connected, the demand of higher data rates to satisfy multiple markets like PCs, media players, phones, cameras, flash drives, has led to the development of USB type C connector, ending with adoption of multiple connectors like type A, micro USB, mini USB, to simplify the consumer choice. The huge demand for implementation, due to commercialization and the easy way to use, connect, and disconnect, brings the necessity to standardize the protocol on a worldwide scale.

The USB-IF is a consortium that is in charge of guiding the standard, developing the specifications for USB over multiple generations, to certify the correct signal integrity performance of the receiver and transmitter.

The motivation of this Document to share and present a methodology for validation the high speed interface USB4, since the electrical point of view covering the signal integrity as well as

compliance validation, and this validation is necessary to achieve the USB-IF logo, requirement for any product commercialization, in other words, without this USB IF logo the product cannot be in the market, this fact is critical for the companies.

Chapter one is focused on the USB, general information about it, with a focus on USB4, the standard with higher speed and data transfer, architecture, power, and, very important, the protocol with the logical layer machine state.

For the second chapter is dedicated to talk about the signal integrity, starting with a general overview and how is affecting the electrical part, how to determine the worst-case scenario for transmission and reception of the signal, also talking about the problems generated by the PCB and how can affect the signal at the connector and therefore the protocol.

For the third chapter, the main point is the compliance test for the USB4 protocol, including the electrical portion and signal integrity area, covering the transmission and de reception of the electrical portion, how the analog area reads the transactions to send as valid values to the logical part.

Content

Introduction

In the world of Electronics, the main constant is change, and in the search for continuous growth, it has been pursuing some milestones that require a change in technology. Just to mention some examples could start with the size of the transistor is something that is constantly being worked on, to reach smaller sizes, for the simple fact that by reducing the size of a transistor we can have more transistors in the same package therefore this can turn to increase the capacities of the same product, which generates greater revenue for the companies, referring to Moore's law, where in simple terms tell us the observation that the number of transistors on an integrated circuit will double every two years with minimal rise in cost. The consequence of this growth for electronics world, brings with it many opportunities, more dynamic changes, challenges in design at the chip level as well as the PCB level, in the same way the interconnections are at higher speed, the PCB traces become challenges due to effects that were not previously present at low frequencies and with few lanes.

Signal integrity generates uncertainty once an electrical signal is transmitted, mainly considering potential issues like noise, distortion, and loss. Electrical circuits face limitations in flow along the PCB path, and those signals experience attenuation along the electrical path. Although digital signals are inherently analog, they can be transmitted effectively over short distances at lower bit rates using simple conductors; however, at high bit rates and over longer PCB traces or through interconnections, these effects can degrade the signal, leading to errors and potential system or device failure.

The USB connectivity allows a simple, friendly, and easy way of connection with high-speed data transfer communication between devices. The huge demand for implementation, due to commercialization and the easy way to use, connect, and disconnect, brings the necessity to standardize the protocol regarding electrical, form factor, mechanical, speed, protocol architecture, and data link layer.

USB 4.0 is a consequence of the previous USB standard versions, improving speed, data transmission, connectivity, and mechanical connection. USB 4.0 supports speeds up to 40 Gbps, doubling the bandwidth of the previous version. It uses the USB-C connector with the goal of creating a universal connector that could be used with a wide range of devices and that would be capable of transmitting data, video, and power. This connector is smaller and more versatile than previous USB connectors, and it is designed to be reversible, so it can be plugged in either way.

1. Universal Serial Bus

1.1. Universal Serial Bus (USB) Introduction

USB is the acronym for “Universal Serial Bus”. In electronics, “bus” refers to an interconnection between components whose job is to transfer data or power. The part “serial” refers to the way it transmits the data, which is sequential; put in another way, it transmits one bit at a time (or clock cycle) through a single wire. USB is a standardized electrical specification that defines characteristics of the connectors and cables used to interconnect several devices within a system [1].

Over the years, USB has been evolving to satisfy the fast-increasing bandwidth demand and peripherals, which reflects in different USB versions, each with faster transfer speeds and more enhanced features than the previous generation.

There are four generations of the USB specification:

- USB 1.0, which is also known as full speed.
- USB 2.0 or high speed
- USB 3.2 Gen 1 and Gen 2 (SuperSpeed and SuperSpeed+)
- USB 4.0

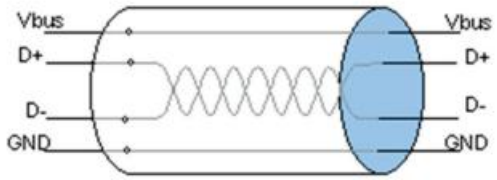


Fig. 1.1 The electrical structure inside a Universal Serial Bus (USB) 1.0 cable, which shows its serial data receiver and transmitter and its power lines. Figure taken from [2].

TABLE I
PERFORMANCE FIGURES FOR USB 3.0 AND USB 3.1. TABLE TAKEN FROM [1].

Performance figures for USB3.0 and USB3.1	
Version	Transfer speed
USB 2.0	480 Mbps
USB 3.0	5 Gbps
USB 3.1	10 Gbps

USB 3.2 introduced two new transfer modes, over the new USB Type-C Connector, increasing the bandwidth by using both lanes of the Type-C Connector at the same time, now capable of 20 Gbps in x2 mode (two lanes), and 10 Gbps using x1 mode (one lane) [2].

With the arrival of USB 3.2, the Type-C connector began to take over the widely used USB-A connector. What makes Type-C so popular is that it supports higher data transfer speeds and faster charging for peripheral devices, making it the preferred connector for USB 3.2 Gen 2 and now USB 4.0 [4]. Fig. 1.2 below summarizes the different release versions of USB in general.

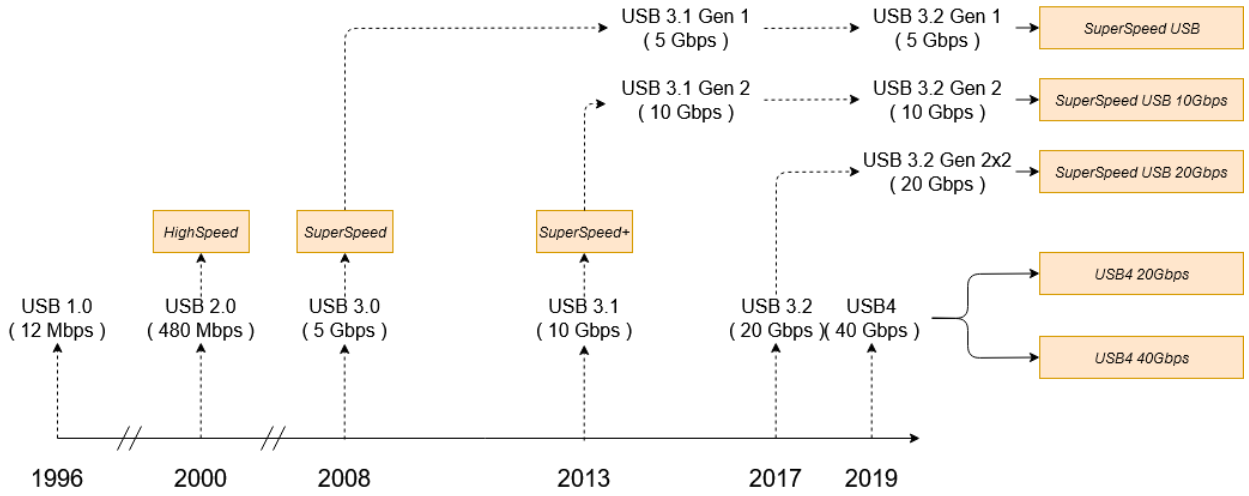


Fig. 1.2 Evolution of USB standards, starting from USB 1.0 up to USB 4.0. Figure taken from [3].

1.2. USB 4.0

USB 4.0 is the most complex USB specification to date; designers need to have a comprehensive understanding of USB 4.0, and all of the previous USB versions, in addition to USB Power Delivery specifications. Additionally, familiarity with PCIe and DisplayPort specifications is essential for many USB 4.0 designs.

The key distinction between USB 4.0 and USB 3.2 is that USB 4.0 can tunnel Host-to-Host communication, PCIe, DisplayPort audio/video, and USB data through the same link and Type-C connector. This tunneling capability allows audio, video, data, and power to be transmitted simultaneously at higher speeds compared to USB 3.2 and DisplayPort Alternate Mode. PCIe tunneling supports high-speed applications like mass storage and AI acceleration. USB 4.0 achieves 20 Gbps and 40 Gbps speeds by combining the two Tx and Rx lanes on the Type-C connector, with each lane operating at 10 Gbps or 20 Gbps [5].

As data rates for high-speed interfaces increase, maintaining signal integrity in the channel becomes a challenge due to parasitic effects from interconnects that were negligible at lower data rates. In electrical design, it is essential to establish and adhere to the insertion loss specifications to be capable of supporting the faster 20 Gbps data rates. Trace length and routing within the package form factor must be meticulously managed to prevent crosstalk violations and comply with the insertion loss and crosstalk requirements [7].

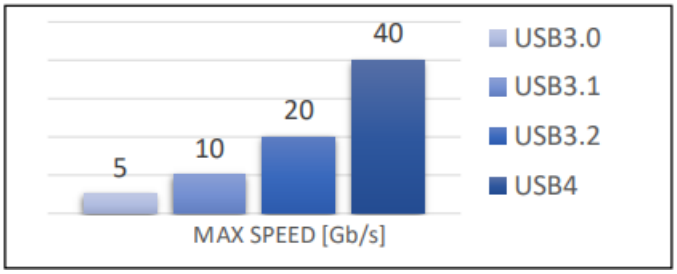


Fig. 1.3 USB 4.0 Highest speed compared to different generations of USB 3.0 in Gb/s. Figure taken from [6].

Table II describes the USB 4.0 cable interconnect configurations:

TABLE II
INTERCONNECT CONFIGURATIONS FOR USB 4.0 CABLES. TABLE TAKEN FROM [4].

Speed per lane	Passive cables	Active cables
Gen 2 (10 Gbps)	2m (1)	10's of meters
Gen 3 (20 Gbps)	0.8 (2)	10's of meters

(1) Normative cable spec of 12 dB at 5GHz
(2) Normative cable spec of 7.5 dB at 10GHz

1.3. USB 4.0 Fabric Connection

The USB 4.0 Fabric is designed to meet the requirements of several transport protocols, it is the main method for transmitting data in USB 4.0, it is an interconnected graph of one or more domains, providing the infrastructure for routing traffic, ensuring flow control, and maintaining data integrity, it allows USB, DisplayPort, and PCIe signals to be sent through the same physical cable, as described in Fig. 1.4.

In previous USB versions, USB-C could only support DisplayPort or Thunderbolt via Alt Modes, which required direct port connections. By integrating DisplayPort and some characteristics of Thunderbolt (including PCIe) into the USB 4.0 fabric specification, it enables displays and high-bandwidth devices to connect anywhere within the USB 4.0 infrastructure.

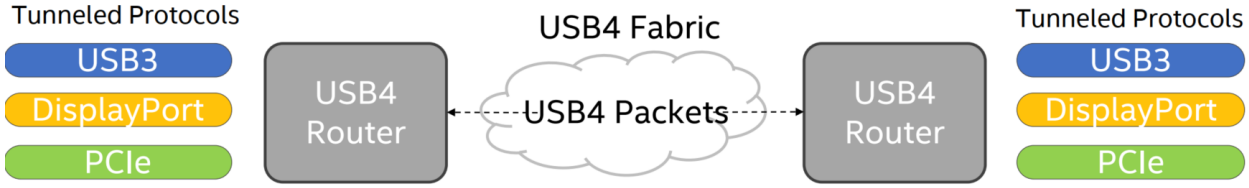


Fig. 1.4 Tunneling of USB3, PCIe, and DisplayPort protocols across USB 4.0 Fabric Connection. Figure taken from [8].

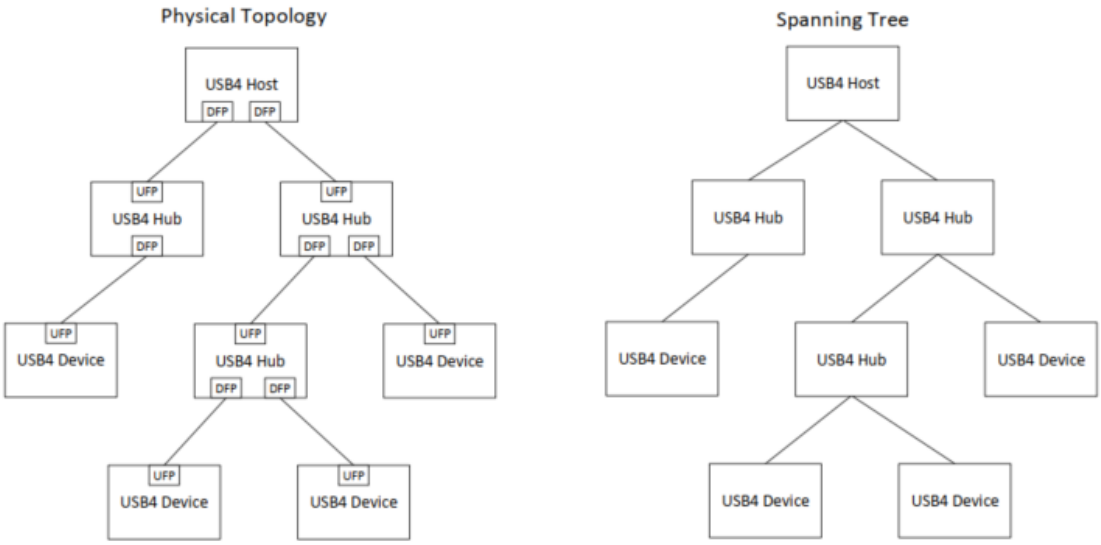


Fig. 1.5 Example USB 4.0 Physical Topology and Spanning Tree. Figure taken from [9].

The USB 4.0 Fabric uses a connection-oriented, tunneling architecture to dynamically share total speed and performance. Key components of the USB 4.0 Fabric include Routers, Ports, and Links, which all work together to manage and transport packets across the network. The topology of a USB 4.0 Fabric typically resembles a tree, with a USB 4.0 host at the root and USB 4.0 hubs and peripheral devices connected downstream [9], as described in Fig. 1.5.

1.4. Protocol Tunneling

USB 4.0 protocol tunneling is designed to combine several protocols onto a single physical interface, enabling various protocols to operate independently over the USB 4.0 transport and physical layers. These protocols include [9]:

- Enhanced SuperSpeed USB (USB3) tunneling: This includes USB3 Gen X tunneling, which utilizes the USB 3.2 protocol, and USB 3.0 Gen T tunneling, which uses a modified version of the USB 3.2 protocol to utilize higher bandwidth more efficiently within a USB 4.0 Domain.
- Display tunneling based on DisplayPort (DP): This allows DisplayPort audio/video traffic to be tunneled through the USB 4.0 Fabric.

- Protocol and load/store tunneling for PCIe: This allows PCIe traffic to be tunneled through the USB 4.0 Fabric, enabling high throughput mass storage, AI acceleration, etc.

Protocol tunnels use specific protocol adapters for each protocol. USB 3 Gen X and PCIe protocols need native USB hubs and PCIe switches to manage packet routing and buffering. In contrast, display tunneling, host-to-host communication, and USB3 Gen T tunneling do not require intermediate protocol-specific logic, as these tunnels are established as direct end-to-end links.

USB 4.0 tunneling requires different components for optimum compatibility:

A router, which is the key component of the USB 4.0 architecture, it responsible for mapping tunneled protocol traffic to USB 4.0 packets and routing them through the USB 4.0 fabric, some of its elements are: a router core that interconnects between ports and provides router-wide services, ports and links, a time management unit [8] and additionally each router can contain up to 64 adapters, as shown in Fig. 1.6.

Adapters serve as interfaces between the router and external entities. There are three types of adapters [9] that are described in Fig. 1.7:

- Protocol Adapters
- Lane Adapters.
- Control Adapters.

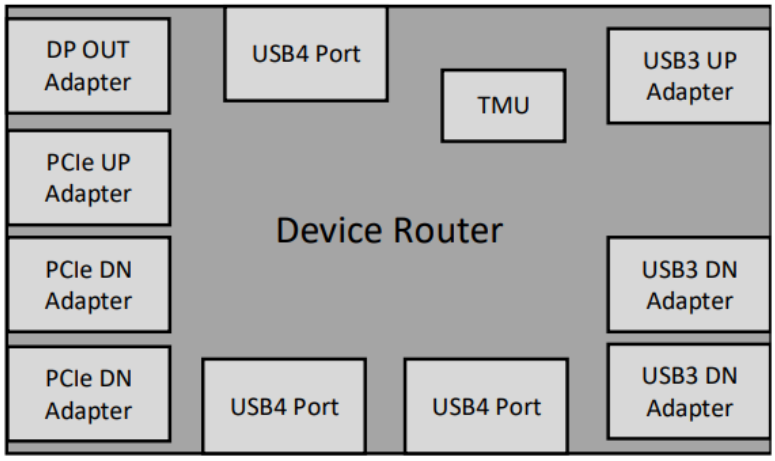


Fig. 1.6 Router example, describing the architecture of a Device Router and its elements: Ports, time management unit, and adapters. Figure taken from [8].

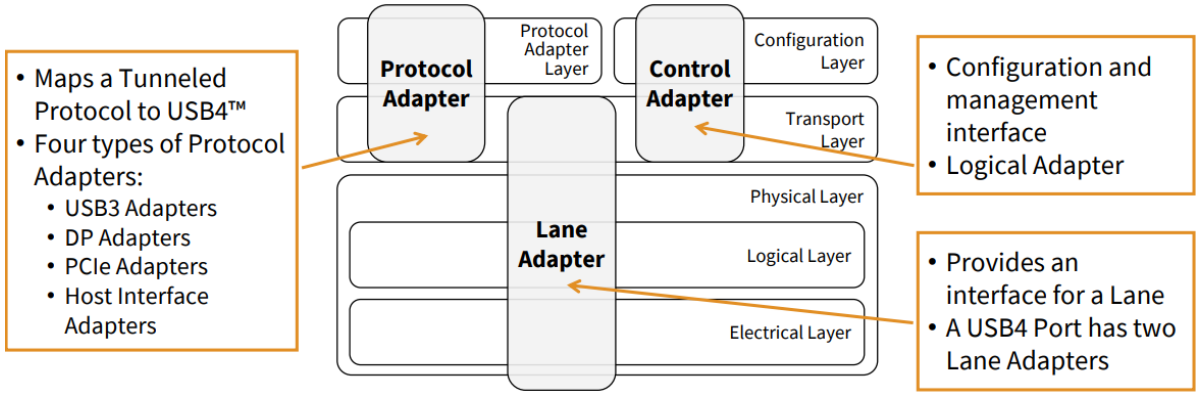


Fig. 1.7 Description of adapters and their purpose in the different USB 4.0 layers, which serve as interfaces between the router and external entities. Figure taken from [8].

An USB 4.0 link which is the logical connection between two ports, it consists of transmitter and receiver lanes along with a two-wire sideband channel that is responsible of link initialization and management, additional components are devices which can include peripheral devices, hubs, and USB4-based docks, also requires a host interface with a host router to facilitate data exchange between a host computer system and various USB 4.0 peripherals Fig. 1.8, these host include re-timers and are used to extend high-speed data links by reconditioning signals to prevent degradation from long cables or PCB traces, and finally, the connection manager handles tasks such as setting up and tearing down paths, managing hot plug/unplug events, bandwidth management and enables host-to-host tunneling, it operates on the platform that includes the host router [8], [9].

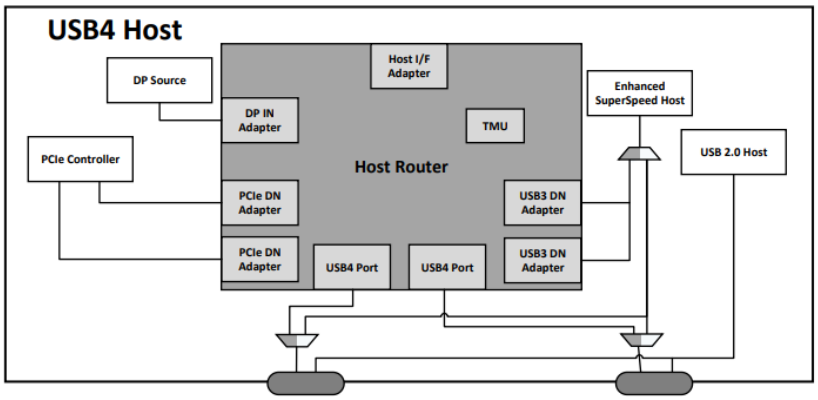


Fig. 1.8 USB 4.0 Host architecture, containing a host router, an internal USB host controller, and a DisplayPort source. Figure taken from [8].

1.5. Lane Initialization

Lane Initialization refers to the process where the electrical layer of a lane transitions from an inactive state to start transmitting and receiving traffic. This process is managed using the sideband channel and involves several phases [9], described in Fig. 1.9.

Phase 1 is responsible for the determination of initial conditions. It searches for the "answers" to some questions, for example: is it a USB 4.0 link? reverse insertion of a USB-C connector? Does it use an active cable with re-timers? Or is it a TBT3 active cable? Does the cable support Gen3? The Router will continue to phase 2 only if the link is USB 4.0 and has gathered all the information required.

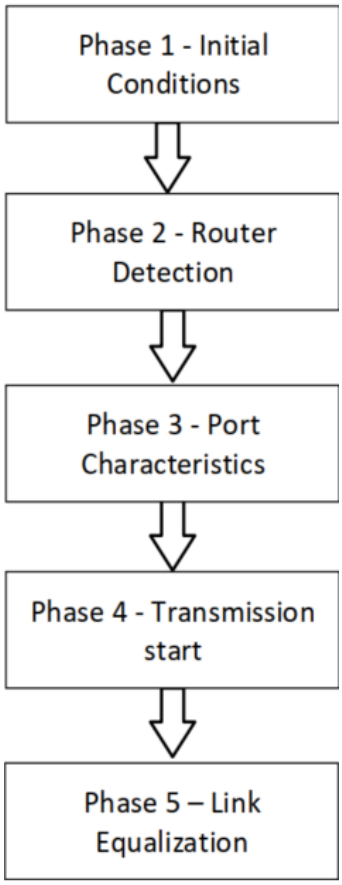


Fig. 1.9 Overview of the 5 phases of Lane Initialization. Figure taken from [9].

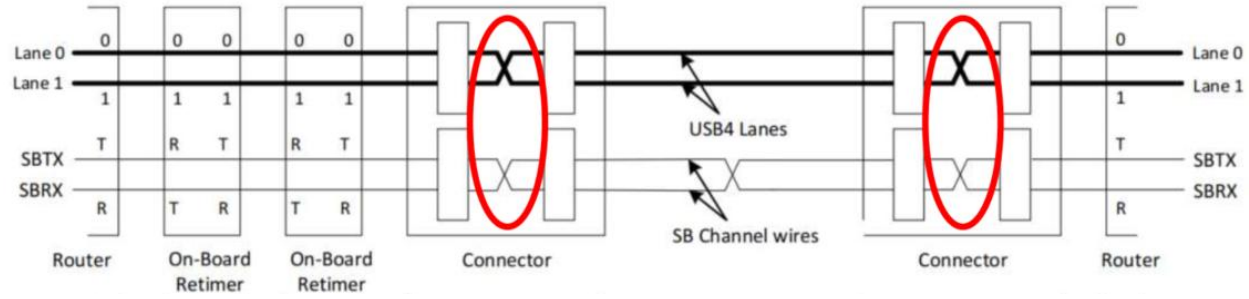


Fig. 1.10 Path that the re-timers follow before the correction when encountering a lane mismatch. Figure taken from [10].

In case of a reverse insertion of a USB-C cable, which is called lane mismatch or reversal, the power delivery controller notifies the router and re-timers in order to solve the mismatch on its side. This process is described in Fig. 1.10 and Fig. 1.11, where in Fig. 1.10, can be observed the path that the retimers follow when connected in the wrong orientation.

When the controller notifies the router and re-timers, the path is then updated for the right communication through the connection, shown in Fig. 1.11.

In phase 2, the Router detection happens, the detection is initialized by driving the side-band Tx to logic high on all its downstream-facing ports. When a Device Router detects a logic high on its Rx signal wires, it drives the Tx wires high on all of its USB 4.0 ports, the connections are described in Fig. 1.12, then transitions to phase 3.

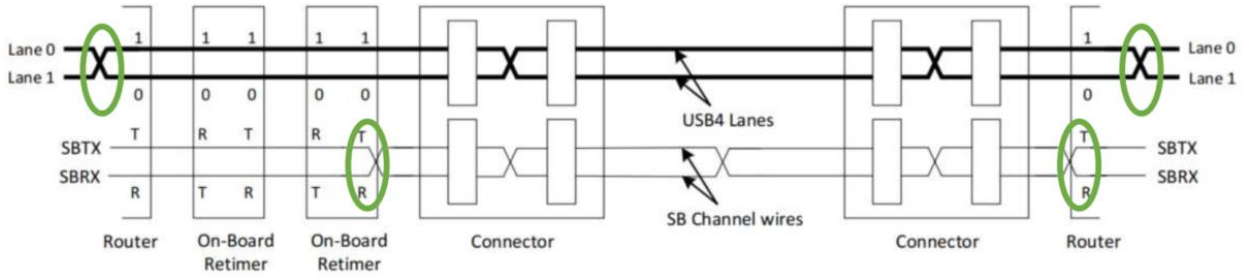


Fig. 1.11 Path that the re-timers follow after the correction when encountering a lane mismatch. Figure taken from [10].

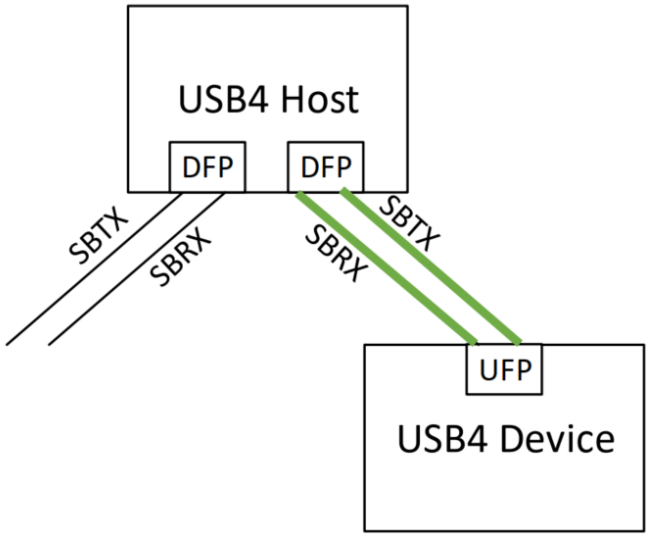


Fig. 1.12 USB 4.0 Downstream Facing Ports (DFP) Side-Band Rx and Tx signals connected to an Upstream Facing Port (UFP) of a USB 4.0 Device. Figure taken from [10].

Phase 3 purpose is to determine the USB 4.0 port characteristics, through the reading of the Link Configuration register using AT transactions, which are transactions used by a Router to read from or write to the connected Router. These transactions facilitate the communication and configuration between Routers and other devices on the USB4 Fabric.

Then decides on the next link parameters, which are taken by specific rules, described in Appendix A.

- Enabling: If there is an enabling request, proceeds to initialize lanes on each side.
- Dual-Lane – If requested, 2 Lanes & Lane Bonding are enabled on both sides.
- Lane Speed – Checks if the adapters and cable are Gen3 capable or not.
- RS-FEC – Enabled if both sides request it. RS-FEC is an error correction mechanism.

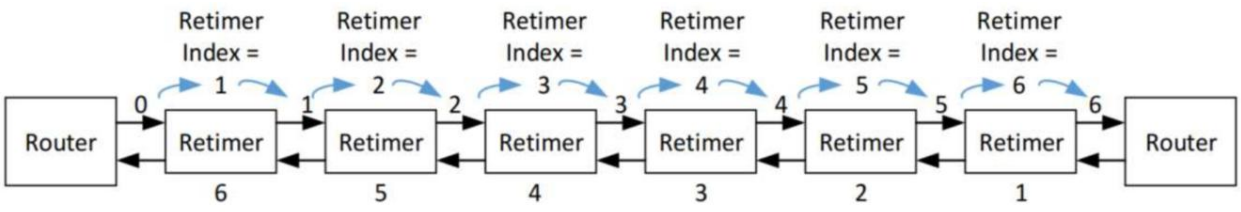


Fig. 1.13 Broadcast RT transaction enumerates Re-timers on the link. Figure taken from [10].

When finished acquiring all information, starts phase 4.

In Phase 4, the lane parameters are synchronized, and transmission begins. The port sets the lane speed and starts transmitting data. During this phase, each Router periodically sends a Broadcast RT transaction, which is a type of transaction issued by a Router to communicate with Re-timers along the link. In this case is used to enumerate the re-timers on the link, shown in Fig. 1.13. Upon receiving a Broadcast RT transaction, a Router activates its transmitter, starts sending the training sequence, and then transitions to Phase 5 [10].

In Phase 5, the final phase, lane equalization takes place. The receiver initiates Transmitter Feed Forward Equalization (TxFFE) to set transmitter parameters, listed in Appendix B, enhancing the signal quality between each Router/Re-timer and its adjacent Router/Re-timer. During parameter negotiation, the receiver tests several preset values defined in the electrical specification and selects the optimal preset value to use.

Fig. 1.14 illustrates a Link shared by two Routers and their Re-timers. In this figure, the Tx at Router A starts TxFFE negotiation with the receivers of On-Board Re-timer 1; meanwhile, the transmitters in On-Board Re-timer 6 conduct TxFFE negotiation with the receivers of Router B [9].

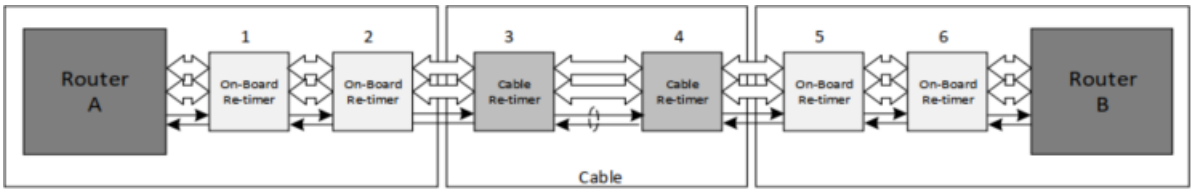


Fig. 1.14 Progression of Link Equalization between Router A and Router B and six re-timers. Figure taken from [9].

1.6. Lane Adapter State Machine

Understanding the challenges of testing USB 4.0 transmitters and receivers can help with the successful integration and testing of devices and hosts. The key is to first understand the concepts of link initialization and training. For USB 4.0, the Lane Adapter State Machine outlines the behavior of the logical link layer during the linkup sequence and manages state transitions for the lane, such as enabling/disabling the lane, lane initialization, training, and lane bonding. This behavior varies slightly depending on the Link speed, whether Gen 2 or Gen 3, and provides an interface for a specific lane within the ports, which each port contains two lane adapters, one for lane 0 and lane 1. The Lane Adapter State Machine includes states like Disabled, CLd (Common Lane disabled), Training, CL0 (Common Lane 0), Lane Bonding, and low power states such as CL0s, CL1, and CL2, each with specific behaviors and transitions [9], [11]. Fig. 1.15 below describes the behavior of the Lane Adapter State Machine sequence and all the conditions for each state.

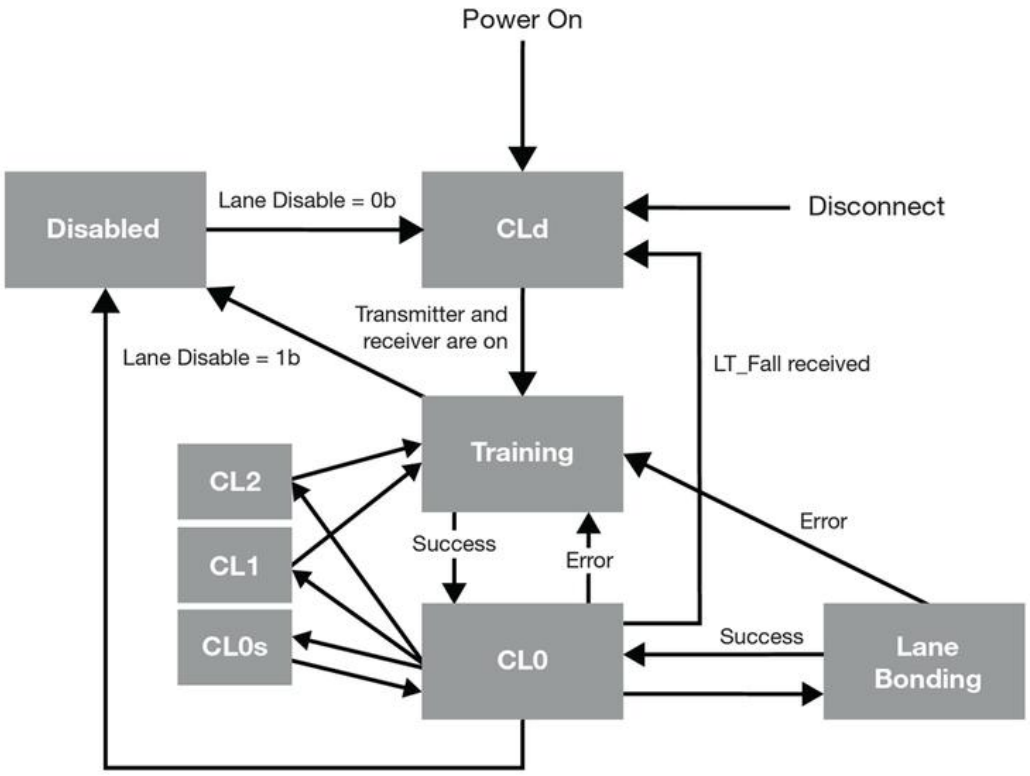


Fig. 1.15 The Lane Adapter State Machine for a Gen 2 and Gen 3 Link. Figure taken from [11].

Below is a detailed description of each state that comprises the Lane Adapter State Machine from Fig. 1.15 [9], [10].

- Disabled state: The Lane Adapter disables the lane, ensuring that the lane remains inactive until properly re-enabled.
- CLd state: The Lane Adapter sends the transmitter and receiver to be in an inactive mode.
- Training state: State where symbol synchronization and Transmitter Feed Forward Equalization negotiation is performed.
- CL0 state – The Lane Adapter starts to actively transmit and receive packets across the lane.
- Lane Bonding state: State where the single-lane links bond together into a symmetric link.
- CL0s, CL1, CL2 states: Low power states.

1.7. Power Delivery

Along with the USB 4.0 Electrical Specification, there is a USB PD specification which enables the negotiation of power requirements between USB devices, it includes hosts, devices, hubs, chargers, and cable assemblies. The Physical Layer is responsible for sending and receiving messages across either VBUS or CC wires between a port pair, defining the signaling technology, and handling the transmission of packets. The power supply behavior in USB Power Delivery systems includes specific sequences and timing parameters for transitions in voltage and current, ensuring smooth changes in power delivery.

The logical structure of USB Power Delivery capable devices is described in Fig. 1.16; the structure assumes that providers have source power capabilities and consumers have sink power capabilities. Devices may have configurations such as single or multiple ports and dedicated or shared power supplies.

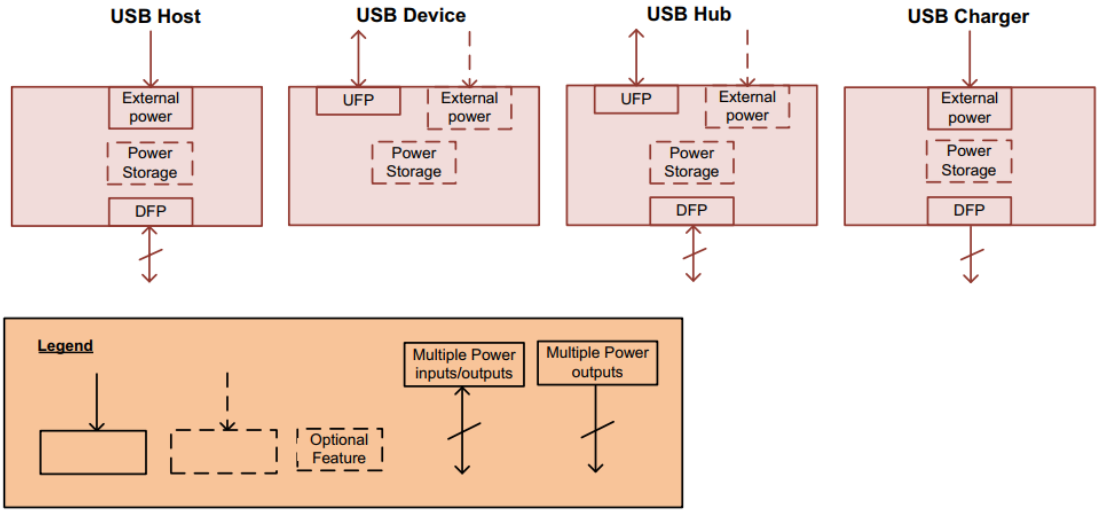


Fig. 1.16 Logical Structure of USB PD. Figure taken from [12].

The architecture is designed to indicate key concepts that each device should include, the following components [12]:

- Upstream Facing Port (UFP): Typically, responsible for sinking power from the power conductor and may also assume the role of a USB device.
- Downstream Facing Port (DFP): Equivalent to the port a device is attached to, it serves as the Host and is responsible of sourcing power.
- Power source: Can be external, storage (Battery/Power Bank), or derived from a bus-powered Hub.
- A sink: Can be used to storage power, or to power internal functions or devices attached to other devices.

1.8. USB Type-C Connector

USB Type-C connector is the new connector standard for USB, it is a single connector standard for data, video and power that can be used for all devices, such as different form factors (phone to workstation) and peripherals (displays, docks, storage), it is small, flippable (can be used in both orientations) and uses symmetrical cables [8].

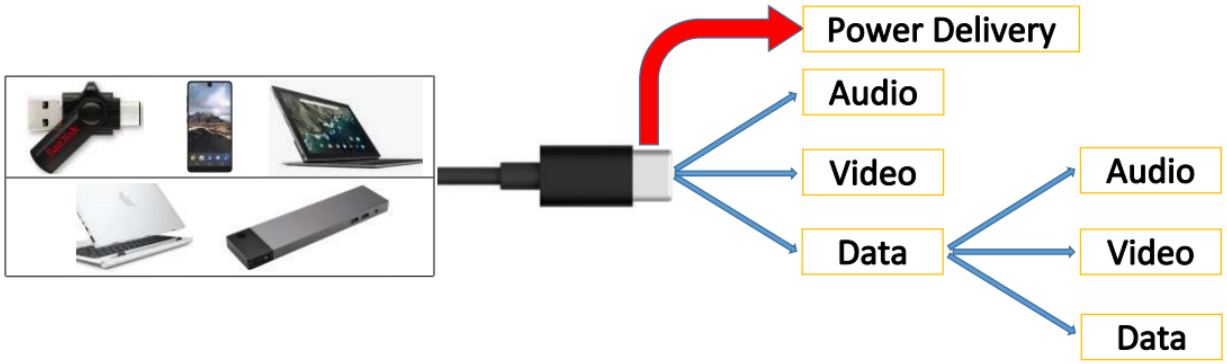


Fig. 1.17 Different topologies and devices converged into a single USB Type-C, which supports Audio, Video, and Data delivery. Figure taken from [8].

The USB Type-C connector supports various protocols through what are known as alternate modes. This capability allows for adapters that can output HDMI, VGA, DisplayPort, or other types of connections typically found on laptops to converge into a single type of port [2], as shown in Fig. 1.17.

USB-C supports several transfer speeds based on the USB version in use. Initially, with USB 3.1, it could achieve speeds up to 10 Gbps. Subsequent standards have further improved these speeds, with USB 3.2 reaching 20 Gbps and USB 4.0 achieving 40 Gbps. Additionally, the USB Type-C connector can carry high-definition video and audio, supporting resolutions of 4K and higher [13].

The USB Type-C connector has 24 pins. Fig. 1.18 below describes the pinouts.

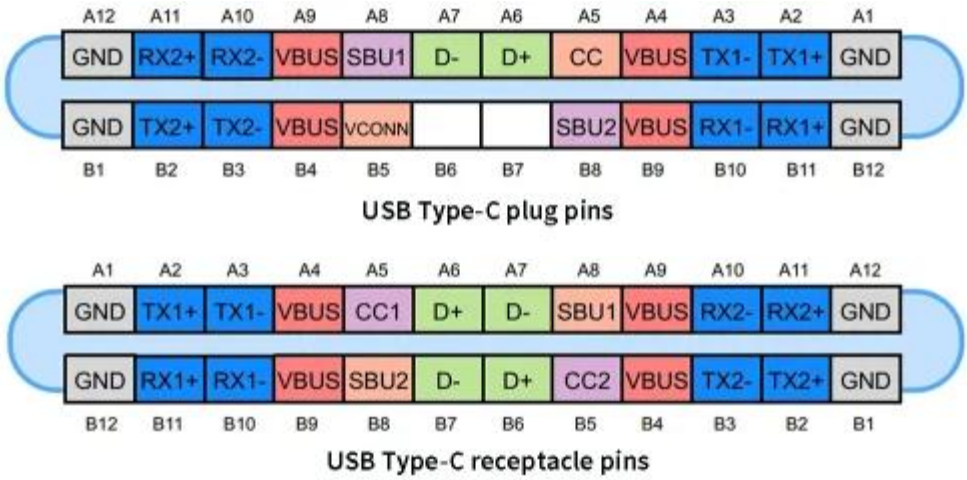


Fig. 1.18 USB Type-C plug and receptacle connectors pinout. Figure taken from [14].

2. Signal Integrity

Time ago, with a clock frequencies in the MHz range, voltage range in volts, most of the circuit board and packages used to be two layer boards, the electrical properties interconnections were not so critical, mainly because at this frequency did not affect the performance of the systems, in this sense, we say that "the interconnects were transparent to the signals."

The clock frequencies have been increasing due to the development of new technologies that demand higher speeds, like USB 4.0. This has caused the rise times to become faster in the order of picoseconds. These high-frequency clocks have become important in the data transmitted, so the interconnections are not transparent, which leads to multiple challenges arising in the systems. Once this clock frequencies increase and rise time decreases, the signal integrity becomes a problem, getting into a multiple physics phenome, coming for imperfection coupling and details learned or studied as math or physics effects but never measured or simulated in a real-world environment, at that moment it was necessary to learn and study all those effects in the PCB design. Independent of IC design, the effects were the same: signal integrity became necessary to work on design rules, and now software and IC design tools include those kinds of rules to avoid SI problems.

Signal Integrity ensures that the signal transmitted in an interconnection from a digital system 0's and 1's are received correctly, an example of interconnection can be considered as a cable, PCB transmission lines, connectors, all the components in the high-speed digital systems should be considered as each component can contribute to que quality of a signal.

Effects like electromagnetic interference, crosstalk, impedance mismatch, capacitive coupling, and conductive coupling play a key role in an optimal interconnect solution for high-speed systems.

Fig. 2.1 shows a representation of a data pattern sent from point A to B and vice versa through a channel, while Fig. 2.2 shows the representation of the waveform.

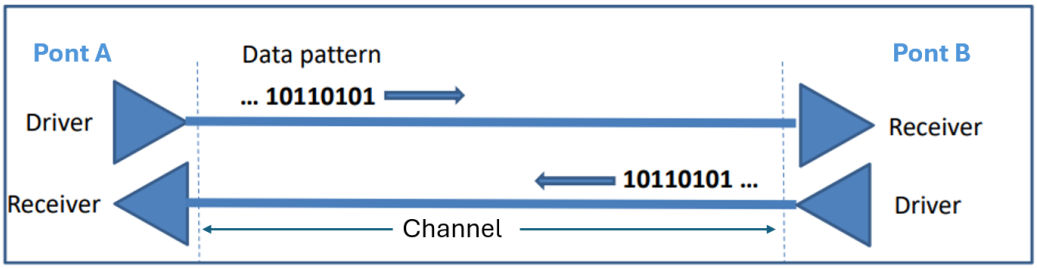


Fig. 2.1 Transmission of a data pattern from "Point A" to "Point B" through a channel.

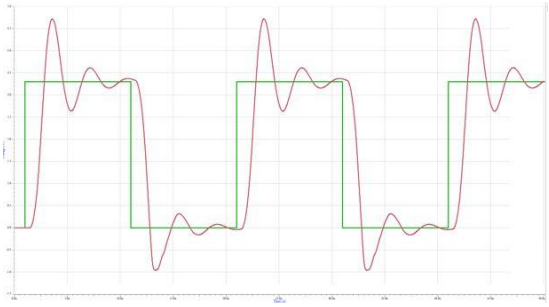


Fig. 2.2 Representation of an electrical signal and how accurately it represents its intended shape when sent through a channel. Figure taken from [16].

The proposal of Fig. 2.3 is to show all the problems related to Signal integrity in a waveform.

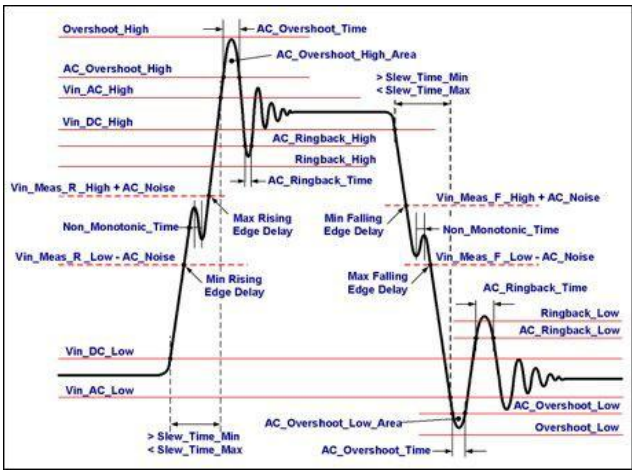


Fig. 2.3 Example waveform of an electrical signal showing all the issues related to signal integrity. Figure taken from [17].

2.1. USB 4.0 Compliance testing

Once the USB IF consortium is formalized, shaped, and specifications are completed, the following steps will be the definition of the compliance test for all cases. Compliance testing guarantees that the system and the manufacturing process meet regulatory requirements and industry standards.

USB certification is required to pass through the compliance testing, and this certification is a set of requirements and procedures to verify that the design aligns with a variety of specifications set out by the official USB4 standard. USB certification involves testing the electrical layer, logical layer, and interoperability of a design. One example can be found in Fig. 2.4, showing the eye diagram in red, with the mask in gray, particularly this case without failures touching the mask, the red area is the transition bit and the number of bits read help us to

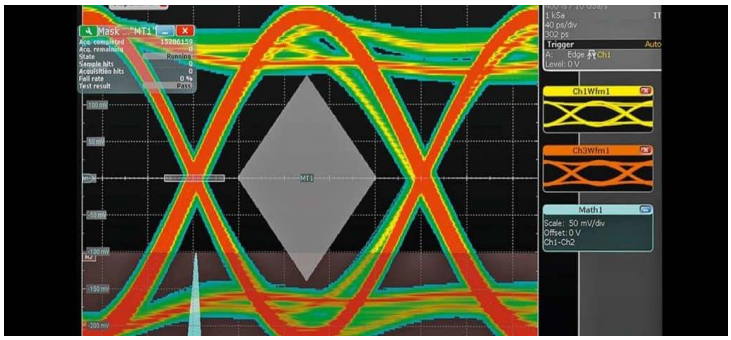


Fig. 2.4 Eye diagram taken from an oscilloscope, area in grey being the eye mask. Figure taken from [18].

accomplish the BER specification, one of the critical specs for the compliance.

Without USB 4.0 compliance testing, companies cannot legally display the USB 4.0 logo on their products. And the critical point is, without the logo, the product cannot be commercialized; this document focuses on electrical layer testing.

2.1.1 USB 4.0 Transmitter Electrical Specification

Anytime an electrical signal is transmitted, signal integrity is a concern. Electrical circuits are subject to attenuation along the signal path. At its most basic level, signal integrity ensures that a signal transmitted from point A to point B with a sufficient quality or integrity to allow effective

communication. Transmitter compliance specification is based on a series of tests to verify that the electrical design portion of the PHY complies with the electrical specification to send the data, in other words, sends the transaction achieving all the specifications. For an analog signal is necessary to compliance according to the place where the measurement is taken, which could be at the silicon pin, or the USB connector, implementing a loss channel for the measurement, or with a standard cable. Taking into account all the electrical parameters like voltage, timing, rise and fall time, as well as spread spectrum, just to mention the critical values of a waveform, the signal integrity for the transmitter is a big list of parameters to measure. The next image represents a graphical view of these parameters.

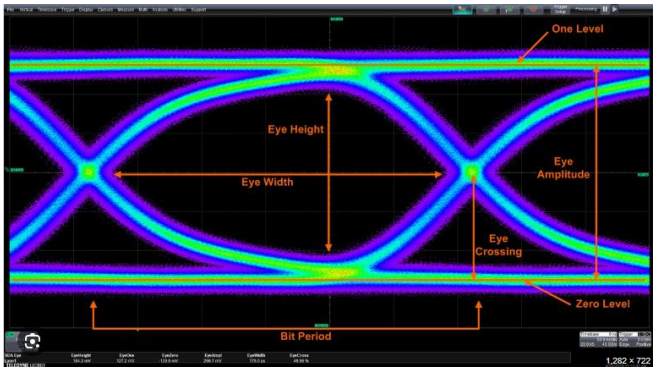


Fig. 2.5 Example of an eye diagram seen through an oscilloscope, which provides insight into the performance of a serial data link. Figure taken from [20].

2.1.2 USB 4.0 Receiver Electrical Specification

The receiver electrical compliance test is focused on the capacity of understand the electrical data and processing to logical values passing through the compliance channel, to talk about the receiver electrical specification, is necessary to learn about a Signal integrity parameters used only for this specific test, talking about frequency domain, S-parameters, channel, jitter, insertion loss, crosstalk but regarding time domain can be mentioned about impedance, delay, skew also rise and fall time, those parameters are part of the Rx specification and to accomplish is necessary to see the full picture of the data link.

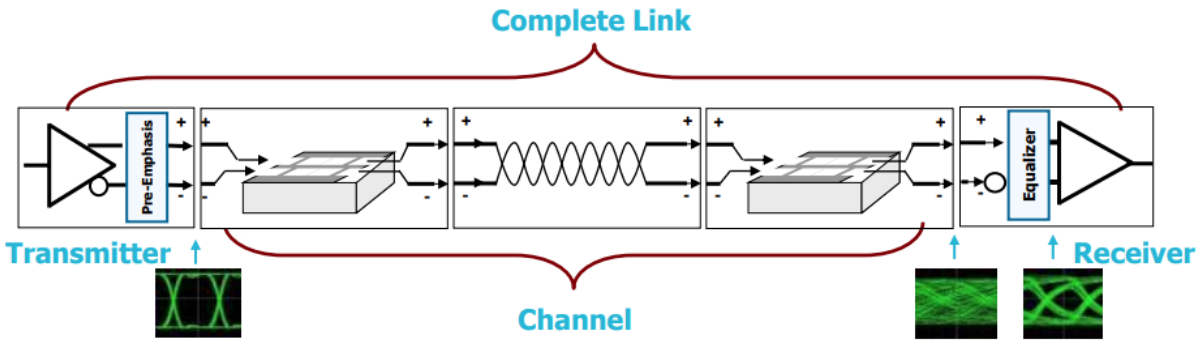


Fig. 2.6 Example Anatomy of a Serial Data Link. Figure taken from [19].

For the receiver electrical specification, the calibration of the worst-case channel is a little bit complicated, because the specification is related to insertion loss in dB. For example in a Host-Device connection where the channel is small in a consumer world, means a simple PCB for a commercial PC or laptop where the signal has good strength but problems to switch from 0 to 1 due to the mutual capacitance in the PCB, and the opposite side is a big channel with connector across the path and different types of jitter created by the diverse types of channel, like PCB, PCB-Stub, USB-Connector, cable, etc.

That means the calibration must be accurate according to the channel settings specified in the electrical specifications, including values like low pass filter, all kinds of jitter, passive loss in a particular PCB, write noise for all frequencies spectrum, and finally, the connector and our PCB. Mainly because is a simulated worst-case scenario for the signal channel in a real situation, talking about a final user or customer. On another hand, the electrical PHY has the capability to understand the electrical data, clean the signal, amplify it, and send to the logical values according to the USB protocol.

Finally, the importance of accomplishing the serial bus specifications for the transmitter and receiver data, with a BER of 1E-12 or lower.

3. USB 4.0 Electrical Compliance Test

USB 4.0 Electrical compliance testing is key for ensuring that hosts and devices meet the industrial standards set for USB 4.0 technology. Compliance testing ensures that USB 4.0 hosts can work seamlessly with other USB devices, regardless of the manufacturer.

USB 4.0 offers significant improvements in data transfer speeds, power delivery, and overall performance, electrical compliance testing verifies that hosts and devices can achieve these performance benchmarks, ensuring that users benefit from the full capabilities of USB 4.0, by adhering to the electrical standards, hosts and devices are less likely to experience failures or malfunctions. Compliance testing helps identify and rectify potential issues before the devices reach the market, enhancing their reliability and longevity.

Devices that pass USB 4.0 compliance testing can be certified by the USB Implementers Forum (USB-IF). This certification is a mark of quality and reliability, making the devices more attractive to consumers and increasing their market acceptance.

3.1. Rx Compliance Test Specification

Rx compliance testing for the host is crucial as it ensures that the USB 4.0 receiver can handle the worst-case incoming signal and operate reliably at a bit error rate (BER) of 1E-12 or lower. This testing validates the host's ability to tolerate signal variations and interference, ensuring robust and error-free communication in real-world scenarios. It involves a stressed receiver test and multiple test setups to evaluate performance across different conditions and supported speeds.

Router Assembly receiver compliance testing is conducted at the TP3' (Test Point 3’) reference point using a "golden" plug fixture and at the TP3 reference point using a "golden" receptacle fixture.

As described in Fig. 3.1, TP3' refers to the measurement point located on the plug side of the Rx input, while TP3 denotes the measurement point at the USB Type-C Tx on the far-end side of a passive cable. All measurements should be aligned to the described test points [22].

3. USB 4.0 ELECTRICAL COMPLIANCE TEST

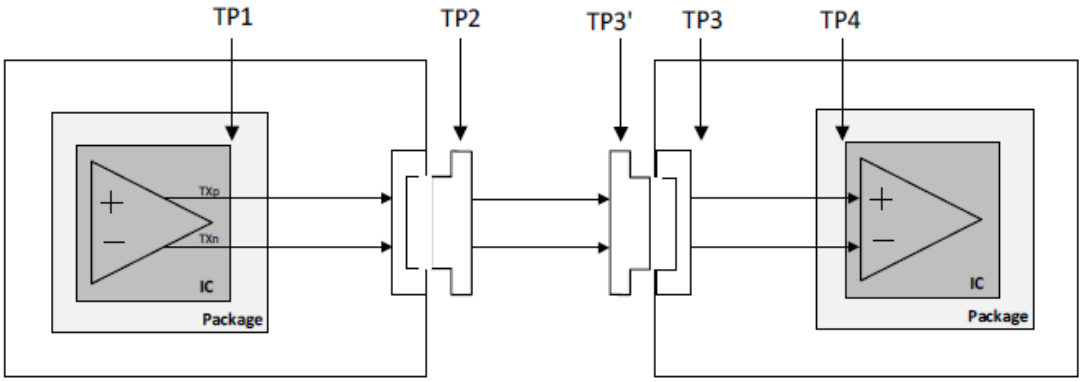


Fig. 3.1 USB 4.0 compliance test points definition, as specified in the USB 4.0 Electrical Compliance Test Specification. Figure taken from [22].

All post-processing for Rx calibration, stressed eye, and signal frequency variations is performed using a specialized software tool used for testing and validating the electrical performance of USB 4.0 devices and hosts. It is designed to ensure that USB 4.0 devices/hosts meet the electrical compliance specification set by the USB-IF.

Table III below describes the several receiver compliance tests required for USB 4.0 certification.

TABLE III
USB 4.0 RECEIVER COMPLIANCE TESTS.

Speed	Test category name	Tests under category
10Gbps and 20Gbps	Test at TP3' (Case 1)	Gen2 Rx Compliance test portA 10G TP3'
		Gen3 Rx Compliance test portA 20G TP3'
		Gen2 Rx Signal Frequency Variations Training test 10G TP3’
		Gen3 Rx Frequency Variations test 10G TP3’
	Test at TP3 (Case 2)	Gen2 Rx Compliance test portA 10G TP3
		Gen3 Rx Compliance test portA 20G TP3
		Gen2 Rx Frequency Variations test 10G TP3
		Gen3 Rx Frequency Variations test 10G TP3

3.1.1 Jitter Tolerance Test

A method to evaluate high-speed link performance is by measuring the bit error rate (BER), which is used to assess Rx jitter tolerance for compliance, its importance relies in verifying whether the Device Under Test (DUT) meets the receiver Compliance Test Specification defined in the USB 4.0 standard, in other words, ensures that that the Rx can maintain an acceptable BER under worst-case conditions. This ensures compatibility and interoperability with other compliant devices, which is vital in a multi-vendor environment. The test involves using a BER tester (BERT) to vary the injected periodic jitter; it should be performed for various periodic jitter frequencies in distinct procedures, until bit errors occur. It evaluates the number of symbol errors when all jitter types and the eye height are adjusted to their specified limit values [22].

3.1.2 Signal Frequency Variations Training Test

The Signal Frequency Variations Training Test ensures that frequency variations during Link training remain within specified limits. This test is essential for verifying the frequency stability of the Device Under Test (DUT) during the critical Link training phase. It uses a special Spread Spectrum Clocking (SSC) modulation with the following parameters:

- Triangle modulation wave.
- 32 kHz in modulation frequency.
- Must have a spread deviation of +300 ppm to -5300 ppm.

Fig. 3.2 describes the special clk-switch SSC modulation profile used for the Signal Frequency Variations Training Test. This specific SSC modulation configuration ensures that the DUT can handle the frequency variations introduced by the SSC without losing lock or producing errors during the Link training phase [22].

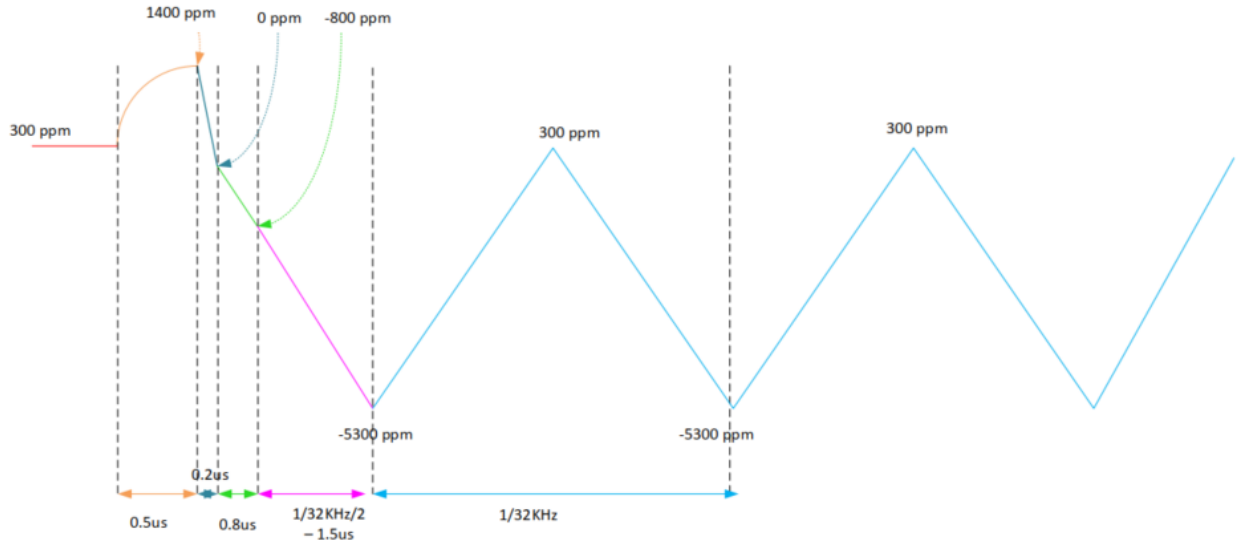


Fig. 3.2 Special clk-switch SSC modulation profile for Signal Frequency Variations Training Test. Figure taken from [22].

3.2. Rx Compliance Test Setup

Testing USB4 PHY receivers for compliance requires a testbed that includes a Bit Error Rate Tester (BERT), a high-bandwidth oscilloscope used for calibration, a receiver test application software which automates the test execution and performs the required measurements and calibrations according to the USB 4.0 Electrical Compliance Test Specification developed by the USB-IF, and a USB 4.0 microcontroller test module. Additional equipment such as a network analyzer, voltage meter, and scope with a high impedance probe are used for measuring return loss and sideband TX/RX signal testing [24].

The USB 4.0 Rx compliance test setup is designed to evaluate the receiver's ability to tolerate the worst-case signal. The setup involves a calibration process to ensure that the equipment and cables are properly calibrated and requires a proper de-embedding of coaxial cables. This is achieved by fine-tuning the transmitter equalizer and precisely calibrating the BERT's stress signal with a high-performance oscilloscope [22].

There are two setups used in Rx testing that are described in the USB 4.0 Electrical Compliance Test Specification: the calibration setup and the test setup. Fig. 3.3 illustrates the calibration setup.

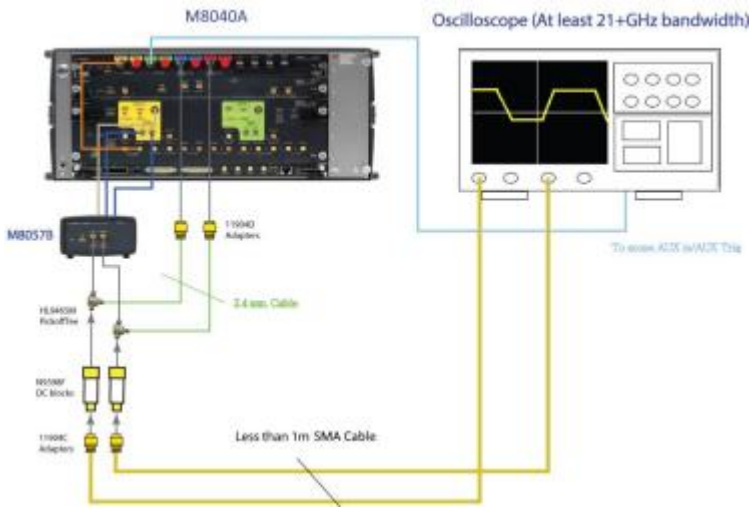


Fig. 3.3 Receiver Calibration Setup, as described in the USB 4.0 Electrical Compliance Test Specification. Figure taken from [25].

There are two different Test Setups for Receiver testing, the first one, described in Fig. 3.4, is used for tests at TP3' (described in section 3.1 Rx Compliance Test Specification).

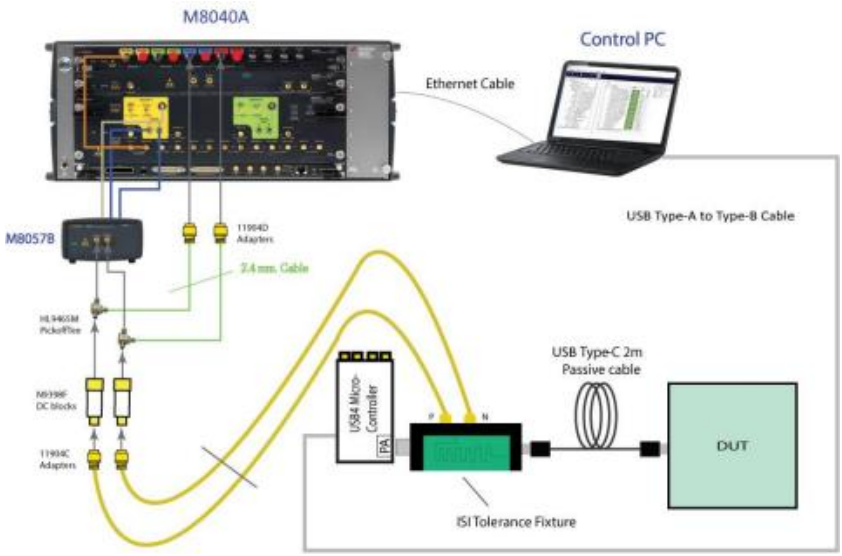


Fig. 3.4 Setup for Receiver at TP3' tests, as described in the USB 4.0 Electrical Compliance Test Specification. Figure taken from [25].

Second Test Setup, described in Fig. 3.5, is used for tests at TP3 (described in section 3.1 Rx Compliance Test Specification).

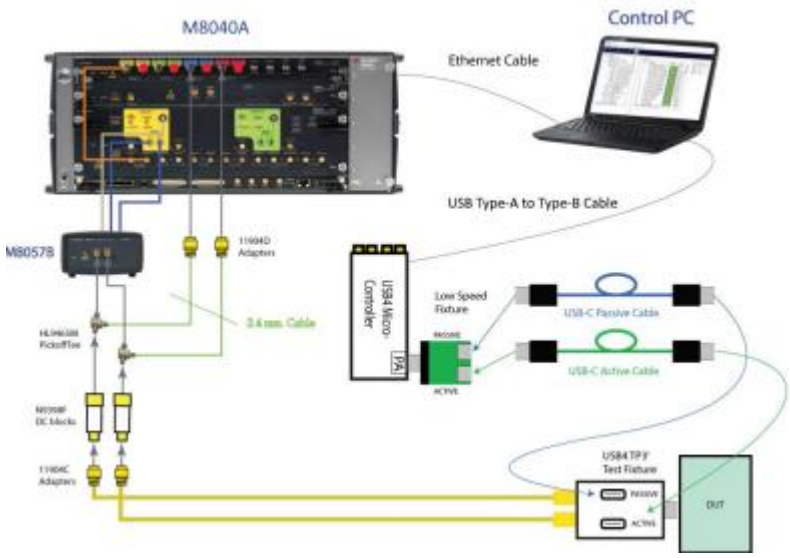


Fig. 3.5 Setup for Receiver at TP3 tests, as described in the USB 4.0 Electrical Compliance Test Specification. Figure taken from [25].

3.3. Tx Compliance Test Specification

Tx compliance testing is essential for ensuring that the transmitter in a USB 4.0 host/device meets the required electrical standards, its purpose is to verify that the electrical signals transmitted by the host/device adhere to the USB 4.0 specifications, ensuring interoperability, signal integrity, and reliable data transfer across various USB 4.0 capable devices and cables.

It involves measuring jitter to prevent data errors, assessing the eye diagram for signal quality, and verifying rise and fall times to avoid inter-symbol interference. Additionally, it ensures that voltage levels are within specified ranges to prevent issues like insufficient signal strength or excessive power consumption. Signal integrity parameters such as return loss, common mode voltage, and differential mode voltage are evaluated to ensure robust data transmission. Frequency and phase deviations are also checked to maintain signal integrity during clock changes.

Transmitter compliance testing is performed at TP2 using a "golden" plug fixture and at TP3 using a "golden" receptacle fixture. As described in Fig. 3.1, TP2 refers to the measurement

point located at the Type-C plug connected to the Tx output, while TP3 denotes the measurement point at the Type-C receptacle output. All measurements are referenced to the TP2/TP3 compliance points [22]. Table IV provides an overview of the various transmitter compliance tests that are essential for achieving certification.

TABLE IV
USB 4.0 TRANSMITTER COMPLIANCE TESTS

Speed	Test category name	Set of tests under category
10Gbps and 20Gbps	Tx Rise/Fall time	Tx rt
		Tx fl
	Tx Jitter	Tx uncorrelated jitter
		Tx uncorrelated deterministic jitter
		Tx data dependent jitter
		Tx duty cycle distortion
		Tx low frequency uncorrelated deterministic jitter
		Tx total jitter
		Tx uncorrelated jitter TP3
		Tx total jitter TP3
		Tx eye diagram TP3
	Tx unit interval and SSC modulation	Tx minimum unit interval, min
		Tx minimum unit interval, max
		Tx Spread Spectrum Clocking minimum down-spread rate
		Tx Spread Spectrum Clocking maximum down-spread rate
		Tx Spread Spectrum Clocking minimum down-spread range
		Tx Spread Spectrum Clocking maximum down-spread range
		Tx Spread Spectrum Clocking slew-rate
		Tx Spread Spectrum Clocking phase deviation
	Tx TP2 Eye diagram	Tx TP2 Eye diagram
	Tx AC Common mode voltage	Tx AC Common mode voltage
	Tx electrical idle voltage	Tx electrical idle voltage
	Tx equalization	Tx equalization preshoot
		Tx equalization deemphasis
		Tx swing preset 15
	Tx frequency variation training	Tx frequency variation training
	Tx return loss measurement	Tx differential return loss
		Tx common mode return loss
	Rx return loss measurement	Rx differential return loss
		Rx common mode return loss

3.3.1 Rise/Fall Time

Rise/fall time tests for transmitter compliance involve measuring the time it takes for a signal to switch from a low to a high state (rise time) and from a high to a low state (fall time). The importance of these tests lies in verifying that the transmitter can generate signals that meet the required timing characteristics, which is important for maintaining the integrity of the signal and ensuring proper communication between devices. If the transitions are too fast or too slow, it can cause signal distortion, increased error rates, and communication failures. Therefore, verifying that the rise/fall times are within the acceptable range is essential for reliable and efficient data transmission in USB 4.0 systems.

During the tests, the differential signal's voltage is monitored, and the times for the transitions between 20% and 80% of the voltage swing are measured. If these measured times are less than TX_FREQ_VARIATIONS_TRAINING value in Appendix C, the test fails, indicating non-compliance [22].

Fig. 3.6 Example of a 100kHz square signal, describing Rise Time and Fall Time measurements of the 20% to 80% swing voltage.

3.3.2 Jitter

The objective of this test is to verify that the transmitter's total jitter, including uncorrelated jitter (deterministic and random components), data-dependent jitter, low-frequency uncorrelated deterministic jitter, duty cycle distortion jitter, and eye diagram, all comply with the USB 4.0 Specification limits, described in appendix E for Gen 2 and appendix F for Gen 3 [24].

Jitter refers to the deviation or displacement of pulse timing in a high-frequency digital signal, representing the temporal variation of a signal's edges from their ideal positions. It can be caused by factors such as electromagnetic interference, crosstalk, power supply noise, and other internal and external noise sources. Fig. 3.7 describes the expected transmitted signal compared to the actual received waveform, affected by the interpreted waveform, which is affected by jitter.

Jitter affects the integrity of the transmitted signal. Excessive jitter can lead to data corruption, where the receiver may misinterpret the data being sent. By ensuring that jitter remains within specified limits, the signal integrity can be maintained, leading to reliable data transmission.

Total jitter is decomposed into deterministic and random jitter. It involves measuring total jitter using a digital oscilloscope with specialized software. Deterministic jitter, which is predictable and repeatable, includes data-dependent and periodic jitter, caused by bit patterns and periodic interference. Random jitter, which is unpredictable and follows a Gaussian distribution, is typically caused by thermal noise and other random effects, characterized by its RMS value. Fig. 3.8 describes the different compositions of jitter [27].

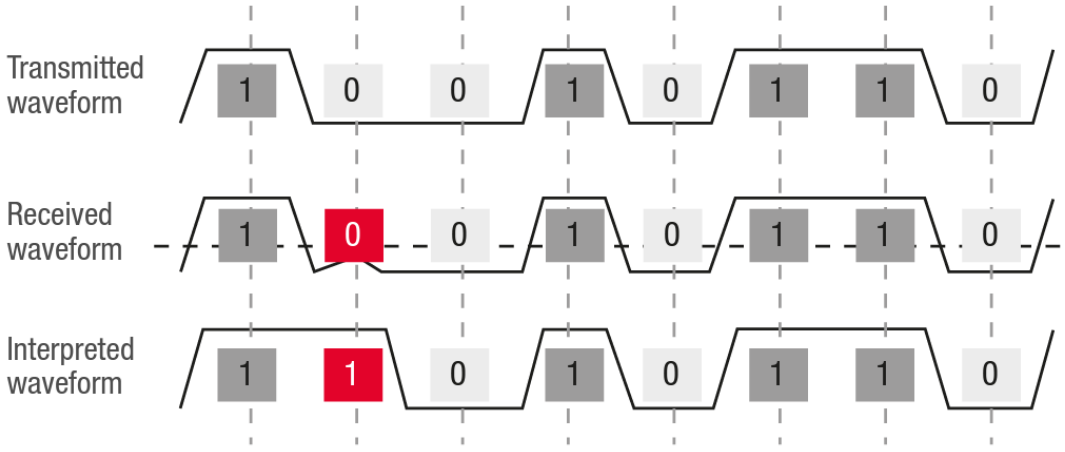


Fig. 3.7 Example of a signal with jitter, which can cause a receiver to misinterpret transmitted digital data. Figure taken from [26].

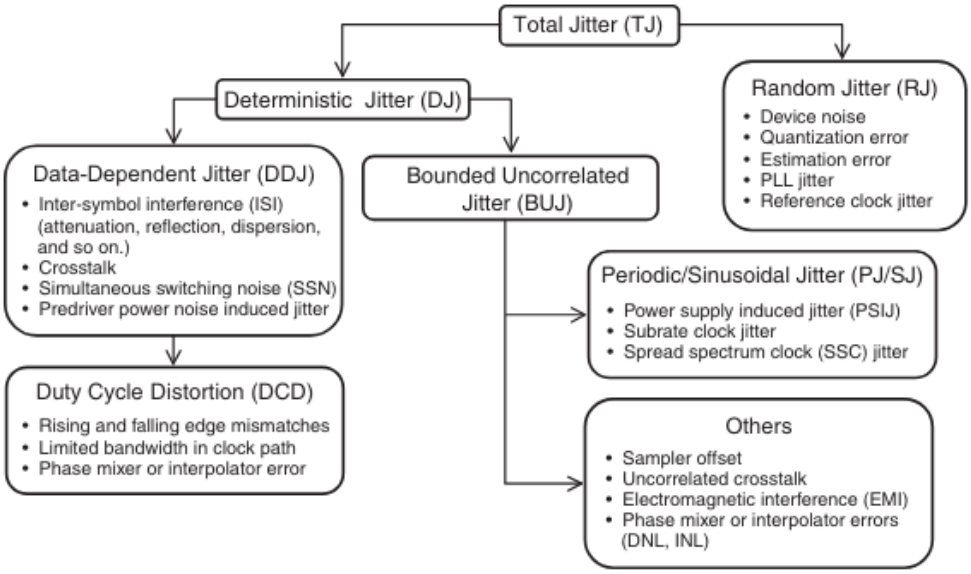


Fig. 3.8 Total Jitter Component Decompositions (Deterministic Jitter and Random Jitter). Figure taken from [27].

3.3.3 Unit Interval and Spread Spectrum Modulation

Unit Interval (UI) tests are designed to verify that the mean and minimum unit intervals of the transmitter are within specified limits, described in Appendix E for Gen 2 and Appendix F for Gen 3, ensuring that the data rate does not exceed the defined minimum or maximum limits [24]. These tests are crucial for maintaining data integrity and signal quality, as a stable and consistent UI prevents timing errors that can lead to data corruption and communication failures.

The UI denotes the duration of a single clock cycle and, for NRZ or NRZI encoded data, corresponds to the minimum time the transitions take in the serial data [28]. This is illustrated in Fig. 3.9, which shows the data of an NRZI signal alongside the associated clock ticks.

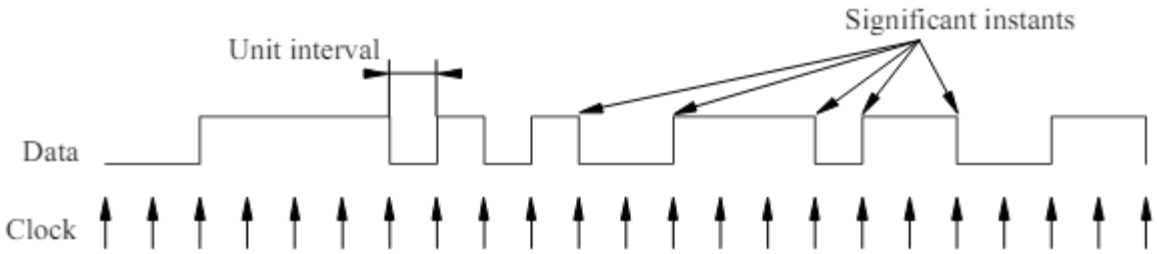


Fig. 3.9 Relationship of data and clock for SDI (Serial Digital Interface) signals showing unit interval and significant instants. Figure taken from [28].

SSC tests, on the other hand, verify that the link clock down-spreading modulation rate and depth are within specified limits, monitoring parameters such as SSC phase deviation, slew rate, downspread rate, and range [22]. The purpose of SSC is to reduce electromagnetic interference by spreading the signal energy over a wider frequency range, ensuring compliance with EMI regulations and reducing the risk of interference with other electronic devices.

3.3.4 Test Point 2 Eye Diagram

An eye diagram is a powerful tool used in digital communications to visualize the quality of a signal in a high-speed digital transmission system. It is created by repeatedly sampling a pseudorandom bit stream, using the clock reference as the trigger point, and overlaying each received cycle on the previous one; this results in a pattern that resembles an open eye. The eye opening in the diagram indicates the time interval where the signal can be sampled without error, suggesting better signal quality and less timing jitter. Conversely, the eye closure indicates signal degradation caused by noise, inter-symbol interference (ISI), or other distortions [29].

The purpose of the Tx Test Point 2 Eye Diagram is to assess the quality of the differential signal transmitted over each USB 4.0 differential lane. The objective is to confirm that the differential signal on each lane has an eye opening that meets the limits described in the USB 4.0 Electrical Specification, this is performed by comparing the measured data eye to the TP2 eye diagram mask, this way, manufacturers can identify and rectify any signal degradation issues, ensuring reliable and high-performance data transfer [22].

Fig. 3.10 below illustrates the eye mask described in the USB 4.0 Electrical Specification.

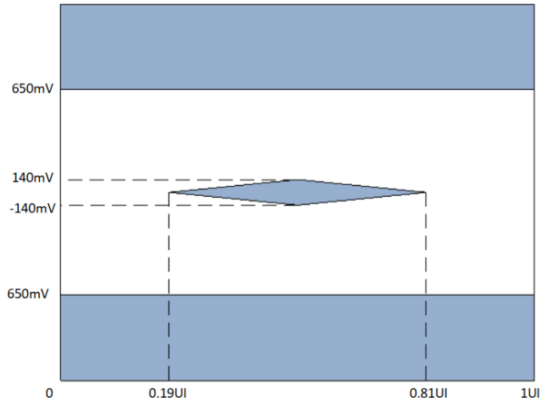


Fig. 3.10 Pass Condition for Tx Test Point 2 Eye Diagram Tests as described in the USB 4.0 Electrical Specification. Figure taken from [22].

3.3.5 AC Common Mode Voltage

The AC common voltage refers to the voltage level that is common to both the positive and negative terminals of a differential signal, in this case, the USB 4.0 Tx_p and Tx_n signals. In high-speed digital communication systems, differential signaling is often used to improve noise immunity and signal integrity. Fig. 3.11 illustrates an example.

The AC Common Mode Voltage Transmitter Test for USB 4.0 involves measuring and confirming that the common mode voltage on the transmitter differential signals fall within the specified limits of the USB 4.0 Electrical Specification [22], described in appendix E for Gen 2 and appendix F for Gen 3, ensuring that it meets the necessary standards for reliable and efficient data transmission, the importance of this test resides in that excessive common mode voltage can lead to electromagnetic interference (EMI) issues and signal distortions, which can degrade the performance of USB 4.0 devices and hosts.

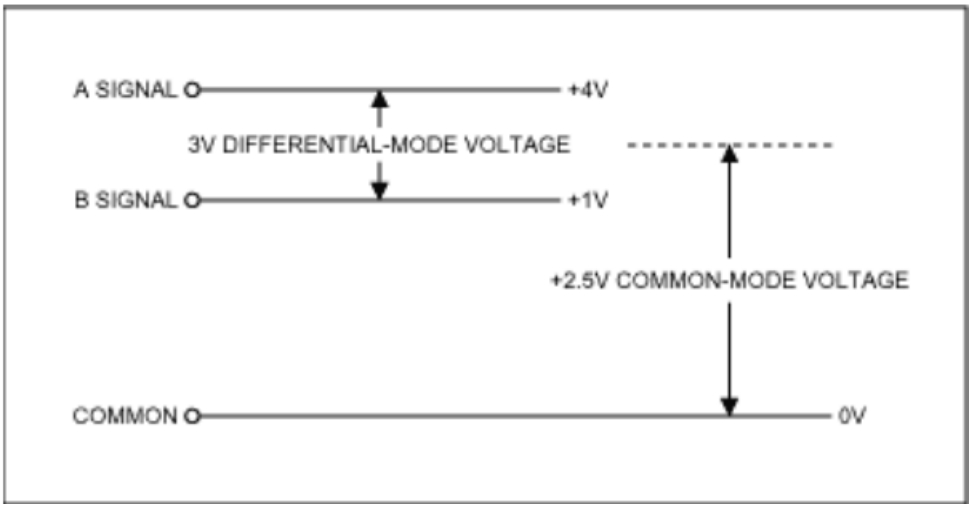


Fig. 3.11 Common-mode DC offset voltage, technically, the common-mode voltage is one-half the sum of the amplitude of the differential signals. Figure taken from [30].

3.3.6 Electrical Idle Voltage

The electrical idle state in USB 4.0 is a low-power, inactive state of the transmitter characterized by minimal differential signal voltage, meaning no data is being transmitted, it helps to maintain proper power management.

Idle packets are sent in order to have a continuous byte stream provided to the logical layer while no other packets are being transmitted. USB 4.0 has different power management states, called CL0s, CL1, and CL2 Low Power states, and are an important feature to minimize transmitter and receiver power consumption when a Lane is idle [9].

This test verifies that the differential signal voltage during electrical idle, according to the USB 4.0 electrical specification, is less than or equal V_ELEC_IDLE value described in appendix C [22]. This ensures that the transmitter is indeed in an idle state without transmitting any active data.

Fig. 3.12 below is an example of a transmitted signal, a typical implementation for transitioning from LFPS (Low Frequency Periodic Signal) via electrical idle to USB 4.0 data.

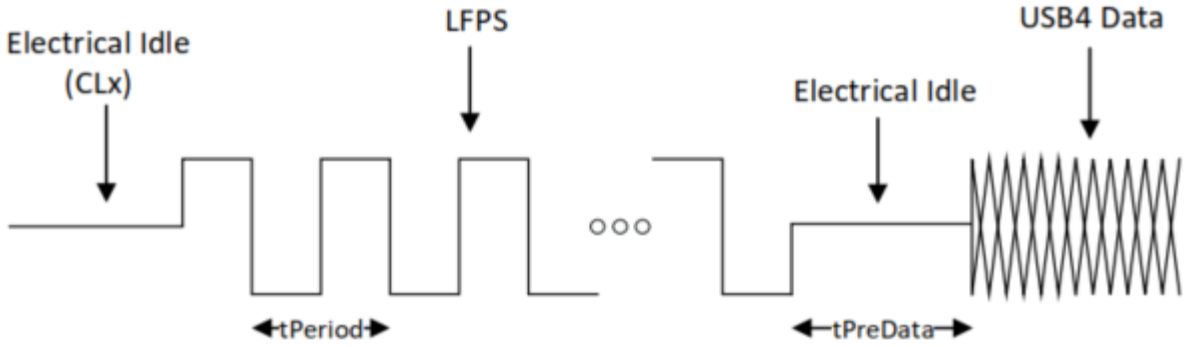


Fig. 3.12 Example of a USB 4.0 transmitted signal transitioning from LFPS to USB 4.0 data via electrical idle, where tPeriod refers to the period of the LFPS cycle and tPreData is the time in which electrical-idle shall be set. Figure taken from [9].

3.3.7 Transmitter Equalization

The transmitter equalization tests in USB 4.0 are designed to verify that the transmitter's equalization is compliant with the USB 4.0 Electrical Specification. The tests are divided into three categories: Tx Equalization Preshoot, Tx Equalization Deemphasis, and Tx Swing Preset 15 [22].

The equalizer is a 3-tap UI-spaced finite-impulse-response (FIR) filter as shown in Fig. 3.13. The transmitted level (tx_out_n) shall be generated as follows (3-1) [9]:

$$tx\_out_n = \sum_{k=-1}^{1} data\_in_{n-k} \bullet C_k \tag{3-1}$$

Where:

- tx_out_n is the transmitted level at time instant n
- $data\_in_{n-k}$ is the data symbol at time instant n-k (may be +1 or -1)
- Ck is the kth coefficient of the FIR filter

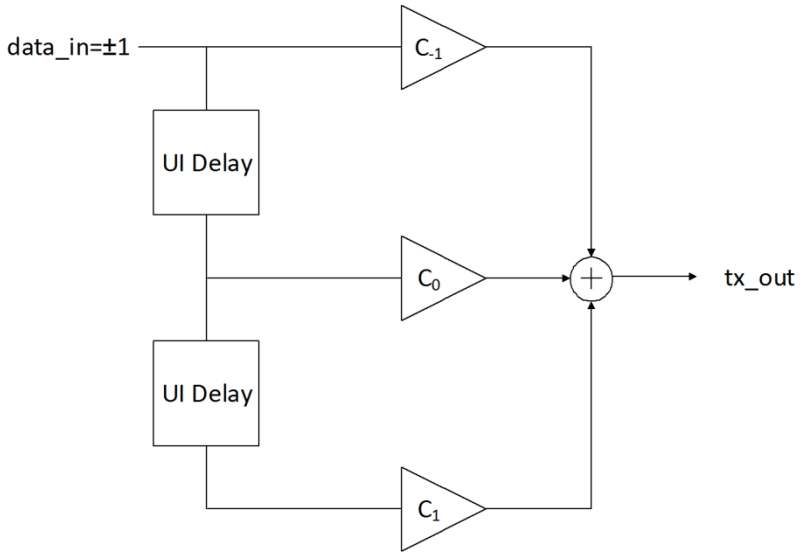


Fig. 3.13 Tx equalizer based on a 3-tap UI-spaced finite-impulse-response (FIR). Figure taken from [9].

Pre-shoot and de-emphasis are important concepts for USB 4.0 transmitter equalization. Pre-shoot is a technique used to improve signal quality by boosting the signal before a transition,

counteracting inter-symbol interference (ISI), while De-emphasis reduces the amplitude of the signal after a transition, minimizing distortion.

Transmitter equalization presets and their corresponding filter coefficients adjust the pre-shoot and de-emphasis levels to shape the transmitted signal for optimal performance. Each preset configuration involves specific coefficient values that define the pre-shoot and de-emphasis levels.

The values are calculated based on the steady-state voltages obtained with different tap configurations of the FIR transmitter equalizer.

Fig. 3.14 shows the waveform of a de-emphasized signal, where the signal's amplitude is reduced after one Unit Interval (UI).

TABLE V
USB 4.0 TRANSMITTER EQUALIZER (FIR) PRESETS.
TABLE TAKEN FROM [13].

Preset Number	Pre-shoot [dB]	De-emphasis [dB]	Informative Filter Coefficients		
			C_{-1}	C_0	C_1
0	0	0	0	1	0
1	0	-1.9	0	0.9	-0.1
2	0	-3.6	0	0.83	-0.17
3	0	-5	0	0.78	-0.22
4	0	-8.4	0	0.69	-0.31
5	0.9	0	-0.05	0.95	0
6	1.1	-1.9	-0.05	0.86	-0.09
7	1.4	-3.8	-0.05	0.79	-0.16
8	1.7	-5.8	-0.05	0.73	-0.22
9	2.1	-8	-0.05	0.68	-0.27
10	1.7	0	-0.09	0.91	0
11	2.2	-2.2	-0.09	0.82	-0.09
12	2.5	-3.6	-0.09	0.77	-0.14
13	3.4	-6.7	-0.09	0.69	-0.22
14	3.6	0	-0.17	0.83	0
15	1.7	-1.7	-0.05	0.55	-0.05

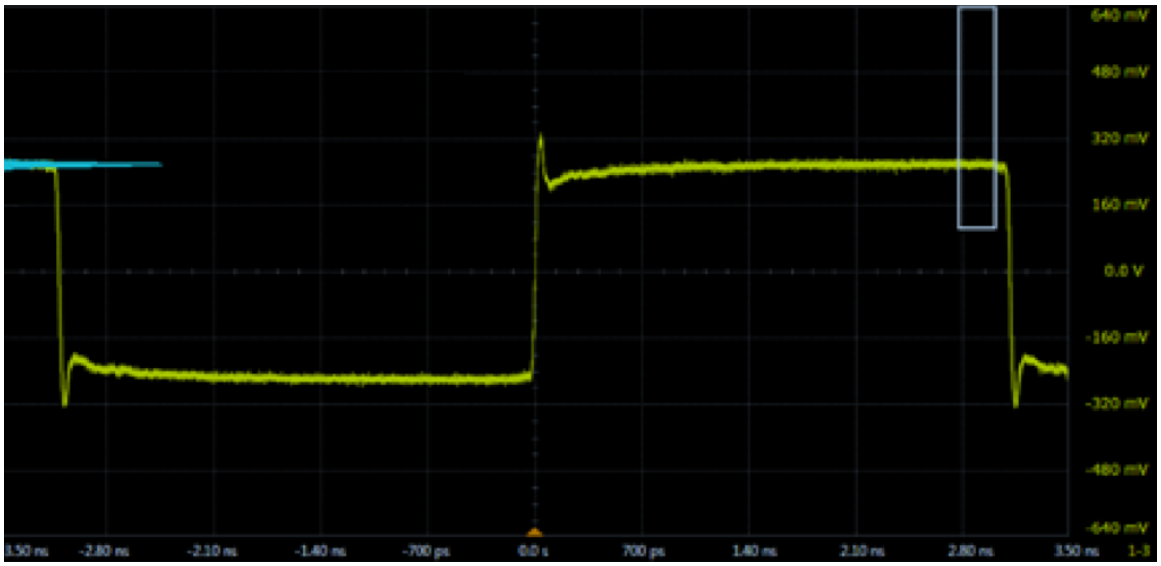


Fig. 3.14 USB 4.0 square pattern without pre-shoot and with de-emphasis. Figure taken from [22].

Fig. 3.15 on the other hand, shows the waveform of a signal with pre-shoot that boosts the signal before a transition.

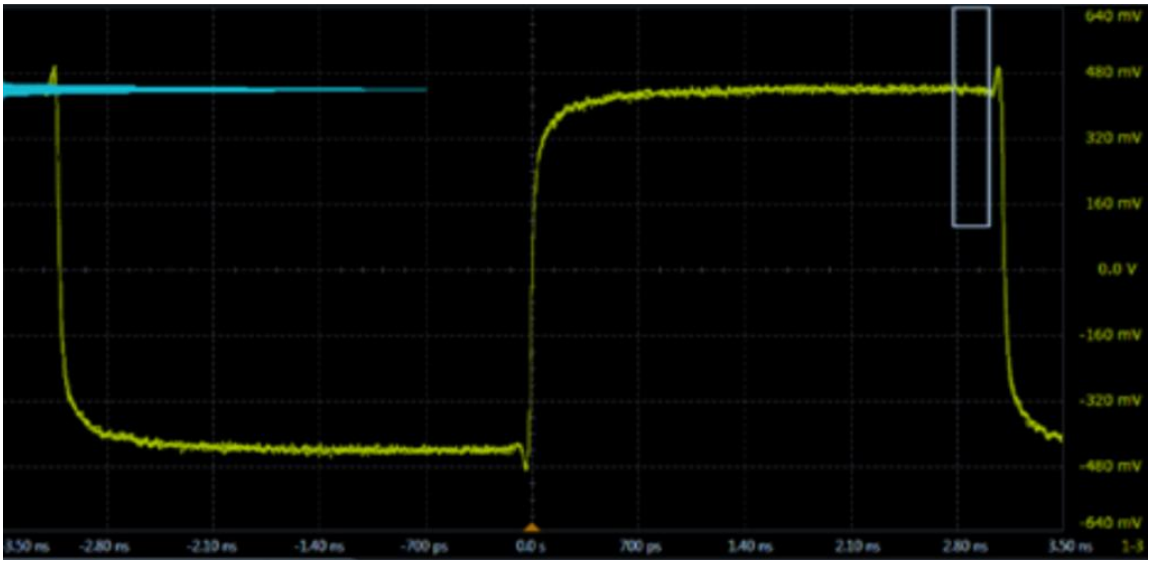


Fig. 3.15 USB 4.0 square pattern with pre-shoot and without de-emphasis. Figure taken from [22].

3.3.8 Frequency Variation Training

This test specifically assesses the behavior of the transmitter frequency during the link training process, especially in the presence of Re-timers [22].

A USB 4.0 Link can include up to 6 Re-timers, which forward data from one end of the Link to the other end, Re-timers play a critical role in maintaining signal integrity over longer distances and through multiple connectors; they help to regenerate the signal, correcting any degradation that occurs during transmission.

All Re-timer transmitters are initially clocked at a local constant frequency, they do not forward the incoming data but instead send a predetermined ordered set, as the link training progresses, Re-timers switch to forwarding the incoming data, this transition is done sequentially, ensuring synchronization across the link.

Once all Re-timers have switched to the incoming frequency, the system reaches a steady state, at this point, the data is forwarded with SSC, maintaining the integrity and proper timing of the signal [9].

Fig. 3.16 describes the transmitter frequency variation during training, also described in the TX_FREQ_VARIATIONS_TRAINING value in Appendix C, starting from the data transmission using the local clock, then the re-timer switches to use the recovered clock, and when recovered, starts the steady-state operation.

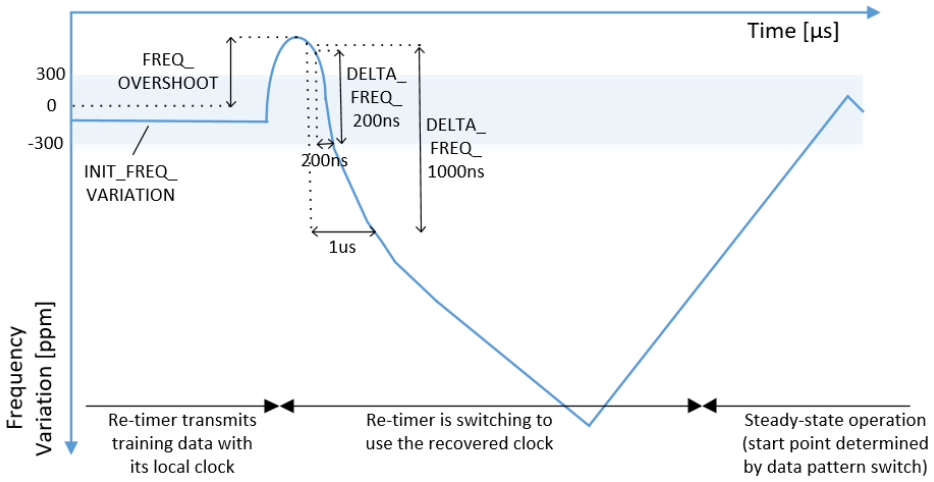


Fig. 3.16 Router Assembly Transmitter Frequency Variation During Training. Figure taken from [9].

3.3.9 Transmitter and Receiver Return Loss Measurement

I/O return loss is a very important parameter that is part of several electrical specifications for high-speed digital interfaces. It assesses the performance of their transmitter and receiver transmission lines. It measures the signal energy reflected at package pins due to impedance mismatches between the test fixture or connector and the DUT's I/O impedance.

Some factors that can contribute to return loss degradation can be the capacitive discontinuities caused by parasitic capacitance from on-chip drivers or receivers, Electrostatic Discharge (ESD) diodes and wiring, as well as the packaging [31].

The purpose of the Transmitter (Tx) and Receiver (Rx) return loss measurement in USB 4.0 is to evaluate the quality of signal reflections at the ports of the USB 4.0 device/host. The Tx return loss measurement involves sending a signal through the Tx port and quantifying the reflected signal that returns to the Tx port, ensuring that the transmitter is not reflecting excessive amounts of signal power towards itself, which could degrade signal quality and affect communication reliability. Similarly, the Rx return loss measurement involves sending a signal to the Rx port and measuring the reflected signal coming back from the Rx port, ensuring that the receiver can accept signals with minimal reflection, maintaining clear signal reception, and reducing potential data errors.

Return loss is defined by the equation (3-2):

$$R_L|dB| = 20\log\left|\frac{Z_L - Z_O}{Z_L + Z_O}\right| \tag{3-2}$$

Where:

- Z_L is the load impedance at the receiver input or transmitter output
- Z_0 is the impedance of the transmission line feeding the input signal to the receiver or transmitter [31]

For USB 4.0, transmitter (SDD22) and receiver (SDD11) differential return-loss measurements shall be referenced to a single-ended impedance of 42.5 Ω, the differential mode return loss limits are described by the equation (3-3) for transmitter and (3-4) for receiver [22]:

$$SDD22(f) = \begin{cases} -8.5 & 0.05 < fGHz \leq 3 \\ -3.5 + 8.3 * \log_{10}(\frac{fGHz}{12}) & 3 < fGHz \leq 12 \end{cases} \quad (3\text{-}3)$$

$$SDD11(f) = \begin{cases} -8.5 & 0.05 < fGHz \leq 3 \\ -3.5 + 8.3 * \log_{10}(\frac{fGHz}{12}) & 3 < fGHz \leq 12 \end{cases} \quad (3\text{-}4)$$

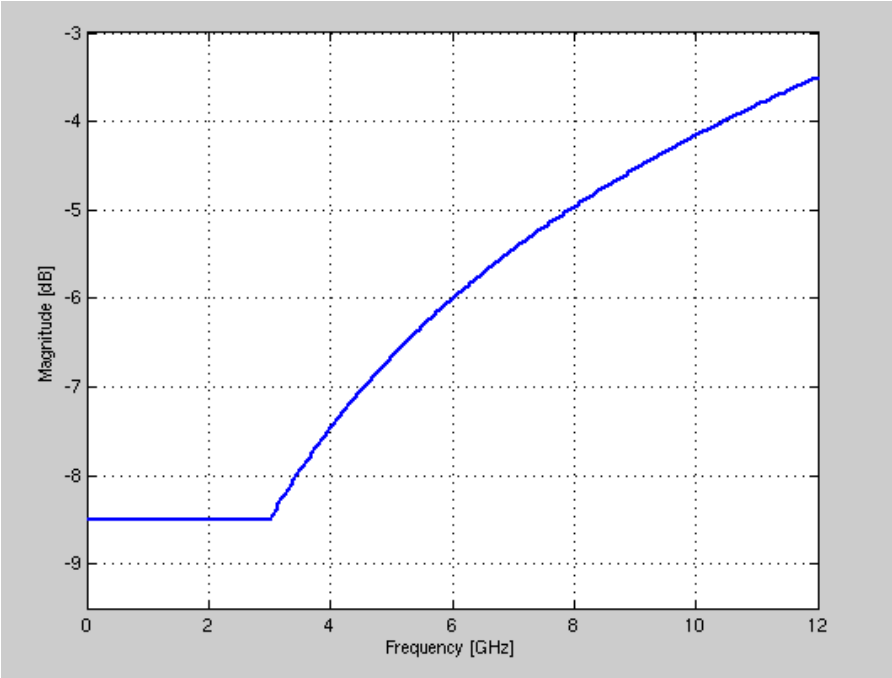


Fig. 3.17 Transmitter and Receiver Differential Return Loss Mask described by the equation (3-3) and (3-4). Figure taken from [22].

The common-mode return loss should comply with the limits described in equation (3-5) for transmitter and (3-6) for receiver [22]:

$$SCC22(f) = \begin{cases} -6 & 0.05 < fGHz \leq 2.5 \\ -3 & 2.5 < fGHz \leq 12 \end{cases} \quad (3\text{-}5)$$

$$SCC11(f) = \begin{cases} -6 & 0.05 < fGHz \leq 2.5 \\ -3 & 2.5 < fGHz \leq 12 \end{cases} \quad (3\text{-}6)$$

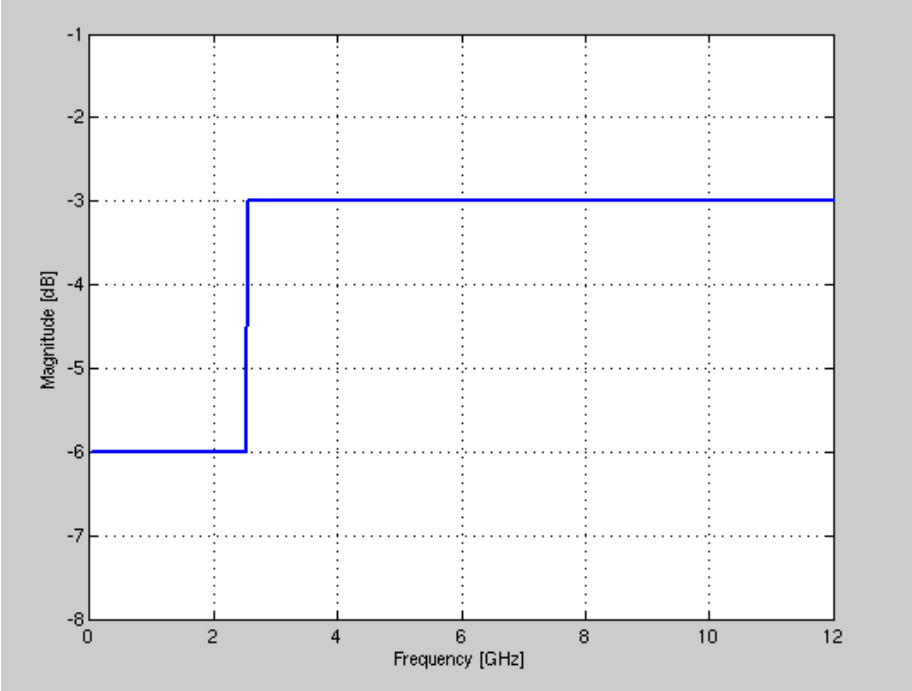


Fig. 3.18 Transmitter/Receiver Common-Mode Return Loss Mask described in equation (3-5) and (3-6). Figure taken from [22].

3.4. Tx Compliance Test Setup

USB 4.0 transmitter testing requires several instruments for an appropriate evaluation of the host/device, a high-performance real-time oscilloscope with a sampling rate of 50 GSa/s or greater on two channels simultaneously and 50 M samples of memory per channel is needed, its job is to capture the electrical signals transmitted by the DUT and allow for detailed analysis to ensure they meet USB 4.0 electrical specification requirements [24].

Additionally, for easier and faster validation, a compliance test software is required that automates the execution of various transmitter tests, ensuring consistency and accuracy, and provides reports of test results, including waveform analysis to show the pass or fail margins for each test [32].

In order to test the transmitter signals, test fixtures are used, which are the physical hardware setups that provide a standardized environment, ensuring consistent and repeatable connections between the DUT and the testing equipment, such as the oscilloscope. These fixtures

simulate the actual USB 4.0 connection environment and maintain the correct impedance and signal integrity required for high-speed transmissions.

Test fixtures are utilized alongside a microcontroller, which is responsible for controlling and managing the test process. It interacts with both the DUT and the test equipment to automate test sequences, manage power supply, apply test patterns, and control the timing and synchronization of test signals. Microcontrollers aid in the collection and processing of test data, ensuring that tests are conducted in accordance with USB 4.0 specifications and compliance requirements.

Together, the oscilloscope, automation software, test fixtures, and microcontrollers ensure accurate, reliable, and standardized compliance testing for USB 4.0 transmitters. Fig. 3.19 below shows how the physical setup should be connected.

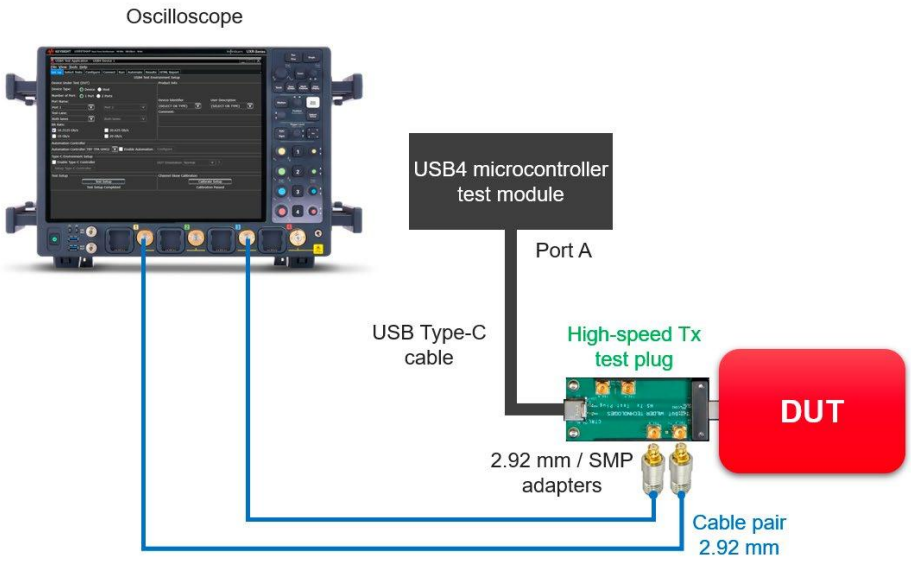


Fig. 3.19 Transmitter compliance test setup for Test Point 2 and Test Point 3 tests. Figure taken from [32].

3.5. Results

The results of transmitter and receiver compliance tests are presented in reports generated by the respective test application. These reports can be viewed, exported, and printed, and they include detailed test results, observable data, and pass/fail outcomes.

For transmitter tests, the results include metrics like jitter, eye diagrams, unit interval measurements, and equalization settings. Each test group, such as Tx Uncorrelated Jitter, Tx Data Dependent Jitter, and Tx Eye Diagram, would have specific results displayed.

For receiver tests, the results shown include various test points like TP3 and TP3', and they describe the data such as jitter tolerance, signal frequency variations, and bit error rate (BER). The results indicate whether the DUT meets the compliance specifications.

In the USB 4.0 Automated Test Application, the results are presented in a summary format, with detailed sections for each test performed. The application also provides tools for generating HTML reports for further analysis and documentation.

Overall, the test application provides a comprehensive view of compliance test results, ensuring that all relevant data is accessible for verification and validation.

As for the Receiver compliance test, there are different results reports:

- Rx compliance test at TP3 (case 1) and Rx compliance test at TP3’ (case 2).
- Rx frequency variations test at TP3 and TP3’.

When completed, the Receiver compliance test at TP3 and TP3' generates a summary described in Fig. 3.20 and Fig. 3.21 that includes the results of tests previously conducted under identical conditions, except for the jitter frequencies. For instance, a summary would be created for Gen 2 at TP3' with jitter frequencies of 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz [33].

RxCompTestSum L0 10 TP3'

[Not Compliant]

USB4 USB4_Router_Assembly

----General----	
Offline	True
Software Version	3.5.0.17
Compliant	False
Non-compliance reason(s)	Procedure offline
----General----	
Full PG initialization only once per test block?	True
----Generator----	
Pattern	PRBS31
SSC	True
SSC Amplitude downwards	-5300 ppm
SSC Amplitude upwards	300 ppm
SSC Frequency	32 kHz
----Spec Values----	
Total Jitter	350 mUI
Eye Height	700 mV
Random Jitter	140 mUI
Periodic Jitter	170 mUI
AC CM Amplitude	100 mV
AC CM Frequency	400 MHz
----BER Test----	
Error Detector Type	USB4 ElectricalTestTool
USB4 ETT Executable	C:\USB4ETT\USB4ElectricalTestTool
Script Run Location	Local
Request user interaction if linktraining fails	False
Reset DUT	Once per test procedure
Bus powered device	False
Wait after InitScript	0 s
----Instruments----	
Data Generator	Name: Keysight M8040A J-BERT ; C
AcCm Source	M8054A/M8195A

Fig. 3.20 Receiver compliance test summary – Description of the calibrated test parameters. Figure taken from [33].

Result	PJ Frequency [MHz]	AC CM Set Amplitude [mV]	PRBS Set Amplitude [mV]	RJ Set Value (RMS) [mUI]	PJ Set Value [mUI]	Final Preset Value	3 Injected Errors Check	Negotiation Checks	Component	Errors 1st Run	Symbol count 1st Run	Errors 2nd Run	Symbol count 2nd Run
pass	1	131	876	9.50	2125	11	Pass (3 of 3)	4	Router Retimer1	0 0	2500000000 2530850000	-	-
pass	2	131	876	8.70	680	10	Pass (3 of 3)	4	Router Retimer1	0 0	2500000000 2530850000	-	-
pass	10	131	876	11.10	173	6	Pass (3 of 3)	4	Router Retimer1	0 0	2500000000 2530850000	-	-
pass	50	131	876	11.10	173	8	Pass (3 of 3)	4	Router Retimer1	0 0	2500000000 2530850000	-	-
pass	100	131	876	6.40	225	14	Pass (3 of 3)	4	Router Retimer1	0 0	2500000000 2530850000	-	-

Fig. 3.21 Receiver compliance test summary – Results for each periodic jitter frequency. Figure taken from [33].

In Fig. 3.21, different values are shown that are set by following the electrical specification. Below is a description of the most informative and important parameters [33]:

- Result: Pass or fail according to specification limits.
- PJ Frequency: Frequency of the PJ applied.
- PRBS Set Amplitude: The differential voltage amplitude applied to the signal.
- RJ Set Value: Amount of applied random jitter.
- PJ Set Value [mUI]: Amount of PJ.
- Errors 1st/2nd Run: Number of detected bit errors.

The next receiver test is the Rx signal frequency variations training test at TP3 and TP3', which, when finished, creates a results report which contains the following information, illustrated in Fig. 3.22 and Fig. 3.23:

FreqVarTest L0 10G TP3a

[Not Compliant]

USB4 USB4_Router_Assembly

----General----	
Offline	True
Software Version	3.5.0.17
Required-calibration SW Version	3.5.0.17
Compliant	False
Non-compliance reason(s)	Procedure offline; Required cal 100MHz, Receiver Eye Diagram Cal Calibration, Random Jitter Calib
----General----	
Full PG initialization only once per test block?	True
Detected Retimers	1
Detected USB4 ETT version	1.1.2
----Generator----	
Pattern	PRBS31
SSC	True
SSC Amplitude downwards	-5300 ppm
SSC Amplitude upwards	300 ppm
SSC Frequency	32 kHz
----Spec Values----	
Total Jitter	350 mUI
Eye Height	700 mV
Random Jitter	140 mUI
Periodic Jitter	170 mUI
----BER Test----	
Error Detector Type	USB4 ElectricalTestTool
USB4 ETT Executable	C:\USB4ETT\USB4ElectricalTestToo
Script Run Location	Local
Request user interaction if linktraining fails	False
Reset DUT	Once per test procedure
Bus powered device	False
Wait after InitScript	0 s
----Instruments----	
Data Generator	Name: Keysight M8040A J-BERT ; C
AcCm Source	M8054A/M8195A

Fig. 3.22 Receiver signal frequency variations training test summary – Description of the calibrated test parameters. Figure taken from [33].

Result	Repetition	Final Preset Value	Component	ERRCTR	DWCTR	BER
pass	1	15	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	2	7	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	3	6	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	4	11	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	5	13	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	6	2	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	7	2	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	8	8	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	9	3	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	10	8	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	11	13	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	12	5	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	13	1	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	14	12	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	15	9	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	16	14	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	17	3	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	18	6	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	19	4	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0
pass	20	15	Router Retimer1	0 0	3259736094 3299961237	0.0e0 0.0e0

Fig. 3.23 Receiver signal frequency variations training test summary – Results for each repetition. Figure taken from [33].

In Fig. 3.23, different values are shown that are set by following the electrical specification. Below is a description of the most informative and important parameters [33]:

- Result: Pass or fail according to specification limits.
- Component: Specifies which retimer is tested.
- BER: The result of the BER test.

As for transmitter, when the Automated Test Application finishes performing test runs, the results of all selected tests are displayed in the application Results tab, some parameters shown are test indicators, pass/fail limits, trials, and reference images such as eye diagrams, signal waveforms, etc.

As shown in Fig. 3.24, the upper pane displays a summary of each test that was selected to run in a project; the most important elements of the test results displayed are:

- Test Name: It shows the name of the test run.

- Actual value: The value obtained when the waveforms are post-processed and analyzed by the application.
- Margin %: How much margin is left until the test starts failing, according to values described in the electrical compliance test specification.
- Pass Limits: Limits specified in the CTS for each test.
- # Trials: How many times the specified test was run.

Every time a test is executed on the test application, it produces a test report in HTML format, which can be accessed under the HTML Report tab. This Test Report, shown in Fig. 3.25, systematically presents the configuration data followed by the resulting information [34].

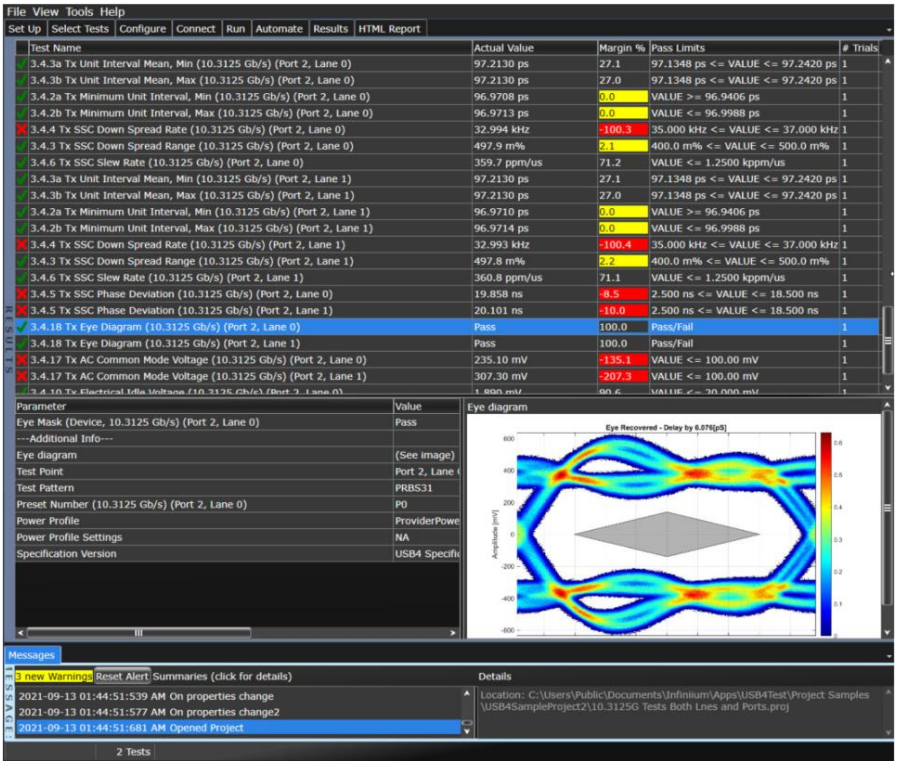


Fig. 3.24 USB 4.0 Automated Transmitter Compliance Application results tab, showing a summary of the results and specified limits of the tests ran. Figure taken from [34].

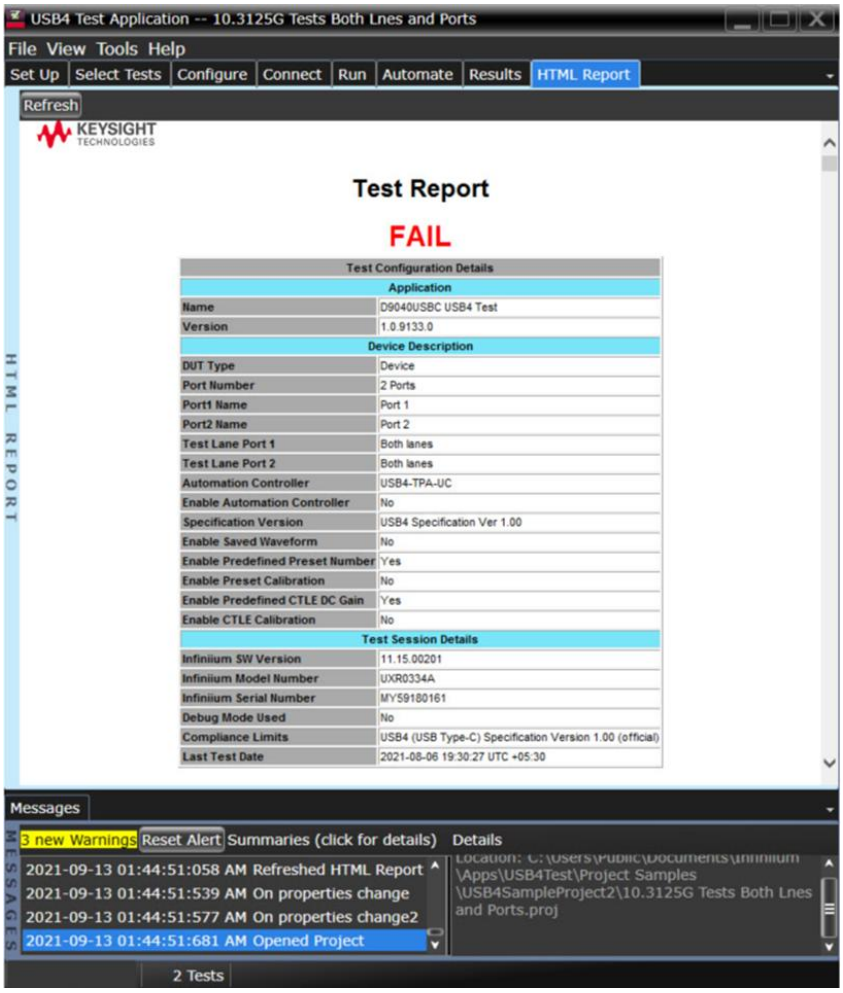
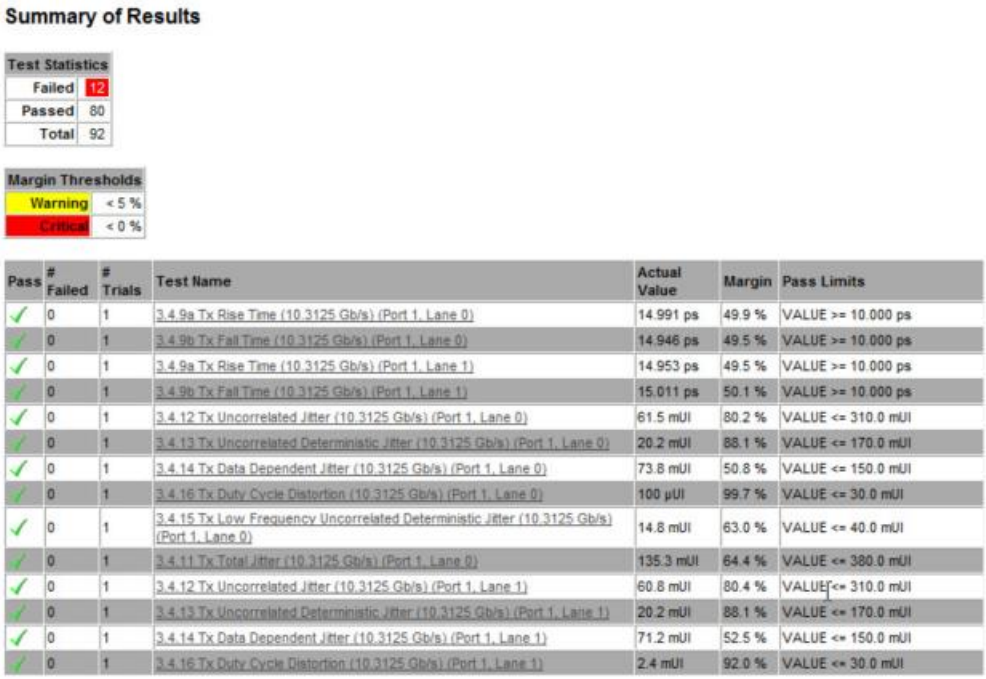


Fig. 3.25 Transmitter compliance HTML results report under "HTML Report" tab. Figure taken from [34].

The Overall Result indicates whether the current set of test runs has passed or failed; even if one trial of a test does not meet the defined specifications, this field will display FAIL.

The HTML Report is divided into different sections. The top section contains the report header, which provides an overview of the most recent test run and the parameters configured within the Test Application.



Summary of Results

Test Statistics	
Failed	12
Passed	80
Total	92

Margin Thresholds	
Warning	< 5 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	3.4.9a Tx Rise Time (10.3125 Gb/s) (Port 1, Lane 0)	14.991 ps	49.9 %	VALUE >= 10.000 ps
✓	0	1	3.4.9b Tx Fall Time (10.3125 Gb/s) (Port 1, Lane 0)	14.946 ps	49.5 %	VALUE >= 10.000 ps
✓	0	1	3.4.9a Tx Rise Time (10.3125 Gb/s) (Port 1, Lane 1)	14.953 ps	49.5 %	VALUE >= 10.000 ps
✓	0	1	3.4.9b Tx Fall Time (10.3125 Gb/s) (Port 1, Lane 1)	15.011 ps	50.1 %	VALUE >= 10.000 ps
✓	0	1	3.4.12 Tx Uncorrelated Jitter (10.3125 Gb/s) (Port 1, Lane 0)	61.5 mUI	80.2 %	VALUE <= 310.0 mUI
✓	0	1	3.4.13 Tx Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 1, Lane 0)	20.2 mUI	88.1 %	VALUE <= 170.0 mUI
✓	0	1	3.4.14 Tx Data Dependent Jitter (10.3125 Gb/s) (Port 1, Lane 0)	73.8 mUI	50.8 %	VALUE <= 150.0 mUI
✓	0	1	3.4.16 Tx Duty Cycle Distortion (10.3125 Gb/s) (Port 1, Lane 0)	100 µUI	99.7 %	VALUE <= 30.0 mUI
✓	0	1	3.4.15 Tx Low Frequency Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 1, Lane 0)	14.8 mUI	63.0 %	VALUE <= 40.0 mUI
✓	0	1	3.4.11 Tx Total Jitter (10.3125 Gb/s) (Port 1, Lane 0)	135.3 mUI	64.4 %	VALUE <= 380.0 mUI
✓	0	1	3.4.12 Tx Uncorrelated Jitter (10.3125 Gb/s) (Port 1, Lane 1)	60.8 mUI	80.4 %	VALUE <= 310.0 mUI
✓	0	1	3.4.13 Tx Uncorrelated Deterministic Jitter (10.3125 Gb/s) (Port 1, Lane 1)	20.2 mUI	88.1 %	VALUE <= 170.0 mUI
✓	0	1	3.4.14 Tx Data Dependent Jitter (10.3125 Gb/s) (Port 1, Lane 1)	71.2 mUI	52.5 %	VALUE <= 150.0 mUI
✓	0	1	3.4.16 Tx Duty Cycle Distortion (10.3125 Gb/s) (Port 1, Lane 1)	2.4 mUI	92.0 %	VALUE <= 30.0 mUI

Fig. 3.26 Transmitter compliance HTML results report under "HTML Report" tab - Summary of results. Figure taken from [34].

The Summary of Results section shown in Fig. 3.26, provides an overview of each test that was run [34]:

- Pass column: Indicates whether the tests passed or failed.
- Actual Value: Shows the actual case value across all trials.
- Margin: Displays the percentage of pass or fail, based on the electrical specification.

Finally, the Report Detail section shown in Fig. 3.27 shows the detailed parameters for each of the selected measurements.

Fig. 3.27 Transmitter compliance HTML results report under "HTML Report" tab - Report detail. Figure taken from [34].

Conclusions

The increasing demand for higher data rates is driving the development of new USB generations, which introduce new challenges in post-silicon validation. The complexity of new compliance tests, instruments, and electrical parameters in USB products is demanding extensive knowledge and understanding of signal integrity requirements for high-speed protocols during post-silicon validation, this is due that high frequency data rates are more susceptible to degradation caused by factors like attenuation, crosstalk, EMI, and reflections. To expedite the process for engineers to fully understand the electrical and compliance test specifications of USB 4.0, we propose a methodology guide for USB 4.0 Tx and Rx testing. This guide aims to help engineers quickly familiarize themselves with each parameter, required tests, recommended cables, fixtures, and instruments, enabling them to commence validation promptly and leverage the comprehensive research already conducted in this document. This approach ensures fast action while maintaining the high-quality assessment of the performance.

In order to prepare for the creation of this document, trainings sessions were held at our labs, presented by experts at USB 4.0, who are part of the USB Implementers Forum. These experts helped design the necessary fixtures and instruments required and to develop the test automation software for both receiver and transmitter validation. The training covered several topics, including an introduction to USB 4.0, differences in electrical compliance tests compared to its predecessor USB3.2, required equipment such as instruments, cables, fixtures, microcontrollers, adapters, software and licenses, how to install the software and usage, connection procedures for various test setups, test execution methods and understanding of the test results.

In chapter 1, a brief introduction to USB in general and some key and innovative points of USB 4.0 was presented. This overview is essential for understanding the significance of innovation within USB technology, how it has improved over the years and the rapid increase of data rates, and with it, new requirements for different connectors which must maintain backward compatibility with older USB versions while supporting faster data rates, and how this compatibility is achieved by adding new and more complex features to its architecture.

Chapter 2 presented the importance of signal integrity in high-speed interfaces, the challenges that emerge as data rates increase, the necessity of precise electrical specifications along

with stable, repeatable, and well-documented electrical compliance tests, which ensure high-quality certified USB 4.0 products. Certification guarantees interoperability, adds value, assures quality, aids in debugging and troubleshooting, and grants the right to use the logo and icon.

Finally, in chapter 3, all the required tests for certification were described; several tests are performed for both receiver and transmitter, which require different test points. Instruments, cables, fixtures, and software were briefly described, though specific equipment details were omitted for confidentiality. Diagrams of connection setups were provided to visually explain how the tests are performed, aiding the reader's understanding of all the described tests.

The test description and methodology presented in this thesis, together with the USB 4.0 validation documentation developed over the year, will allow to accelerate the process of electrical validation and certification. A potential future project could involve adding a series of test case recommendations under varying temperature and voltage conditions, as well as guidelines for setting up the testing environment. This would enhance the coverage of all the worst-case and best-case scenarios for signal integrity.

Appendix

A. DECISION CRITERIA FOR LANE ATRIBUTES DURING PHASE 3 OF LINK INITIALIZATION.

Please refer to “Table 4-30. Lane Attributes” described in the Universal Serial Bus 4 Specification in [9].

B. TXFFE TRANSMIT EQUALIZATION PRESETS FOR PHASE 5 IN LANE INITIALIZATION.

Please refer to “Table 3-4. Transmit Equalization Presets” described in the Universal Serial Bus 4 Specification in [9].

C. TRANSMITTER SPECIFICATIONS FOR GEN 2 AND GEN 3 (AT TP2).

Please refer to “Table 3-2. Transmitter Specifications for Gen 2 and Gen 3 (at TP2)” described in the Universal Serial Bus 4 Specification in [9].

D. TRANSMITTER FREQUENCY VARIATION LIMITS DURING LINK TRAINING BEFORE OBTAINING STEADY-STATE.

Please refer to “Table 3-3. Transmitter Frequency Variation Limits During Link Training Before Obtaining Steady-State” described in the Universal Serial Bus 4 Specification in [9].

E. GEN 2 TRANSMITTER SPECIFICATIONS AT TP2.

Please refer to “Table 3-5. Gen 2 Transmitter Specifications at TP2” described in the Universal Serial Bus 4 Specification in [9].

F. GEN 3 TRANSMITTER SPECIFICATIONS AT TP2.

Please refer to “Table 3-6. Gen 2 Transmitter Specifications at TP3” described in the Universal Serial Bus 4 Specification in [9].

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