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OPTIMIZATION OF DECOUPLING CAPACITORS IN POWER DELIVERY NETWORKS THROUGH CO-SIMULATION FOR ENHANCED SIGNAL AND POWER INTEGRITY

TESIS que para obtener el **GRADO** de
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TÍTULO: **Optimization of Decoupling Capacitors in Power Delivery Networks Through Co-Simulation for Enhanced Signal and Power Integrity**

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Dedication

I dedicated this thesis to my mother, Elena, and without her support and constant motivation, I would not have achieved everything I have in my life.

To my brother and sister, who have always been by my side and have never doubted me.

To my partner, who stayed with me from the beginning, by my side during my sleepless nights and moments when I felt time was not enough.

To God, trusting that He always has something better prepared for me and being my guide in my decisions.

Summary

This thesis presents a transient co-simulation approach to analyze signal and power integrity (SI-PI) in chiplet-based interconnect systems that comply with the Universal Chiplet Interconnect Express (UCIe) standard. The power delivery network (PDN) is modeled using an equivalent circuit, and the UCIe channel is represented as a black-box system characterized by S-parameters. UCIe, an open industry interconnect standard, enables the seamless integration of chiplets from multiple suppliers and functionalities into a single package, positioning it as a key technology that will define the future of semiconductor integration. This thesis focuses on optimizing the placement and number of decoupling capacitors at various stages of the PDN. These capacitors are crucial for maintaining voltage stability and reducing noise, thereby improving both signal integrity and power integrity. By employing a co-simulation technique, the thesis enables a comprehensive SI and PI analysis within a unified simulation framework, ensuring that voltage stabilization strategies directly contribute to improved signal performance. The main objectives of this thesis include developing a methodology to identify optimal decoupling capacitor configurations to improve signal integrity and reduce power-related noise, calculating the minimum number of decoupling capacitors based on PI and SI optimization parameters defined according to the UCIe Gen 1 specification, and integrating SI and PI analysis through a co-simulation framework that combines MATLAB and Keysight ADS. The proposed PDN optimization procedure exploiting SI-PI co-simulation is implemented by using several classical optimization methods: Nelder–Mead, quasi-Newton, and conjugate gradients, highlighting their relative advantages in terms of accuracy, convergence speed, and computational efficiency. This thesis provides a practical methodology for SI-PI co-design in UCIe-based systems and offers valuable insight into how optimizing power distribution can enhance signal quality in high-speed integrated architectures. The proposed methodology lays the foundation for more advanced co-design strategies in next-generation high-speed computer platforms, where performance, cost, and integration requirements must be balanced simultaneously.

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I would also like to express my gratitude to Intel Corporation for providing me with an academic scholarship and motivating me to pursue this master's degree. In addition, I also thank the agreement with ITESO, given my employment at Intel, which enabled me to achieve this goal.

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Introduction

In the constantly evolving landscape of high-speed and high-performance computer platforms, ensuring reliable signal transmission and stable power distribution has become critical to the success of modern technology, especially in interconnects and power distribution circuitry. As circuits continue to advance in complexity and speed, the signals carrying critical data have led to several types of issues. Power delivery networks (PDN), which supply voltage and current to all active devices, play a central role in this context. When the data speeds increase, signals are hampered by voltage noise generated in the power supply, this noise can impact the switching frequency of transistors in the devices, causing time margin errors. Furthermore, unsuccessful noise control on the PDN will cause the amplitude of the eye diagram in the vertical direction to collapse due to the voltage noise.

In pursuing signal integrity (SI) and power integrity (PI), new methodologies emerge for designing and validating computer platform high-speed interconnects operating under strict noise constraints. A common technique in the industry involves employing multiple decoupling capacitors in parallel to reduce the magnitude of the impedance profile of the PDN, ensuring it remains below a specific threshold. This is done to minimize fluctuations in the power supply voltage when substantial changes in current load occur. The more decoupling capacitors employed, the better impedance profile can be achieved [Ambasana-23]. However, it may not be feasible to accommodate an excessive number of decoupling capacitors given the available space within the PDN. Additionally, an excessive number of decoupling capacitors unnecessarily increases the manufacturing costs.

The electrical behavior of physical interconnects in a computing platform can be analyzed by using high-frequency circuit simulators as well as electromagnetic (EM) simulation tools, such as those provided by Keysight ADS. The SI and PI design parameters should be optimized to meet the industrial interface-specific electrical compliance requirements by thorough analysis of simulation data. Packaging structures have become the key factor to determine the overall chip performance at the system level. Particularly, one of the most important factors in packaging structures is the interconnection between separate chips. To achieve the best performance of chips, the physical interconnects must have a high bandwidth, since the die-to-die link can become a

major bottleneck for overall performance.

The Universal Chiplet Interconnect Express (UCIe) is a new high-speed interconnect industrial standard specification for chip links [UCIe-25]. It is then important for SI design the analysis for the UCIe channel characteristics, considering the parameters defined by this industrial specification for standard packages. A chiplet is a sub processing unit that is controlled by a controller chip. Each chiplet can have different functions on the same package. Many electronic companies agreed to establish the UCIe specification including protocol, logical, physical, and electrical layers for the universal links between chiplets.

In a chiplet system, various chips from other vendors are integrated into one package using common UCIe channels. Since the standard package is often used in applications with moderate performance requirements, the SI specification is representing the UCIe channel as a black-box system characterized by S-parameters.

This thesis explores a co-simulation approach to analyze and optimize SI and PI in UCIe-based systems. By modeling the PDN with an equivalent circuit and representing the UCIe channel as a black-box system characterized by S-parameters, this work proposes and evaluates a methodology for optimizing decoupling capacitor configurations and voltage regulator parameters. The methodology leverages MATLAB and Keysight ADS in a unified simulation framework, employing several optimization algorithms such as Nelder–Mead, Quasi-Newton, and Conjugate Gradient to meet UCIe performance requirements, particularly eye height and eye width, while minimizing the number of decoupling capacitors, and in consequence the cost. The present thesis is organized as follows.

Chapter 1 introduces power delivery networks and the UCIe signal integrity specification, discussing the PDN model, power integrity principles, and the role of decoupling capacitors. Additionally, the chapter introduces the voltage regulator model and examines power integrity within UCIe systems.

Chapter 2 presents the circuital models for PDN analysis, details the co-simulation methodology used for simultaneous SI and PI analysis. It also explores UCIe channel simulation and the power-aware IBIS model within ADS Keysight, as well as the use of UCIe S-parameters in ADS and the effects of signal and line width/spacing on the eye diagram and crosstalk.

Chapter 3 formulates the optimization problem and defines the objective function for minimizing capacitor count while meeting SI-PI constraints.

Chapter 4 applies the proposed optimization approach to a buck voltage regulator and PDN design, presenting and analyzing simulation results.

Chapter 5 compares different optimization methods, evaluating their effectiveness in PDN design. It covers the Nelder-Mead method, the Quasi-Newton optimization algorithm using the Broyden Fletcher Goldfarb and Shannon (BFGS) formula, and the Conjugate Gradient optimization algorithm using the Fletcher-Reeves formula. This comparison provides insights into the most suitable methods for various PDN optimization scenarios.

Finally, the Conclusions summarize the key contributions of this thesis and outline opportunities for future research in SI-PI co-design and optimization for next-generation chiplet-based systems.

1. Power Integrity Modeling for UCIe Systems

Power delivery has become a central challenge in modern high-performance computer platforms, especially as devices operate at higher speeds and incorporate multiple integrated dies within the same package. The power delivery network (PDN) must provide a stable voltage supply to all circuits while supporting rapid changes in load current and maintaining performance across a wide frequency range. When the PDN is unable to respond effectively to these demands, voltage noise and transient voltage droop can degrade timing margins, reduce reliability, and interfere with the operation of high-speed interfaces such as UCIe.

This chapter introduces the fundamental concepts required to understand how a PDN behaves in advanced multi-die systems. It begins with an overview of power integrity and the role of the PDN impedance profile in evaluating voltage stability. It then describes the models used in this thesis, including a state-averaged representation of a buck regulator and a multi-stage decoupling structure that incorporates bulk, package-level, and die-side capacitance. Together, these components form the simplified PDN model that will be used throughout this work.

The chapter concludes with a discussion on power integrity considerations specific to UCIe systems and explains why accurate PDN modeling is necessary for evaluating the interaction between power behavior and signal quality. This provides the foundation for the combined SI and PI simulation framework presented in the next chapter.

1.1. Universal Chiplet Interconnect Express (UCIe)

The continued scaling of monolithic integrated circuits is increasingly constrained by reticle limits, yield challenges, and escalating fabrication costs. As a result, chiplet-based architecture has emerged as a viable alternative for constructing complex systems by integrating multiple smaller dies within a single package. Chiplets allow heterogeneous integration, enabling each die to be manufactured in a process node optimized for its specific function, such as logic, memory, analog, or I/O.

In chiplet-based systems, a substantial portion of the communication that was traditionally handled through board-level interconnects is moved inside the package. This shift places stringent

requirements on die-to-die interconnects in terms of bandwidth density, latency, energy efficiency, and electrical robustness. These requirements motivated the development of an open, standardized die-to-die interconnect suitable for chiplet-based systems.

1.1.1 Overview of Universal Chiplet Interconnect Express (UCIe)

Universal Chiplet Interconnect Express (UCIe) is an industry-driven open standard that defines a die-to-die interconnect for in-package communication. The objective of UCIe is to enable interoperability among chiplets from different vendors, fostering a broad chiplet ecosystem similar to that enabled by PCI Express at the board level [UCIe-25]. The UCIe specification defines multiple layers of the interconnect stack, including the physical layer, link management, and protocol adaptation. At the physical level, UCIe targets short-reach channels implemented using micro-bumps, redistribution layers (RDLs), silicon interposers, or organic substrates. These channels typically span on the order of millimeters to a few centimeters and are optimized for high bandwidth density and low energy per bit [UCIe-25], [Sharma-23].

UCIe supports multiple protocol modes, including streaming and PCIe/CXL-based operation, allowing it to serve as a flexible foundation for a wide range of system architectures. By standardizing both electrical and logical aspects of die-to-die communication, UCIe reduces integration risk and enables scalable system design across heterogeneous technologies [Sharma-23].

1.1.2 UCIe Electrical Characteristics and Signaling Environment

UCIe links operate at multi-gigatransfer-per-second (GT/s) data rates per lane, with current specifications supporting rates ranging from 16 GT/s up to 32 GT/s, with future UCIe generations extending support to 48 GT/s and 64 GT/s using advanced routing structures [UCIe-25]. At these data rates, signal integrity is strongly influenced by the package environment, including conductor loss, dielectric loss, characteristic impedance discontinuities, and electromagnetic coupling between signal and power structures. Unlike board-level links, UCIe channels exhibit very short electrical lengths but extremely high interconnect density. This environment leads to tight coupling between signal paths and their return currents, which are largely controlled by the package power

and ground distribution network. Consequently, the electrical behavior of UCIe links cannot be accurately assessed without considering the interaction between the signaling structures and the power delivery network.

1.2. Importance of SI–PI Co-simulation for UCIe

Traditional design flows often treat signal integrity (SI) and power integrity (PI) as largely independent problems. However, for high-speed in-package interconnects such as UCIe, this separation is no longer sufficient. SI–PI co-simulation provides a unified framework in which the interaction between signal paths, return currents, and the PDN is explicitly modeled.

Prior research has demonstrated that simultaneous switching noise and PDN impedance characteristics can significantly affect high-speed I/O performance, particularly in dense packaging environments [Bogatin-18], [Kim-23]. For UCIe systems, co-simulation enables the evaluation of how PDN design choices, especially the decoupling capacitor values and position, and their inherent parasitics, impact both voltage stability and signal quality. This close coupling between the UCIe signaling environment and the PDN motivates the systematic optimization of PDN components as part of the overall interconnect design process.

1.3. Power Integrity in UCIe Systems

Power integrity (PI) encompasses the ability of an electronic system to deliver stable and reliable power from the source to the load under all operating conditions. It includes power conversion, distribution, and circuit-level behavior across the board, package, and silicon domains, as well as the thermal and mechanical factors that influence electrical performance. As described in [DiBene-14], PI can be viewed as “the study of the efficacy of the power delivered from the source to the load within an electronic system.”

A central part of PI analysis is understanding the behavior of the PDN. From the perspective of the chips, the PDN is evaluated through its impedance profile, which can be examined in both the time and frequency domains. Under the assumptions of linearity, time-invariance, and passivity, both domains contain equivalent information. Maintaining a sufficiently

low PDN impedance profile across frequency is critical because voltage noise, voltage droop, and power-ground bounce directly affect the timing and reliability of high-speed circuits [Choi-11].

To control the PDN impedance profile, industry practice relies on multiple decoupling capacitors of different values placed in parallel and at different physical locations to cover a wide frequency range. However, these arrays of capacitors introduce parallel resonant frequencies (PRFs) where impedance peaks may occur [Moreno-Mojica-19]. If a transient current contains energy near one of these peaks, the PDN can actually amplify noise instead of attenuating it [Moreno-22]. Voltage regulator modules (VRM) are essential components in a PDN. A notable PI undesired effect is the resonance between the VRM's effective output inductance and the bulk capacitor, which may indicate potential VRM stability issues [Smith-17].

Frequency-domain analysis helps identify these resonances and ensures the impedance profile stays below the target impedance for the system's operating conditions. Designers typically begin with bulk-capacitor recommendations from the voltage-regulator vendor, which are based on simulations of transient response and control-loop stability.

Time-domain analysis, on the other hand, evaluates the PDN's response to switching currents, including the magnitude of transient voltage droops, and is essential for preventing reliability issues at the device level.

These PI considerations become especially important in UCIe-based multi-die systems. The UCIe standard defines the logical, protocol, physical, and electrical specifications for high-speed chiplet-to-chiplet links integrated within the same package [UCIe-25]. Modern UCIe packages include multiple dies, each with its own local PDN requirements, as illustrated in Fig. 1.1. The interconnects supporting UCIe links, spanning approximately 10 mm to 25 mm across organic package substrates, operate at data rates up to 32 GT/s in current deployments, with future UCIe generations extending support up to 64 GT/s using advanced routing structures.

Power integrity ensures the PDN remains stable enough to support reliable high-speed signaling. Voltage noise, simultaneous switching noise (SSO), and droop events in the PDN can distort threshold levels, modulate driver behavior, and collapse eye-diagram margins. Given UCIe's aggressive roadmap and high-performance requirements, maintaining PI is vital to sustaining link reliability across generations.

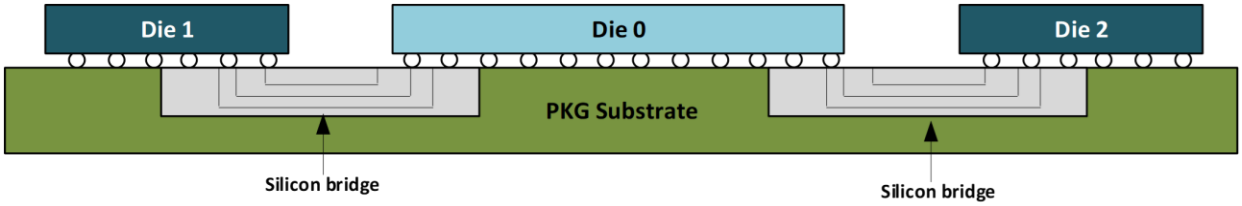

Fig. 1.1 UCIe standard package interface representation. Figure taken from [UCIe-25]

In this thesis, the UCIe channel routing dimensions are derived from the physical platform (PHY) requirements, and complete interconnect structures, including signal/ground patterns and micro-bump arrays at both the transmitter and receiver, are modeled. Performance is evaluated using the voltage transfer function and UCIe-specified eye-diagram margins, allowing assessment of how PDN behavior influences high-speed chiplet communication.

1.4. PDN Modeling

Every computer platform requires a PDN to supply stable voltage and current to its components. When the various devices in a PDN start switching, current surges occur, resulting in voltage noise. Unsuccessful noise reduction on the PDN can lead to performance degradation and even to catastrophic functional failures on high-speed platforms.

According to [Smith-17], the PDN comprises all the devices and interconnects that distribute the electrical power supply (biasing voltages) and return the electrical current across a board in an electronic system. Its primary function is to maintain adequate power across all operating conditions. A complete PDN typically includes the voltage regulator module (VRM), bulk and ceramic capacitors, PCB and package power planes, connectors, and on-chip capacitance [Kadlec-19]. These elements can be grouped into six major elements, shown in Fig. 1.2, namely:

1) Voltage regulator module (VRM): the component responsible for converting and

regulating input voltage to a suitable level for the load, with associated bulk capacitors for immediate power stabilization.

2) Bulk capacitors: larger capacitors that smooth out voltage fluctuations and provide charge storage for sudden changes in load current.
3) PCB power planes: broad conductive paths on the printed circuit board that distribute regulated voltage across the board, interfacing with bulk and ceramic capacitors.
4) Package power planes: conductive layers within the chip package that distribute power efficiently, connecting the PCB power planes to the silicon die.
5) Ceramic capacitors: board-level capacitors that manage high-frequency noise and transient loads, enhancing voltage stability on the PCB.
6) On-chip capacitance: integrated capacitors within silicon die that provide rapid response to transient loads, ensuring stable power delivery directly to the load circuits.

This hierarchical perspective highlights how different PDN components respond at different time scales and contribute to maintaining stable power during dynamic operation. Because these elements interact electrically, adjusting or evaluating any one of them in isolation does not fully represent the behavior of the complete system.

Within this multi-stage structure, the capacitors and power-distribution elements work together to supply charge during rapid changes in load current. Although parallel capacitor groups help supporting the device biasing across a wide range of switching activity, the interaction between their parasitic elements can introduce resonant behavior. These resonances may appear in the time domain as significant voltage fluctuations or transient dips during fast switching events. Understanding how each tier of the PDN responds under these conditions is essential to

maintaining reliable performance.

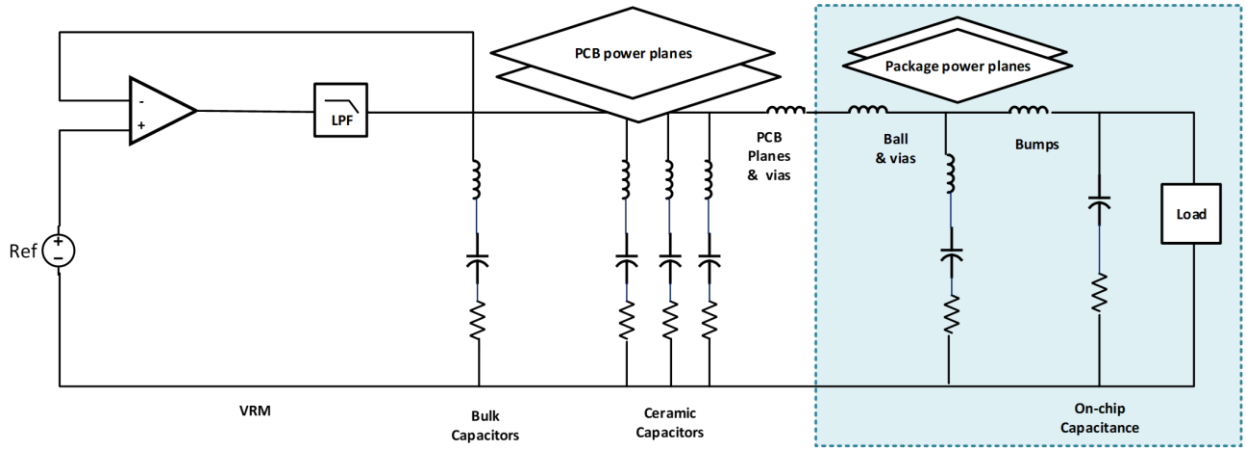

Fig. 1.2 Schematic of the PDN ecology showing its main elements. Figure taken from [Smith-17].

1.4.1 Voltage Regulator Model

The voltage regulator, often a DC-DC converter, is the system's primary power source and ideally should maintain a constant DC biasing voltage level to the multiple active devices while reducing noise or ripple. The acceptable voltage level variability for the chips is determined by the frequency spectrum of the current they draw and the PDN impedance profile. To construct the PDN, the worst-case transient current drawn by the chips must be known.

The feedback circuit of a voltage regulator (VR) maintains constant voltage despite changes in input voltage or effective load impedance, as described in [Kamo-23]. It is essential to highlight the VR's behavior depending on frequency. At low frequencies, the VR is the major contributor to voltage noise in a PDN [Kamo-23]. At high frequencies, voltage noise originates from voltage drops caused by transient currents when devices start switching.

For this thesis, a state average model of a buck converter is chosen, as in [Moreno-Mojica-21]. The equivalent circuit of the converter used in this work is shown in Fig. 1.3, whose component values are in Table 1.1. The circuit consists of a single-ended input amplifier, a compensation amplifier, an output amplifier, and an output filter. The output amplifier is the power stage portion of the regulator.

A simple output filter of the VR is connected to the power delivery network input. The physical connection between the Buck Regulator and the UCIe channel is marked as "Connection to sense point," it shows where the sense point will be connected to UCIe channel with the IBIS power aware model. This connection is crucial for ensuring that the power supplied is adequate for the signal transmission requirements. The compensation circuit amplifies the error between the reference voltage and the amplified feedback signal coming from the sense point on the PDN. To obtain the open loop gain Bode plots, the simulation circuit is modified following [Shanley-03], by adding a small-signal AC perturbation to open the loop.

1.4.2 Decoupling Capacitors in the PDN Ecology

In industry, the PDN design typically relies on a multi-stage decoupling strategy, where capacitors are distributed across the board, package, and die, to keep the impedance profile low across a wide frequency range [Zheng-03]. Designers use this hierarchy because no single capacitor type can effectively respond to all current transients: bulk capacitors address low-frequency demands, package capacitors support intermediate frequencies, and near-die capacitance manages the fastest switching events [Paul-92]. This tiered approach is widely adopted in high-speed multi-die systems, where power integrity strongly influences timing margins and overall system reliability.

Accurately modeling the full physical PDN, including package routing, detailed capacitor

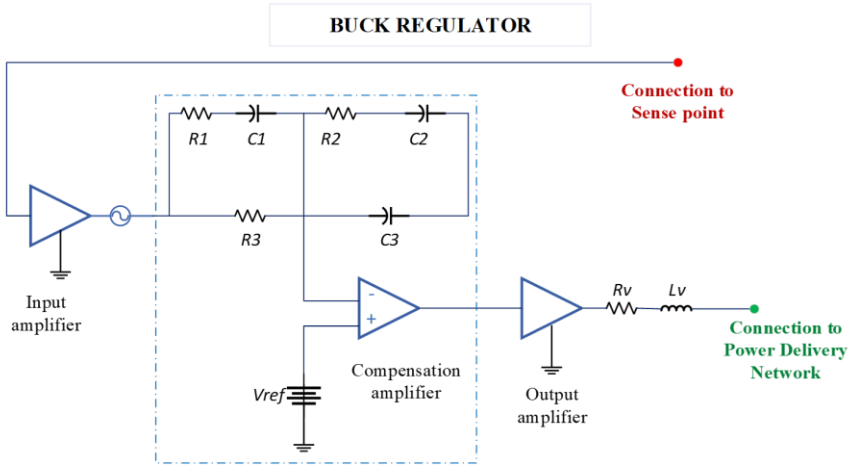

Fig. 1.3 Equivalent circuit of the voltage regulator (VR), considering an average model of a buck converter. Figure taken from [Moreno-Mojica-21].

layouts, and silicon power grids, can be computationally expensive and unnecessary when the focus is on transient voltage droop and its impact on signal integrity. For this reason, industry and academic work commonly replace distributed structures with lumped RLC representations that capture the essential impedance characteristics without the overhead of full electromagnetic extraction [Moreno-21]. This simplification is routinely recommended because it allows designers to analyze resonances, evaluate capacitor placement strategies, and run rapid design iterations. Following [Smith-17], the PDN is represented as a three-stage network of capacitors [Phillips-25], as illustrated in Fig. 1.4, consisting of:

1) Bulk capacitors (low-frequency tier). They are located on the motherboard and they supply charge for slow and large-magnitude current variations. They stabilize the DC rail, support regulator dynamics, and maintain low impedance at low frequencies where the VRM response is limited.
2) Cavity or land side capacitors (LSC) (mid-frequency tier). They are placed on the package, closer to the die. They respond to medium-frequency current demands and bridge the gap between the slow VRM/bulk response and the fast die activity. These capacitors mitigate the "second droop" by providing charge during mid-frequency transients [Sotman-06].
3) Die side capacitors (DSC) on the package (high-frequency tier). They sit closest to silicon and address the highest-frequency components of switching activity. They supply immediate charge during rapid transients, tens of picoseconds to a few nanoseconds,

minimizing the "first droop" at the die pads. This tier has the most direct impact on high-speed signaling stability.

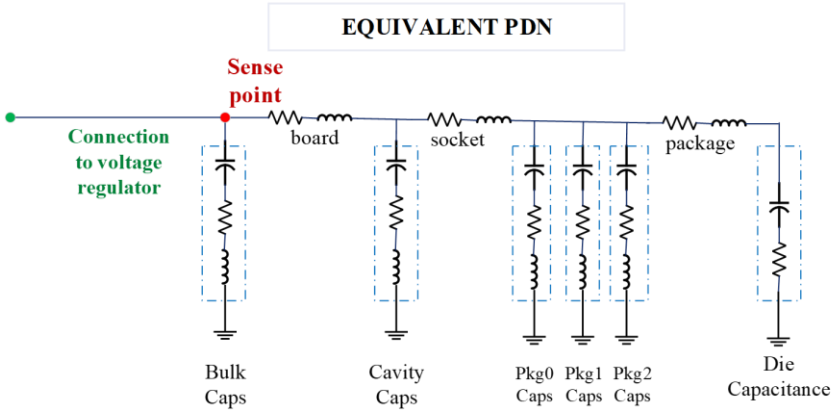

Fig. 1.4 Simplified multi-stage PDN ecology model adopted in this thesis. Figure taken from [Moreno-21].

For this thesis, we adopt a simplified PDN ecology model that reflects this industry practice, as shown in Fig. 1.5. Each stage is modeled using lumped RLC elements that approximate the dominant electrical behavior of the corresponding physical structures. This abstraction captures the main contributors to voltage droop, often described as the first, second, and third droop, while avoiding unnecessary modeling complexity.

Fig. 1.5 also provides a hierarchical perspective highlighting how different PDN components respond at different time scales and contribute to maintaining stable power during dynamic operation. Because these elements interact electrically, adjusting or evaluating any one of them in isolation does not fully represent the behavior of the complete system. Within this multi-stage structure, the capacitors and power-distribution elements work together to supply charge during rapid changes in load current [Deutschmann-23].

The resulting PDN model preserves the frequency-dependent characteristics relevant to evaluating power integrity and its interaction with signal integrity. It is therefore well-suited for the co-simulation and optimization framework developed in this work, balancing realism with computational efficiency. Table 1.1 lists specific values of all pre-assigned VR lumped elements and PDN parameters, including the resistors, capacitors, and inductors that define the control loop and steady-state characteristics.

1.5. Conclusions

This chapter established the basis for the power integrity analysis used in this thesis. It outlined the main functions of a PDN and examined how elements such as the voltage regulator, interconnect structures, and various tiers of decoupling capacitance contribute to the distribution of power throughout a multi-die system. The importance of the PDN impedance profile was highlighted, describing in general terms how resonances, load transients, and capacitor selection influence voltage stability at different frequencies.

TABLE 1.1 DESIGN PARAMETER VALUES FOR PDN CIRCUIT AND BUCK REGULATOR

PDN Parameters	Value	Buck Regulator Parameters	Value
Bulk Capacitance	418.7 µF	R_1	10 kΩ
Cavity Capacitance	12.7 µF	R_2	8.112 Ω
Pkg0 Capacitance	1.14 µF	R_3	21.546 mΩ
Pkg1 Capacitance	402.68 nF	C_1	120.544 pF
Pkg2 Capacitance	6.34 µF	C_2	2.397 nF
		C_3	92.278 nF
		L_V	300 nH

To support the thesis presented in subsequent chapters, a simplified PDN model was defined. This model includes a state-averaged buck regulator and a three-tier decoupling structure composed of bulk capacitors, cavity or land-side capacitors, and die-side capacitance. These components capture the dominant frequency-dependent behavior of the PDN while maintaining the computational efficiency required for system-level analysis.

The chapter also described in general terms how power integrity affects UCIe-based chiplet systems, where voltage droop, simultaneous switching noise, and fluctuations in the supply can alter threshold levels and introduce timing uncertainty. These considerations motivate the need for a co-simulation approach that evaluates both signal integrity and power integrity at the same time. The next chapter presents the proposed methodology and explains how the PDN model introduced here is integrated into the overall simulation framework.

2. Signal Integrity Modeling for UCIe Systems

High-speed chiplet interfaces, such as Universal Chiplet Interconnect Express (UCIe), require precise control of signal quality to ensure reliable communication between dies integrated within the same package. As data rates reach 16 GT/s, the electrical behavior of the interconnect becomes increasingly sensitive to waveform distortion caused by crosstalk, inter-symbol interference (ISI), electromagnetic coupling, and discontinuities within the package structures. Even small distortions can reduce voltage and timing margins at the receiver, leading to errors in data interpretation [Bogatin-09]. Because UCIe defines strict electrical requirements for interoperability across chiplets, understanding the mechanisms that affect signal integrity is essential.

This chapter presents the fundamental principles of signal integrity as they apply to UCIe-based interfaces. It describes the channel impairments that arise in multi-die packages, explains the role of the eye diagram as the primary electrical compliance metric, and outlines the modeling representations used in this thesis, including the S-parameter-based UCIe channel model and the power-aware IBIS models for the transmitter and receiver. These concepts establish the foundation needed to analyze waveform quality at high data rates and to evaluate whether a UCIe channel can satisfy the electrical margins defined in the specification [UCIe-25].

2.1. Signal Integrity in UCIe Systems

UCIe supports multiple signaling rates depending on the specification generation, including up to 16 GT/s and 32 GT/s in UCIe 1.x, with newer revisions extending support to higher rates; in this thesis, a signaling rate of 16 GT/s is selected. Operating at such high speeds presents significant challenges. In these environments, the integrity of the signals can be severely compromised by factors such as crosstalk, inter-symbol interference (ISI), and electromagnetic noise. Crosstalk refers to the unwanted transfer of signals between adjacent channels, which can lead to interference. ISI occurs when signals from different symbols overlap, causing at the receiver distortion and errors in signal interpretation [Pandit-11].

Additionally, electromagnetic noise can introduce further interference and distortion, affecting the quality and reliability of data transmission [Bogatin-09]. Therefore, addressing these

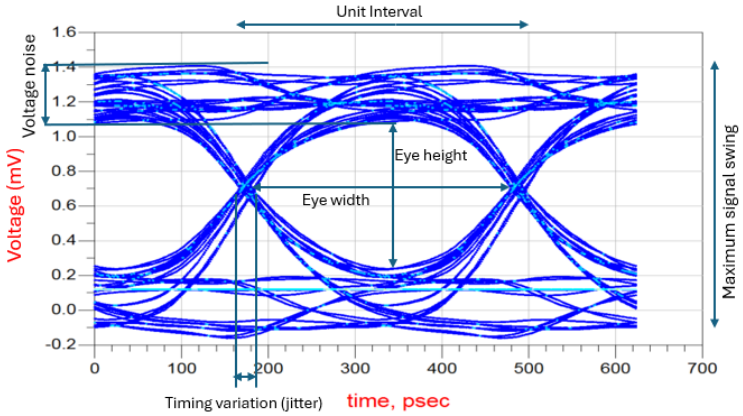

Fig. 2.1 Main characteristics of an eye diagram: a graphical tool to assess signal integrity in high-speed serial data transmission.

issues is crucial to maintaining signal integrity and ensuring the effective performance of UCIe systems at high data rates.

The eye diagram is typically employed as analytical tool to monitor and assess signal integrity, offering a visual depiction of signal quality. A well-formed eye diagram with clearly defined eye height and eye width indicates strong signal integrity. In contrast, a collapsed eye diagram indicates issues like voltage noise or insufficient signal margins, which can result in data errors and compromised performance [Pandit-09]. The eye diagram can collapse if signal integrity is not properly maintained, leading to timing uncertainties and data errors.

UCIe packages integrate multiple chiplets operating at high data rates, each with distinct and dynamic power requirements. These variations in current draw voltage fluctuations and power/ground noise in the PDN. These fluctuations can introduce jitter into the data signals, further compromising signal integrity. If the PDN is not well-designed, voltage noise can propagate through the interconnect, affecting the transistors' switching speeds and overall system stability. Fig. 2.1 shows the main features of a typical eye diagram, a key tool for evaluating signal integrity in UCIe interfaces. An eye diagram is created by slicing the time-domain signal waveform into small, symbol-length chunks and overlaying them. The horizontal axis of the eye diagram represents time, typically spanning one or two symbols or unit intervals (UI) wide, while the vertical axis corresponds to the signal's voltage amplitude. The open area in the center, known as

the "eye opening," reflects the region where the receiver can reliably sample the signal. A larger eye opening indicates stable signal and power conditions, while a narrower one suggests degradation due to losses, jitter, inter-symbol interference, or voltage noise propagated from the PDN.

The dimensions of the eye opening, specifically its width and height seen at the receiver, are important key indicators for evaluating link quality and overall system performance. In UCIe-based interfaces, these parameters determine whether the transmitted data can be correctly interpreted under realistic power and signal noise conditions. Fig. 2.2 illustrates an eye diagram with an applied compliance mask, which defines the allowable voltage and timing margins at the receiver input. The receiver setup, hold window, voltage specifications, and all jitter and noise

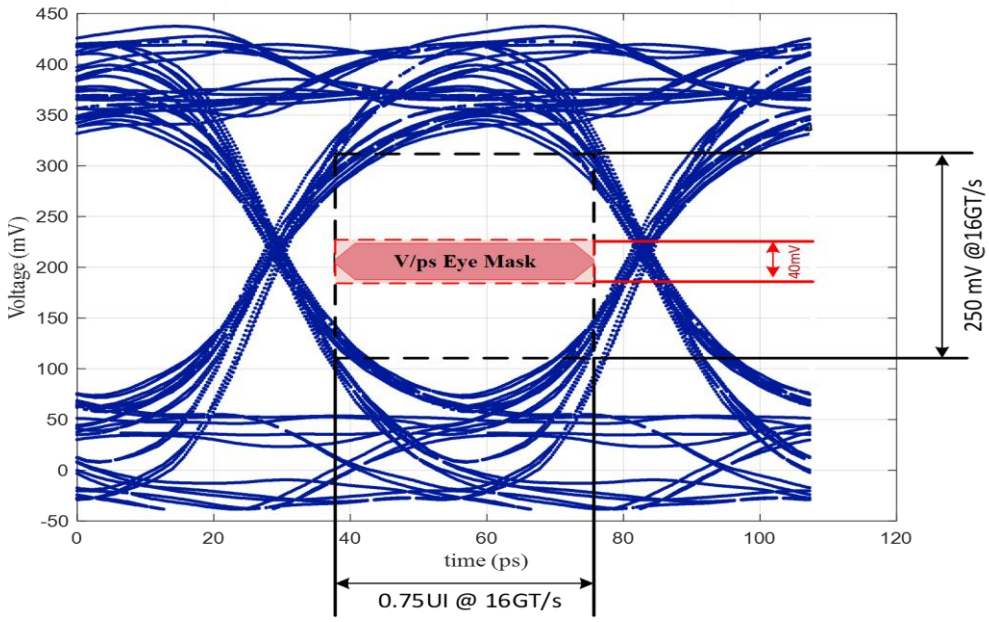

Fig. 2.2 Eye diagram with compliance mask indicating allowable voltage and timing margins at the UCIe transmitter.

terms are all included in the mask [UCIe-25]. When the eye remains fully open within this mask region, the link meets the required signal integrity specifications. Conversely, any intersection between the eye trace and the mask boundary indicates excessive jitter, noise, or voltage variation originating from the PDN or interconnect. Therefore, the mask provides a standardized means to verify whether the simulated or measured eye complies with the UCIe timing and noise criteria.

Receiver eye margins may be small at higher data speeds, and any skew between the data lanes may further degrade the link's performance. Under channel compliance simulation settings

TABLE 2.1. UCIE EYE REQUIREMENTS [UCIE-25]

Data rate (GT/s)	Eye height (mV)	Eye width (UI)
4, 8, 12, 16	40	0.75
24, 32	40	0.65

using noiseless and jitter-less behavioral TX and RX models, the UCIe interconnect channel must meet the minimum rectangular eye open requirements shown in Table 2.1 [UCIe-25].

UCIe interconnect channel needs to meet the requirement of minimum rectangular eye open mask under noiseless jitter-less conditions, for a worse or ideal situation, it is important to get lower and higher ranges limits, as well as a minimum eye-opening width. Various factors, such as jitter, mismatches, or noise generated by power noise, are characterized by frequency. Fig 2.2 illustrates the minimum rectangular eye in red color that, according to Table 2.1, should correspond to an eye height of 40 mV. For the 16 GTs data rate, the channel eye mask changes to a minimum rectangular eye width of at least 0.75 UI and an eye height of 250 mV for a Tx swing of 0.75 V [UCIe-25].

2.2. Channel and Buffer Modeling

Accurate signal-integrity evaluation requires models that capture the electrical behavior of both the interconnect channel and the I/O circuitry at the transmitter and receiver. In UCIe systems, the short-reach die-to-die path consists of package traces, redistribution layers, vias, and micro-bump arrays, all of which introduce frequency-dependent impairments. To represent these effects, this thesis uses an S-parameter extraction of a UCIe channel, which provides a broadband, passive, and causal description of the channel's behavior across frequency.

2.2.1 UCIe Channel as an S-Parameter Network

The S-parameter model represents the UCIe interconnect as a multiport linear network that characterizes how differential signals propagate from the transmitter bumps to the receiver bumps. This representation captures the dominant SI-related channel behavior, including:

- Insertion loss, which attenuates high-frequency components and contributes to inter-symbol interference (ISI), as described in [Pandit-11].
- Return loss, associated with impedance mismatches due to discontinuities, such as vias, bumps, and routing transitions.
- Crosstalk, arising from capacitive and inductive coupling (electromagnetic coupling) between adjacent differential pairs within the organic package.
- Mode conversion, resulting from asymmetries or geometrical discontinuities that convert differential energy into common-mode energy.

Because UCIe links operate at short distances but wide bandwidth, these frequency-dependent characteristics determine the extent to which the symbol transitions remain sharp and free from distortion. The S-parameter model therefore provides an essential foundation for understanding channel impairments without requiring a full and detailed geometric representation of the package.

The S-parameters representation of the physical UCIe channel is normally obtained from interconnect modeling using 3D EM modeling software tools and a Vector Network Analyzer (VNA) [Zhao-08]. The pre-silicon flow predicts channel behavior from physics-based EM models, including the S-parameter extraction of the UCIe interface routed on the interposer. In this thesis, the S-parameters were measured directly with a VNA, covering the physical prototype, including package bumps, RDL, and the routed traces on the interposer connecting the two dies. The VNA is first calibrated to move the reference plane as close as possible to the channel boundaries, then the raw S-parameters are captured across the full bandwidth of interest. Any fixture, connector, or probe effects that sit outside the desired reference plane are removed via de-embedding, leaving the true electrical response of the channel, from TX die through the interposer routing to the RX die. The result is a clean Touchstone file ready for UCIe compliance analysis. For direct comparison of eye diagrams, S-parameters must be converted into time domain responses, enabling their use in time domain link simulations [Kaller-05].

2.2.2 Power-Aware IBIS Models for Transmitter and Receiver

In addition to the channel behavior, the I/O circuitry must be modeled carefully, since its characteristics influence both timing and amplitude margins. In this work, the UCIe transmitter (TX) and receiver (RX) are represented using power-aware IBIS models [Ming-17], which describe the nonlinear voltage- and current-dependent behavior of the buffers.

Power-aware IBIS models incorporate:

- I/O voltage swing and output impedance, which define the strength of the transmitted signal and its sensitivity to load variations.
- Rise and fall transition characteristics, which determine edge rate and jitter susceptibility.
- Receiver threshold levels and input termination, which influence sampling margin and noise tolerance.

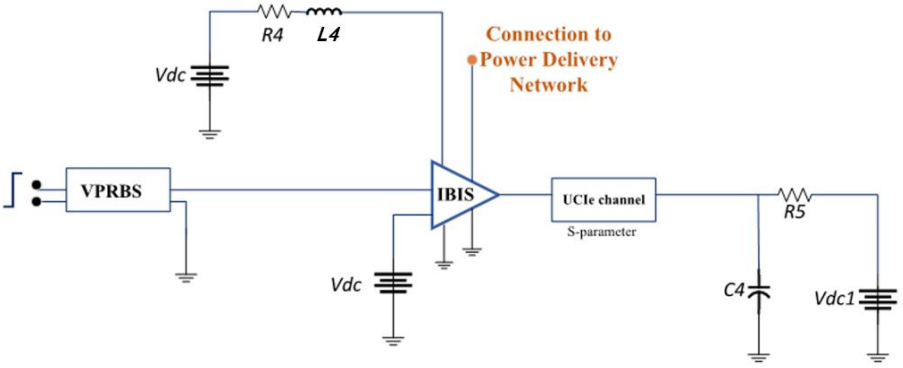

Fig. 2.3 Circuit model combining an IBIS power aware buffer model with the S-parameters representation of the UCIe channel. Figure taken from [Ming-17]

- Supply-rail sensitivity, capturing the effect of voltage fluctuations on buffer behavior, consistent with the SI degradation mechanisms outlined in [Pandit-09].

The inclusion of supply-rail sensitivity is especially important because voltage variations can alter the switching threshold or delay inside the receiver, compressing the eye opening and degrading SI margins. The use of power-aware IBIS models ensures that the buffer representation remains physically accurate under conditions expected in UCIe operation.

2.2.3 Combined Signal Integrity Modeling Perspective

The combination of the S-parameter-based channel model with the power-aware IBIS buffer models provides a comprehensive electrical representation of the UCIe signaling path, as shown in Fig. 2.3. The S-parameter network defines how the physical package shapes the transmitted signal [Ming-17], while the IBIS models define how the signal is launched and interpreted at the die interfaces. In Fig. 2.3, the component VPRBS generates pseudo-random bit signals to stress-test the channel, while R4 and L4 serve as input termination, filtering noise before the buffer. Multiple Vdc sources provide necessary DC biasing at both input and output sides of the channel. The IBIS block models real-world I/O buffer behavior and connects directly to the PDN, allowing accurate simulation of power integrity effects. The channel is abstracted as a UCIe block using S-parameters to capture transmission properties. At the receiver end, R5 and C4 function as output terminations; R5 controls impedance, and C4 filters noise to ground. The "Connection to PDN", is directed to the buck regulator circuits and the equivalent PDN. This is not a second polarization, but a dedicated supply path for the buffer.

This modeling framework enables detailed understanding of the waveform distortions introduced by insertion loss, crosstalk, and discontinuities, as well as the impact of buffer characteristics such as finite edge rate, termination accuracy, and sensitivity to amplitude variations. Together, these elements describe the essential factors that govern signal quality in UCIe systems and form the basis for evaluating the eye-diagram-based compliance requirements defined by the UCIe specification [UCIe-25].

2.3. Conclusions

This chapter introduced the key signal-integrity concepts relevant to UCIe chiplet links and described in general terms the physical mechanisms that degrade waveform quality at high data rates. Crosstalk, ISI, package losses, geometric discontinuities, and high-frequency attenuation were identified as dominant contributors to eye-diagram closure and reduced sampling margins. The chapter also reviewed the UCIe electrical requirements for eye height and eye width, which define the minimum allowable margins for compliant operation across supported data rates.

In addition, the chapter described the modeling structures used in this work to represent the UCIe signaling path. The S-parameter-based channel model captures the frequency-dependent behavior of the package and interconnect, while the power-aware IBIS transmitter and receiver

models represent the nonlinear and supply-sensitive characteristics of the I/O circuitry. Together, these models provide a complete electrical description of the UCIe link and offer the basis for assessing its signal-integrity performance.

These foundations prepare the way for the subsequent chapter, where these models are used to analyze the behavior of UCIe channels under the required operating conditions.

3. SI and PI Co-Simulation Methodology

For a UCIe system to function reliably, it is essential to perform co-simulations that consider both signal integrity (SI) and power integrity (PI) simultaneously. Traditionally, these aspects were analyzed separately, with signal integrity focusing on the quality of the electrical signals and power integrity dealing with the stability of the power distribution network (PDN). However, in high-speed, high-bandwidth systems like UCIe, the interaction between these two domains becomes crucial.

The signals traveling across the die-to-die interconnects must remain clean and within the designated voltage and timing margins to ensure accurate communication between chiplets. By considering both SI and PI together, designers can ensure that the system operates reliably under various conditions. For example, reducing PDN noise improves SI, and optimizing signal paths minimizes the impact of simultaneously switching output (SSO) on power integrity [Pandit-11]. In UCIe systems, chiplets are interconnected via high-speed links, and any noise in the PDN can propagate through these interconnects, affecting both signal transmission and chiplet communication. Co-analysis ensures that these high-speed links are robust against voltage and signal noise. Performing SI-PI co-analysis helps identify performance bottlenecks early in the design process, enabling engineers to adjust to ensure the system meets stringent performance requirements. This leads to better system reliability and fewer issues in the field.

The block diagram in Fig. 3.1 illustrates the general architecture considered for co-simulation. It shows a high-level overview of the interaction between power regulation and signal transmission quality.

This chapter presents the SI–PI co-simulation methodology used in this thesis. It describes the simulation flow, software tools, and resulting analyses used in this work to evaluate UCIe channel performance under dynamic supply conditions.

3.1. Unified SI–PI Co-Simulation Methodology

The SI–PI co-simulation follows a structured sequence that allows power-supply noise and high-speed waveform behavior to be evaluated within the same simulation environment.

The first step in the co-simulation methodology is to run AC simulations to examine how the PDN responds across frequency. For instance, this step can be done using Keysight ADS. This allows identification of resonance regions and frequency bands where voltage supply fluctuations may occur. These results provide the baseline supply-noise characteristics used in later steps.

Next, transient simulations are performed to observe the voltage droop. Again, Keysight ADS transient analysis can be used to capture how the voltage supply responds to rapid current

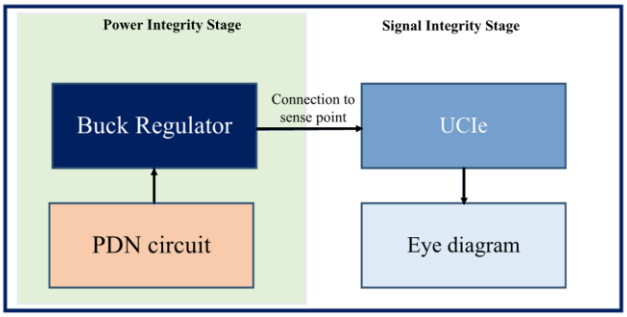

Fig. 3.1 Block diagram of the co-simulation setup integrating power and signal integrity analysis.

changes and to generate realistic voltage-noise waveforms that will later be applied to the transmitter (Tx) and receiver (Rx) circuitry. With the PI simulations complete, SI simulations are run to evaluate eye-diagram behavior. In this step, the UCIe channel is stimulated with high-speed patterns, and Keysight ADS can be used to observe the resulting waveform quality at the receiver.

The key step in the methodology is applying the time-domain voltage supply-noise waveform extracted from the PI simulations to the I/O buffers during SI analysis. In Keysight ADS, the noise waveform is connected directly to the power pins of the I/O blocks. This allows the eye diagram, jitter, and timing margins to be evaluated under realistic supply-noise conditions. As a result, the simulation directly reveals how the PDN disturbances affect UCIe signal quality.

Figure 3.2 shows the complete circuit used for the SI-PI co-simulation. The SI–PI simulation flow produces three major categories of results that describe the combined behavior of the supply network and the high-speed channel:

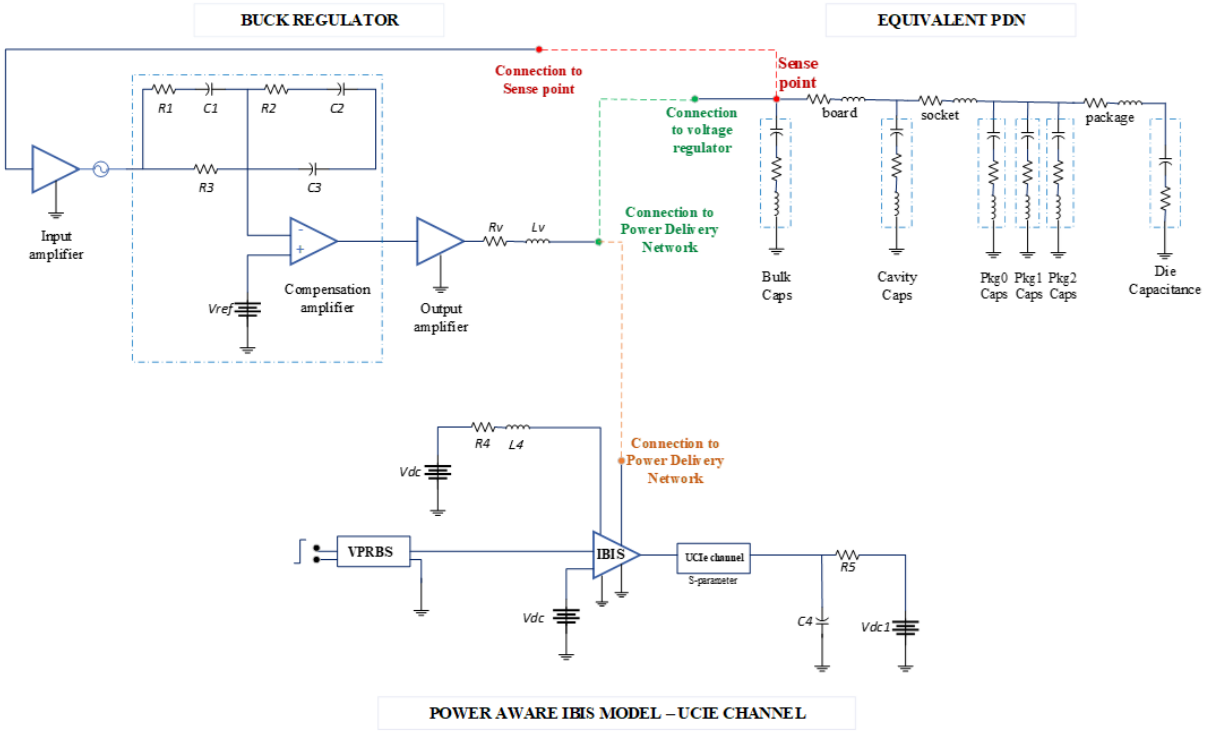

Fig. 3.2 Proposed equivalent circuit employed for SI-PI co-simulation.

1) From the PI simulations, the frequency-domain analysis reveals the PDN impedance profile characteristics and highlights resonance regions where the supply may be more sensitive to disturbances.
2) The time-domain analysis quantifies transient voltage-noise behavior, including supply droop and ground-bounce events that occur during switching activity.
3) The SI simulations, together with the injected supply-noise waveform, generate the eye diagram and determine whether the combined SI–PI system satisfies the UCIe electrical mask requirements for the selected data-rate mode.

By examining these results together, designers can trace signal degradation back to specific PDN phenomena, optimize decoupling strategies, and validate that UCIe channels remain robust under realistic supply conditions.

3.2. Tool Environment and Automation

The SI–PI analysis in this work is carried out primarily in Keysight ADS, with MATLAB used as the automation layer. ADS serves as the main simulation platform and is responsible for all circuit-level analyses. It performs AC simulations to evaluate the PI behavior in the frequency domain and transient simulations to capture time-domain supply-noise events such as voltage droop and ground bounce. ADS is also used for high-speed SI simulations, including waveform propagation through the channel and extraction of eye-diagram characteristics. In the final stage of the co-simulation flow, ADS combines SI and PI by applying the time-domain supply-noise waveform directly to the power pins of the transmitter and receiver, allowing the resulting eye-diagram degradation and timing effects to be observed under realistic operating conditions. In this way, ADS provides a unified environment in which all electrical interactions are evaluated, this process is described at high-level in Fig. 3.3.

MATLAB complements ADS by automating the generation and control of simulation configurations. It constructs ADS netlists programmatically, manages parameter sweeps, and modifies circuit settings across multiple test conditions without requiring manual editing. Through an ADS–MATLAB driver interface, MATLAB launches simulations and retrieves the resulting data for analysis and comparison. This automated workflow enables rapid exploration of design variables and efficient execution of SI–PI co-simulation campaigns, ensuring a consistent and repeatable process throughout the study.

3.2.1 ADS-Keysight and MATLAB Driver to Generate Eye Diagram

As mentioned before, the eye diagram is used to evaluate the quality of the UCIe signal transmission, serving as a standard performance indicator in digital transmission systems [UCIe-25]. In the context of this thesis, the eye diagram is employed to verify whether the UCIe interface meets the required specifications at 16 GT/s. Due to the construction method of the eye diagram, it is generally difficult to identify the specific bit-stream pattern responsible for eye collapse and increased jitter [Bogatin-09]. Additionally, the eye diagram provides valuable insights into crosstalk issues that may occur on parallel communication buses implemented on PCBs.

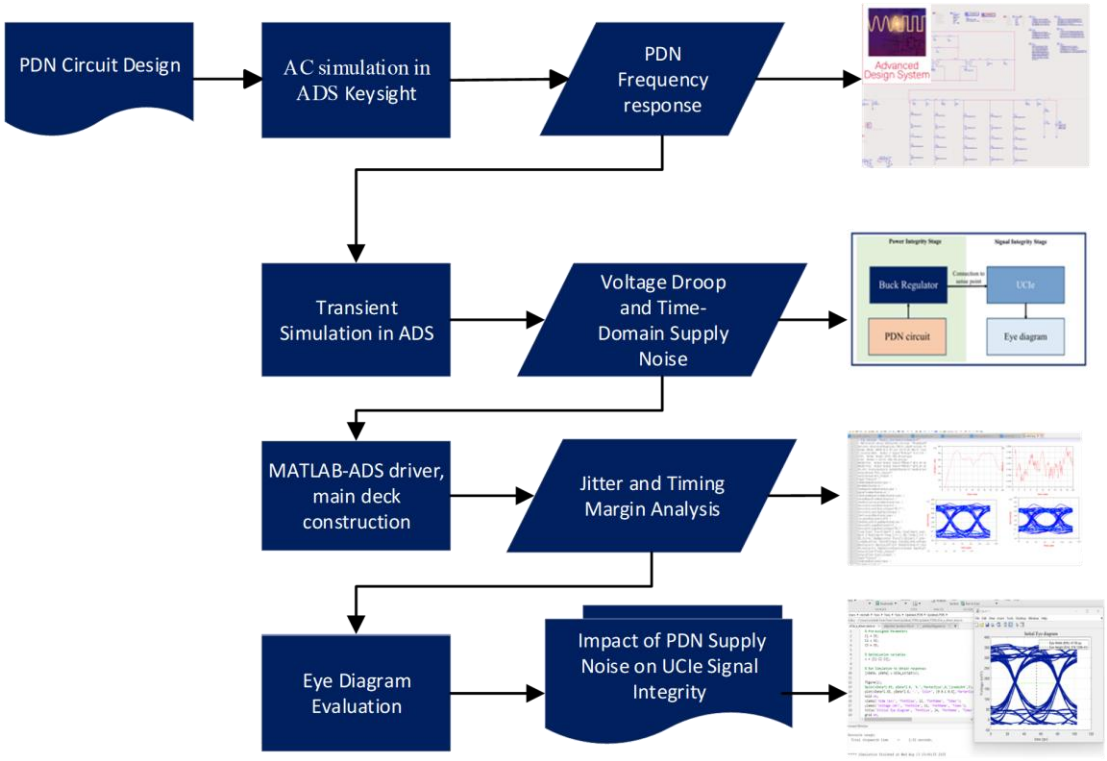

Fig. 3.3 Overall working process flow for the ADS-MATLAB unified environment to evaluate the SI-PI interactions and generate the resultant UCIe eye diagram.

In this thesis, a MATLAB driver was implemented to perform ADS circuit simulations. The basic MATLAB code that facilitates running ADS simulations from MATLAB is provided in [Leal-Romo-17] and [Rayas-Sánchez-20].

Upon a successful simulation, a "spectra.raw" file is generated in the project's working directory, which contains all necessary data for post-processing. The MATLAB code used to read the voltage output and current probe data from the PDN co-simulation is shown in Fig. 3.4. The behavior and amplitude observed in all related plots (voltage output, net voltage, and current probe) are identical to those obtained directly from ADS, as expected. Similarly, the density plot generated to construct the eye diagram from channel 1 of the UCIe stage in MATLAB shows perfect agreement with the responses directly obtained from ADS, e.g., as those presented in Fig.

2.1.

```
function  [xData,yData] = UCIe_script(x)

% ADS Netlist File Name
ScriptFileName = 'netlist.log';

% Define ADS netlist as a parameterized Cell array, ca
ar = 'ASCII_Rawfile=yes';

% Number of parallel capacitors
C1 = num2str(x(1));
C2 = num2str(x(2));
C3 = num2str(x(3));

ca{1} = '; Top Design: "SSO_Simulation_lib:Lab3:schematic"';
ca{2} = '; Netlisted using Hierarchy Policy: "Standard"';
...
```

Fig. 3.4 A MATLAB script showing settings to format plots and figures. This script was used to generate the plots from ADS-Keysight [Appendix-A].

3.3. Conclusions

This chapter presented the simulation-based SI–PI co-analysis framework used in this thesis. The methodology relies on ADS for AC, transient, SI, and combined SI–PI simulations, while MATLAB provides automation for deck construction and parameter exploration. The co-simulation results include voltage supply-noise waveforms, eye-diagram characteristics, jitter, and timing margins, as well as their combined behavior when power-supply noise is applied to the high-speed I/O circuits. This integrated simulation flow enables realistic evaluation of UCIe channel robustness under dynamic operating conditions.

4. Proposed Optimization Framework for PDN and Voltage Regulator Design

This chapter presents an optimization framework designed to refine the power-delivery network (PDN) and voltage-regulator (VR) configuration used in SI–PI analysis in typical UCIe channels. Traditional PDN design often selects a fixed and empirically determined number of decoupling capacitors, which can lead to excessive component usage and unnecessarily high manufacturing costs. To overcome these limitations, this thesis introduces a minimax-based optimization methodology which incorporates the number of capacitors directly as an optimization variable, aiming to meet signal integrity requirements for a 16-GT/s UCIe channel. These requirements are evaluated through both frequency-domain PDN behavior and time-domain eye diagram metrics, as in [Moreno-Mojica-22a y 22b], ensuring that the optimized PDN configuration satisfies UCIe voltage and timing margin requirements.

The overall process flow is illustrated in Fig. 4.1, which summarizes the interaction between PDN model extraction, lumped-element approximation, numerical optimization, and SI evaluation. As shown in the figure, the process begins with the extraction of a distributed PDN model, followed by the construction of a simplified lumped topology. These preliminary modeling steps are described in previous chapters. Building upon that foundation, this chapter focuses on the subsequent optimization and SI evaluation stages the optimization flow starts by extracting a distributed PDN model, which is then simplified into a lumped topology with fixed L, R, and C elements. This initial model undergoes iterative refinement using minimax optimization algorithms. At each iteration, the model is checked to ensure UCIe channel voltage and timing margins are met; if not, further optimization is performed. Once the model satisfies all UCIe margin requirements, the number of function evaluations, iterations, and total required decoupling capacitors are reported. The finalized result is then integrated into the signal integrity simulation environment for eye diagram analysis.

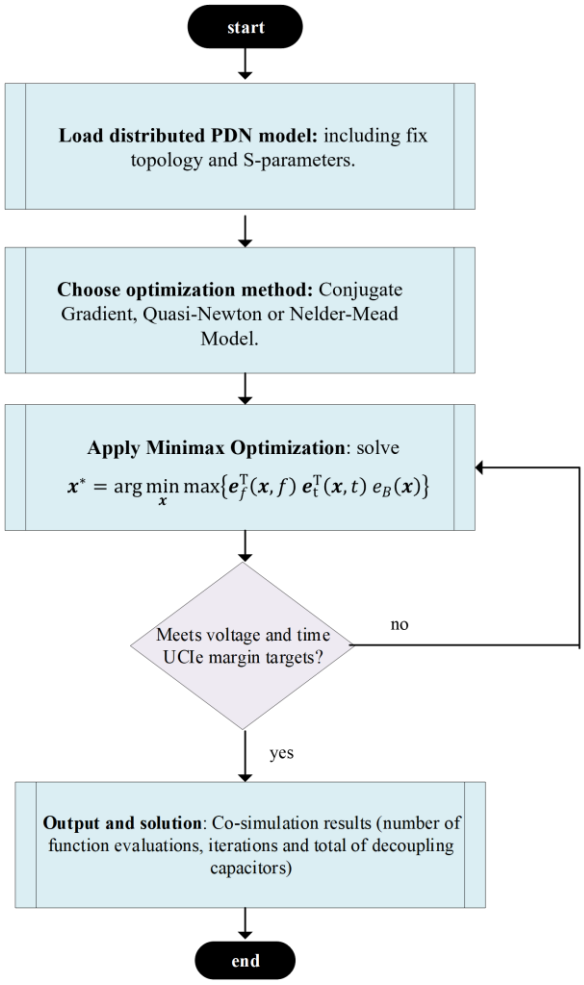

Fig. 4.1 PDN extraction, minimax optimization and SI integration workflow for UCIe channel analysis overall optimization process flow.

4.1. Parameter Definitions for Objective Function Formulation

Here, the PDN design problem is formulated as a numerical optimization problem in which the overall system performance is evaluated through a scalar objective function. This objective function maps frequency- and time-domain PDN behavior, as well as signal integrity metrics, into a unified scalar measure that can be minimized using classical optimization algorithms. In this thesis, a minimax formulation is adopted aiming to satisfy multiple design specifications with the largest margins, including voltage noise limits and eye diagram constraints.

Building on the PDN and voltage regulator circuit descriptions introduced in previous chapters, this section summarizes the numerical parameters required to construct the objective function used in the optimization framework. These parameters define which elements of the system are treated as fixed or pre-assigned, and which ones are designated as optimization variables.

Parameters that are predetermined by voltage regulator datasheet specifications, manufacturer recommendations, or physical constraints of the UCIe package are treated as fixed and are not subject to optimization. These parameters are collected into a pre-assigned parameter vector $\boldsymbol{p} \in \Re^m$, where m denotes the total number of fixed parameters defining the PDN and voltage regulator configuration. The elements of $\boldsymbol{p}$ include regulator characteristics, parasitic elements, and package-related parameters that were introduced section 1.4.2 in Table 1.1. The vector $\boldsymbol{p} = [Bulk, Cavity, Pkg0, Pkg1, Pkg2\ Capacitance, R_1, R_2, R_3, C_1, C_2, C_3, L_V]$ defined in Table 4.1 with their fixed value.

TABLE 4.1 PRE-ASSIGNED PARAMETER VECTOR $\boldsymbol{p} \in \Re^m$

$\boldsymbol{p}$ Parameters	Value
Bulk Capacitance	418.7 µF
Cavity Capacitance	12.7 µF
Pkg0 Capacitance	1.14 µF
Pkg1 Capacitance	402.68 nF
Pkg2 Capacitance	6.34 µF
$\boldsymbol{R_1}$	10 kΩ
$\boldsymbol{R_2}$	8.112 Ω
$\boldsymbol{R_3}$	21.546 mΩ
$\boldsymbol{C_1}$	120.544 pF
$\boldsymbol{C_2}$	2.397 nF
$\boldsymbol{C_3}$	92.278 nF
$\boldsymbol{L_V}$	300 nH

The design optimization variables are in vector $\boldsymbol{x} \in \Re^n$, where n denotes the number of optimization variables considered in the PDN design problem. In this case, $\boldsymbol{x} = [N_{BulkCap}\ N_{CavityCap}\ N_{Pkg0Cap}]^T$, these variables are chosen from the "Equivalent PDN" circuit of Fig. 1.5, the elements of $\boldsymbol{x}$ correspond to the adjustable parameters associated with the decoupling network, specifically the quantities of bulk, cavity, and package 0 decoupling capacitors included in the lumped PDN representation. Bulk capacitors filter low-frequency

fluctuations, cavity capacitors address mid-frequency noise, and package 0 capacitors mitigate high-frequency transients near the die [Ambasana-23].

4.2. Objective Function

Here, the objective function to be minimized is defined, as well as some constraints for the optimization variables. To avoid negative quantities of capacitors and to constrain the maximum number of capacitors, a lower bound as $LB = 1$ and and upper bound $UB = 150$ are used for each element in $\boldsymbol{x}$. The objective function $u: R^n \rightarrow R$ depends on the optimization variables and the corresponding responses of interest, denotes as $Rw(\boldsymbol{x},t)$ and $Rh(\boldsymbol{x},t)$. In this formulation, $Rw(\boldsymbol{x},\mathrm{t})$ contains the PDN voltage ripple response, where t is the simulated time and Rw to the eye width margin.

$Rh(\mathrm{x},\mathrm{t})$, refers to the eye height margin, contains the PDN voltage droop response, the amplitude of the transient voltage of the PDN.

Error vector functions are employed to measure the degree to which the responses satisfy or violate the performance specifications. Although timing jitter is present in the simulated eye diagrams, its mitigation is outside the scope of this work and is therefore not considered as an optimization target. Jitter-related improvements are left for future investigation. In consistency with the UCIe channel at 16-GT/s, the performance specifications selected are a maximum target voltage ripple at 250 mV, and the 0.75 UI (Unit Interval) is the required minimum timing margin. The waveform data:

- Time samples: x_i
- Voltage samples: y_i for $i = 1, \ldots, n$

Constants:

$$H_{target} = 250\ mV, \qquad W_{target} = 0.75\ UI, \qquad R_b = 16\ Gb/s \tag{4-1}$$

Unit interval in ps:

$$UI_{ps} = 10\text{^}3/R_b \ \ for\ R_b = 16\ \ \therefore\ \ UI_{ps} = 62.5\ ps \tag{4-2}$$

The eye width target is 46.87 ps (0.75 UI).

Eye height:

$$y_{max} = \max_i y_i, \qquad y_{min} = \min_i y_i, \tag{4-3}$$

$$Eye\ Height = (y\_max - y\_min) \cdot 1000\ mV \tag{4-4}$$

Threshold level:

$$y_{th} = \frac{y_{max} - y_{min}}{2} \tag{4-5}$$

Eye width in UI:

$$Eye\ width = \frac{width_{ps}}{UI_{ps}} \tag{4-6}$$

As mentioned before, a minimax formulation is used to solve the optimization problem. The optimal design $\boldsymbol{x}^*$ is obtained by solving

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} \max\left\{\boldsymbol{e}_f^{\mathrm{T}}(\boldsymbol{x}, f)\ \boldsymbol{e}_{\mathrm{t}}^{\mathrm{T}}(\boldsymbol{x}, t)\ e_B(\boldsymbol{x})\right\} \tag{4-7}$$

where the error function $e_B(\boldsymbol{x})$ is used to keep the optimization variables within feasible bounds and is defined as

$$e_B(\boldsymbol{x}) = \begin{cases} LB - \boldsymbol{x} \\ \dfrac{N_{BulkCap} + N_{CavityCap} + N_{Pkg0Cap} - 1}{UB} \end{cases} \tag{4-8}$$

The error vector function $\boldsymbol{e}$t($\boldsymbol{x}$, t) is used to ensure a desired maximum target voltage ripple, where f is the simulated frequency, and is defined as

$$\boldsymbol{e}_f^{\mathrm{T}}(\boldsymbol{x}, f) = \begin{cases} 1 - \dfrac{W_{target}(\boldsymbol{x}, f)}{0.75UI} \end{cases} \tag{4-9}$$

The error vector function $\boldsymbol{e}$f($\boldsymbol{x}$, t) is used to ensure a desired maximum transient voltage droop, where t is the simulated time.

$$\boldsymbol{e}_t^{\mathrm{T}}(\boldsymbol{x},t) = \begin{cases} 1 - \dfrac{H_{target}(\boldsymbol{x},t)}{250mV} \end{cases} \tag{4-10}$$

4.3. Conclusions

This chapter introduced a numerical optimization framework for the power delivery network (PDN), the process integrates the validated model into signal integrity simulations for final eye diagram assessment. The PDN design problem was formulated to systematically address multiple signal integrity and power integrity requirements, ensuring compliance with voltage noise and eye diagram specifications for a 16-GT/s UCIe channel.

The framework allows PDN-induced noise effects to be evaluated within the context of full link performance. This integration supports efficient assessment of PDN adequacy without requiring repeated simulations of large, distributed models, thereby improving design efficiency and enabling iterative SI–PI co-design.

5. Results and Comparison of the Simulation Time of the Different Optimization Methods

This chapter presents and analyzes the results obtained from the SI-PI co-simulation and optimization framework developed in the previous chapters. Building on the optimization framework introduced in Chapter 4, this chapter presents the implementation of several numerical optimization methods used to minimize the number of decoupling capacitors required to satisfy UCIe performance specifications.

The following sections apply the Nelder–Mead, Conjugate Gradient, and Quasi-Newton optimization methods to improve eye-diagram performance by refining the PDN decoupling capacitor configuration while maintaining voltage regulator stability. The optimization methods are compared using multiple quantitative criteria, including convergence behavior, number of iterations, total simulation time, and the resulting distribution and total count of decoupling capacitors across the PDN. In addition, eye-diagram metrics, specifically eye height and eye width relative to UCIe compliance masks, are used to assess whether the optimized designs satisfy voltage and timing margin requirements.

By systematically comparing these results, this chapter highlights the trade-offs between derivative-free and gradient-based optimization approaches in simulation driven SI-PI co-design. The findings provide insight into which optimization strategies are most suitable for high-speed PDN design problems where computational efficiency and electrical compliance must be balanced simultaneously.

5.1. General Optimization Flow

Figure 5.1 illustrates the general optimization flow common to all methods employed in this thesis and serves as the unifying framework for all numerical optimization methods implemented in this chapter. As shown in the figure, the process begins with the extraction of an initial distributed PDN model. Following PDN model extraction, an initial estimate of the number of decoupling capacitors is selected. Bounds on the optimization variables are enforced through an error function embedded in the objective function, ensuring that all candidate solutions remain physically meaningful.

Once the initial PDN configuration is defined, one of the selected optimization algorithms, Nelder–Mead, Conjugate Gradient, or Quasi-Newton, is executed. As indicated in Fig. 5.1, the optimization loop proceeds through repeated objective function evaluations. Each evaluation involves a co-simulation step in which MATLAB and Keysight Advanced Design System (ADS) are coupled. MATLAB manages the optimization logic and updates the design variables according to the selected algorithm, while ADS generates the corresponding UCIe eye-diagram, which are then returned to MATLAB for objective function evaluation [Lindfield-00].

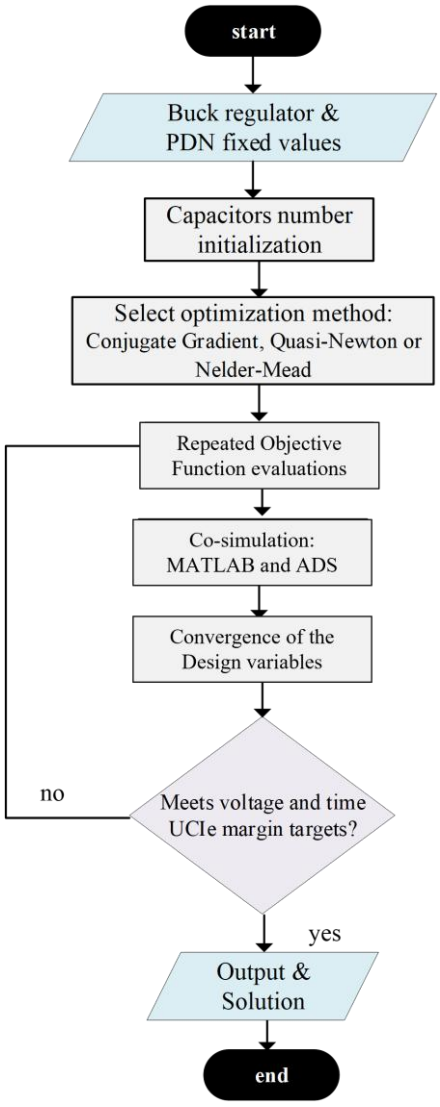

Fig. 5.1 Optimization flow diagram.

The objective function quantifies compliance with UCIe specifications while simultaneously accounting for VR stability criteria, as defined in Chapter 4. Based on this evaluation, the optimization algorithm updates the design variables within their prescribed bounds and advances to the next iteration.

This iterative loop continues until one of the termination criteria indicated in Fig. 5.1 is satisfied, such as convergence of the design variables or reaching the maximum number of iterations. Upon termination, the optimization framework reports the best solution identified during the search. This solution corresponds to a PDN decoupling capacitor configuration that improves UCIe eye-diagram performance while maintaining stable VR operation. The same optimization flow is applied consistently across all numerical methods considered in this chapter, allowing their performance and robustness to be compared under identical modeling and simulation conditions.

5.2. Nelder-Mead Results

The Nelder-Mead optimization method is employed in this thesis as a derivative-free baseline technique for solving the nonlinear optimization problem associated with PDN decoupling capacitor selection [Nelder-65]. This method is particularly well suited for problems in which the objective function is evaluated through time-consuming circuit simulations and where analytical gradients are unavailable or impractical to compute. In MATLAB, the Nelder-Mead algorithm is implemented through the *fminsearch* function, which performs unconstrained nonlinear optimization using a simplex-based direct search strategy [Lagarias-98].

The Nelder-Mead optimization method is applied to the PDN decoupling capacitor minimization problem. This is a derivative-free method and is well suited for simulation-driven optimization problems in which analytics gradients are unavailable and objective function evaluations are computationally expensive.

In this study, the Nelder-Mead algorithm is used to optimized the number of bulk, cavity, and package-level decoupling capacitors while simultaneously enforcing frequency-domain PDN constraints and time-domain eye-diagram requirements for a UCIe link operating at 16 GT/s. Multiple optimization runs were performed using different initial seed values to assess the sensitivity of the method to starting conditions.

The numerical results obtained from these optimization runs are summarized in TABLE 5.1, which lists the initial seed values and the corresponding optimized capacitor distributions. The table shows that, for all tested seeds, the Nelder-Mead algorithm converges to solutions that satisfy the UCIe electrical specifications. However, the final capacitor distributions and total number of decoupling capacitors vary noticeably across different initial conditions. This behavior indicates sensitivity to the starting point and suggests the presence of multiple local optima in the PDN design space, which is characteristic of simplex-based optimization methods.

A more detailed quantitative comparison of the optimized results is provided in TABLE 5.4, which reports the final eye-diagram metrics achieved after Nelder–Mead optimization. These results confirm that UCIe compliance is achieved consistently across all seed values. Nevertheless, optimized solutions generally require a relatively large total number of decoupling capacitors, reflecting a trade-off between robustness and design efficiency.

Fig. 5.2 also demonstrates that different combinations of the selected decoupling capacitor values affect the eye diagram; however, for both baseline cases, the initial PDN configuration fails to meet the UCIe electrical compliance requirements at 16 GT/s. Insufficient timing margin is observed due to supply-induced degradation captured through the SI–PI co-simulation. For the three diagrams, the PDN configuration reflects the initial, non-optimized decoupling capacitor values as described in Chapter 4. This outcome confirms that manual or nominal PDN design is inadequate for this operating regime and motivates the application of systematic numerical optimization

Overall, the Nelder–Mead method proves effective in restoring UCIe signal integrity under supply-noise conditions and serves as a reliable baseline optimization approach. However, its sensitivity to initial conditions, moderate convergence speed, and tendency to produce solutions with higher capacitor counts motivate the exploration of gradient-based optimization methods. The following section applies the Conjugate Gradient algorithm to the same PDN optimization problem and evaluates whether improved convergence efficiency and reduced component count can be achieved.

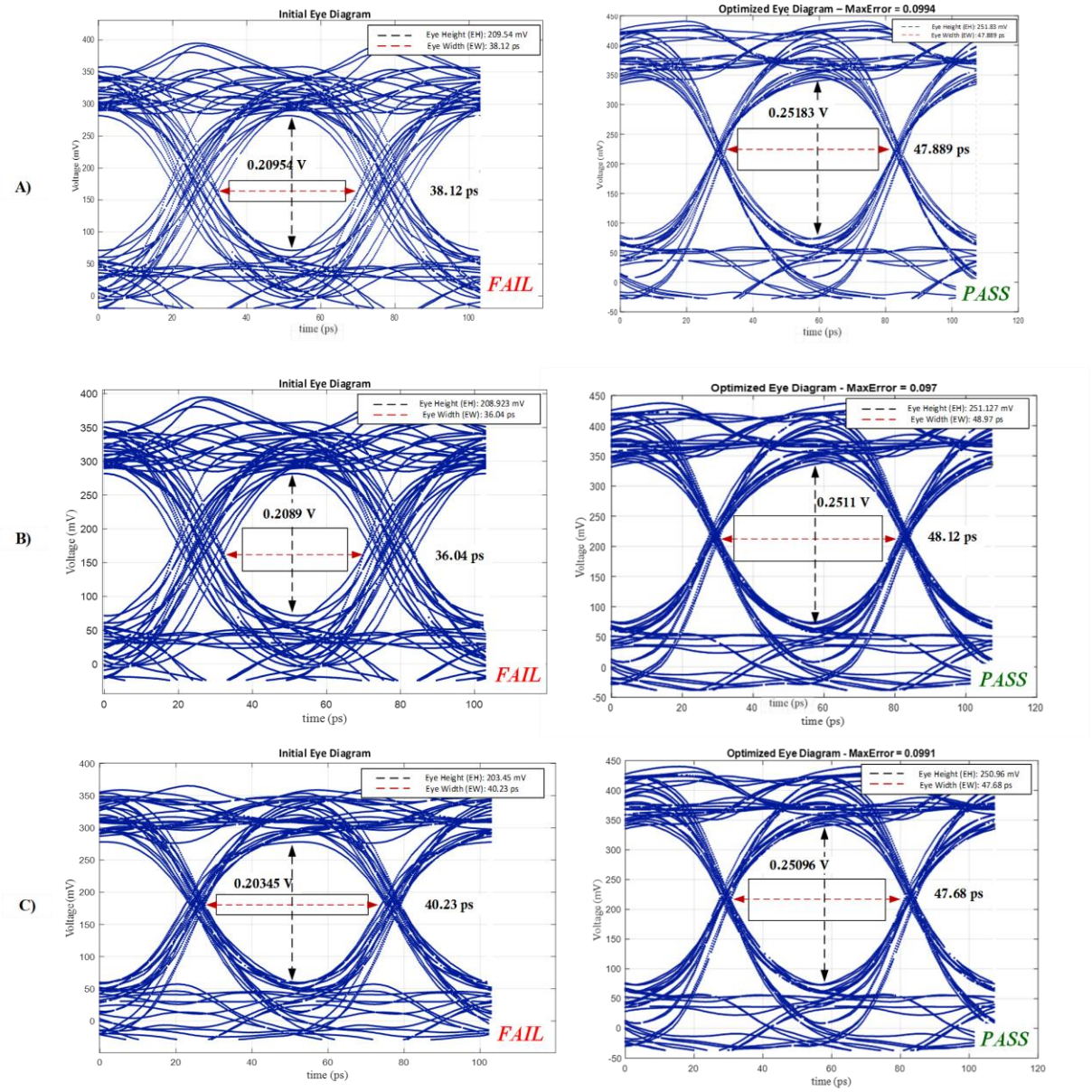

Fig. 5.2 Nelder-Mead method showing: A) Seed [1, 1, 1]; B) Seed [1, 10, 10]; C) Seed [33, 33, 33]; with cavity, bulk, and package 0, and corresponding eye diagram results before and after optimization in accordance with the UCIe specification at 16 GT/s [UCIe-25].

TABLE 5.1. NELDER-MEAD OPTIMIZATION METHOD WITH THREE DIFFERENT SEED INITIAL NUMBER OF CAPACITORS

Capacitor	Cavity	Bulk	Pkg0	Total
Seed A	1	1	1	3
Optimized A	12	59	35	106
Seed B	1	10	10	21
Optimized B	14	54	23	91
Seed C	33	33	33	99
Optimized C	9	58	26	93

5.3. Conjugate Gradient Results

The Conjugate Gradient optimization method is employed in this thesis as a gradient-based approach using the Fletcher–Reeves formulation. Compared to derivative-free techniques, this method can achieve faster convergence when reliable gradient information is available, making it well suited for problems with smooth objective functions and a moderate number of design variables. This custom implementation allows full control over gradient computation, line-search strategy, stopping criteria, and direction-reset mechanisms, ensuring consistency with the minimax objective function defined in Chapter 4. The Fletcher–Reeves formulation constructs a sequence of search directions that are conjugate with respect to a quadratic approximation of the objective function, thereby avoiding the zigzagging behavior commonly observed in steepest descent methods and improving convergence efficiency [Venkataraman-01].

The Conjugate Gradient optimization method is applied to the PDN decoupling capacitor minimization problem [Roda-20]. Unlike the Nelder–Mead method, the Conjugate Gradient algorithm exploits gradient information to accelerate convergence and is theoretically well suited for smooth optimization problems with a moderate number of design variables.

As in the Nelder–Mead study, the Conjugate Gradient method is used to optimize the number of bulk, cavity, and package-level decoupling capacitors while enforcing frequency-domain PDN constraints and time-domain eye-diagram requirements for a UCIe link operating at 16 GT/s. Multiple optimization runs are performed using different initial seed values in order to assess robustness and sensitivity to initial conditions.

The numerical results obtained from the Conjugate Gradient optimization are summarized in TABLE 5.2, which lists the initial seed values and the corresponding optimized capacitor distributions. The results show that, for all tested seeds, the algorithm converges to solutions that satisfy the UCIe electrical specifications in the first and third optimizations, whereas the second optimization does not meet the UCIe criteria. However, compared to the Nelder–Mead method, the Conjugate Gradient approach generally requires a larger number of iterations and function evaluations to reach convergence, reflecting the added computational cost associated with numerical gradient estimation and line-search procedures.

The impact of the Conjugate Gradient optimization on signal integrity is illustrated in Fig. 5.2, which presents representative eye diagrams obtained after convergence. Relative to the

baseline results shown in Section 5.1, the optimized eye diagrams exhibit clear improvements in eye height and eye width, achieving compliance with the UCIe eye mask at 16 GT/s. These results confirm that the Conjugate Gradient method is effective in restoring signal integrity under supply-noise conditions through PDN optimization.

While UCIe compliance is consistently obtained across all seed values, the optimized solutions tend to require a relatively high number of decoupling capacitors, comparable to or

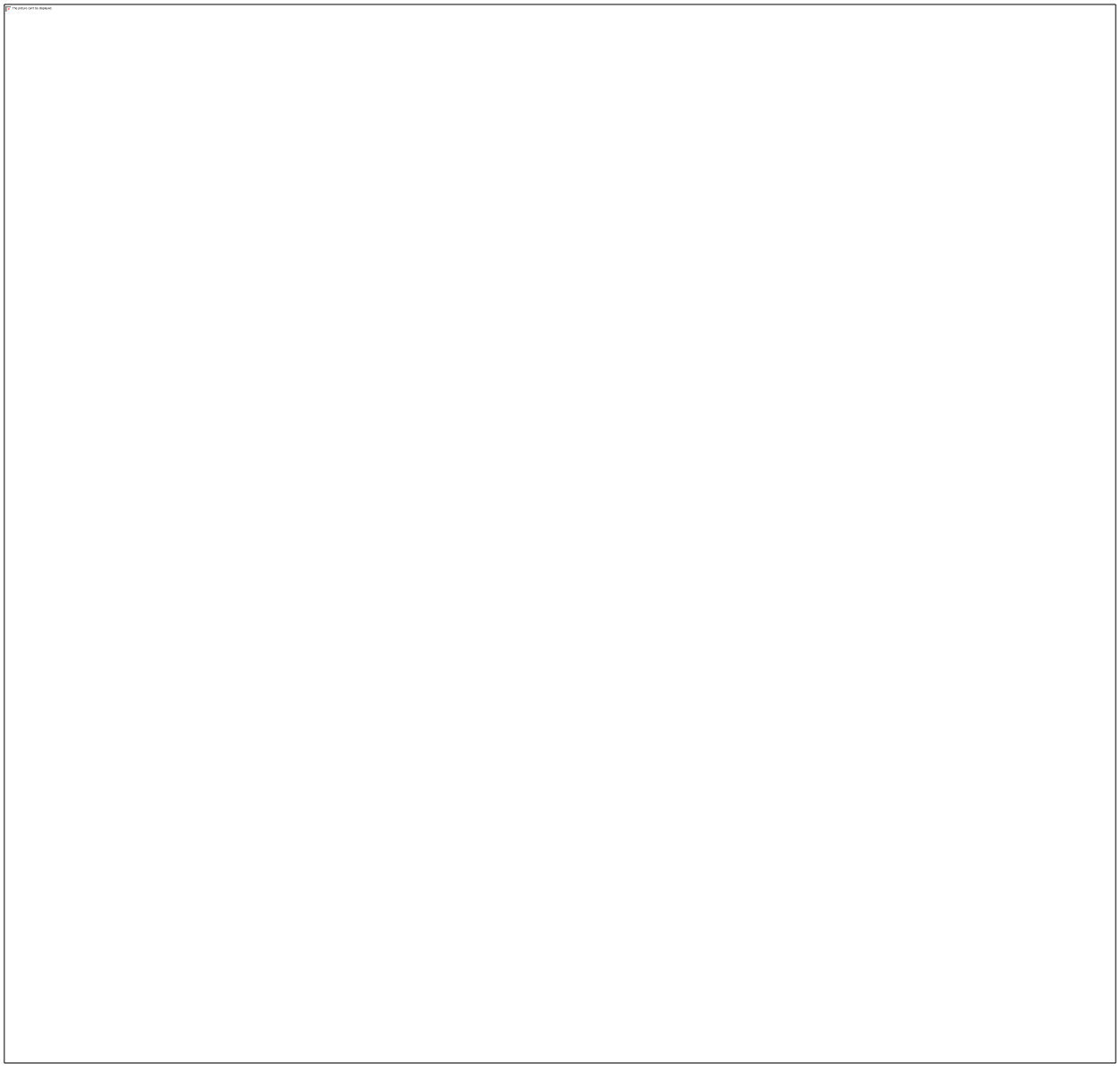

Fig. 5.3 Conjugate Gradient method showing: D) Seed [1, 1, 1]; E) Seed [1, 10, 10]; F) Seed [33, 33, 33]; with cavity, bulk, and package 0, and corresponding eye diagram results before and after optimization in accordance with the UCIe specification at 16 GT/s [UCIe-25].

greater than those produced by the Nelder–Mead method. In addition, noticeable variability in the final capacitor distributions across different seeds indicates continued sensitivity to initial conditions.

Overall, the Conjugate Gradient method successfully achieves UCIe-compliant solutions and demonstrates the feasibility of gradient-based optimization for SI–PI co-design problems. However, the increased computational burden associated with numerical gradient evaluation, together with its sensitivity to initial conditions and limited reduction in total capacitor count, reduces its practical advantage over the derivative-free Nelder–Mead approach in this application. These observations motivate the exploration of Quasi-Newton optimization techniques, which aim to retain the convergence benefits of gradient-based methods while reducing computational cost. The following section applies the Quasi-Newton (BFGS) algorithm to the same PDN optimization problem.

TABLE 5.2. CONJUGATE GRADIENT OPTIMIZATION METHOD WITH THREE DIFFERENT SEED INITIAL NUMBER OF CAPACITORS

Capacitor	Cavity	Bulk	Pkg0	Total
Seed D	1	1	1	3
Optimized D	17	54	18	89
Seed E	1	10	10	21
Optimized E	12	58	18	88
Seed F	33	33	33	99
Optimized F	19	43	14	95

5.4. Quasi-Newton Results

The Quasi-Newton optimization method is employed in this thesis as a gradient-based alternative to the Conjugate Gradient algorithm, with the objective of improving convergence behavior through the use of curvature information. In particular, the Broyden–Fletcher–Goldfarb–Shanno (BFGS) formulation is adopted due to its robustness and widespread use in nonlinear optimization problems [Chong-97] [Broyden-84].

The Quasi-Newton optimization method is applied to the PDN decoupling capacitor minimization problem to evaluate whether improved convergence efficiency and reduced component count could be achieved relative to the Nelder–Mead and Conjugate Gradient

approaches. This method approximates second-order curvature information through iterative updates of an inverse Hessian estimate, enabling faster convergence than standard gradient-based techniques while avoiding the computational expense of exact Hessian evaluation [Venkataraman-01].

As in the previous optimization studies, the Quasi-Newton method is used to optimize the number of bulk, cavity, and package-level decoupling capacitors while enforcing both frequency-domain PDN constraints and time-domain eye-diagram requirements for a UCIe link operating at 16 GT/s. Multiple optimization runs are performed using different initial seed values to assess robustness and sensitivity to initial conditions.

The numerical optimization outcomes are summarized in TABLE 5.3, which lists the initial seed values and the corresponding optimized capacitor distributions obtained using the Quasi-Newton method. Compared to the results obtained with Nelder–Mead and Conjugate Gradient optimization, the Quasi-Newton approach consistently converges to solutions with a reduced total number of decoupling capacitors. In addition, the final capacitor distributions show less variability across different initial seeds, indicating improved robustness and reduced sensitivity to starting conditions.

The improvement in signal integrity achieved through Quasi-Newton optimization is illustrated in Fig. 5.3, which presents representative eye diagrams obtained after convergence. Relative to the baseline eye diagrams shown in Section 5.1 and to the optimized results obtained with the previous methods, the Quasi-Newton solutions exhibit wider and cleaner eye openings, with increased eye height and eye width. The results show that, while the first optimization case failed to satisfy the UCIe eye-mask requirements at 16 GT/s, the optimized eye diagrams in the second and third cases do meet these requirements, confirming that the reduced capacitor configurations in these cases remain fully compliant with the electrical specifications.

A more detailed quantitative summary of the optimization performance is provided in TABLE 5.4, which reports the number of iterations, function evaluations, and total optimization time required for each seed value. The results demonstrate that the Quasi-Newton method achieves convergence with fewer iterations and function evaluations than both Nelder–Mead and Conjugate Gradient methods. This improvement reflects the benefit of incorporating approximate curvature information through the BFGS update, which enables more efficient navigation of the PDN design space.

Overall, the Quasi-Newton optimization method demonstrates superior performance for the PDN decoupling capacitor minimization problem considered in this work. It consistently achieves UCIe-compliant eye-diagram performance while requiring fewer decoupling capacitors and reduced computational effort. These results indicate that Quasi-Newton methods offer a favorable balance between robustness, convergence efficiency, and design optimality for SI–PI co-design problems involving simulation-driven objective functions. The following section

Fig. 5.4 Quasi-Newton method showing: G) Seed [1, 1, 1]; H) Seed [1, 10, 10]; I) Seed [33, 33, 33]; with cavity, bulk, and package 0, and corresponding eye diagram results before and after optimization in accordance with the UCIe specification at 16 GT/s [UCIe-25].

compares the computational cost and simulation resources required by all three optimizations methods in a unified manner.

TABLE 5.3 QUASI-NEWTON OPTIMIZATION METHOD WITH THREE DIFFERENT SEED INITIAL NUMBER OF CAPACITORS

Capacitor	Cavity	Bulk	Pkg0	Total
Seed G	1	1	1	3
Optimized G	6	31	39	76
Seed H	1	10	10	21
Optimized H	24	45	13	82
Seed I	33	33	33	99
Optimized I	18	43	9	70

5.5. Co-simulation Time and Computing Resources

This section compares the computational cost and simulation resources required by the three optimization methods considered in this chapter and contrasts their performance. All simulations were executed on the same hardware platform to ensure a fair comparison. The simulations were run on a conventional laptop equipped with an Intel Core Ultra 7 165U processor operating at 1.7 GHz and 32 GB of RAM, demonstrating that the proposed optimization framework can be executed without access to high-performance computing resources.

The average number of iterations and total optimization time required by each method are summarized in TABLE 5.4. Among the three automated optimization approaches, the Quasi-Newton method consistently achieves convergence with the fewest iterations and the lowest total elapsed time. On average, the Quasi-Newton algorithm requires 124 iterations and approximately 385 seconds to converge. The Nelder–Mead method follows with an average optimization time of approximately 423 seconds, while the Conjugate Gradient method exhibits the highest computational cost, requiring an average of approximately 494 seconds. The increased runtime of the Conjugate Gradient approach is primarily attributed to the numerical gradient evaluations and line-search procedures required at each iteration. The Quasi-Newton method demonstrates the highest computational efficiency among the evaluated approaches, as evidenced by its requirement for the fewest function evaluation calls.

To provide additional context for these results, TABLE 5.5 compares the computational resources required by the three automated optimization methods. The table highlights the relative efficiency of each approach in terms of total elapsed simulation time. Among the methods evaluated, the Nelder–Mead algorithm exhibits the lowest normalized execution time, followed by the Conjugate Gradient and Quasi-Newton methods. Despite these differences, all three optimization strategies demonstrate comparable orders of magnitude in computational cost, confirming that automated optimization enables efficient exploration of the PDN design space within a practical runtime envelope.

TABLE 5.4 SIMULATION TIME COMPARISON OF THE OPTIMIZATION MODELS

	Nelder-Mead			Conjugate Gradient			Quasi-Newton		
Seed Value	Iteration #	Function Evaluations	Time [s]	Iteration #	Function Evaluations	Time [s]	Iteration #	Function Evaluations	Time [s]
[1 1 1]	145	286	445	233	397	531.1	135	135	415.1
[1 10 10]	131	243	394	198	367	490.3	121	259	378.2
[33 33 33]	150	339	430.2	181	312	460.2	116	198	360.8
Average	142	289.33	423.066	204	358.66	493.866	124	226.66	384.7

It is important to note that, in all cases, the transient simulation dominates the total computational cost, consuming the majority of the elapsed simulation time. This observation is consistent with expectations for SI–PI co-simulation workflows, where time-domain analyses are significantly more expensive than frequency-domain or steady-state simulations.

TABLE 5.5. SIMULATION RESOURCES COMPARISON OF THE OPTIMIZATION MODELS

Modeling Type	Total elapsed time (seconds)
Conjugate-Gradient model	423.066
Quasi-Newton model	493.866
Nelder-Mead model	384.7

Among the automated methods evaluated, the Quasi-Newton algorithm offers the most favorable balance between convergence speed, computational cost, and design efficiency, reinforcing its suitability for simulation-driven SI–PI co-design in high-speed UCIe systems.

5.6. Conclusions

This chapter presented a comparative evaluation of three numerical optimization methods, Nelder–Mead, Conjugate Gradient, and Quasi-Newton, applied to the problem of decoupling capacitor minimization in a power delivery network under UCIe signal-integrity constraints. The analysis was carried out using a unified SI–PI co-simulation framework and identical modeling assumptions, enabling a direct and fair comparison of the methods.

The results demonstrate that all three optimization approaches are capable of achieving UCIe-compliant eye-diagram performance at 16 GT/s when appropriate PDN configurations are identified. In each case, the optimization process successfully mitigates supply-induced signal degradation and restores both eye height and eye width to within the specified compliance limits. These findings confirm the effectiveness of automated optimization for PDN design in high-speed chiplet-based systems.

However, significant differences are observed in convergence behavior, robustness, and design efficiency. The Nelder–Mead method provides a robust, derivative-free baseline and consistently converges to compliant solutions, but exhibits sensitivity to initial seed values and typically results in higher total decoupling capacitor counts. The Conjugate Gradient method, while theoretically benefiting from gradient information, incurs additional computational overhead due to numerical gradient evaluation and line-search procedures, and does not offer a clear advantage in terms of convergence speed or component reduction for this application.

In contrast, the Quasi-Newton method demonstrates superior overall performance, achieving compliant solutions with fewer iterations, reduced sensitivity to initial conditions, and consistently lower total decoupling capacitor counts. By incorporating approximate curvature information through the BFGS update, the Quasi-Newton algorithm navigates the PDN design space more efficiently and provides a favorable balance between computational cost and design optimality.

Overall, the results of this chapter indicate that Quasi-Newton optimization offers the most effective strategy among the methods evaluated for simulation-driven SI–PI co-design problems. These findings motivate the use of quasi-Newton techniques for practical PDN optimization workflows and provide a strong foundation for the broader conclusions drawn in the following chapter.

General Conclusions

This thesis presented a simulation-driven methodology for the co-design of signal integrity (SI) and power integrity (PI) in high-speed chiplet-based systems compliant with the Universal Chiplet Interconnect Express (UCIe) standard. By integrating power delivery network (PDN) modeling, high-speed channel simulation, and numerical optimization within a unified SI–PI co-simulation framework, the proposed approach enables systematic evaluation and optimization of PDN design choices under realistic operating conditions.

A central contribution of this thesis is the formulation of the PDN design problem as a constrained optimization task in which the number of decoupling capacitors is treated explicitly as a design variable. Rather than relying on heuristic or over-provisioned decoupling strategies, the proposed framework identifies PDN configurations that satisfy UCIe electrical requirements, specifically eye height and eye width at 16 GT/s, while minimizing component count. This formulation directly links PDN behavior to signal-level performance, demonstrating the importance of co-simulation for high-speed interfaces in dense packaging environments.

The SI–PI co-simulation methodology developed in this work combines frequency-domain PDN analysis, time-domain transient simulations, and eye-diagram evaluation within a single automated workflow. Keysight ADS is used as the primary circuit simulation environment, while MATLAB provides automation, parameter control, and optimization logic. This integration enables repeatable and efficient exploration of the PDN design space and allows the impact of supply-induced noise on high-speed signaling to be quantified directly.

Three numerical optimization methods, Nelder–Mead, Conjugate Gradient, and Quasi-Newton, were implemented and evaluated using identical modeling assumptions and constraints. The comparative results demonstrate that all three methods are capable of achieving UCIe-compliant eye-diagram performance when appropriate PDN configurations are identified. However, clear differences emerge in convergence behavior, robustness to initial conditions, and design efficiency. Among the evaluated methods, the Quasi-Newton algorithm consistently provides the best overall performance, achieving compliant solutions with fewer iterations, reduced sensitivity to initial seed values, and lower total decoupling capacitor counts. These results highlight the advantages of incorporating approximate curvature information in simulation-driven SI–PI optimization problems.

From a practical perspective, the results confirm that automated numerical optimization is an effective and scalable approach for PDN design in high-speed chiplet systems. The proposed framework enables engineers to move beyond manual tuning and intuition-based design, providing a systematic path toward PDN configurations that balance electrical performance, component count, and computational cost. Importantly, the entire workflow is demonstrated on a conventional computing platform, indicating that the methodology is accessible and applicable in typical design environments.

While this thesis focuses on a UCIe channel operating at 16 GT/s and on decoupling capacitor count as the primary optimization variable, the methodology is general and extensible. Future work may include extending the optimization framework to higher UCIe data rates, incorporating additional PDN parameters such as capacitor placement and parasitic variation, and integrating jitter and timing-noise metrics directly into the objective function.

In summary, this thesis demonstrates that SI–PI co-simulation combined with numerical optimization provides a powerful and practical approach for PDN design in next-generation chiplet-based systems. The proposed methodology establishes a foundation for more advanced co-design strategies in which signal integrity, power integrity, performance, and cost are addressed simultaneously within a unified design framework.

Appendices

A. MATLAB SCRIPTS

1. ADS-Keysight Driver Code

```
% MATLAB           Michel Ibarra             May, 2025
% Utility Functions required:
% cell2file, file2cell, cell2matrix, ADSformatRawFile


function  [xData,yData] = UCIe_script(x)

% ADS Netlist File Name
ScriptFileName = 'netlist.log';

% Define ADS netlist as a parameterized Cell array, ca
ar = 'ASCII_Rawfile=yes';

% Number of parallel capacitors
C1 = num2str(x(1));
C2 = num2str(x(2));
C3 = num2str(x(3));

ca{1} = '; Top Design: "SSO_Simulation_lib:Lab3:schematic"';
ca{2} = '; Netlisted using Hierarchy Policy: "Standard"';
ca{3} = ['Options ResourceUsage=yes ' ar ' UseNutmegFormat=no EnableOptim=no
TopDesignName="SSO_Simulation_lib:Lab3:schematic" DcopOutputNodeVoltages=yes
DcopOutputPinCurrents=yes DcopOutputAllSweepPoints=no DcopOutputDcopType=0'];
ca{4} = 'simulator lang=spice';
...
ca{95} = 'V_Source:SRC3  ven 0 Type="V_DC" Vdc=1.2 V SaveCurrent=1';
ca{96} = ['C={' C1, ',' C2, ',' C3 ',33,33}'];


% Save Cell Array into and ASCII File
cell2file(ca,ScriptFileName);

system(['hpeesofsim -r spectra.raw ' ScriptFileName]);

format shortEng;
format compact;
fid = fopen('spectra.raw','r');

linesToSkip = 269298;

for ii = 1:linesToSkip-1
    fgetl(fid);
end

% Read data in from csv file
readData = textscan(fid,'%f %f %f','Headerlines',1,'Delimiter',',');
```

```
% Extract data from readData
index_Data = readData{1,1}(:,1);
% Identify the unique indices
uni_idx=unique(index_Data);
xData = readData{1,2}(:,1);
yData = readData{1,3}(:,1);

% Erase Output Files
delete spectra.raw;
```

2. Nelder Mead Code

```
%% Fminsearch optimization algorithm

options = optimset('Display', 'iter', 'MaxIter',1000);
[xopt,FunEval, EF, output_fmin]=fminsearch(@objective_function_check,x,options);
ResultsTable1 = table(output_fmin.iterations, output_fmin.funcCount,
EF,'VariableNames', {'Iterations', 'Function_Evals', 'Exit_Flag'});

% % Load your eye diagram data using the UCIe_script function
[xData1, yData1] = UCIe_script(xopt);
```

3. Conjugate Gradient Code

```
function [x, Iter, FunEval, EF] = Conjugate_Gradient(fun, x0, MaxIter, epsg, epsx)
    % Conjugate Gradient optimization algorithm using Fletcher-Reeves formula
    %
    % Inputs:
    %   fun: function handle to the objective function
    %   x0: initial guess (row vector)
    %   MaxIter: maximum number of iterations
    %   epsg: gradient tolerance
    %   epsx: minimum relative change in x
    %
    % Outputs:
    %   x: optimized solution
    %   Iter: number of iterations
    %   FunEval: number of function evaluations
    %   EF: exit flag
    %       1: successful optimization (gradient is small enough)
    %       2: algorithm converged (relative change in x is small enough)
    %      -1: maximum iterations reached without convergence

    % Initialize variables
    x = x0;                     % Initial guess
    g = Grad(fun, x);           % Compute initial gradient
    d = -g;                     % Initial search direction (steepest descent)
    Iter = 0;                   % Initialize iteration counter
    FunEval = 0;                % Initialize function evaluations
    EF = 0;                     % Exit flag
    reset_period = length(x0);  % Reset search direction every n iterations
```

```
    % Iterative process
    while Iter < MaxIter
        Iter = Iter + 1;         % Increase iteration count
        FunEval = FunEval + 1;   % Count function evaluations
        g_norm = norm(g);        % Compute gradient norm

        % Line search: optimize step size along direction d
        linesf = @(alpha) fun(x + alpha * d');  % Function to minimize
        alpha_opt = fminbnd(linesf, 0,1);       % Using fminbnd command for step size
alpha
        x_new = x + alpha_opt * d';             % Update x

        rel_change = norm(x_new - x) / (norm(x) + eps); % Avoid division by zero

        % Stopping criteria: check gradient norm
        if g_norm < epsg
            EF = 1;                              % Successful optimization, gradient
is small enough
            break;
        elseif rel_change < epsx                 % Compute relative change in x
            EF = 2;                              % Algorithm converged
            break;
        end

        % Compute new gradient
        g_new = Grad(fun, x_new);                % Gradient at the new x
        FunEval = FunEval + 1;                   % Count function evaluation

        % Compute Fletcher-Reeves beta
        beta = (norm(g_new)^2) / (norm(g)^2);

        % Reset search direction every n iterations
        if mod(Iter, reset_period) == 0
            d = -g_new;
        else
            d = -g_new + beta * d;
        end

        % Update values
        x = x_new;
        g = g_new;
    end

    % If maximum iterations exceeded, set exit flag to -1
    if Iter >= MaxIter
        EF = -1;
    end
end
```

4. Quasi-Newton BFGS Code

```
function [x, Iter, FunEval, EF] =  Quasi_Newton_BFGS(fun, x0, MaxIter, epsg, epsx)
```

```
    % BFGS Quasi-Newton Optimization Algorithm
    %
    % Inputs:
    %   fun: function handle to the objective function
    %   x0: initial guess (row vector)
    %   MaxIter: maximum number of iterations
    %   epsg: gradient tolerance
    %   epsx: minimum relative change in x
    %
    % Outputs:
    %   x: optimized solution
    %   Iter: number of iterations
    %   FunEval: number of function evaluations
    %   EF: exit flag
    %       1: successful optimization (gradient is small enough)
    %       2: algorithm converged (relative change in x is small enough)
    %      -1: maximum iterations reached without convergence

    % Initialize variables
    x = x0(:);                  % Ensure column vector, initial guess
    Iter = 0;                   % Initialize iteration counter
    FunEval = 0;                % Initialize function evaluations
    EF = 0;                     % Exit flag
    B = eye(length(x));                 % Initial inverse Hessian approximation
    g = Grad(fun, x);           % Compute initial gradient
    n = length(x);              % Number of elements
    while Iter < MaxIter


        % Compute search direction
        d = -B * g';

        % Line search: optimize step size along direction d
        linesf = @(alpha) fun(x + alpha * d);    % Function to minimize
        alpha_opt = fminbnd(linesf, 0,1);            % Using fminbnd command for step
size alpha
        x_new = x + alpha_opt * d;                      % Update x

        % Compute new function value and gradient
        g_new = Grad(fun, x_new);
        FunEval = FunEval + 1;

        rel_change = norm(x_new - x) / (norm(x) + eps); % Avoid division by zero
        g_norm = norm(g_new);        % Compute gradient norm
        % Stopping criteria: check gradient norm
        if g_norm < epsg
            EF = 1;  % Successful optimization, gradient is small enough
            break;
        elseif rel_change < epsx % Compute relative change in x
            EF = 2;  % Algorithm converged
            break;
        end

        % BFGS Update formula
        s = x_new - x;
```

```
        y = g_new - g;

      % BFGS Update formula
        rho = 1 / (y' .* s);
        I = eye(n);
        B = (I - rho .* s .* y') .* B .* (I - rho .* y .* s') + rho .* (s .* s');

        % Update variables
        x = x_new;
        g = g_new;
        Iter = Iter + 1;         % Increase iteration count
        FunEval = FunEval + 1;   % Count function evaluations

    end

    % If max iterations reached, set EF to -1
    if Iter >= MaxIter
        EF = -1;
    end
end
```

5. Objective Function Code

```
function MaxError = objective_function16G(x)
    % Inputs: x = [N_BulkCap, N_CavityCap, N_PkgoCap]
    % Objective: Penalize designs that fail to meet eye height and width targets

    % UCIe specification targets
    eyeHeightTarget = 250;   % mV
    eyeWidthTarget = 0.75;   % UI
    bitrate_Gbps = 16;
    UI_ps = 1e3 / bitrate_Gbps;

    % Run ADS simulation
    [xData, yData] = UCIe_script(x);

    % Eye Metrics
    eyeHeight = (max(yData) - min(yData)) * 1000;  % in mV
    yThresh =(max(yData)+min(yData))/2;
    crossings = find(diff(yData > yThresh));
    if length(crossings) >= 2
        width_ps = xData(crossings(end)) - xData(crossings(1));
    else
        width_ps = 0;
    end
    eyeWidth = width_ps / UI_ps;

    % eB Penalty
    LB = 1;                % Lower bound
    UB = 100;              % Upper bound
    N_BulkCap    = x(1);
    N_CavityCap  = x(2);
    N_PkgoCap    = x(3);
```

```
    % Eqn (4-2): eB(x)
    eB = max( [LB-N_BulkCap, LB-N_CavityCap, LB-N_PkgoCap,...
               N_BulkCap+N_CavityCap+N_PkgoCap-1, ...
               N_BulkCap-UB, N_CavityCap-UB, N_PkgoCap-UB] );

    % Eqn (4-3): ef^T(x,f) - Voltage Ripple (Eye Width, assumes Rw = eyeWidth)
    ef = 1 - (eyeWidth / eyeWidthTarget); % penalize if less than target

    % Eqn (4-41): et^T(x,t) - Transient Droop (Eye Height, assumes Rh = eyeHeight)
    et = 1 - (eyeHeight / eyeHeightTarget); % penalize if less than target

    ef = max(0, ef);
    et = max(0, et);
    eB = max(0, eB);

    % Combine all errors
    e = [ef et eB];
    MaxError = max(e);  % minimax error

    % plot for visualization
    figure; clf;
    plot(xData, yData* 3.1, 'k.');
    xlabel('Time (ps)'); ylabel('Voltage (V)');
    title(sprintf('Eye Diagram - MaxError = %.3f', MaxError));
    grid on;
    drawnow;

    % Debug print
    disp(['EyeHeight = ', num2str(eyeHeight, '%.1f'), ' mV, EyeWidth = ',
num2str(eyeWidth, '%.2f'), ' UI, eB = ', num2str(eB, '%.2f'), ', MaxError = ',
num2str(MaxError, '%.3f')]);
    fprintf('N_BulkCap: %.2f \n', N_BulkCap);
    fprintf('N_CavityCap: %.2f \n', N_CavityCap);
    fprintf('N_PkgoCap: %.2f \n', N_PkgoCap);
end
```

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