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Fast Jitter Tolerance Testing for High-Speed Serial Links in Post-Silicon Validation

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***Abstract*— Post-silicon electrical validation of high-speed input/output (HSIO) links is a critical process for product qualification schedules of high-performance computer platforms under current aggressive time-to-market (TTM) commitments. Improvements in signaling methods, circuits, and process technologies have allowed HSIO data rates to scale well beyond 10 Gb/s. Noise and EM effects can create multiple signal integrity problems, which are aggravated by continuously faster bus technologies. The goal of post-silicon validation for HSIO links is to ensure design robustness of both receiver (Rx) and transmitter (Tx) circuitry in real system environments. One of the most common ways to evaluate the performance of a HSIO link is to characterize the Rx jitter tolerance (JTOL) performance by measuring the bit error rate (BER) of the link under worst stressing conditions. However, JTOL testing is extremely time-consuming when executed at specification BER considering manufacturing process, voltage, and temperature (PVT) test coverage. In order to significantly accelerate this process, we propose a novel approach for JTOL testing based on an efficient direct search optimization methodology. Our approach exploits the fast execution of a modified golden section search with a high BER, while overcoming the lack of correlation between different BERs by performing a downward linear search at the actual target BER until no errors are found. Our proposed methodology is validated in a realistic industrial server post-silicon validation platform for three different computer HSIO links: SATA, USB3, and PCIe3.**

***Index Terms*— bit error rate, golden section, HSIO link, ISI, jitter, jitter tolerance, PCIe, post-silicon validation, SATA, USB.**

I. I. Introduction

Noise and undesired electromagnetic (EM) effects, such as jitter, inter-symbol interference (ISI), attenuation, reflection, crosstalk, and others, can create multiple signal integrity problems for high-speed input/output (HSIO) circuits in computer platforms. This is aggravated by the fact that channel speeds keep increasing from one generation bus technology to the next one. In general, the higher the signaling frequency, the more vulnerable the interconnect becomes to undesired EM effects. This is of particular concern for HSIO interfaces, such as Peripheral Component Interconnect Express (PCIe), Serial Advanced Technology Attachment (SATA), Universal Serial Bus (USB), and Ethernet interfaces.

Post-silicon electrical validation implies testing hundreds of silicon samples in realistic system application conditions, with the purpose of checking design robustness by measurements on both receiver (Rx) and transmitter (Tx) circuitry of the HSIO links. These measurements must comply with industrial standards, ensuring correct operation under worst case stressing conditions [1]. The combined effects of product complexity, performance requirements, and time-to-market (TTM) add tremendous pressure on industrial post-silicon validation. These challenges motivate the quest for novel strategies to make reliable validation faster and cheaper [1].

One of the most common ways to assess the performance of a HSIO link is by measuring the bit error rate (BER) of the link [2]. BER measurement is typically used to characterize the Rx jitter tolerance (JTOL) to determine compliance with industry standard specifications, such as XAUI [3], PCIe [4], USB [5], and SATA [6]. The goal of JTOL testing is to verify that the Rx under test is capable to operate at an acceptable BER under worst case signaling conditions. JTOL is usually measured with a BER tester (BERT) instrument by sweeping the injected periodic jitter (J_P) amplitude across a range of frequencies until bit errors are detected. The test is passed when the measured error-free J_P amplitude is above the threshold defined by the protocol specification for each frequency point. A typical JTOL test can take several hours.

Fast and reliable JTOL testing methods are of great interest to industry. Most of the alternative methods use extrapolation to save testing time. However, extrapolation is only as good as the model used to describe the behavior of the device under test (DUT), which has prevented the wide adoption of these methods for compliance testing [7]. The extrapolated results may be useful in jitter problem solving, but uncertainty compared to a direct measurement persists. Therefore, there is currently a demand from the test instrumentation user community for faster measurement methods.

In this paper, we present a novel approach to dramatically accelerate JTOL testing based on a modified golden section direct search optimization algorithm. As demonstrated in Section V, our approach to accelerate JTOL testing follows a completely different strategy to those reported in the literature. Our proposed method exploits the fast convergence of the golden section algorithm, modified for a binary objective function, and applied with a high BER, with no need of gradients estimation. The lack of correlation between different BERs is solved by performing a downward linear search at the

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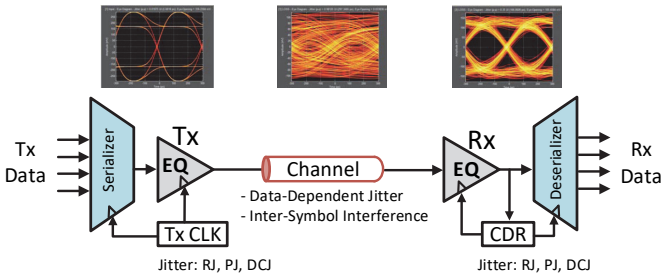

Fig. 1. Main sources of jitter in a HSIO link in post-silicon computer platforms' validation. Equalization (EQ) coefficients are tuned to cancel out the undesired effects.

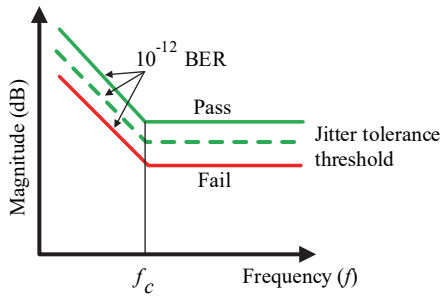

Fig. 2. Rx jitter tolerance threshold for testing [16].

actual target BER until no errors are seen, requiring just a few additional evaluations. Our proposed method is validated by applying it to three different computer HSIO links in a realistic industrial server platform: SATA, USB3, and PCIe3; demonstrating that JTOL testing can be extremely accelerated with respect to the current industrial practice.

This paper significantly expands our work in [8] by incorporating the following new aspects: a) several additional jitter measurement techniques are provided to complete the current industrial practice for which our proposed methodology is applicable; b) an updated and more complete review on existing approaches to speed-up JTOL testing is presented; c) more details are provided regarding the proposed modified golden section search strategy to deal with discrete (binary) objective functions; and d) further validation of our JTOL testing approach is achieved by two additional and more complex HSIO computer interfaces, USB and PCIe, whose bandwidth limitations, data rates, and more complex calibration procedures, render harder test cases to our methodology, confirming the robustness of the proposed methodology.

The rest of our paper is organized as follows. Section II provides a brief description of post-silicon validation. Section III describes JTOL testing. Section IV reviews existing techniques to speed-up JTOL testing. The proposed optimization technique to accelerate JTOL testing is presented in Section V. Finally, Sections VI and VII present the results obtained and our conclusions, respectively.

II. Post-Silicon Electrical Validation

In the context of modern computer platforms testing, silicon validation can be generally classified as pre-silicon and post-silicon. During the pre-silicon stage, testing is implemented in a virtual environment with complex simulation models, emulation and formal verification tools. Once the first silicon is available at the laboratory, post-silicon validation is done in a system environment looking for bugs that cannot be found in pre-silicon validation. In that stage, validation is performed at several levels, including functional validation (FV), bench design validation (BDV), and electrical validation (EV), among others. All of these validation levels are executed in parallel, with the objective of qualifying a product over different operation conditions, process corners, and usage models [9].

EV focuses on testing electrical parameters and EM phenomena, as well as performance of microprocessor circuitry in a system environment. This includes validation of HSIO links, phase-locked loops (PLLs), analog/mixed-signal circuits, clock network, power delivery network, and physical layer (PHY) equalization settings tuning. The goal is to statistically validate the electrical/EM behavior in a real system environment across different process corners and operating conditions. Such a validation leads to a reasonable product release qualification (PRQ) decision.

A large portion of EV is devoted to the validation of HSIO links. Given that the data rate of HSIO interfaces is in the order of several gigabits per second (Gbps), the specifications associated to those interfaces regarding the timing budget is very stringent. This timing budget is reflected in several jitter specifications. On the Tx side, it is specified by the amount of timing deviation the Tx can generate to consume the total jitter budget. Whereas on the Rx side, it specifies how much timing deviation the Rx can tolerate before a false detection occurs.

III. Jitter Tolerance Testing in Post-Silicon Validation

Post-silicon electrical validation looks for Rx jitter tolerance performance in order to determine compliance with the industry standard specifications for all HSIO links, which implies using industry standard instruments and following standard protocols for jitter testing.

In a typical PHY serializer/de-serializer (SerDes), the clock data recovery (CDR) circuitry generates from the received serial data a clock to re-time the received data, which are restored to parallel format by the de-serializer. This SerDes mechanism needs encoding and decoding logic to manipulate the transmitted data transition density to ensure that the CDR works correctly. The CDR guarantees that the clock and data are in phase when the jitter frequency is in the bandwidth of the CDR. However, if there is high frequency jitter in the data stream, the CDR may not track the data, yielding bit errors. Limiting jitter to meet typical BER targets is critical when designing a robust Rx architecture [10], [11].

Typical jitter sources in HSIO links that contribute to the overall accumulated jitter at the Rx are illustrated in Fig. 1. Some level of jitter is already induced by the non-ideal clock synthesizer inside the Tx. Depending on the channel quality, ISI as well as reflections and crosstalk may degrade the signal

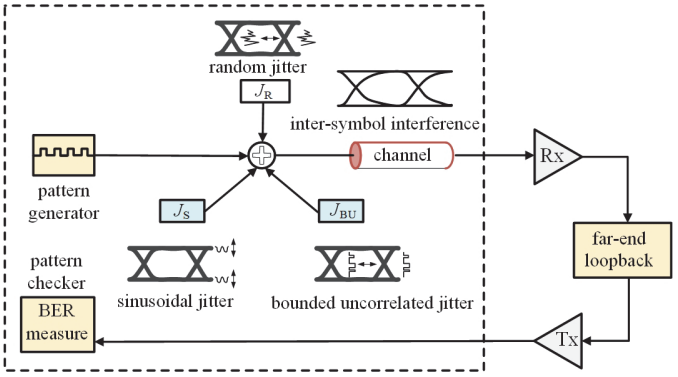

Fig. 3. A generic test setup for Rx jitter tolerance (JTOL) testing.

integrity through the transmission media. At the Rx side, a non-ideal equalizer and the PLL inherent phase noise of the CDR will additionally induce their own timing jitter [12]-[15].

JTOL testing consists of verifying that the measured Rx clock-recovery tolerance across frequencies is above the target threshold. If the measured JTOL curve is above the threshold curve, it indicates a passing result, thus the Rx can tolerate more jitter. On the other hand, if the measured curve is below the threshold curve, it indicates a failing result. Both scenarios are depicted in Fig. 2 [16].

HSIO links specifications require the measurement of various jitter components, which can be performed using different techniques, such as time interval error (TIE) measurement, jitter histograms, JTOL, and BER bathtub, among others. To perform a JTOL test, each protocol specification defines a calibration procedure prior to the JTOL execution. This procedure defines the specific random jitter (J_R), bounded uncorrelated jitter (J_{BU}), duty-cycle distortion (DCD), and ISI values injected to the test pattern, which remain constant throughout the JTOL test, while J_P is varied in both amplitude and frequency.

In the traditional way to run JTOL testing, at each frequency point, the value of J_P is initialized at a sufficiently low starting point to guarantee a PASS result from the BER tester (BERT). Then, J_P is increased by a certain amount, typically equivalent to the minimum value allowed by the BERT equipment for best accuracy. Then, a test is performed at the compliance BER. This is iteratively done until the BER tester yields a FAIL. The result reported at each frequency point is the last J_P value that yields a PASS.

Figure 3 shows a generic JTOL testing setup. It requires an instrument capable of generating a protocol-compliant test pattern and an error detector to measure the BER. Jitter measured with a BERT is the standard against which other methods are judged. Instead of quantifying the jitter of a system's own signals, a BERT provides a bit stream and compares the system's output to the known input.

The relationship between test time and BER confidence level is studied in [17] and [18], finding that the quantity N of data bits needed to guarantee a target BER is

$$N = \frac{1}{B}\left[-\ln(1-a)+\ln\left(\sum_{k=0}^{E}\frac{(N\times B)^k}{k!}\right)\right] \quad (1)$$

where B is the desired BER level, a specifies the statistical probability or confidence level of a BER value being less than B, and E is the number of detected errors. When no bit errors occur (E = 0), then the second term of (1) is zero and the solution is simplified. Assuming a confidence level a = 95%, it is necessary to transmit $N = 3\times10^{12}$ bits without errors in order to meet a BER = 10^{-12}, as typically defined in HSIO standards with no forward error correction.

For instance, in SATA3 the time per testing frequency point per jitter amplitude step is N/speed = $(3\times10^{12}\text{b})/(6\times10^{9}\text{bps})$ = 8.3 minutes. In order to build a chart as that one in Fig. 2, several frequency points specified in the corresponding protocol standard must be tested. In the case of SATA, 5 frequency points are needed. Following the conventional JTOL testing procedure, each frequency point is tested by increasing the jitter amplitude until a BER failure is found. Assuming a margin of 100 mUI per frequency point from the starting point until a BER test fails, and a test equipment configured to change the jitter amplitude in steps of 3 mUI, it would take 33 measurements per frequency point. In addition, each test is repeated 3 times in order to capture and analyze the measurement noise, yielding a test execution of around 68.5 hours. Such a long time for a single JTOL test is prohibitive in PHY tuning and high-volume production testing, especially when considering that many design parameters and DUT settings affect JTOL performance.

IV. Existing Acceleration Techniques for Jitter Tolerance Testing

Some alternatives for JTOL testing time reduction have been reported. In [19], a higher BER mask is presented as a means to approximate a pass/fail criterion at a BER of 10^{-12} by slightly increasing the injected noise profile and executing the test at a BER of 10^{-10}. Another common approach is to characterize the tolerated amplitude degradation between 10^{-10} and 10^{-12} tests. However, for both cases it is still needed to run a full test at the target BER to guarantee that the Rx passes the compliance test, mainly due to the lack of correlation between the 10^{-10} and 10^{-12} results.

An extrapolation algorithm for JTOL is proposed in [20] to predict JTOL at low BER based on high BER region data, with the objective to reduce the JTOL testing time. However, this algorithm failed when we applied it in a post-silicon validation compliance environment, as opposed to using it in high volume manufacturing testers. Under the high variation of measurements typically seen in system compliance tests, the linear regression of the Q factor [21] has a poor fit, which translates to poorly predicted values of J_P at low BER that do not correlate with real measurements. Moreover, the Q-factor regression is more suitable to extrapolate across J_R values which behave linearly in the Q scale, however, J_P does not have such a linear behavior, making extrapolation to typically fail in a system compliance environment.

Another set of innovative approaches have been proposed to accelerate jitter testing by using low-cost equipment on HSIO links. In [22], authors propose an algorithm for jitter testing

by employing a method that requires only a single test with a high frequency input sine wave, and then a fast Fourier transform (FFT) is performed only once. Another solution for at-speed jitter performance testing on automated test equipment (ATE) is proposed in [23], focusing on jitter compliance test of a DUT Tx port but not considering full jitter tolerance test. In [24] a new data dependent jitter estimation approach is proposed by using stochastic analysis, where the authors create surrogate models of the HSIO link for jitter calculation by using polynomial chaos theory and linear regression. Two low-cost jitter generators for jitter tolerance testing are proposed in [25]; while these circuits work on bench, they cannot be used for compliance with the industry standard specifications.

While many solutions to reduce the testing cost and time of JTOL measurements have been investigated, most of them focused on cost-effective ways of generating data streams with the desired jitter, and then trying to eliminate the need for an external equipment [26]-[29]. However, these solutions imply additional design efforts (e.g. on-die instruments, CDR with adaptive JTOL circuits, etc.) beyond just designing the CDR, and then additional costs. Therefore, none of these methods has been adopted so far for JTOL industrial testing.

V. Proposed Fast JTOL Testing Approach

Based on our description in Section III, a JTOL response R_J can be defined as

$$R_J = u\left(J_P, f\right) \tag{2}$$

where J_P is the periodic jitter amplitude injected by the BERT, and f is the frequency of the periodic jitter.

The evaluation of u in (2) implies sending a certain number of bits from the BERT, receiving the data stream at the Rx of the DUT, looping back the data to the Tx of the DUT, and receiving it once again at the BERT to check for bit errors. The equipment then computes the BER and returns a PASS if the number of errors is below the target BER, or a FAIL if there are more errors that those allowed to comply with the target BER. Therefore, u is a discrete function with continuous arguments; moreover, R_J is binary, since it can only have a PASS or a FAIL value. Given that there is usually a well-defined frontier between J_P values that yield a PASS and those that yield a FAIL, u can be treated as a unimodal function. Additionally, for a fixed value of f, the problem of finding the largest value of J_P that yields a PASS becomes a unidimensional optimization problem.

From the above perspective, we propose an optimization algorithm to accelerate JTOL testing time divided in two main stages: 1) execution of a direct search method based on a modified golden section strategy [30] at a high BER, typically 10^{-11}, and 2) a downwards linear search at the compliance BER, i.e. 10^{-12}, starting from the value obtained from the previous step. This technique clearly takes advantage of the fast execution of the golden section search strategy for a unimodal function in the interval of interest, as applied with a high BER, and overcomes the lack of correlation between different BERs by performing a downward linear search at the actual target BER until no errors are seen.

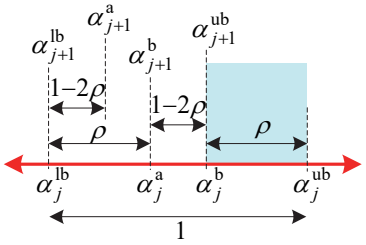

Fig. 4. Nature of the searching strategy of the golden section algorithm at the j-th iteration.

A. Modified Golden Section Search

The golden section algorithm is one of the most effective and widely used unidimensional direct search optimization methods. It aims at finding in a given searching interval a minimizer of a scalar unidimensional objective function $u(\alpha)$: $\Re \rightarrow \Re$. If $u(\alpha)$ is a unimodal function in the selected searching interval, the golden section method ensures finding the global minimum α^* in the interval of interest.

The search strategy used by the golden section method is illustrated in Fig. 4. Assuming a unitary searching interval defined by lower α_j^{lb} and upper α_j^{ub} bounds at the j-th iteration, the two interior points α_j^{a} and α_j^{b} are selected at a distance ρ from the extremes. The interval reduction is then accomplished by comparing the function values at the interior points. If $u(\alpha_j^{a}) < u(\alpha_j^{b})$, the minimum lies in the subinterval $[\alpha_j^{lb}, \alpha_j^{b}]$, as illustrated in Fig. 4, eliminating the shaded subinterval. However, if $u(\alpha_j^{a}) > u(\alpha_j^{b})$ then the minimum lies in the subinterval $[\alpha_j^{a}, \alpha_j^{ub}]$. At the next iteration, j+1, one of the prior interior points is re-used, and only one new interior point is generated at a distance ρ from the corresponding extreme. The relative reduction ρ at all iterations is kept fixed and given by the so-called golden ratio $\rho = (3-\sqrt{5})/2$.

The pseudo-code of our modified golden section direct search algorithm as applied to JTOL testing with a high BER is shown in Fig. 5. The initial searching interval is $[\alpha^{lb}, \alpha^{ub}]$. The same strategy for interval reduction is employed as described above, however, the objective function u is treated as a discrete function, for which we adjust the corresponding decision criteria to determine the next searching interval at each iteration. It is also worth noting that our algorithm modifies the manner in which an interval is eliminated, so that the final optimal point is the PASS/FAIL boundary of the test, instead of a maximum or minimum function value in the traditional algorithm. In other words, the modifications done to the algorithm allow to find the maximum J_P tolerated by the Rx before failing a BER test. The proposed algorithm is iterated, as depicted in Fig. 7, until the following stopping criterion is met:

$$\alpha_j^{ub} - \alpha_j^{lb} \leq \varepsilon_{step} \tag{3}$$

where ε_{step} is defined as either the minimum J_P increment allowed by the BERT or the known repeat measurement variability.

In JTOL testing, the evaluation of the objective function u in (2) returns a PASS or FAIL response from the BER test at a certain J_P and f. Our implementation of the golden section

begin

$j = 0\ ;\ \alpha_j^{\mathrm{lb}} = \alpha^{\mathrm{lb}}\ ;\ \alpha_j^{\mathrm{ub}} = \alpha^{\mathrm{ub}}\ ;\ \rho = (3-\sqrt{5})/2$

$\alpha_j^{\mathrm{a}} = \alpha_j^{\mathrm{lb}} + \rho(\alpha_j^{\mathrm{ub}} - \alpha_j^{\mathrm{lb}})\ ;\ \alpha_j^{\mathrm{b}} = \alpha_j^{\mathrm{lb}} + (1-\rho)(\alpha_j^{\mathrm{ub}} - \alpha_j^{\mathrm{lb}})$

$u_j^{\mathrm{a}} = u(\alpha_j^{\mathrm{a}})\ ;\ u_j^{\mathrm{b}} = u(\alpha_j^{\mathrm{b}})$

repeat until *StoppingCriteria*

if $u_j^{\mathrm{a}} = \mathrm{PASS} \wedge u_j^{\mathrm{b}} = \mathrm{FAIL}$

$\alpha_{j+1}^{\mathrm{lb}} = \alpha_j^{\mathrm{lb}}\ ;\ \alpha_{j+1}^{\mathrm{ub}} = \alpha_j^{\mathrm{b}}$

$\alpha_{j+1}^{\mathrm{b}} = \alpha_j^{\mathrm{a}}\ ;\ \alpha_{j+1}^{\mathrm{a}} = \alpha_{j+1}^{\mathrm{lb}} + \rho(\alpha_{j+1}^{\mathrm{ub}} - \alpha_{j+1}^{\mathrm{lb}})$

$u_{j+1}^{\mathrm{a}} = u(\alpha_{j+1}^{\mathrm{a}})\ ;\ u_{j+1}^{\mathrm{b}} = u_j^{\mathrm{a}}$

else if $u_j^{\mathrm{a}} = \mathrm{PASS} \wedge u_j^{\mathrm{b}} = \mathrm{PASS}$

$\alpha_{j+1}^{\mathrm{lb}} = \alpha_j^{\mathrm{a}}\ ;\ \alpha_{j+1}^{\mathrm{ub}} = \alpha_j^{\mathrm{ub}}$

$\alpha_{j+1}^{\mathrm{a}} = \alpha_j^{\mathrm{b}}\ ;\ \alpha_{j+1}^{\mathrm{b}} = \alpha_{j+1}^{\mathrm{lb}} + (1-\rho)(\alpha_{j+1}^{\mathrm{ub}} - \alpha_{j+1}^{\mathrm{lb}})$

$u_{j+1}^{\mathrm{a}} = u_j^{\mathrm{b}}\ ;\ u_{j+1}^{\mathrm{b}} = u(\alpha_{j+1}^{\mathrm{b}})$

end

$j = j + 1$

end

$\alpha^* = (\alpha_j^{\mathrm{lb}} + \alpha_j^{\mathrm{ub}})/2$

end

Fig. 5. Pseudo code implementation of the modified golden section algorithm as applied to the binary JTOL objective function.

algorithm differs from the classical one [30] since it is based on a discrete binary function response rather than a continuous one. Consequently, the decision of which search range to discard is based on the feasibility to approach on every iteration the actual boundary between the PASS and FAIL responses, which is our optimal point. The optimal value returned by the algorithm, α^*, is the average between the upper and lower bounds at the last iteration, as seen in Fig. 7.

B. Downwards Search

The second stage of the proposed algorithm performs a search starting from α^* found in the previous stage, but now executing at the compliance BER. The search is performed in a downwards direction, meaning that the J_P is decremented in linear steps equivalent to ε_{step} (or a percentage of ε_{step} in accordance to precision used in the traditional method) until no errors are seen, or in other words, until the BER test passes. The range reduction achieved by the golden section search allows to decrease the number of evaluations in the downwards search. Typically, only one to three evaluations are needed at the compliance BER, thus the overall test time is dramatically reduced.

VI. Test Cases

The proposed methodology described in Section VI was tested in three different computer HSIO links: SATA3, USB3, and PCIe3. These HSIO links are part of an Intel platform controller hub (PCH) that works in conjunction with the CPU through the direct media interface (DMI) on a server platform [31], as shown in Fig. 6.

The three HSIO links are tested under a specific set of

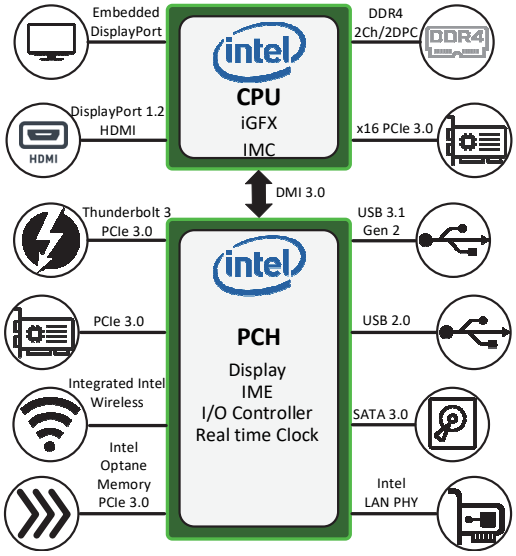

Fig. 6. Architecture of the system under test, including the platform controller hub (PCH) and CPU, as well as the USB, SATA, and PCIe HSIO links.

impairments and a compliance pattern, which are described by the specifications of each HSIO link. In order to guarantee that the JTOL test is compliant with the stress required by the specifications, a BERT calibration is required.

The starting point of the BERT calibration is the eye height (EH), of which the amplitude is defined in the standards and can be measured with an oscilloscope. After setting the amplitude, the Tx equalization presets including de-emphasis and pre-shoot are calibrated for each HSIO link. Once the calibrated BERT Tx can guarantee the delivery of compliant EH amplitude and presets equalization, the electrical impairments are calibrated and added to the transmitted signal.

The three HSIO links require the use of J_R and J_P as part of the impairments and are calibrated accordingly. Furthermore, the transmitted compliance pattern must interact with the discontinuities and losses present in the channel, therefore, the presence of J_{DD} is granted. High frequency components are attenuated due to channel losses, causing a stressed EH. In the case of PCIe, the EH is additionally stressed by adding the common mode interference (CMI) and the differential mode interference (DMI). The CMI and DMI must be calibrated, as these impairments emulate cross-talk aggressors.

Since the validation is executed in an industrial environment, 3 repetitions of each test are typically executed in order to capture and analyze the measurement noise. Our test time reported for each test case considers the overall duration of the 3 repetitions executed consecutively. For comparison purposes, we set the same initial value of J_P at each frequency point for both methods (traditional and proposed). A summary of the comparison between the traditional and the proposed methods for the three test cases is shown in Table I.

A. Test Case 1: HSIO SATA3

The JTOL setup for SATA is comprised of a system platform that includes the DUT and a SATA connector, as well as a SATA3 Fixture, a SATA ISI Channel that emulates

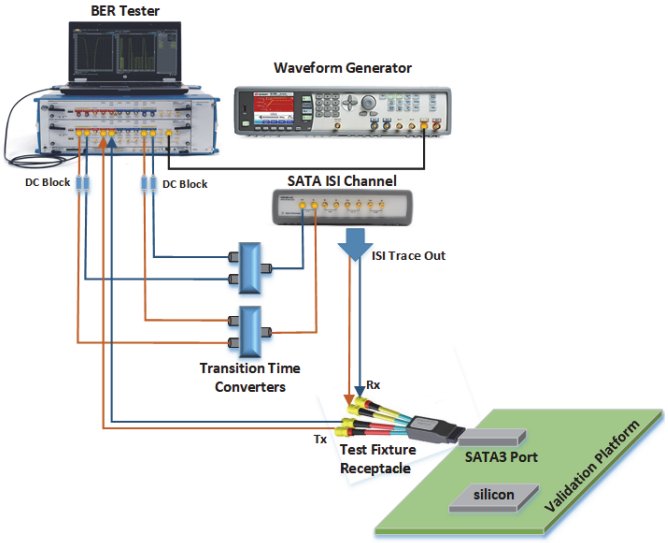

Fig. 7. SATA JTOL test setup.

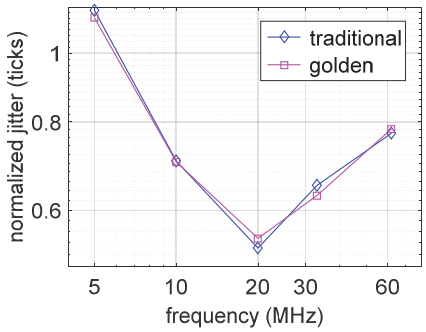

Fig. 8. SATA JTOL testing results for the traditional approach and the proposed golden section algorithm implementation.

the loss of a compliant 1-m cable, two transition time converters that allow to have specification-compliant slew rates, two power dividers which combine the signals from the two BERT channels in order to properly generate the out-of-bound signaling required for the interface initiation, and DC blocking capacitors, as shown in Fig. 7. During the Rx JTOL test, the BERT pattern generator sends a compliance test pattern with added jitter through the compliance channels connected with fixtures to the Rx. Prior to running the test, the port should transition to loopback state. Once in loopback, the data received from the DUT is compared to the data generated and errors are counted by the BERT.

The JTOL execution following our proposal took 5.3 hours to complete 3 repetitions at five different frequency points, as compared to 72.6 hours that the traditional method required. Our proposal needs only 7.3% of the time required by the traditional approach to reach a comparable solution, as confirmed in Fig. 8.

B. Test Case 2: HSIO USB3

In the test case of USB3, the JTOL setup includes the system platform that contains the DUT and a USB3 connector where USB3 fixtures are inserted, one BERT and direct current (DC) blocking capacitors, as shown in Fig. 9, where we can see that, similarly to SATA3, the connection from the

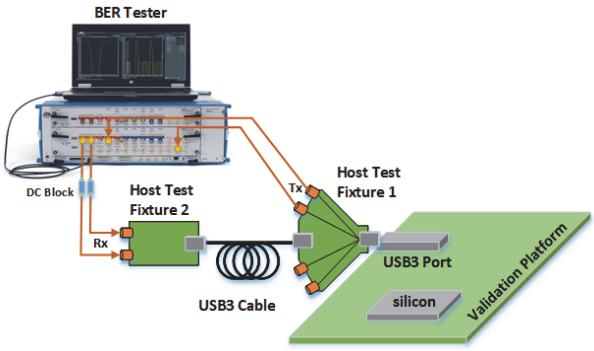

Fig. 9. USB3 JTOL test setup.

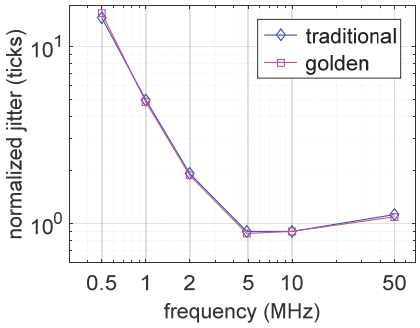

Fig. 10. USB3 JTOL results for the traditional approach and the proposed golden section algorithm implementation.

BERT to the Tx path is direct, whereas on the Rx path, the setup includes an actual USB3 cable, calibrated with the standard loss required for compliance tests. Validation time was significantly decreased using our JTOL algorithm as compared with the traditional methods, without sacrificing accuracy. In this test case, the JTOL results for the traditional approach and those with the proposed golden section algorithm were practically the same, as seen in Fig. 10, however, the validation time was reduced by up to 96.1% with respect to the traditional approach. Current methods require around 6 days for a complete execution, while the method proposed in this work can be completed in a few hours.

C. Test Case 3: HSIO PCIe3

Finally, for the PCIe test case, the JTOL setup consists of the BERT output connected with DC blocking capacitors to the compliance load board (CLB) fixture card, which is connected to the system platform that contains the DUT to reach its Rx, as shown in Fig. 11. Unlike SATA3 and USB3, this PCIe topology works on a common clock manner, where the host sends a clocking signal to the device to synchronize the incoming data. To emulate this in a compliance test, an additional reference clock connection is needed between the BERT and the CLB. To enable a common clock topology, the reference clock is taken from the system platform by the CLB fixture card and goes into the BERT. Additionally, the preset values for pre-cursor and post-cursor are set in the BERT, which sends the PCIe compliance sequence patterns to set loopback mode with the DUT.

With the traditional JTOL method, test lasted 263.6 hours to run 3 repetitions for twelve different frequencies points (about

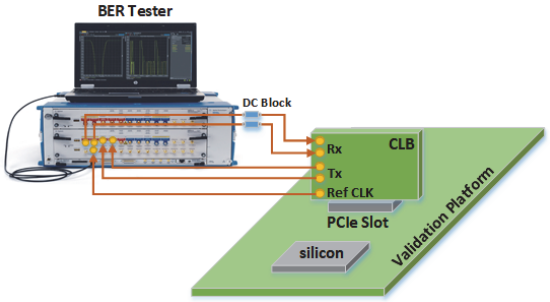

Fig. 11. PCIe3 JTOL test setup.

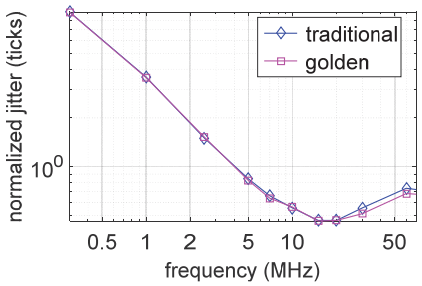

Fig. 12. PCIe3 JTOL results for the traditional approach and the proposed golden section algorithm implementation.

TABLE I
TIME REQUIRED FOR JITTER TOLERANCE TESTING

Interface	Traditional method (hours)	Proposed method (hours)	Time reduction
SATA3	72.59	5.29	92.7%
USB3	158.48	6.2	96.1%
PCIe3	263.6	10.02	96.2%

11 days), whereas with the proposed algorithm the same 3 repetitions just took about 10 hours to be completed, reducing test time of the traditional approach by 96.2% and obtaining very similar results, as shown in Fig. 12.

VII. Conclusion

We have described a novel approach to fast and reliable JTOL testing for HSIO links validation. The proposed approach has proven its effectiveness for reducing the jitter tolerance validation time as compared with the traditional method: it has been demonstrated that the JTOL testing time can be reduced by around 95% as compared to the traditional approach, without compromising measurement accuracy. The algorithm was tested on SATA, USB3 Gen1, and PCIe Gen3 CEM & BASE standards, with outstanding results. The proposed methodology can easily be ported to other standards based in the receiver JTOL test, such as XAUI, among others. The incorporation of the proposed algorithm to post silicon validation provides several potential benefits: a) a very significant reduction of TTM by reducing validation time; b) an increase in the product quality by making feasible more unit coverage; c) a more feasible incorporation of multiple frequency points to cover the ambiguity of the standards; and d) a much lower execution cost of validation across PVT conditions.

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