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Development of a Cost-Efficient Video Acquisition System for Medical Applications using a Dual-Core Cortex-M Microcontroller

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Presenta: **SNAIDER ALAIN BAUTISTA GUERRERO**

Director **LUIS ENRIQUE GARABITO SIORDIA**

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Development of a Cost-Efficient Video Acquisition System for Medical Applications using a Dual-Core Cortex-M Microcontroller

Snaider Alain Bautista Guerrero
Embedded Systems Specialization
ITESO University
Guadalajara, Mexico.
snaider.bautista@iteso.mx

***Abstract*—Video acquisition systems, consisting of video capture, encoding, transmission and display, are widely used in medical applications. However, current systems present challenges such as higher costs, power consumption, and reduced availability. Therefore, this paper proposes a video acquisition system using a dual-core Cortex-M microcontroller. Tests showed the system is suitable for video acquisition, processing, and display. The storage component presented limitations, by only achieving the correct saving of 32.36 % of the acquired video. Finally, it is shown that a Dual-Core Cortex-M microcontroller could be used for low-cost medical applications that do not require high quality video storage.**

Keywords— video acquisition system, medical application, microcontroller, dual-core cortex.

I. INTRODUCTION

Video acquisition systems are essential for a wide range of medical applications, such as endoscopy, bronchoscopy, and laparoscopy. Video monitoring facilitates both medical and patient education, and video recording of procedures provides permanent documentation for patient files [1]. Video acquisition systems, in combination with computer electronics and digital image processing, help in clinical diagnosis, disease tracking, and treatment determination. These systems typically consist of a front-end video capture, encoding, transmission, and display [2].

The development of cost-effective video acquisition systems for medical applications is critical for improving patient outcomes and reducing healthcare costs [3]. Such systems typically rely on General Purpose Processors (GPP), Graphic Processing Units (GPU), and Digital Signal Processors (DSP) to parallel architectures like Application Specific Integrated Circuits (ASICs) or even Field-Programmable Gate Arrays (FPGAs). These solutions present a range of challenges such as power consumption [4], higher costs, reduced availability, and overheating when placed in constrained spaces, resulting in performance and reliability issues that affect the end user.

To address these limitations, this paper proposes a video acquisition system for medical applications using a dual-core Cortex M microcontroller. The system provides three primary functionalities: video acquisition, video processing for real-time display on an embedded screen, and video storage onto an external SD memory using an open-source real-time operating system (FreeRTOS) for task management. This video acquisition system's simple structure ensures the clarity of image acquisition as well as the real-time stability of image display and storage. This system lays the groundwork for using Cortex-M processors in medical video systems.

This article explains the development and implementation of an image acquisition system for a medical application using a dual-core cortex M-microcontroller. First, the description of the system is mentioned, which contains the hardware components, the architectural description, the image acquisition process, the image processing and the image display, and storage. Then, the results are presented and structured to show the capture performance test, the debayering algorithm test, and the display performance test. Finally, the conclusions of the article are explained.

II. SYSTEM DESCRIPTION AND IMPLEMENTATION

A. Hardware Components

A typical digital camera system consists of a Central Processor Unit (CPU), a camera module, a TFT-LCD controller for driving the display screen, a Synchronous Dynamic Random-Access Memory (SDRAM), and an external memory such as an SD card. The central processor unit controls various operations, including image processing, and storage management, and display functions. The camera module captures images, which are then processed and stored by the central processor unit. The TFT-LCD controller enables the display of the captured images. The SDRAM serves as temporary storage for frame buffers, while the external memory provides additional storage capacity for long-term data retention. These components form an integrated digital camera system capable of capturing, processing, displaying, and storing images.

The STM32H7 microcontroller (MCU) family offers a range of peripherals that are specifically designed to enhance the performance of embedded video systems. These peripherals include an LCD-TFT controller interface with dual-layer support, a MIPI Display Serial Interface (MIPI-DSI) interface for driving DSI displays, the ChromART Accelerator™ for

efficient graphical content creation, and a JPEG hardware accelerator for fast encoding and decoding of JPEG data. The LCD-TFT controller interface enables effective management of complex graphical content, while the MIPI-DSI interface ensures seamless integration with DSI displays with better speeds than other commonly used protocols. The ChromART Accelerator™ optimizes graphical content creation, freeing up the MCU's core processing power for other application needs. Additionally, the JPEG hardware accelerator offloads the CPU, enabling swift and efficient processing of JPEG data to save the coded image in the external memory [5].

Moreover, this family contains a Cortex-M7 core and a Cortex-M4 core. The Cortex-M7 is the highest performance in the M series, providing a scalar performance of 5.01 CoreMarks/MHz. The Cortex-M4 provides low power, low interrupt latency and a Floating Point Unit (FPU) suitable for image processing [6].

B. Architectural Description of the System

The proposed system consists of four layers shown in Fig. 1:

1) Microcontroller abstraction layer (MCAL): This layer directly accesses on-chip microcontroller (MCU) peripheral modules and external devices that are mapped to memory. The peripherals used by this system include a flexible memory controller, a general-purpose input output, a serial peripheral interface, a direct memory address and a display controller peripheral.

2) ECU abstraction layer: Interface with MCAL to access devices inside or outside the microcontroller.

3) Middleware: Provides an abstraction software layer to interface with ECU.

4) Service layer: Provides operating system functions and software modules for the application.

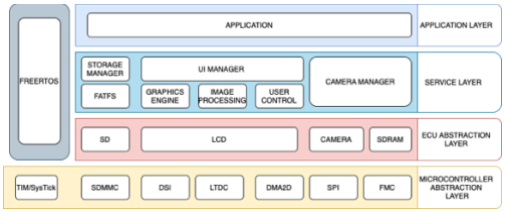

Fig. 1. System architecture

C. Image Acquisition

The image acquisition process involves interfacing the camera module with the MCU using an SPI (Serial Peripheral Interface) with a single-ended interface as shown in Fig. 2. To establish communication, several steps need to be followed. First, the camera module should be reset to ensure a clean initialization. Then, the SPI clock is started to enable data transfer between the camera module and the MCU. The frame rate is set to determine the desired speed at which image frames are captured.

To synchronize the data transfer, the MCU sends dummy clock cycles to the camera module until the frames are available for retrieval. Once the initialization is complete, the camera module starts capturing frames.

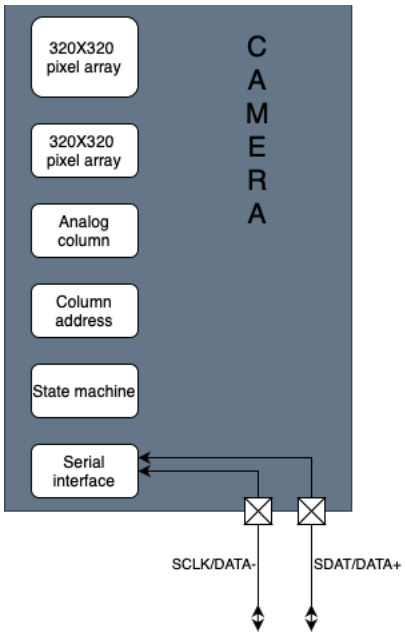

Fig. 2. Camera communication interface

Upon receiving the frames from the camera module, they are stored in a queue. This queue acts as a buffer, holding the frames temporarily before they are sent to the display and storage modules. The use of a queue ensures a reliable and efficient transfer of image frames, allowing for further processing or immediate display/storage, as required by the application. The architecture uses two queues that work alternately, allowing continuous capture and processing of image frames. To accommodate the double buffer architecture and ensure sufficient memory capacity, the buffers are placed in an SDRAM module.

D. Image Processing

The images were reconstructed from the sensor with a Color Filter Array (CFA). To calculate the missing color in each pixel, a demosaicing or debayering algorithm was implemented using a bilinear interpolation technique. This technique is based on the fact that there is a high probability that the value of a missing pixel has a similarity with the value of its existing adjacent pixels, the interpolation can be done in the missing values in each channel by taking the average of its adjacent pixels.

For example, to find the value of a green pixel located at Gx in Fig. 3, the value of the average of the 4 adjacent green pixels is calculated.

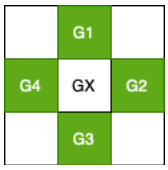

Fig. 3. Bilinear Interpolation example to find the green value of the pixel Gx.

Similarly, to find the value of the blue pixel located at Bx in Fig. 4, the value of the average of the 4 adjacent blue pixels is calculated.

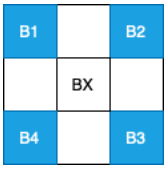

Fig. 4. Bilinear Interpolation example to find the blue value of the pixel Bx.

Finally, to find the value of the red pixel located at Rx in Fig. 5, the average value of the 4 adjacent red pixels is calculated.

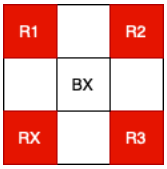

Fig. 5. Bilinear Interpolation example to find the red value of the pixel Bx.

The image encoding uses the integrated hardware accelerator called the JPEG codec, specifically designed for efficient JPEG image encoding and decoding. This codec includes a hardware JPEG header generator and parser, enabling seamless handling of JPEG files. Notably, the codec operates entirely in hardware, allowing it to deliver one data pixel per cycle without imposing any CPU load. The process of video recording with the JPEG codec involves three main steps as shown in Fig. 6. First, the camera captures and processes the image, resulting in an ARGB8888 format. Next, the ARGB8888 image undergoes processing and compression to convert it into JPEG format. Finally, each JPEG frame is sequentially stored in AVI format, forming the recorded video.

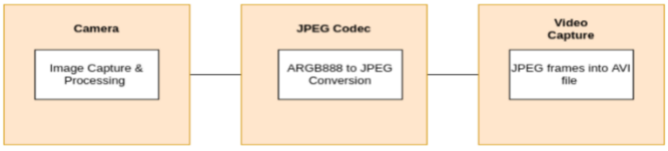

Fig. 6. JPEG Coding flow diagram

E. Image Display and Storage

The system utilizes SD card storage with the FATFS library for video recording. The video recording process involves image capture and processing, where the captured image is processed into ARGB8888 format. The processed image is then compressed into JPEG format. Each JPEG frame is sequentially stored in AVI format on the SD card. The SD card used is of the SDHC type and supports Ultra High Speed I (UHS-I) bus system.

The image display capability of the system was developed through the implementation of the ST7796S LCD driver for the hysteroscope prototype. This LCD driver was developed to accommodate different display options based on the size of the acquired video.

The LCD driver uses the MIPI DSI protocol, which is a high-speed and low-latency interface designed for mobile devices and displays. The utilization of MIPI DSI facilitates faster data transfer, thereby allowing the processor more time to execute other tasks efficiently.

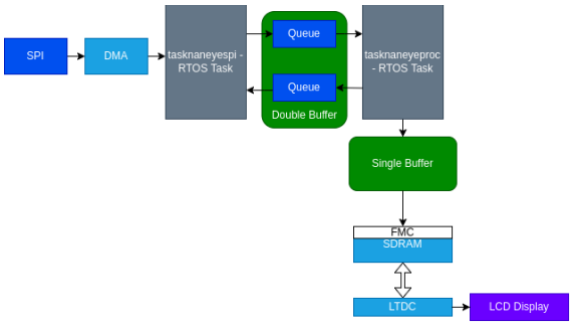

Fig. 7. System FreeRTOS flow diagram

III. RESULTS

To evaluate the performance of the video acquisition system, 10 videos were captured to evaluate the acquisition, processing, and storage of the system.

Acquisition was evaluated by measuring the time it takes to capture one camera frame. The time to capture a frame is given by the time per rows between the frame and the reading time,

$$t_{frame} = t_{rows\_btw\_frame} + t_{rows\_matrix} \quad (1)$$

The pixel period (PP) corresponds to the duration of a data word with respect to the pixel frequency. The system works with a pixel frequency of 24.7 MHz. Given a resolution of 320 x 320 pixels, the estimated acquisition time is,

$$t_{frame} = 320 \times 320\ PP + 8\ PP = 104\ us \quad (2)$$

The time of the frame was measured using an oscilloscope and the average of the 10 videos was a t_{frame} of 127 us. Measured times are shown in Fig. 9.

The processing algorithm was evaluated by using a 32x32 pixel resolution camera data array following the Bayer BGGR pattern shown in Fig. 8

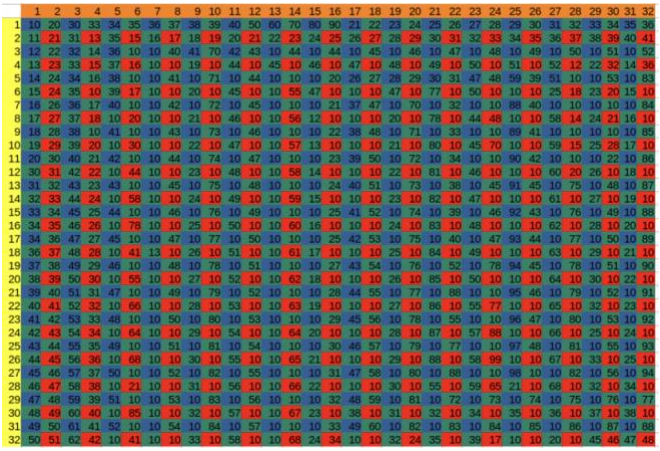

Fig. 8. Image test array for demosaicing algorithm

Using the demosaicing algorithm, the data was converted to AARRGGBB algorithm, which consists of alpha, red, green, and blue components as shown in Fig. 9.

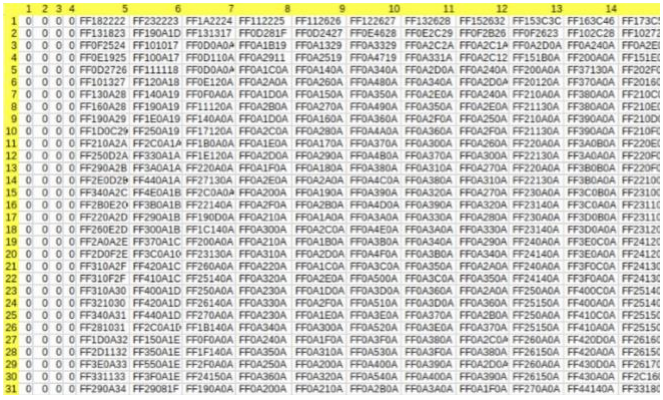

Fig. 9. Demosaicing algorithm result using the bilinear interpolation method in AARRGGBB format.

Storage was evaluated by analyzing the frames per second and the average video size stored in an SDHC Ultra High Speed memory with the camera sending 19 frames per second. The average number of frames captured per second is 6.15, with an average file size of 1.898 MB. This represents that the system is capable of storing 32.36% of the acquired video. The storage results are summarized in Table 1.

TABLE I. STORAGE RESULTS

Captured frames	Duration (s)	Frames per second	Data rate (bytes/s)	File size (MB)
60	10	6	187167	1.785659
59	9	6.5	203530	1.909343
60	10	6	190748	1.819808
59	9	6.5	229361	2.151584
60	10	6	213179	2.033729
60	10	6	198698	1.895622
60	10	6	176797	1.686767
60	10	6	201199	1.919479
58	9	6.5	194711	1.795684
60	10	6	209655	2.000118

IV. CONCLUSION

In this paper, a video acquisition system for medical applications using a dual-core Cortex-M microcontroller is presented. The system aimed to provided video acquisition, real-time processing, and storage functionalities. The acquisition and display aspects of the system were successfully implemented, but the storage component encountered challenges due to the system's design priorities and the limitations of the camera's slow data transmission protocol.

The chosen microcontroller, the STM32H7 family, offered several advantageous peripherals, such as an LCD-TFT controller interface, a MIPI-DSI interface, a ChromART Accelerator™, and a JPEG hardware accelerator. These features facilitated efficient image acquisition, processing, and display.

The system architecture comprised four layers: a microcontroller abstraction layer (MCAL), an ECU abstraction layer, a middleware, and a service layer. This layered approach ensured seamless interaction between hardware components and software modules, contributing to optimal performance and functionality.

To address the storage challenges, an alternative solution is to use a different camera module with faster transmission protocols, such as Low Voltage Differential Signaling (LVDS) or DCMI (Digital Camera Interface). These protocols offer higher data transfer rates, enabling more efficient and reliable video storage. By replacing the current camera module with one supporting faster transmission protocols, the system could achieve improved storage performance while maintaining real-time acquisition and display capabilities.

Despite the limitations found in storage, the proposed video acquisition system, utilizing a dual-core Cortex M microcontroller, remains a cost-effective solution for medical applications. The system's focus on real-time acquisition and display makes it suitable for various medical procedures. With the suggested improvement of using a different camera module, the system could overcome the storage challenges and provide enhanced performance in medical settings.

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