

# Equalization Tuning of the PCIe Physical Layer by Using Machine Learning in Industrial Post-silicon Validation

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## ABSTRACT

The increasing complexity of high-speed computer platforms has made post-silicon validation a highly demanding industrial task. A large portion of the circuits to be validated in modern microprocessors corresponds to high-speed input/output (HSIO) links, imposing the need to efficiently tune the transmitter (Tx) and receiver (Rx) equalizers [1].

Peripheral component interconnect express (PCIe) is one of the most complex HSIO interfaces and the primary interface for a host central processing unit (CPU) to connect with input/output (I/O) devices. PCIe has been continuously evolving and the new PCIe Gen6 specification has reached a data rate of 64 giga-transfers per second (GT/s). However, as transmission speeds increase, undesired signal integrity effects are more severe, causing the signals to become more susceptible to errors [2]. Additionally, PCIe channels are bandwidth-limited by default, causing large signal attenuation at high frequencies. This generates distortion and spreading of the transmitted data over multiple symbols, exacerbating inter-symbol interference (ISI), which can make the signal unreadable at the Rx, producing bit errors. The most practical solution to this problem is signal conditioning to open the eye diagram [3].

PCIe specification defines an adaptive mechanism for equalization (EQ) to determine the optimum values of the Tx and Rx EQ coefficients within a fixed time limit, across the allowed channel types. The most widely used current method consists of using maps of EQ coefficients, which are obtained from massive eye diagram measurements. The EQ maps are used to characterize the PCIe link across different channel losses and devices. Once the full characterization is completed, the best Tx EQ values are selected based on the input of an experienced validation engineer. This is a very time-consuming process and prone to human errors.

Machine learning algorithms are useful to build statistical models from examples, which are then used to make predictions when faced with cases not seen before [4]. Unsupervised machine learning algorithms are designed to learn patterns from untagged data. On the other hand, supervised machine learning models are trained to predict outputs from a given set of inputs. The large volume of data generated from typical post-silicon testing suggests the application of machine learning techniques to identify underlying patterns, such as channel effects on the analog behaviour of the HSIO link.

In this work, we first use unsupervised machine learning techniques [5] to cluster all available post-silicon data from different channels, dividing them into distinct sets of channel conditions. We then develop statistical supervised machine learning models [6], based on Gaussian process regression (GPR), to predict the eye diagram margins within each data subset. We finally optimize the GPR-based models to obtain the optimal tuning settings for the specific channels. Our proposed method is validated by measurements of the functional eye diagram of an actual industrial computer platform.

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