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PCI Express Gen6 FIR Filter Optimization by Space Mapping for Post-Silicon Validation

Francisco E. Rangel-Patiño[#*$1], José E. Rayas-Sánchez[$2], and Aurea Edna Moreno-Mojica[$&3]

[#] Intel Corp. Zapopan, Jalisco, 45019 Mexico

[*] National Institute of Technology of Mexico, José Mario Molina Pasquel y Henríquez Technological Institute, Zapopan Academic Unit, Jalisco, 45017 Mexico

[$] Department of Electronics, Systems, and Informatics, ITESO – The Jesuit University of Guadalajara, Tlaquepaque, Jalisco, 45604 Mexico

[&] Synopsys. Zapopan, Jalisco, 45010 Mexico

[1]francisco.rangel@intel.com, [2]erayas@iteso.mx, [3]edna.moreno@synopsys.com

***Abstract*— The evolution of PCI Express technology to Gen6, and the forthcoming Gen7, has markedly increased data transfer speeds, presenting new challenges for signal integrity. To tackle these challenges, advanced design strategies, such as enhanced equalization (EQ) techniques, are necessary. Traditional EQ methods typically involve extensive laboratory measurements, rendering the EQ process highly time intensive. In this paper, we introduce an optimization methodology for the PCIe Gen6 transmitter (Tx) equalizer utilizing the Aggressive Space Mapping (ASM) algorithm. Our ASM approach employs a computationally efficient surrogate as coarse model to estimate eye diagram margins. An implicit mapping between the coarse and fine model equalizer settings is established, leading to an efficient optimization for the EQ tuning process. The effectiveness of the ASM methodology is confirmed through simulations with the MATLAB SerDes Toolbox, resulting in notable enhancements in the eye diagram area and overall system margins.**

***Keywords*— Aggressive Space Mapping, Gaussian Process Regression, PCIe, post-silicon validation, signal integrity, transmitter equalizer.**

I. Introduction

The evolution of the peripheral component interconnect express (PCIe) technology to Generation 6 (Gen6) and Generation 7 (Gen7) for high-performance computer platforms has brought about significant advancements in data transfer rates, pushing the boundaries of high-speed communication. However, these improvements come with heightened signal integrity challenges. PCIe Gen6 operates at data rates of 64 giga-transfers per second (GT/s), doubling the 32 GT/s rate of its predecessor, Gen5 [1]. As the industry anticipates the rollout of PCIe Gen7, which is expected to further double the data rate to an unprecedented 128 GT/s, operating with a 32 GHz Nyquist frequency. This frequency imposes even more stringent demands on signal integrity.

The leap in frequency from Gen6 to Gen7 exacerbates issues such as crosstalk, signal loss, and reflections, which are already complex at lower speeds. The increased data rates also mean that the margin for timing errors shrinks, requiring more accurate clock recovery mechanisms to maintain data integrity. Moreover, the higher frequency operation of PCIe Gen7 will likely intensify the effects of power supply noise and ground bounce, which can induce jitter and further compromise the integrity of the signal. The design of printed circuit boards (PCBs), connectors, and other system components must be optimized to handle these higher frequencies without significant loss or distortion of the signal [2]. To address these signal integrity issues, engineers must employ advanced design techniques, such as improved equalization (EQ) methods, sophisticated channel modeling, and robust error correction protocols.

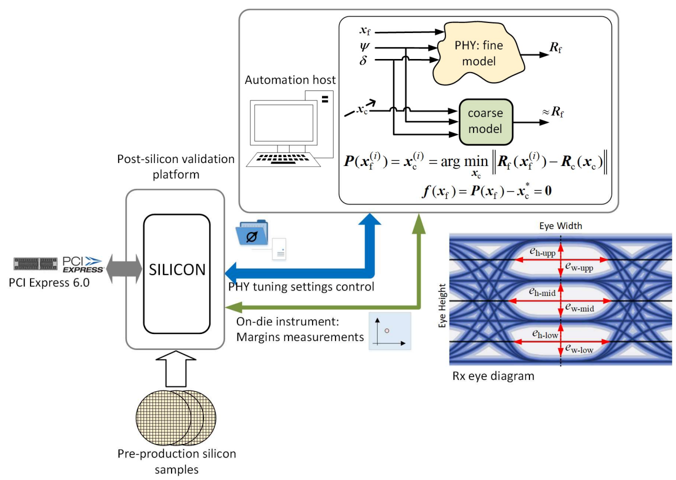


Fig. 1. ASM test setup using a server post-silicon validation platform.

The PCIe standard specifies a dynamic EQ process that ascertains the ideal settings for the transmitter (Tx) finite impulse response (FIR) filter coefficients within a predetermined time frame, considering various channel conditions. The predominant method currently in use involves the creation of EQ coefficient maps, which are derived from comprehensive eye diagram measurements. These maps provide a detailed representation of the PCIe link performance over a range of channel losses and device scenarios. Nonetheless, this thorough characterization procedure is extremely time-intensive and relies heavily on the skill and judgment of validation engineers to choose the optimal EQ settings, which introduces susceptibility to human error [3].

This makes it one of the most time-consuming processes in post-silicon validation [4], [5]. Several methods have been proposed to address this challenge. One such method is a statistical framework referred to as Bayesian model fusion (BMF), as proposed in [6]-[8]. However, the BMF approach is not feasible in a post-silicon environment where insufficient pre-silicon data is available.

To overcome this limitation, other methods [9] have been proposed that use surrogate models from a set of learning base points generated from the design of experiments (DoE) [10]. These metamodels treat the system as a black box, aiming to approximate the input-output relationship for the system under study [11]. Once a highly accurate surrogate model is developed, direct optimization can be applied to find the optimal PHY tuning parameters.

While an accurate surrogate model is desirable for direct surrogate-based optimization (SBO), it can be computationally expensive to develop. By combining an adequate modeling technique with a suitable DoE approach, a coarse surrogate model can be efficiently developed with a significantly reduced set of data, as demonstrated in [12]. Once this coarse model is available, space mapping (SM) techniques can be exploited.

In this paper, we employ the Broyden-based input space mapping algorithm, more commonly referred to as aggressive SM (ASM) [13], [14], [15] for optimizing the Tx FIR equalizer in PCIe Gen6. Ideally, the fine model would be a measurement-based post-silicon validation platform, as that one illustrated in Fig. 1. However, due to the absence of silicon samples with PCIe Gen6 at our facility, we are validating the proposed method by using a detailed model implemented in the MATLAB SerDes Toolbox. In line with [3], we initially apply unsupervised machine learning to cluster the available data from various channels, enabling us to categorize the data into distinct channel condition groups. Subsequently, we utilize supervised machine learning to create statistical models using Gaussian Process Regression (GPR) to forecast the functional margins of the eye diagram within each subset of data. In contrast to [3], where we optimize the GPR model to improve the fine model, here we use the GPR model as our coarse model in an ASM optimization. This allows us determining the optimal PCIe Tx FIR equalizer settings for each identified set of channel conditions.

II. Space Mapping Setup

Space mapping (SM) techniques are designed to optimize models that are resource-intensive in terms of computation. The ASM method stands out as the most widely employed SM strategy for efficient design optimization [13]. ASM skillfully determines a near-optimal design, known as the space mapped solution $\boldsymbol{x}_{\mathrm{f}}^{\mathrm{SM}}$, for the computationally expensive model (referred to as the fine model) by leveraging a surrogate model that is less accurate but more computationally efficient (known as the coarse model) [15]. The primary objective of ASM is to derive an $\boldsymbol{x}_{\mathrm{f}}^{\mathrm{SM}}$ that aligns the response of the fine model $\boldsymbol{R}_{\mathrm{f}}$ closely with the intended outcome.

A. Fine Model

Our fine model is intended to be an Intel server post-silicon validation platform in an industrial environment, as depicted in Fig. 1 [15]. The measurement system relies on an Intel-developed procedure known as system margin validation (SMV) [9], [16], which is a methodology for evaluating the design margin relative to the silicon characteristics and process variations that occur over time, including those related to voltage and temperature. Since a physical validation platform for PCIe Gen6 is not yet available at our facility, here we validate our proposed methodology through precise simulations of the eye diagrams using the MATLAB SerDes Toolbox, which is taken as $\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}_{\mathrm{f}})$, where $\boldsymbol{R}_{\mathrm{f}}$ contains the corresponding critical eye diagram parameters and $\boldsymbol{x}_{\mathrm{f}}$ has the Tx FIR equalizer settings.

B. Coarse Model

Surrogate models can be constructed using data from high-fidelity simulations or from actual measurements, providing quick approximations of the original system or component at new design points. In this paper, we follow the methodology described in [3], and [17]. Initially, we employ unsupervised machine learning techniques to cluster all the available post-silicon data from various PCIe channels, categorizing them into distinct groups based on channel conditions. Subsequently, we develop a non-parametric, probabilistic model using Gaussian process regression (GPR) to predict the eye diagram margins for each group of data. The resultant GPR models are used as the corresponding coarse model responses $\boldsymbol{R}_{\mathrm{c}}(\boldsymbol{x}_{\mathrm{c}})$.

C. Objective Function and Optimization

We aim at finding the optimal set of Tx FIR EQ settings, $\boldsymbol{x}^*$, to maximize both critical eye diagram parameters, e_{w} and e_{h} based on the margin responses, which can be calculated either with $\boldsymbol{R}_{\mathrm{f}}$ or with $\boldsymbol{R}_{\mathrm{c}}$. In both cases, they are the smallest of the three PAM4 eye height and eye width measurements (lower, middle, and upper), as shown in Fig. 1, that are functions of the Tx equalizer settings contained in vector $\boldsymbol{x}$, i.e.,

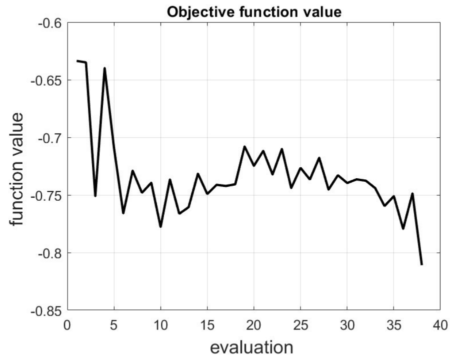
$$e_{\mathrm{w}}(\boldsymbol{x}) = \min(e_{\text{w-low}}(\boldsymbol{x}), e_{\text{w-mid}}(\boldsymbol{x}), e_{\text{w-upp}}(\boldsymbol{x})) \quad (1)$$

$$e_{\mathrm{h}}(\boldsymbol{x}) = \min(e_{\text{h-low}}(\boldsymbol{x}), e_{\text{h-mid}}(\boldsymbol{x}), e_{\text{h-upp}}(\boldsymbol{x})) \quad (2)$$

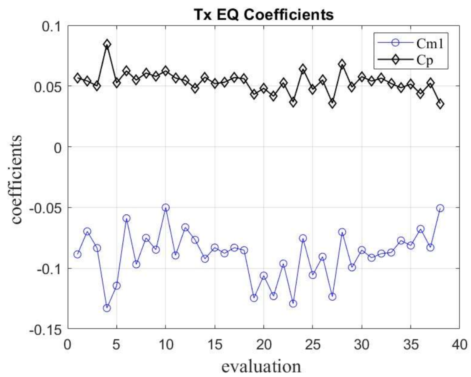
We follow [7] to define an initial objective function as

$$u(\boldsymbol{x}) = -[e_{\mathrm{w}}(\boldsymbol{x})][e_{\mathrm{h}}(\boldsymbol{x})] \quad (3)$$

Depending on the number of channels, we may end up with numerous EQ maps. We then calculate the median of all $u(\boldsymbol{x})$ values across these channels to consolidate them into a single EQ map. As described in [18], we need to ensure the optimal system margin response falls within a suitable region in the coefficients search space of the EQ map. Then we follow the procedure described in [3] to define an unconstrained formulation, such that the optimal set of coefficients maximizes the system response without violating the lower bound of 0.8 $u(\boldsymbol{x}^*)$ in the vicinity, as defined in [7],



a)



b)

Fig. 2. SM optimization iterations: a) objective function; b) Tx EQ coefficients values.

$$U(\boldsymbol{x}) = u(\boldsymbol{x}) + L(\boldsymbol{x})\left[\frac{|u(\boldsymbol{x}^{(0)})|}{\max\{\boldsymbol{l}(\boldsymbol{x}^{(0)})\}}\right] \tag{4}$$

where $\boldsymbol{x}^{(0)}$ is the starting point and $L(\boldsymbol{x})$ is defined as

$$L(\boldsymbol{x}) = \max\{0, \max\{\boldsymbol{l}(\boldsymbol{x})\}\} \tag{5}$$

with matrix $\boldsymbol{l}(\boldsymbol{x})$ given by

$$\boldsymbol{l}(\boldsymbol{x}) = 0.8u(\boldsymbol{x})\begin{bmatrix}1 & 1\\1 & 1\end{bmatrix} - \begin{bmatrix}u(\boldsymbol{x}-[1\ 0]^{\mathrm{T}}) & u(\boldsymbol{x}+[1\ 0]^{\mathrm{T}})\\ u(\boldsymbol{x}-[0\ 1]^{\mathrm{T}}) & u(\boldsymbol{x}+[0\ 1]^{\mathrm{T}})\end{bmatrix} \tag{6}$$

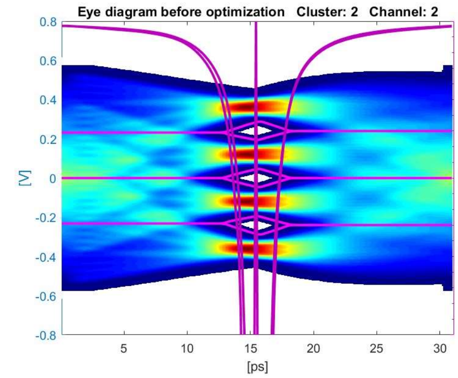
Then, the original optimization problem to be solved is

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} U(\boldsymbol{x}) \tag{7}$$

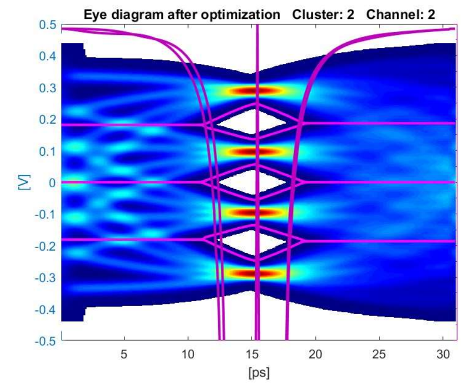
We aim at solving (7) by using the ASM method, *i.e.*, by frugally evaluating $\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}_{\mathrm{f}})$ based on intensively using $\boldsymbol{R}_{\mathrm{c}}(\boldsymbol{x}_{\mathrm{c}})$.

III. ASM Optimization Results

Upon implementing the ASM algorithm [13], we quickly converge to a space-mapped solution $\boldsymbol{x}_{\mathrm{f}}^{\mathrm{SM}}$ in just 37 iterations (or fine model evaluations), as illustrated in Fig. 2. The set of Tx FIR EQ coefficients in $\boldsymbol{x}_{\mathrm{f}}^{\mathrm{SM}}$ results in a PCIe receiver eye height and width that are as open as those predicted by the optimized GPR model, $\boldsymbol{R}_{\mathrm{c}}(\boldsymbol{x}_{\mathrm{c}}^*)$. The fine model response at the space-mapped solution $\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}_{\mathrm{f}}^{\mathrm{SM}})$ achieves a 126% enhancement in e_{h} and 47% in e_{w} of the fine model compared to those at the initial EQ settings, $\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}_{\mathrm{c}}^{(0)})$, and a 21% improvement in e_{h} and 5% improvement in e_{w} over those at the optimal solution of the coarse model, $\boldsymbol{R}_{\mathrm{f}}(\boldsymbol{x}_{\mathrm{c}}^*)$ found in [3]. Fig. 3 shows the Gen6 eye diagrams before and after the ASM optimization. The evident improvements in Fig. 3 directly translate to a more robust signal, capable of tolerating greater levels of noise, jitter, and channel loss without compromising data integrity.



a)



b)

Fig. 3. Comparison between the system fine model responses: a) at the initial Tx EQ coefficients, $\boldsymbol{x}_{\mathrm{c}}^{(0)}$; b) at the space-mapped solution found, $\boldsymbol{x}_{\mathrm{f}}^{\mathrm{SM}}$.

The ASM proposed method can be applied to different channel conditions, and its ability to automate the equalization process make it a significant advancement over manual tuning methods, which are prone to error and time inefficiencies. These results highlight the method's potential for broader applicability in future generations of PCIe interfaces and other high-speed communication systems.

IV. Conclusion

In this paper, we demonstrate the effectiveness of the ASM algorithm in fine-tuning the FIR settings for the PCIe Gen6 Tx equalizer to maximize the eye diagram margins and ensure compliance with the PCIe specification. We achieved this by utilizing a cost-effective, low-precision surrogate model based on Gaussian process regression (GPR), as coarse model, in tandem with MATLAB SerDes Toolbox simulations of the functional eye diagram for a Gen6 link, as fine model. Our results underscore the efficiency of our method in generating an optimal eye diagram. The approach not only significantly improves performance but also streamlines the EQ tuning process, which is traditionally time-consuming. Once the first processors with PCIe Gen6 are available at the validation facility, this methodology can be readily implemented for post-silicon industrial validation, thereby accelerating the typically lengthy EQ tuning process.

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